Review Test Submission: Quiz 10 (11/19)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 10 (11/19)
Started	11/19/20 9:26 PM
Submitted	11/19/20 9:28 PM
Due Date	11/19/20 11:59 PM
Status	Completed
Attempt Score	50 out of 50 points
Time Elapsed	1 minute out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

10 out of 10 points

With single-issue, in-order execution, and the classical five-stage pipeline with no bypassing, WAW hazards never cause any stalls in the pipeline.

Selected Answer: ✓ True

Answers: ✓ True

False

Question 2

10 out of 10 points

One of the main benefits of scoreboarding the CPU is the reduction of WAR and WAW hazards through register renaming.

Selected Answer: ✓ False

Answers: True

✓ False

Question 3

10 out of 10 points

An LRU replacement policy will always be better than a random replacement policy for managing virtual memory pages.

Selected Answer: ✓ False

Answers: True

✓ False

Question 4

10 out of 10 points

Cache memory is the fastest part of register memory.

Selected Answer: False
Answers: True
False

Question 5

10 out of 10 points

An assembler takes binary code and translates it into assembly language for the processor to execute.

Selected Answer: False
Answers: True
False

Wednesday, December 2, 2020 10:56:18 PM EST

← OK