Review Test Submission: Quiz 6 (10/22)

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Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 6 (10/22)
Started	10/22/20 8:38 AM
Submitted	10/22/20 9:36 AM
Due Date	10/22/20 11:59 PM
Status	Completed
Attempt Score	95 out of 100 points
Time Elapsed	57 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

5 out of 10 points

What is the goal of allowing multiple instructions for issuing in a clock cycle?

Selected Answer: ✗ Higher cache hit rate

Answers: ✓ Multiple issue CPU

Lower cache miss rate

Higher cache hit rate

Multiple issue GPU

Question 2

10 out of 10 points

[A] dependency occurs when two instructions use the same register or memory location.

Selected Answer: ✓ name

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
✓ *Contains*	name	
✓ *Contains*	output	
✓ *Exact Match*	anti-data	

Question 3

10 out of 10 points

In following instructions, OR R7,R1,R8 depends on ADD R1,R1,R6.

```
ADD R1,R2,R3
BEQ R4,L
ADD R1,R1,R6
L: OR R7,R1,R8
...
```

Selected Answer: ✓ True
Answers: ✓ True
False

Question 4

10 out of 10 points

Memory buses are usually picked based on the speed whereas the I/O buses are primarily adopted based on the compatibility (industry standards) and cost.

Selected Answer: ✓ True
Answers: ✓ True
False

Question 5

10 out of 10 points

SIMD architectures exploits instruction-level parallelism.

Selected Answer: ✗ True
Answers: True
✓ False

Question 6

10 out of 10 points

Which cache write mechanism allows outdated data in the main memory?

Selected Answer: ✓ Write Back
Answers: Write Through
✓ Write Back
Write Around
None of Above

Question 7

10 out of 10 points

Parallelism at data level means parallel execution of multiple instructions of the same type.

Selected Answer: ✓ True
Answers: ✓ True

False

Question 8

10 out of 10 points

In a heterogeneous execution model, **[a]** is the host and **[b]** is the device.

Specified Answer for: a ✓ CPU

Specified Answer for: b ✓ GPU

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	CPU	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	GPU	

Question 9

10 out of 10 points

Which one of the following processors has the highest possible MIPS rate, assuming full compiler optimization and no cache misses?

Selected Answer: ✓ A 8-issue VLIW processor driven by a 200 MHz clock.

Answers:
- A 4-issue processor driven by a 300 MHz clock.
- ✓ A 8-issue VLIW processor driven by a 200 MHz clock.
- A 2-issue processor with a 600 MHz clock.
- A single-issue processor driven by a 1.2 GHz clock.

Question 10

10 out of 10 points

Processors with lower CPIs will always be faster.

Selected Answer: ✓ False

Answers:
- True
- ✓ False

Wednesday, December 2, 2020 10:56:10 PM EST

← OK