Review Test Submission: Quiz 3 (9/17)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 3 (9/17)
Started	9/17/20 10:36 PM
Submitted	9/17/20 11:03 PM
Due Date	9/17/20 11:59 PM
Status	Completed
Attempt Score	90 out of 100 points
Time Elapsed	26 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

10 out of 10 points

If there are 5 stages in a pipeline, then 5 is the maximum possible speedup.

Selected Answer: True

Answers: True

False

Response Feedback: Correct!

with 5 pipeline stages, CPI = 5 in worst case

CPI = 1 is the ideal case.

speedup = (5/1)

Question 2

10 out of 10 points

Data dependencies can always be avoided by a bypass logic.

Selected Answer: False

Answers: True

False

Response Feedback: Correct!

Not in the case when memory instruction is followed by an instruction that has data dependency with the memory instruction.

Question 3

10 out of 10 points

ADD instruction requires data memory access.

Selected Answer: False

Answers: True
False

Response Feedback: Correct!

ADD instruction only required register file access.

Question 4

10 out of 10 points

As compared to a single-cycled datapath, a pipelined datapath has lower latency and higher throughput.

Selected Answer: False

Answers: True
False

Response Feedback: Correct!

Pipelined datapath has higher latency and higher throughput as compared to single-cycled datapath.

Question 5

10 out of 10 points

Which of the following is correct for a load instruction?

Selected Answer: MemtoReg should be set to cause the data from memory to be sent to the register file.

Answers: None of the others.

MemtoReg should be set to cause the correct register destination to be sent to the register file.

We do not care about the setting of MemtoReg for loads.

MemtoReg should be set to cause the data from memory to be sent to the register file.

Response Feedback: Correct!

Question 6

10 out of 10 points

Solid-State Drive (*SSD*) are volatile storage devices.

Selected Answer: False

Answers: True
False

Response Feedback: Correct!

They are non-volatile memory devices.

Question 7

0 out of 10 points

Assume that individual stages of a datapathhave the following latencies:

IF	ID	EX	MEM	WB
250ps	200ps	150ps	300ps	200ps

The clock cycle time of pipelined processor is **[A]**;

The clock cycle time of non-pipelined processor is **[B]**.

Specified Answer for: A ✗ 250

Specified Answer for: B ✗ 1050

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	300	
Correct Answers for: B		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	1100	

Response Feedback: Incorrect!

The clock cycle time of pipelined processor is [A] = 250ms as we take max stage time as cycle time

The clock cycle time of non-pipelined processor is [B]= (250 + 200 + 150 + 250 + 200)ms as cycle time is sum of all stages

Question 8

10 out of 10 points

next PC = PC + ___

Selected Answer: ✓ 4

Answers: 8

1

2

✓ 4

Response Feedback: Correct!

As the processor is byte addressable but the instruction is a word (4 bytes)

Question 9

10 out of 10 points

RAID 5 can recover from a two-disk failure.

Selected Answer: False
Answers: True
False

Question 10

10 out of 10 points

RAW hazard is a control hazard.

Selected Answer: False
Answers: True
False

Response Feedback: Correct!

They are data hazards.

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← OK