Review Test Submission: Quiz 5 (10/1)

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Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 5 (10/1)
Started	9/30/20 10:19 PM
Submitted	9/30/20 11:04 PM
Due Date	10/1/20 11:59 PM
Status	Completed
Attempt Score	75 out of 100 points
Time Elapsed	44 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

0 out of 10 points

Which of the following statements are generally true?

Selected Answer: Most of the cost of the memory hierarchy is at the highest level.

Answers:

Memory hierarchies take advantage of temporal locality.

On a read, the value returned depends on which blocks are in the cache.

Most of the cost of the memory hierarchy is at the highest level.

Most of the capacity of the memory hierarchy is at the lowest level.

Question 2

0 out of 15 points

Below is the address field of a direct-mapped cache.

Tag	index	Offset
31-10	9-7	6-0

What is the cache block size (in words)? [A]

Selected Answer: 8

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity

Contains	32	

Question 3

10 out of 10 points

TLBs are placed on a special cache memory.

Selected Answer: True
Answers: True
False

Question 4

10 out of 10 points

Assume a 64KB cache with four-word block size (a word is 4 bytes) and a 32-bit address. If a block has 28 tag bits, what is the type of this cache?

Selected Answer: B. Fully associative

Answers:
A. 2-way set associative
B. Fully associative
C. 4-way set associative
D. Direct mapped

Question 5

10 out of 10 points

High associativity in a cache won't reduce conflict misses.

Selected Answer: False
Answers: True
False

Question 6

10 out of 10 points

For a given capacity and block size, a set-associative cache implementation will typically have a lower hit time than a direct-mapped implementation.

Selected Answer: False
Answers: True
False

Question 7

10 out of 10 points

SRAMs are optimized for storage density.

Selected Answer: False
Answers: True
False

Question 8

10 out of 10 points

Assume a 64KB cache with 16-byte block size and a 32-bit address. What type of a cache would require 17 bits for Tag information?

Selected Answer: ✔ 2-way associative cache

Answers:
- Fully associative cache.
- Directed-mapped cache
- ✔ 2-way associative cache
- 4-way associative cache

Question 9

15 out of 15 points

Design a 8-way set associative cache that has 16 blocks and 32 bytes per block. Assume a 32 bit address.
How many bits for the index?

Selected Answer: ✔ 1

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
✔ *Exact Match*	1	

Thursday, October 8, 2020 7:37:22 AM EDT

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