Fill in the Blanks

1. One hardware solution to control hazard stalls: Branch prediction
2. “Make common case faster” is the outcome of whose law? Amdal's Law
3. A measure of performance in a computer system is: EXECUTION TIME = IC x CPI x CCT.
4. Define each term. IC _Instruction Count____, CPI __Cycles Per Instruction_, CCT __cycle time__
5. Three types of Pipeline Hazards: _____Structural, __control__, __data__.
6. Three types of Data Dependences: ___raw_____, ____waw_____, ___war__.
7. Any two sources of exceptions in the Fetch and Execution stages of a pipelined processor:
   _____page fault_____, _____overflow_____
8. Two solutions to data hazard stalls can be _____forward___, _____reorder_____
9. Pipelining improves the performance by ____improving_____ instruction throughput, as opposed to _____improve_____ the execution time of an individual instruction.
10. Three types of cache misses are. Compulsory, conflict, capacity
11. CPU time for a program can be expressed as Instruction Count * (_____hit time__ + Misses Per Instruction * Miss Penalty) * Clock Cycle Time.
12. One advantage of write-update protocol could be: simple, fast
13. One advantage of write-invalidate protocol could be
14. A solution to reduce hit time: Use direct mapped cache
15. A solution to reduce miss rate: Set associativity
16. A solution to reduce miss penalty: Multiple level cache
17. A solution for higher bandwidth for main memory: Wider main memory
18. A strategy to select the block to replace on a cache miss: LRU
19. An advantage of bus-based I/O interconnection can be: Low cost
20. A disadvantage of bus-based I/O interconnection can be: Can be bottleneck
21. An alternative I/O interconnection to bus-based interconnection: dedicated point-to-point channels
22. When I/O components are considered we need alternative performance measures besides CPU time. The number of tasks completed per unit time is called Throughput
23. Which cache write mechanism allows outdated data in the main memory? Write back cache
24. Goal of software techniques and hardware techniques, is to exploit parallelism

25. When instruction i and instruction j are to write the same register or memory location, it is called name dependency
26. Dependences among iterations of a loop are called loop carried dependency
27. To be gathered in a single register, distance separating elements are called stride
28. Vector instructions which can be potentially executed altogether, is known as Convoy
29. If it is substantially difficult to find and exploit parallelism across branches, then it is known as control hazard
30. A special hardware buffer is required for instruction execution sequence that holds instruction results, this is known as Reorder Buffer
31. A branch-prediction cache which is used to store predicted address for upcoming instruction after branch, is called a branch target buffer
32. Hardware-based speculation method for executing programs, is necessarily a reorder buffer
33. Allowing multiple instructions for issuing in a clock cycle, is a goal of: multiple issue CPU
34. Each bank register of fixed-length maintaining a single vector, is referred to as Vector Register
35. Threads being blocked altogether and being executed in sets of 32 threads, is called a block
36. A microprocessor clocked at a rate of 1.0 GHz has a clock cycle of ____5*10^-10___ seconds.

Short Answers

1. Please do the following four questions based on the following techniques to improve performance with additional hardware and/or code.

    i. Dynamic Scheduling

    ii. Data Forwarding

    iii. Loop Unrolling

    iv. Software Pipelining

    v. Multithreading

    - Which one(s) require a great number of additional registers?
        - Which ones(s) can support multi-issue processors? i
        - Which one requires most static-time preparation? iv
        - Which one(s) may cause code explosion? iii

2. Prior to the early 1980s, machines were built with more and more complex instruction sets. Why has there been a move to RISC machines away from complex instruction machines?
   Several possible answers: simplicity, simple design, lower CPI, low power, low cost, …

3. What are the two characteristics of program memory accesses that caches exploit?

   Temporal and spatial

4. What are the three types of cache misses?

   Compulsory, capacity, conflict

5. What is a Branch-Target Buffer? How does it differ from a Branch-History Table? What would be their sizes in a typical processor?

   A structure that caches the destination PC or destination instruction for a branch. It is usually organized as a cache with tags, making it more costly than a simple prediction buffer.

   A small memory that is indexed by the lower portion of the address of the branch instruction and that contains one or more bits indicating whether the branch was recently taken or not.

6. List pros and cons of VLIW architectures, and their limitations.

   Pros: compiler friendly, exploit instruction level parallelism

   Cons: Statically finding parallelism, Code size, No hazard detection hardware, Binary code compatibility

7. List pros and cons of Superscalar architectures, and their limitations.

   Pros: Binary compatibility

   Cons: More complex

8. Name two main characteristics of programs that would most benefit from GPU processors.

   Matrix Multiplication,

9. Name one limitation in

   No sophisticated addressing modes the use of SIMD systems.

10. Name a major difference between SIMD vector processors and GPUs.