Review Test Submission: Pop Quiz 9 (10/22)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Pop Quiz 9 (10/22)
Started	10/22/20 10:02 AM
Submitted	10/22/20 10:12 AM
Due Date	10/22/20 12:20 PM
Status	Completed
Attempt Score	7 out of 10 points
Time Elapsed	9 minutes out of 10 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

2 out of 2 points

Name dependencies are detected at runtime in superscalar processors.

Selected Answer: True

Answers: True

False

Question 2

2 out of 2 points

Amdahl's law does not apply to multi issue processors.

Selected Answer: False

Answers: True

False

Question 3

0 out of 1 points

GCD can be used to determine if a loop is parallel or not for certain.

Selected Answer: True

Answers: True

False

Question 4

0 out of 2 points

Which of the following statements is false?

Selected Answer: VLIW architectures execute instructions in parallel based on a fixed schedule determined when the code is compiled.

Answers:

A scalar processor processes one data item at a time.

VLIW architectures execute instructions in parallel based on a fixed schedule determined when the code is compiled.

Superscalar architectures with speculative executions are suitable for embedded processors

In a vector processor, a single instruction operates simultaneously on multiple data items.

Question 5

2 out of 2 points

Which of the following statements is false?

Selected Answer: SIMD extension can efficiently handle sparse data by scatter and gather.

Answers:

Software-based scheduling has the advantage of viewing the entire program, and can be more sophisticated.

SIMD extension can efficiently handle sparse data by scatter and gather.

Dynamic scheduling implies out-of-order execution.

In VLIW, several different operations can be executed in one clock cycle.

Question 6

1 out of 1 points

GPU hardware handles

Selected Answer: Thread management

Answers:

Applications

Thread management

Operating System

Virtual memory

Wednesday, December 2, 2020 11:03:38 PM EST

← OK

Review Test Submission: Pop Quiz 11 (11/5)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Pop Quiz 11 (11/5)
Started	11/5/20 9:49 AM
Submitted	11/5/20 9:56 AM
Due Date	11/5/20 12:30 PM
Status	Completed
Attempt Score	10 out of 16 points
Time Elapsed	7 minutes out of 15 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

2 out of 2 points

In a vector processor, a single instruction operates simultaneously on multiple data items.

Selected Answer: True

Answers: True

False

Question 2

2 out of 2 points

Only multicore processors can have simultaneous multithreading.

Selected Answer: False

Answers: True

False

Question 3

2 out of 2 points

Superscalar processors exploit Data Level Parallelism.

Selected Answer: False

Answers: True

False

Question 4

2 out of 2 points

Simultaneous multithreading uses threads to improve resource utilization of dynamically scheduled processors.

Selected Answer: True

Answers: True

False

Question 5

2 out of 2 points

In modern computers, CPU and Memory are connected by BUS

Selected Answer: True

Answers: True

False

Question 6

0 out of 2 points

Which of the following variations of cache technology is strongly associated with superscalar processing?

Selected Answer: Sub-block placement

Answers: "Hit under Miss"

Multi-ported caches

Sub-block placement

Write-back caches

Question 7

0 out of 2 points

Consider a Simultaneous Multithreading (SMT) machine with limited hardware resources. Which of the following hardware constraints would limit the total number of threads that the machine can support most.

Selected Answer: Data Cache Size

Answers: Number of Functional Unit

Number of Physical Registers

Data Cache Size

Data Cache Associativity

Question 8

0 out of 2 points

CUDA groups 16 parallel threads into a

Selected Answer: Warp

Answers: Unit

Warp

Convoy

None of the above

Wednesday, December 2, 2020 11:34:02 PM EST

← OK

Review Test Submission: Quiz 1 (9/3)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 1 (9/3)
Started	9/2/20 12:58 AM
Submitted	9/2/20 1:38 AM
Due Date	9/3/20 11:59 PM
Status	Completed
Attempt Score	80 out of 100 points
Time Elapsed	39 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

10 out of 10 points

A microprocessor clocked at the rate of 2 GHz has a clock cycle time of

Selected Answer: ✓ 0.5 ns

Answers:
2 ns
4 ns
✓ 0.5 ns
1 ns

Response Feedback: Correct!

Cycle time = 1/Frequency

Question 2

10 out of 10 points

Select the three basic building blocks of computers.

Selected Answers:
✓ Computation
✓ Communication
✓ Storage

Answers:
✓ Computation
✓ Communication
✓ Storage

Response Feedback: Correct!

Question 3

10 out of 10 points

RISC architectures are more suitable for portable electronic devices than CISC.

Selected Answer: True

Answers: True
False

Response Feedback: Correct!

RISC architectures usually have simpler design.

Question 4

10 out of 10 points

Given the importance of registers, what is the rate of increase in the number of registers in a chip over time?

Selected Answer: Very slow: Since programs are usually distributed in the language of the computer, there is inertia in instruction set architecture, and so the number of registers increases only as fast as new instruction sets become viable.

Answers:

Very fast: They increase as fast as Moore's Law, which predicts doubling the number of transistors on a chip every 18 months.

Very slow: Since programs are usually distributed in the language of the computer, there is inertia in instruction set architecture, and so the number of registers increases only as fast as new instruction sets become viable.

Response Feedback: Correct!

Question 5

0 out of 10 points

Processors with faster clock rates will always be faster?

Selected Answer: True

Answers: True
False

Response Feedback: Incorrect!

CPUtime = Number of instructions * CPI * Cycle Time

Clock rates only affect Cycle Time.

Question 6

10 out of 10 points

CPUtime = (Instructions / Program) x (Cycles / Instruction) x (Seconds / _____)

Selected Answer: Cycles

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
Contains	Cycle	

Response Feedback: Correct!

CPUtime = Number of instructions * CPI * Cycle Time

Number of instructions = Instructions / Program

CPI = Cycles / Instruction

Cycle Time = Seconds / Cycle

Question 7

0 out of 10 points

$$\text{"}Y \text{ is } p\% \text{ faster than } X\text{"} = \frac{\text{Time of } X}{\text{Time of } Y} = 1 + \frac{p}{100}$$

Selected Answer: False

Answers: True

False

Response Feedback: Incorrect!

The given equation is the definition of speedup.

Question 8

10 out of 10 points

A given application written in C runs 23 seconds on a desktop processor. A new C compiler is released that requires only 70 percent as many instructions as the old compiler. Unfortunately, it increases the CPI by 20 percent. How fast can we expect the application to run using this new compiler?

Selected Answer: 23×0.7×1.2 = 19.3 sec

Answers: 23×0.7×1.2 = 19.3 sec

(23x0.7)/1.2 = 13.4 sec

(23×1.2)/0.7 = 39.4 sec

Response Feedback: Correct!

CPUtime = Number of instructions * CPI * Cycle Time

New compiler's CPU time = (old number of instructions *0.7) * (old CPI * 1.2) * Cycle time

= Old compiler's CPU time * 0.7 * 1.2

Question 9

10 out of 10 points

For a given CPU and benchmark, CPU performance is indirectly proportional to the system clock frequency.

Selected Answer: False

Answers: True

False

Response Feedback: Correct!

CPUtime = Number of instructions * CPI * Cycle Time

= Number of instructions * CPI * (1/Frequency)

and, CPU performance = 1/CPUtime

Question 10

10 out of 10 points

Which speedup could be approximately achieved according to Amdahl's law for infinite number of processors if 20% of a program is sequential and the remaining part is ideally parallel?

Selected Answer: 5

Answers: Infinite speedup

1.2

5

20

Response Feedback: Correct!

Based on Amdahl's law,

Overall speedup = 1/((1-p)+(p/s)) = 1/(0.2+0.8/infinity) = 1/0.2 = 5

Thursday, October 8, 2020 7:24:57 AM EDT

← OK

Review Test Submission: Quiz 2 (9/10)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 2 (9/10)
Started	9/10/20 10:03 PM
Submitted	9/10/20 10:57 PM
Due Date	9/10/20 11:59 PM
Status	Completed
Attempt Score	85 out of 100 points
Time Elapsed	53 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

10 out of 10 points

Data forwarding can resolve all data hazards.

Selected Answer: False

Answers: True

False

Response Feedback: Correct!

Data forwarding cannot prevent stalls when a memory load is immediately followed by an instruction with data dependency.

Question 2

5 out of 10 points

A group of students were debating the efficiency of the five-stage pipeline when one student pointed out that not all instructions are active in every stage of the pipeline. After deciding to ignore the effects of hazards, they made the following four statements. Which ones are correct?

Selected Answers: Allowing branches and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance under all circumstances.

Trying to allow some instructions to take fewer cycles does not help, since the throughput is determined by the clock cycle; the number of pipe stages per instruction affects latency, not throughput.

Answers: Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer, so that instructions take more cycles, but the cycles are shorter. This could improve performance.

You cannot make ALU instructions take fewer cycles because of the writeback of the result, but branches can take fewer cycles, so there is some opportunity for improvement.

Allowing branches and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance under all circumstances.

Trying to allow some instructions to take fewer cycles does not help, since the throughput is determined by the clock cycle; the number of pipe stages per instruction affects latency, not throughput.

Response Feedback: Incorrect!

Question 3

10 out of 10 points

Load and store instructions, sum of contents of base register and sign-extended offset is used as

Selected Answer: a memory address

Answers:
- a register number
- a memory address
- an operand
- operator

Response Feedback: Correct!

Its memory address.

Example:

lw $1, $2($3)

where $2 - offset

$3 - relative address

$2 + $3 - absolute address

Question 4

10 out of 10 points

Consider an implementation of the instruction set architecture P1 has a clock rate of 4.8 GHz and CPIs (Cycles Per Instruction) of 1 for arithmetic, 4 for load/store and 8 for branch. A program execution consists of 1 million instructions, including 50% arithmetic, 30% load/store, and 20% branch instructions. In this case, the average CPI is **[A]**. For a 10% improvement in performance of P1, a load/store instruction will take **[B]** cycles on average if other classes are NOT improved at all.

Specified Answer for: A 3.3

Specified Answer for: B 3

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	3.3	
Correct Answers for: B		

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	3	

Response Feedback: Correct!

CPI = 0.5*1+0.3*4+0.2*8 = 3.3

Performance Ratio = Old P1 / New P1 = 3.3 / (0.5*1+0.3*x+0.2*8) = 1.1, x = 3

Question 5

10 out of 10 points

Loops with no inter-iteration (loop-carried) dependencies can be executed in parallel.

Selected Answer: True

Answers: True
False

Response Feedback: Correct!

It's true. If there is no inter-iteration dependency in a loop then each iteration of the loop can be performed in a different processor without worrying about data hazards.

Question 6

0 out of 10 points

Name dependencies **cannot** be completely eliminated by a hardware mechanism at run-time.

Selected Answer: True

Answers: True
False

Response Feedback: Incorrect!

Question 7

10 out of 10 points

Simplest scheme to handle branches is to

Selected Answer: Both a and b

Answers: Flush pipeline

Freezing pipeline

Depth of pipeline

Both a and b

Response Feedback: Correct!

Flush pipeline - used during branch prediction when there is misprediction

Freeze pipeline - used during control hazards by putting stalls

Question 8

10 out of 10 points

Branch, MemWrite and MemRead are control lines set of

Selected Answer: Memory Access

Answers:
- Memory Access
- Execution
- Instruction Fetch
- Instruction decode

Response Feedback: Correct!

Question 9

10 out of 10 points

Pipelining increases overall instruction throughput but also increases individual instruction latency.

Selected Answer: True

Answers:
- True
- False

Response Feedback: Correct!

In pipelining, all pipelined stages need to be equal and able to fit every stage. Thus, a single instruction's latency is increased but the throughput is increased.

Question 10

10 out of 10 points

Predicting branches at runtime by using run-time information, is known as

Selected Answer: Dynamic branch prediction

Answers:
- Static branch prediction
- Stall prediction
- Dynamic branch prediction
- None of the above

Response Feedback: Correct!

← OK

Review Test Submission: Quiz 3 (9/17)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 3 (9/17)
Started	9/17/20 10:36 PM
Submitted	9/17/20 11:03 PM
Due Date	9/17/20 11:59 PM
Status	Completed
Attempt Score	90 out of 100 points
Time Elapsed	26 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

10 out of 10 points

If there are 5 stages in a pipeline, then 5 is the maximum possible speedup.

Selected Answer: True

Answers: True

False

Response Feedback: Correct!

with 5 pipeline stages, CPI = 5 in worst case

CPI = 1 is the ideal case.

speedup = (5/1)

Question 2

10 out of 10 points

Data dependencies can always be avoided by a bypass logic.

Selected Answer: False

Answers: True

False

Response Feedback: Correct!

Not in the case when memory instruction is followed by an instruction that has data dependency with the memory instruction.

Question 3

10 out of 10 points

ADD instruction requires data memory access.

Selected Answer: False

Answers: True
False

Response Feedback: Correct!

ADD instruction only required register file access.

Question 4

10 out of 10 points

As compared to a single-cycled datapath, a pipelined datapath has lower latency and higher throughput.

Selected Answer: False

Answers: True
False

Response Feedback: Correct!

Pipelined datapath has higher latency and higher throughput as compared to single-cycled datapath.

Question 5

10 out of 10 points

Which of the following is correct for a load instruction?

Selected Answer: MemtoReg should be set to cause the data from memory to be sent to the register file.

Answers: None of the others.

MemtoReg should be set to cause the correct register destination to be sent to the register file.

We do not care about the setting of MemtoReg for loads.

MemtoReg should be set to cause the data from memory to be sent to the register file.

Response Feedback: Correct!

Question 6

10 out of 10 points

Solid-State Drive (*SSD*) are volatile storage devices.

Selected Answer: False

Answers: True
False

Response Feedback: Correct!

They are non-volatile memory devices.

Question 7

0 out of 10 points

Assume that individual stages of a datapathhave the following latencies:

IF	ID	EX	MEM	WB
250ps	200ps	150ps	300ps	200ps

The clock cycle time of pipelined processor is **[A]**;

The clock cycle time of non-pipelined processor is **[B]**.

Specified Answer for: A 250

Specified Answer for: B 1050

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	300	
Correct Answers for: B		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	1100	

Response Feedback: Incorrect!

The clock cycle time of pipelined processor is [A] = 250ms as we take max stage time as cycle time

The clock cycle time of non-pipelined processor is [B]= (250 + 200 + 150 + 250 + 200)ms as cycle time is sum of all stages

Question 8

10 out of 10 points

next PC = PC + ___

Selected Answer: 4

Answers: 8

1

2

4

Response Feedback: Correct!

As the processor is byte addressable but the instruction is a word (4 bytes)

Question 9

10 out of 10 points

RAID 5 can recover from a two-disk failure.

Selected Answer: False
Answers: True
False

Question 10

10 out of 10 points

RAW hazard is a control hazard.

Selected Answer: False
Answers: True
False

Response Feedback: Correct!

They are data hazards.

Thursday, October 8, 2020 7:31:51 AM EDT

← OK

Review Test Submission: Quiz 4 (9/24)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 4 (9/24)
Started	9/24/20 10:19 PM
Submitted	9/24/20 11:50 PM
Due Date	9/24/20 11:59 PM
Status	Completed
Attempt Score	95 out of 100 points
Time Elapsed	1 hour, 31 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

0 out of 5 points

TLBs are typically built to be fully-associative or highly set-associative. In contrast, first-level data caches are more likely to be direct-mapped or 2 or 4-way set associative. Give a reason why this is so.

Selected Answer: [None Given]
Correct Answer: [None]
Response Feedback: [None Given]

Question 2

10 out of 10 points

The speed of the memory system affects the designer's decision on the size of the cache block. Which of the following cache designer guidelines is generally valid?

Selected Answers:
- The shorter the memory latency, the smaller the cache block
- The higher the memory bandwidth, the larger the cache block

Answers:
- The shorter the memory latency, the smaller the cache block
- The shorter the memory latency, the larger the cache block
- The higher the memory bandwidth, the smaller the cache block
- The higher the memory bandwidth, the larger the cache block

Question 3

10 out of 10 points

In a Write-Through cache, a read miss always causes a write to the lower memory level.

Selected Answer: False
Answers: True

False

Response Feedback: Correct!

Write through writes back to the lower level memories when there is a write miss.

Question 4

15 out of 15 points

Design a 4-way set associative cache that has 16 blocks and 64 bytes per block. Assume a 32 bit address. Calculate the following:

How many bits for the byte offset? **[x]**

How many bits for the set (index) field? **[y]**

How many bits for the tag? **[z]**

Specified Answer for: x 6

Specified Answer for: y 2

Specified Answer for: z 24

Correct Answers for: x		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	6	
Correct Answers for: y		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	2	
Correct Answers for: z		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	24	

Response Feedback: Correct!

Design a 4-way set associative cache that has 16 blocks and 64 bytes per block. Assume a 32 bit address. Calculate the following:

#sets = 16/4 = 4

so, set(index) bits = 2

64 bytes per block, so offset = 6

tag = 32 - 6 - 2 = 24

Question 5

10 out of 10 points

For a data cache with a 90% hit rate and a 5-cycle hit latency, calculate the average memory access latency in cycles. Assume that latency to memory and the cache miss penalty together is 130 cycles. Note: The cache must be accessed after memory returns the data.

Selected Answer: 17.5

Correct Answer: 18

Answer range +/- 0.5 (17.5 - 18.5)

Response Feedback: Correct!

AMAT = hit time + miss rate*(miss penalty) = 5 + 0.1*130 = 18

Question 6

10 out of 10 points

Assume a 64KB cache with four-word block size (a word is 4 bytes) and a 32-bit address. If a block has 28 tag bits, what is the type of this cache?

Selected Answer: Fully associative

Answers:
- 4-way set associative
- 2-way set associative
- Fully associative
- Direct mapped

Response Feedback: Correct!

address = 32 bits

tag = 28 bits

as a block is 4 words i.e 4x4 bytes, offset = 4 bits

that means, index = 0 bits

Thus, its fully associative

Question 7

10 out of 10 points

High associativity in a cache reduces conflict misses.

Selected Answer: True

Answers:
- True
- False

Response Feedback: Correct!

It reduces conflict misses.

Question 8

10 out of 10 points

For a given capacity and block size, a set-associative cache implementation will typically have a lower hit time than a direct-mapped implementation.

Selected Answer: False

Answers:
- True
- False

Response Feedback: Correct!

Set-associative cache will have a lower miss rate (leading to lower AMAT) but given a set has multiple blocks the hit time for a particular block is higher.

Question 9

10 out of 10 points

Consider a system with a two-level cache having the following characteristics: L1 Cache has an access time of 1 clock cycle with an average hit rate of 90%; L2 Cache has an access time of 5 clock cycles (after L1 miss) with an average miss rate of 10%. If L2 misses take 40 clock cycles, what would be the average memory access time in clocks?

Selected Answer: 1.75
Correct Answer: 1.9
Answer range +/- 0.2 (1.7 - 2.1)
Response Feedback: Correct!

AMAT = 1+0.1*(5 + 0.1*(40)) = 1.9 cycles

Question 10

10 out of 10 points

RAID systems can have catastrophic failures.

Selected Answer: True
Answers: True
False

Thursday, October 8, 2020 7:35:12 AM EDT

← OK

Review Test Submission: Quiz 5 (10/1)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 5 (10/1)
Started	9/30/20 10:19 PM
Submitted	9/30/20 11:04 PM
Due Date	10/1/20 11:59 PM
Status	Completed
Attempt Score	75 out of 100 points
Time Elapsed	44 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

0 out of 10 points

Which of the following statements are generally true?

Selected Answer: Most of the cost of the memory hierarchy is at the highest level.

Answers:

Memory hierarchies take advantage of temporal locality.

On a read, the value returned depends on which blocks are in the cache.

Most of the cost of the memory hierarchy is at the highest level.

Most of the capacity of the memory hierarchy is at the lowest level.

Question 2

0 out of 15 points

Below is the address field of a direct-mapped cache.

Tag	index	Offset
31-10	9-7	6-0

What is the cache block size (in words)? [A]

Selected Answer: 8

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity

Contains	32	

Question 3

10 out of 10 points

TLBs are placed on a special cache memory.

Selected Answer: True
Answers: True
False

Question 4

10 out of 10 points

Assume a 64KB cache with four-word block size (a word is 4 bytes) and a 32-bit address. If a block has 28 tag bits, what is the type of this cache?

Selected Answer: B. Fully associative

Answers:
A. 2-way set associative
B. Fully associative
C. 4-way set associative
D. Direct mapped

Question 5

10 out of 10 points

High associativity in a cache won't reduce conflict misses.

Selected Answer: False
Answers: True
False

Question 6

10 out of 10 points

For a given capacity and block size, a set-associative cache implementation will typically have a lower hit time than a direct-mapped implementation.

Selected Answer: False
Answers: True
False

Question 7

10 out of 10 points

SRAMs are optimized for storage density.

Selected Answer: False
Answers: True
False

Question 8

10 out of 10 points

Assume a 64KB cache with 16-byte block size and a 32-bit address. What type of a cache would require 17 bits for Tag information?

Selected Answer: ✔ 2-way associative cache

Answers:

- Fully associative cache.
- Directed-mapped cache
- ✔ 2-way associative cache
- 4-way associative cache

Question 9

15 out of 15 points

Design a 8-way set associative cache that has 16 blocks and 32 bytes per block. Assume a 32 bit address.
How many bits for the index?

Selected Answer: ✔ 1

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
✔ *Exact Match*	1	

Thursday, October 8, 2020 7:37:22 AM EDT

← OK

Review Test Submission: Quiz 6 (10/22)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 6 (10/22)
Started	10/22/20 8:38 AM
Submitted	10/22/20 9:36 AM
Due Date	10/22/20 11:59 PM
Status	Completed
Attempt Score	95 out of 100 points
Time Elapsed	57 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

5 out of 10 points

What is the goal of allowing multiple instructions for issuing in a clock cycle?

Selected Answer: ✗ Higher cache hit rate

Answers: ✓ Multiple issue CPU

Lower cache miss rate

Higher cache hit rate

Multiple issue GPU

Question 2

10 out of 10 points

[A] dependency occurs when two instructions use the same register or memory location.

Selected Answer: ✓ name

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
✓ *Contains*	name	
✓ *Contains*	output	
✓ *Exact Match*	anti-data	

Question 3

10 out of 10 points

In following instructions, OR R7,R1,R8 depends on ADD R1,R1,R6.

```
ADD R1,R2,R3
BEQ R4,L
ADD R1,R1,R6
L: OR R7,R1,R8
...
```

Selected Answer: ✓ True
Answers: ✓ True
False

Question 4

10 out of 10 points

Memory buses are usually picked based on the speed whereas the I/O buses are primarily adopted based on the compatibility (industry standards) and cost.

Selected Answer: ✓ True
Answers: ✓ True
False

Question 5

10 out of 10 points

SIMD architectures exploits instruction-level parallelism.

Selected Answer: ✗ True
Answers: True
✓ False

Question 6

10 out of 10 points

Which cache write mechanism allows outdated data in the main memory?

Selected Answer: ✓ Write Back
Answers: Write Through
✓ Write Back
Write Around
None of Above

Question 7

10 out of 10 points

Parallelism at data level means parallel execution of multiple instructions of the same type.

Selected Answer: ✓ True
Answers: ✓ True

False

Question 8

10 out of 10 points

In a heterogeneous execution model, **[a]** is the host and **[b]** is the device.

Specified Answer for: a ✓ CPU

Specified Answer for: b ✓ GPU

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	CPU	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	GPU	

Question 9

10 out of 10 points

Which one of the following processors has the highest possible MIPS rate, assuming full compiler optimization and no cache misses?

Selected Answer: ✓ A 8-issue VLIW processor driven by a 200 MHz clock.

Answers:
- A 4-issue processor driven by a 300 MHz clock.
- ✓ A 8-issue VLIW processor driven by a 200 MHz clock.
- A 2-issue processor with a 600 MHz clock.
- A single-issue processor driven by a 1.2 GHz clock.

Question 10

10 out of 10 points

Processors with lower CPIs will always be faster.

Selected Answer: ✓ False

Answers:
- True
- ✓ False

Wednesday, December 2, 2020 10:56:10 PM EST

← OK

Review Test Submission: Quiz 7 (10/29)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 7 (10/29)
Started	10/29/20 9:41 PM
Submitted	10/29/20 9:44 PM
Due Date	10/29/20 11:59 PM
Status	Completed
Attempt Score	50 out of 50 points
Time Elapsed	2 minutes out of 1 hour
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

10 out of 10 points

Designating a preferred thread sacrifices throughput.

Selected Answer: True

Answers: True

False

Question 2

10 out of 10 points

Which is achieved by performing the same operation on independent data?

Selected Answer: Data-level parallelism

Answers: Instruction-level parallelism

Data-level parallelism

Thread-level parallelism

Task-level parallelism

Question 3

10 out of 10 points

In a GPU, a thread is associated with each data element.

[a] are organized into blocks.

Blocks are organized into a **[b]**.

Specified Answer for: a ✓ threads

Specified Answer for: b ✓ grid

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	thread	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Contains*	grid	

Question 4

10 out of 10 points

Amdahl's Law doesn't apply to parallel computers

Selected Answer: ✓ False

Answers: True

✓ False

Question 5

10 out of 10 points

GPU hardware handles

Selected Answer: ✓ thread management

Answers: none

✓ thread management

applications

OS

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← OK

Review Test Submission: Quiz 8 (11/5)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 8 (11/5)
Started	11/5/20 7:33 AM
Submitted	11/5/20 7:35 AM
Due Date	11/5/20 11:59 PM
Status	Completed
Attempt Score	50 out of 50 points
Time Elapsed	2 minutes out of 1 hour
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

10 out of 10 points

Symmetric multiprocessors architectures, are sometimes known as

Selected Answer: ✓ Uniform memory access

Answers: Variable memory access

Static memory access

✓ Uniform memory access

Question 2

10 out of 10 points

Which of the following systems is the least scalable with respect to its number of processors?

Selected Answer: ✓ Symmetric multiprocessors

Answers: ✓ Symmetric multiprocessors

Noncache-coherent NUMA systems

None

Cache-coherent NUMA systems

Question 3

10 out of 10 points

A Shared Address Space programming model can be used on large scale multiprocessors.

Selected Answer: True
Answers: True
False

Question 4

10 out of 10 points

Which of the following statement is **NOT** true on the Centralized Shared-Memory Architectures?

Selected Answer: Bandwidth of the centralized memory system grows as the number of processors in machines increases

Answers:

The use of large multilevel caches can substantially reduce memory bandwidth demands of a processor.

Bandwidth of the centralized memory system grows as the number of processors in machines increases

It is possible for several (micro)processors to share the same memory through a shared bus.

Question 5

10 out of 10 points

Clusters have separate memories and thus need many copies of the operating system.

Selected Answer: True
Answers: True
False

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← OK

Review Test Submission: Quiz 9 (11/12)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 9 (11/12)
Started	11/12/20 8:45 AM
Submitted	11/12/20 8:47 AM
Due Date	11/12/20 11:59 PM
Status	Completed
Attempt Score	50 out of 50 points
Time Elapsed	2 minutes out of 1 hour
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

10 out of 10 points

In the Centralized Shared Memory, there is uniform access time/latency.

Selected Answer: ✓ True

Answers: ✓ True

False

Question 2

10 out of 10 points

To support Fine-Grained Multithreading, CPU must be able to switch threads every clock.

Selected Answer: ✓ True

Answers: ✓ True

False

Question 3

10 out of 10 points

SMT makes sense with coarse-grained implementation

Selected Answer: ✓ False

Answers: True

✓ False

Question 4

10 out of 10 points

Each thread requires its own user state such as PC, GPRs.

Selected Answer: True
Answers: True
False

Question 5

10 out of 10 points

Course-Grained Multithreading also slows down threads

Selected Answer: False
Answers: True
False

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← OK

Review Test Submission: Quiz 10 (11/19)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 10 (11/19)
Started	11/19/20 9:26 PM
Submitted	11/19/20 9:28 PM
Due Date	11/19/20 11:59 PM
Status	Completed
Attempt Score	50 out of 50 points
Time Elapsed	1 minute out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

10 out of 10 points

With single-issue, in-order execution, and the classical five-stage pipeline with no bypassing, WAW hazards never cause any stalls in the pipeline.

Selected Answer: ✓ True

Answers: ✓ True

False

Question 2

10 out of 10 points

One of the main benefits of scoreboarding the CPU is the reduction of WAR and WAW hazards through register renaming.

Selected Answer: ✓ False

Answers: True

✓ False

Question 3

10 out of 10 points

An LRU replacement policy will always be better than a random replacement policy for managing virtual memory pages.

Selected Answer: ✓ False

Answers: True

✓ False

Question 4

10 out of 10 points

Cache memory is the fastest part of register memory.

Selected Answer: False
Answers: True
False

Question 5

10 out of 10 points

An assembler takes binary code and translates it into assembly language for the processor to execute.

Selected Answer: False
Answers: True
False

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← OK