Review Test Submission: Quiz 4 (9/24)

User	Yuchen Wang
Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 4 (9/24)
Started	9/24/20 10:19 PM
Submitted	9/24/20 11:50 PM
Due Date	9/24/20 11:59 PM
Status	Completed
Attempt Score	95 out of 100 points
Time Elapsed	1 hour, 31 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

0 out of 5 points

TLBs are typically built to be fully-associative or highly set-associative. In contrast, first-level data caches are more likely to be direct-mapped or 2 or 4-way set associative. Give a reason why this is so.

Selected Answer: [None Given]
Correct Answer: [None]
Response Feedback: [None Given]

Question 2

10 out of 10 points

The speed of the memory system affects the designer's decision on the size of the cache block. Which of the following cache designer guidelines is generally valid?

Selected Answers:
- The shorter the memory latency, the smaller the cache block
- The higher the memory bandwidth, the larger the cache block

Answers:
- The shorter the memory latency, the smaller the cache block
- The shorter the memory latency, the larger the cache block
- The higher the memory bandwidth, the smaller the cache block
- The higher the memory bandwidth, the larger the cache block

Question 3

10 out of 10 points

In a Write-Through cache, a read miss always causes a write to the lower memory level.

Selected Answer: False
Answers: True

False

Response Feedback: Correct!

Write through writes back to the lower level memories when there is a write miss.

Question 4

15 out of 15 points

Design a 4-way set associative cache that has 16 blocks and 64 bytes per block. Assume a 32 bit address. Calculate the following:

How many bits for the byte offset? **[x]**

How many bits for the set (index) field? **[y]**

How many bits for the tag? **[z]**

Specified Answer for: x 6

Specified Answer for: y 2

Specified Answer for: z 24

Correct Answers for: x		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	6	
Correct Answers for: y		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	2	
Correct Answers for: z		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Contains	24	

Response Feedback: Correct!

Design a 4-way set associative cache that has 16 blocks and 64 bytes per block. Assume a 32 bit address. Calculate the following:

#sets = 16/4 = 4

so, set(index) bits = 2

64 bytes per block, so offset = 6

tag = 32 - 6 - 2 = 24

Question 5

10 out of 10 points

For a data cache with a 90% hit rate and a 5-cycle hit latency, calculate the average memory access latency in cycles. Assume that latency to memory and the cache miss penalty together is 130 cycles. Note: The cache must be accessed after memory returns the data.

Selected Answer: 17.5

Correct Answer: 18

Answer range +/- 0.5 (17.5 - 18.5)

Response Feedback: Correct!

AMAT = hit time + miss rate*(miss penalty) = 5 + 0.1*130 = 18

Question 6

10 out of 10 points

Assume a 64KB cache with four-word block size (a word is 4 bytes) and a 32-bit address. If a block has 28 tag bits, what is the type of this cache?

Selected Answer: Fully associative

Answers:
- 4-way set associative
- 2-way set associative
- Fully associative
- Direct mapped

Response Feedback: Correct!

address = 32 bits

tag = 28 bits

as a block is 4 words i.e 4x4 bytes, offset = 4 bits

that means, index = 0 bits

Thus, its fully associative

Question 7

10 out of 10 points

High associativity in a cache reduces conflict misses.

Selected Answer: True

Answers:
- True
- False

Response Feedback: Correct!

It reduces conflict misses.

Question 8

10 out of 10 points

For a given capacity and block size, a set-associative cache implementation will typically have a lower hit time than a direct-mapped implementation.

Selected Answer: False

Answers:
- True
- False

Response Feedback: Correct!

Set-associative cache will have a lower miss rate (leading to lower AMAT) but given a set has multiple blocks the hit time for a particular block is higher.

Question 9

10 out of 10 points

Consider a system with a two-level cache having the following characteristics: L1 Cache has an access time of 1 clock cycle with an average hit rate of 90%; L2 Cache has an access time of 5 clock cycles (after L1 miss) with an average miss rate of 10%. If L2 misses take 40 clock cycles, what would be the average memory access time in clocks?

Selected Answer: 1.75
Correct Answer: 1.9
Answer range +/- 0.2 (1.7 - 2.1)
Response Feedback: Correct!

AMAT = 1+0.1*(5 + 0.1*(40)) = 1.9 cycles

Question 10

10 out of 10 points

RAID systems can have catastrophic failures.

Selected Answer: True
Answers: True
False

Thursday, October 8, 2020 7:35:12 AM EDT

← OK