Review Test Submission: Quiz 2 (9/10)

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Course	CSE661/CIS655 - Advanced Computer Architecture - F20
Test	Quiz 2 (9/10)
Started	9/10/20 10:03 PM
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Attempt Score	85 out of 100 points
Time Elapsed	53 minutes out of 2 hours
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

10 out of 10 points

Data forwarding can resolve all data hazards.

Selected Answer: False

Answers: True

False

Response Feedback: Correct!

Data forwarding cannot prevent stalls when a memory load is immediately followed by an instruction with data dependency.

Question 2

5 out of 10 points

A group of students were debating the efficiency of the five-stage pipeline when one student pointed out that not all instructions are active in every stage of the pipeline. After deciding to ignore the effects of hazards, they made the following four statements. Which ones are correct?

Selected Answers: Allowing branches and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance under all circumstances.

Trying to allow some instructions to take fewer cycles does not help, since the throughput is determined by the clock cycle; the number of pipe stages per instruction affects latency, not throughput.

Answers: Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer, so that instructions take more cycles, but the cycles are shorter. This could improve performance.

You cannot make ALU instructions take fewer cycles because of the writeback of the result, but branches can take fewer cycles, so there is some opportunity for improvement.

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Response Feedback: Incorrect!

Question 3

10 out of 10 points

Load and store instructions, sum of contents of base register and sign-extended offset is used as

Selected Answer: a memory address

Answers:
- a register number
- a memory address
- an operand
- operator

Response Feedback: Correct!

Its memory address.

Example:

lw $1, $2($3)

where $2 - offset

$3 - relative address

$2 + $3 - absolute address

Question 4

10 out of 10 points

Consider an implementation of the instruction set architecture P1 has a clock rate of 4.8 GHz and CPIs (Cycles Per Instruction) of 1 for arithmetic, 4 for load/store and 8 for branch. A program execution consists of 1 million instructions, including 50% arithmetic, 30% load/store, and 20% branch instructions. In this case, the average CPI is **[A]**. For a 10% improvement in performance of P1, a load/store instruction will take **[B]** cycles on average if other classes are NOT improved at all.

Specified Answer for: A 3.3

Specified Answer for: B 3

Correct Answers for: A		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	3.3	
Correct Answers for: B		

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	3	

Response Feedback: Correct!

CPI = 0.5*1+0.3*4+0.2*8 = 3.3

Performance Ratio = Old P1 / New P1 = 3.3 / (0.5*1+0.3*x+0.2*8) = 1.1, x = 3

Question 5

10 out of 10 points

Loops with no inter-iteration (loop-carried) dependencies can be executed in parallel.

Selected Answer: True

Answers: True
False

Response Feedback: Correct!

It's true. If there is no inter-iteration dependency in a loop then each iteration of the loop can be performed in a different processor without worrying about data hazards.

Question 6

0 out of 10 points

Name dependencies **cannot** be completely eliminated by a hardware mechanism at run-time.

Selected Answer: True

Answers: True
False

Response Feedback: Incorrect!

Question 7

10 out of 10 points

Simplest scheme to handle branches is to

Selected Answer: Both a and b

Answers: Flush pipeline

Freezing pipeline

Depth of pipeline

Both a and b

Response Feedback: Correct!

Flush pipeline - used during branch prediction when there is misprediction

Freeze pipeline - used during control hazards by putting stalls

Question 8

10 out of 10 points

Branch, MemWrite and MemRead are control lines set of

Selected Answer: Memory Access

Answers:
- Memory Access
- Execution
- Instruction Fetch
- Instruction decode

Response Feedback: Correct!

Question 9

10 out of 10 points

Pipelining increases overall instruction throughput but also increases individual instruction latency.

Selected Answer: True

Answers:
- True
- False

Response Feedback: Correct!

In pipelining, all pipelined stages need to be equal and able to fit every stage. Thus, a single instruction's latency is increased but the throughput is increased.

Question 10

10 out of 10 points

Predicting branches at runtime by using run-time information, is known as

Selected Answer: Dynamic branch prediction

Answers:
- Static branch prediction
- Stall prediction
- Dynamic branch prediction
- None of the above

Response Feedback: Correct!

← OK