Assignment #3

Overview

For this assignment, you will generate a 10 MHz square wave with a 50% duty cycle using two different techniques. In the first technique, you will use software to configure the LPC1769 microcontroller to generate the square wave. In the second technique, you will use an 6 MHz crystal as part of a hardware oscillator followed by a clock multiplier/divider to boost the frequency to 10 MHz. Note that these two techniques are completely separate tasks. The hardware oscillator, clock multiplier, and clock divider circuits are not connected to the microcontroller; the LPCXpresso module has all the necessary hardware already built-in for the first technique.

Additional requirement for 3 person teams

The output frequency should be controllable by a simple SPST pushbutton switch. If the switch is not pressed then the frequency should be 10 MHz as described above. If the switch is pressed then the frequency should decrease to 8 MHz. Releasing the switch should return the output to 10 MHz.

What to demo

1. Show the output waveform for technique #1 (software). Show that the scope measured frequency has an error of less than 1% and the duty cycle has an error of less than 5%, both measured over a 10 second span (use the min/max measurement feature)
2. Show the output waveform for technique #2 (hardware) and the SIGin clock to the PLL. Show that the scope measure frequency has an error of less than 1% and the duty cycle has an error of less than 5%, both measured over a 10 second span. Also show that the SIGin clock has a stable phase relationship to the output waveform (i.e. the PLL is in the locked state)

Preliminary design analysis

There are a few things useful to consider before you start.

1. For the software technique:
    1. Identify the fundamental clock source that you will use (the 4 MHz internal RC source, or the 12 MHz external crystal)
    2. If using the PLL, determine the clock multiplier and divider values needed and the resulting CPU clock (CCLK). Ensure that the PLL's output frequency is within the required 275 MHz to 550 MHz range with these values.
2. For the hardware technique:
    1. Calculate the values of the capacitors needed to match the crystal's expected load capacitance (C_L)
    2. Determine the clock multiplier and divider values needed to convert the 4 MHz clock from the crystal oscillator into the desired frequency.
    3. Determine the nominal voltage controlled oscillator (VCO) frequency and estimate the corresponding resistor and capacitor values needed.

What to put in the report

1. The objectives of the lab assignment (essentially, the overview above in your own words)
2. The design of your solution (the items in the preliminary design analysis above, updated for the final design)
3. Details of your final solution
    1. The hardware schematic
    2. The software source code
4. Oscilloscope snapshots of both of the generated 10 MHz waveforms. For the hardware technique, also show the original 6 MHz clock from the crystal oscillator circuit.
5. The major (EE, CpE, or other) and individual contributions of each team member.

Design notes

It is extremely important to minimize electrical noise, especially near the voltage controlled oscillator and crystal oscillator subcircuits. Be sure to use power rail decoupling capacitors with each IC and make sure they are connected to the IC's power and ground pins as directly as possible. Keep ground connections as direct as possible. Internal LPC1769 clocks are externally visible on CLKOUT (P1.27).

Due date

Februrary 23