Simulation of Multi-input gates with Distinguishing Xs and X-Trees

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ECE 5505 Final Report

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Chapter 1

Introduction

1.1 Overview

The goal of this project was to transform the previous project, which implemented a simulator of circuits containing distinguishing Xs, but only on dual input gates, for gates containing more than 2 inputs; the process of implementing this and the challenges of doing so will be discussed in chapter 2. Another goal of this project was to implement some features that would help gain information from X values that were not squashed and were propagated to the output. The mechanism that was chosen to do this was named an X-Tree, and is a list of all the distinguishing Xs that make up an X value at any gate in the circuit. In addition, the first occurrence of each distinguishing X value and its inverse is tracked in two separate lists, to help identify key gates in the propagation path; this is covered in chapter 3. The final step to help obtain more information about these values was to implement an interface that would allow a user to interact with the circuit and inspect specific gates, as well as manipulate their output to see the effect on the circuit; this will be discussed more in chapter 4.

1.2 Background Research

[1] [2] [3] [4] [5]

Chapter 2

Multi-input gates

2.1 Overview

2.2 AND/OR

fig. 2.1a fig. 3.1

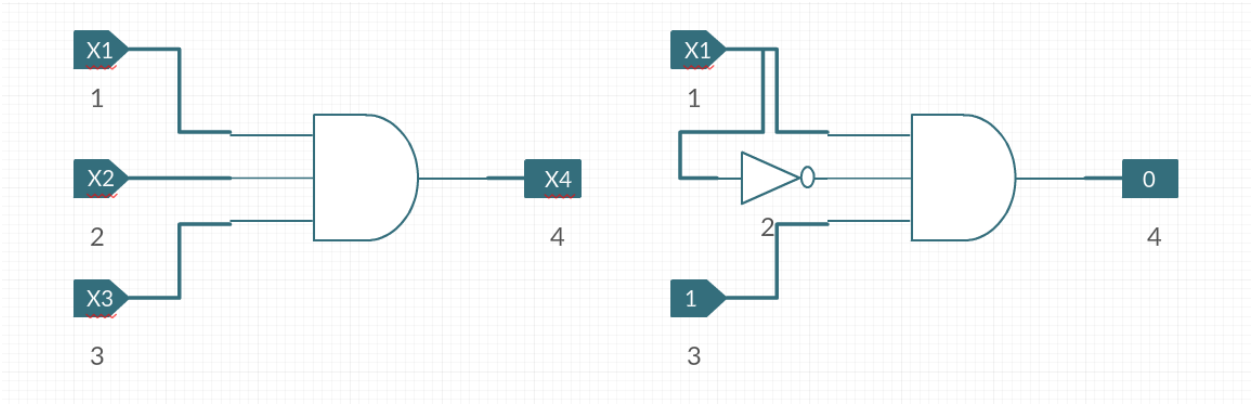
2.2.1 Controlling Values

2.2.2 Major Changes

2.3 XOR

2.3.1 Order of Inputs

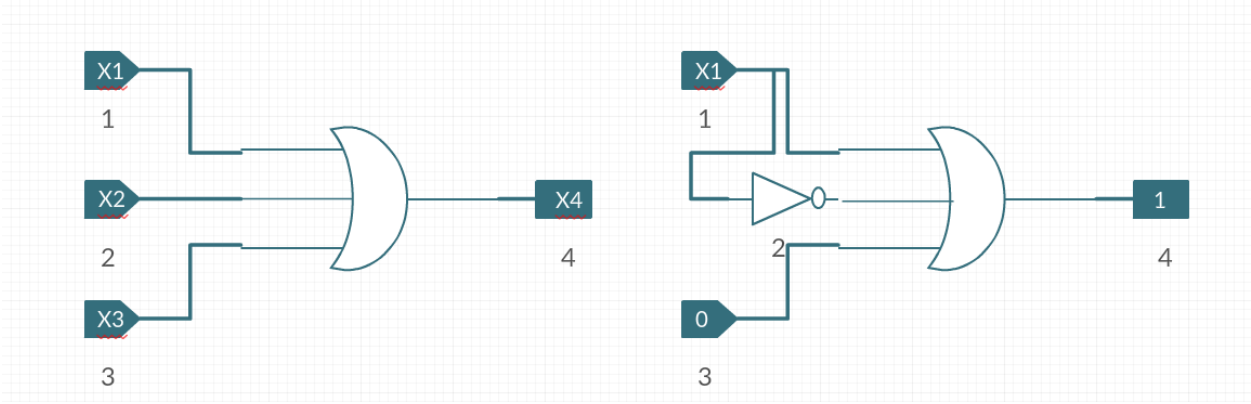
2.3.2 Restoring X's



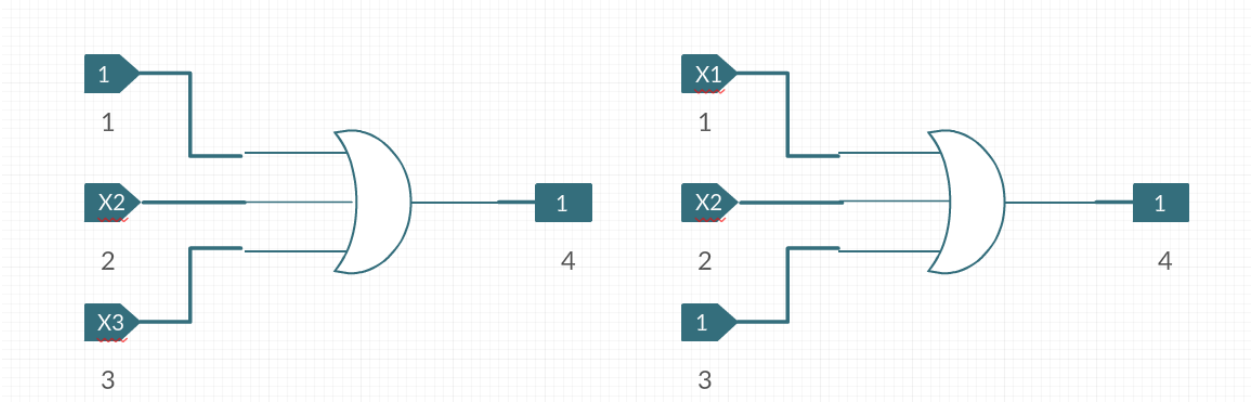
(a) **(b)**

(c) **(d)**

Figure 2.1: Various Multi-input AND Gate Configurations

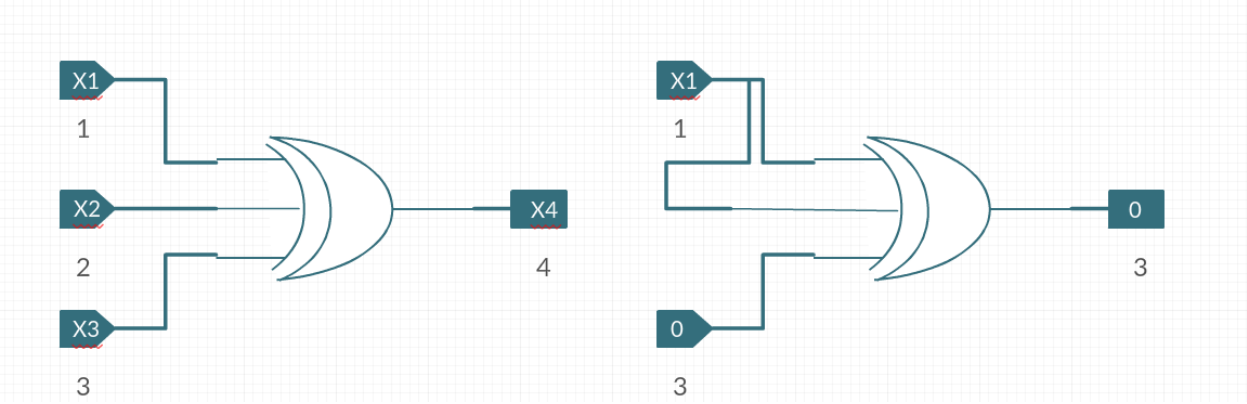


(a) **(b)**

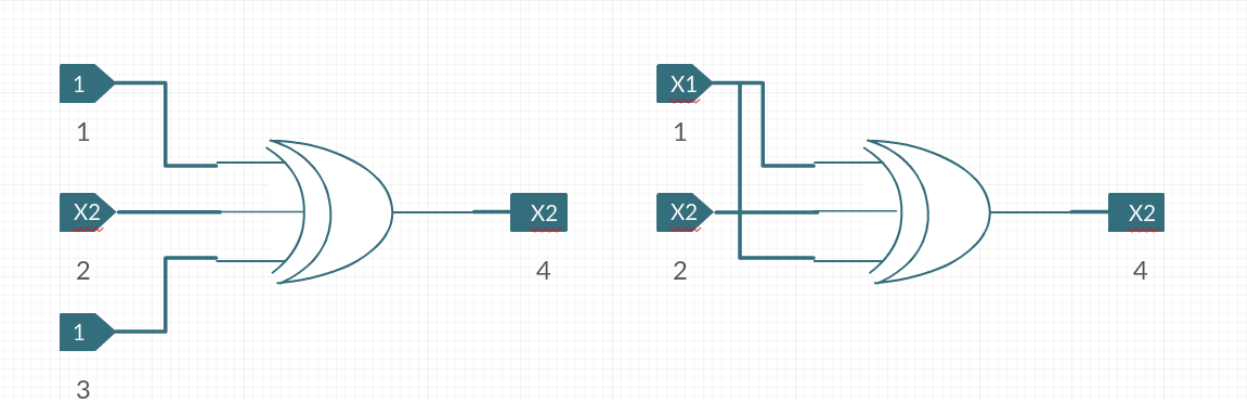


(c) **(d)**

Figure 2.2: Various Multi-input OR Gate Configurations



(a) **(b)**



(c) **(d)**

Figure 2.3: Various Multi-input XOR Gate Configurations

Chapter 3

X-Trees

3.1 Overview

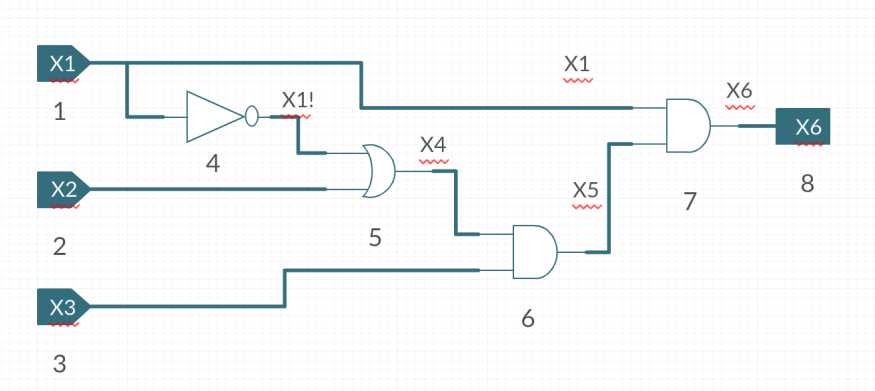


Figure 3.1: The circuit used in the example simulation

```
root@HAL9000:~/ECE5505-Final-Project# ./circuit-simulator-burrow.app -xo tests/xtree-test
Successfully read in circuit:
        3 PIs.
        1 POs.
        0 Dffs.
        9 total number of gates
        6 levels in the circuit.
vector #0:
        X

Gate 8's XTree:
        X1      at gate 1
        X1!     at gate 4
        X2      at gate 2
        X3      at gate 3
        X4      at gate 5
        X5      at gate 6
        X6      at gate 7

Number of vectors: 1
Number of clock cycles elapsed: 0
```

Figure 3.2: An example of the X-Tree output of the simulator

3.2 Effects on Gates

3.2.1 AND/OR

3.2.2 XOR

Chapter 4

User Interface

4.1 Overview

4.2 X-Trees

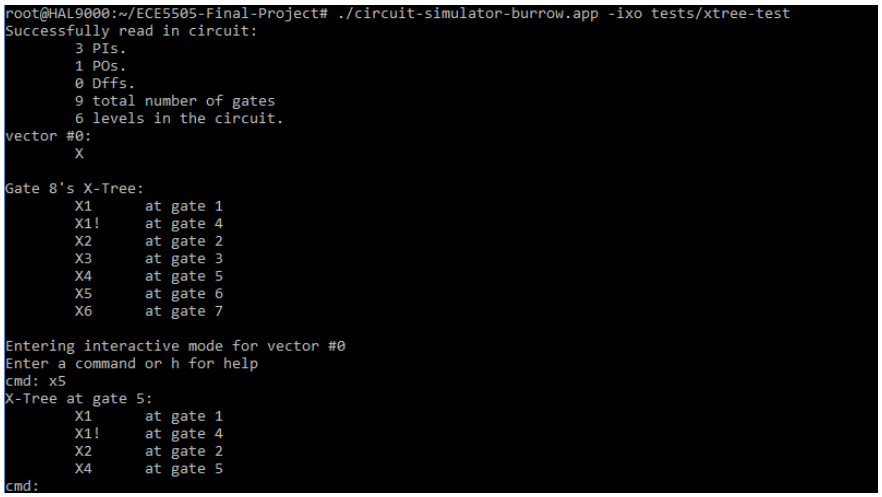


Figure 4.1: An example of the user interface and how to observe the X-Tree of any gate in the circuit

4.3 Controlling Gates

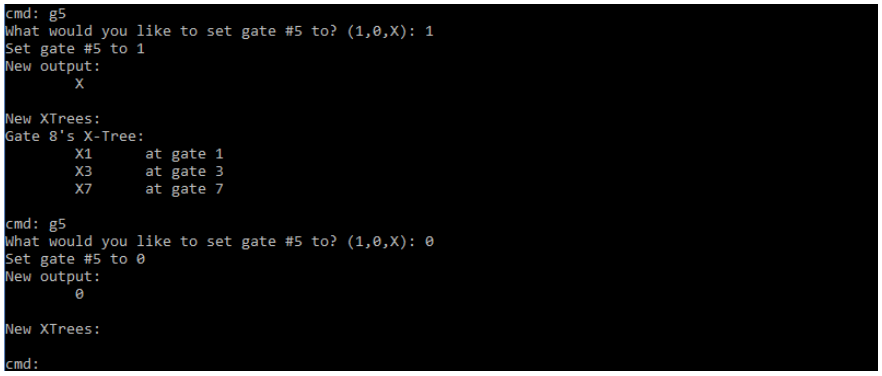


Figure 4.2: An example of the user interface and how to force a value on the output of a gate

Bibliography

[1] N. Sridhar and M. S. Hsiao, "On efficient error diagnosis of digital circuits," in *Proceedings International Test Conference 2001 (Cat. No.01CH37260)*, Nov 2001, pp. 678–687.

[2] X. Yu and R. D. Blanton, "Multiple defect diagnosis using no assumptions on failing pattern characteristics," in *2008 45th ACM/IEEE Design Automation Conference*, June 2008, pp. 361–366.

[3] J. B. Liu, A. Veneris, and H. Takahashi, "Incremental diagnosis of multiple open-interconnects," in *Proceedings. International Test Conference*, Oct 2002, pp. 1085–1092.

[4] V. D. Agrawal, D. H. Baik, Y. C. Kim, and K. K. Saluja, "Exclusive test and its applications to fault diagnosis," in *16th International Conference on VLSI Design, 2003. Proceedings.*, Jan 2003, pp. 143–148.

[5] B. Becker, M. Sauer, C. Scholl, and R. Wimmer, "Modeling unknown values in test and verification," *Formal Modeling and Verification of Cyber-Physical Systems*, pp. 122–150, 2015.