ECE 550, Fall 2017
Homework 1

For this homework, you will be answering three pencil and paper questions, as well as writing VHDL. You should submit your answers to the pencil and paper questions, along with your VHDL code in a .tar, .tar.gz, or .zip format (no other formats will be accepted) to Sakai before the deadline. Your answers to the pencil and paper questions must be in .pdf format (no Word documents will be accepted). For drawings, you are encouraged to draw with a computerized tool, but you may draw by hand and scan the drawings into a pdf format, as long as they are clear and easily readable.

Within one week of the submission deadline, you must demo your VHDL code to a TA, who will ask each group member to explain various aspects of how it works. All group members are responsible for understanding the entire submission.

Question 1 [8 points]

Draw the transistors required to form the following gates:

(a) A 3-input OR gate. [4]

(b) A 4-input NAND gate. [4]

Question 2 [10]

Given the following truth-table:

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(a) Write the sum-of-products formula for the truth table. [3]

(b) Simplify your formula as much as you can. [3]

(c) Draw the logic gates which correspond to your simplified formula. [4]

Question 3 [10]

Convert each of the following numbers to 8-bit signed 2's complement binary, then to hexadecimal (write both the binary and the hex). [2 pts/ea]

(a) 75

(b) -82

(c) 0

(d) -125

(e) 101

Question 4 [12]

Perform each of the following 8-bit additions. For each addition, give the result, and state whether or not the addition suffered from overflow (1) if the numbers are treated as signed (2's complement) numbers and (2) if the numbers are treated as unsigned numbers. Show your work! (for this problem, show where you carried). [3 pts/ea]

(f) 10100010 + 11011001

(g) 01010111 + 01010111

(h) 01011101 + 01101001

(i) 01010111 + 11111100

Question 5 (60 points)

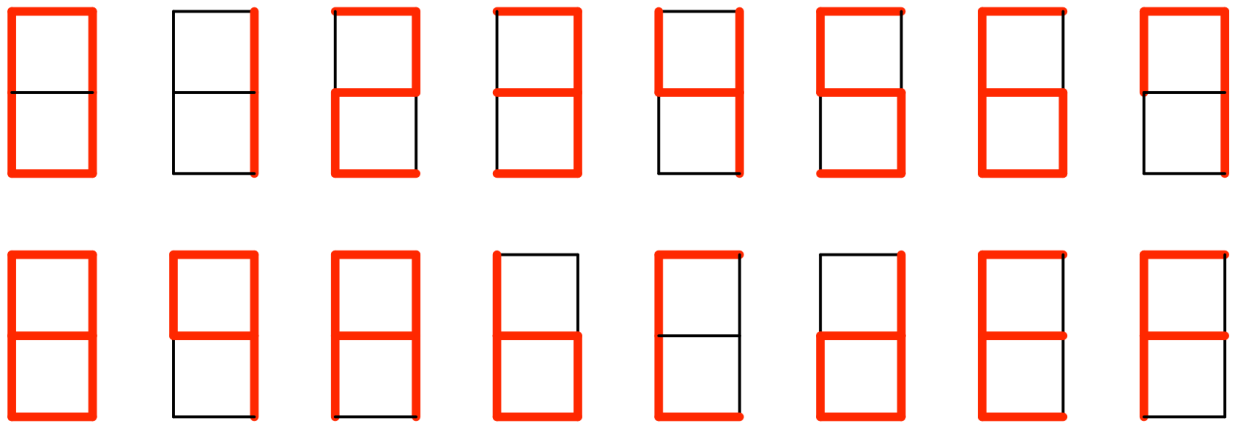
To begin this assignment, download the starter project "`hw1-leds.qar`" from the course site.

***Note**: For this and future assignments in this course, you should not use the VHDL "`process`" statement. The "`process`" statement is useful for specifying the behavior of complex sequential circuits, but its resemblance to software programming leads many introductory students astray, and it can trivialize some aspects of the assignments. If you're interested in completing your understanding of VHDL, including the "`process`" statement, you can take ECE559 ("Advanced Digital System Design"). Homework solutions which use a "`process`" statement will not receive credit.*

For this question, you will be writing VHDL. The DE2 boards have a row of 18 switches (`SW0..SW17`), as well as a set of 8 7-segment LEDs (`HEX0..HEX7`). For this question, you will read the 18 switches as a binary number, and displays it as a hexadecimal number on the 5 right-most (lowest numbered) LEDs.

You should note that the LED segments are "active low" (a value of 0 turns them on, and a value of 1 turns them off). The segments are numbered starting with 0 at the top, and increasing in a clockwise fashion around the outside segments. The horizontal middle segment is numbered 6.

You should use the following figure to show you how to lay out the segments for each hex digit:



Extra credit (+5 points): While KEY0 is depressed, instead of the number N, have the hex display show its one's complement (also known as "NOT N", or ~N).