1 research questions

1. What is the impact of reducing the digital-to-analog converter (DAC) resolution on dnpu performance in hardware and simulations?
   1.1. Is the effect of reducing the DAC resolution consistent over different parts of the input space of a single dnpu?
   1.2. Is the sensitivity to reducing the DAC resolution consistent for all activation electrodes?
   1.3. How is the accuracy of a dnpu for simple tasks affected by reducing the DAC resolution of control voltages?
      1.3.1. How is it affected for a single dnpu?
      1.3.2. How is it affected for different dnpu architectures?

2 experiments

2.1 What is the impact of reducing the digital-to-analog converter (DAC) resolution on dnpu performance in hardware and simulations?

- Create uniform distribution for 7 inputs
- Plot error distribution (error is original minus quantized)
- Plot MSE or RMSE of distribution (original vs quantized) vs number of bits
- Plot original output vs quantized output

2.2 Is the effect of reducing the DAC resolution consistent over different parts of the input space of a single dnpu?

To answer this question these options can be done:

- Create uniform distribution for 7 inputs
- The output from this distribution will be the control result
- Quantize this distribution
- For every point in the output find the error (non-quantized vs quantized)
- Sort the error from small to large
- Find the inputs for which the error is highest (f.e. top 10%)
- From here there are multiple options:

- Plot histogram of input voltages for every input electrode, this way a you can see the distribution for which parts of the inputs space per electrode the error is highest.
- Show IV-curves for electrodes

Second experiment:

- Using the outputs of the uniform distribution create:
- Plots which for discretized parts of the input space for single electrodes show the error distribution. (Find every input from the distribution where the input voltage for electrode 1 is between -1 and -0.8 and find the error distribution for these inputs. Repeat this for the whole input range of the electrode and then for every electrode)

2.3 Is the sensitivity to reducing the DAC resolution consistent for all activation electrodes?

To answer this question the following can be done:

- Create a uniform distribution for 7 inputs, this will be the control result
- Start by quantizing 1 input and keeping the rest of the inputs at full precision
- Find mse (non-quantized vs quantized)
- Repeat this for every configuration of quantized and non-quantized inputs
- Then we can compare the mse to see on which electrodes the error is highest

2.4 How is the accuracy of a single dnpu for simple tasks affected by reducing the DAC resolution of control voltages?

2.4.1 How is it affected for a single dnpu?

- Find 10 solutions for Ring Classification
- Quantize the control voltages for solutions
- Plot accuracy vs bits
- Potential plots are also mse (original output vs quantized) vs bits
- Repeat for different size gaps

2.4.2 How is it affected for different dnpu architectures?

- same procedure as 3.3 but now for different architectures (2-1 or other options)
- Here can also be looked at if the running mean and variance of the batch normalization still represent the actual mean and variance of the quantized outputs of the layer.
- the architectures investigated will be a 2-1 architecture and a 3 dnpu layer
- For the 3 dnpu layer options are:
  1. Connect the 3 dnpus to a single dnpu with 3 inputs
  2. Pass the output of the 3 dnpu layer to a linear layer which maps from 3 to 1 dimensions
  3. Sum outputs of 3 dnpus (It seems this comes closest to actual use of a 3 dnpu layer as there are no extra learnable parameters)