



### FEATURES

RF frequency: 700 MHz to 3000 MHz, continuous

LO input frequency: 200 MHz to 2700 MHz, high-side or low-side injection

IF range: 40 MHz to 500 MHz

Power conversion gain of 9.0 dB

Single sideband (SSB) noise figure of 11.3 dB

Input IP3 of 30 dBm

Input P1dB of 10.6 dBm

Typical LO input drive of 0 dBm

Single-ended, 50  $\Omega$  RF port

Single-ended or balanced LO input port

Serial port interface (SPI) control on all functions

Exposed pad, 7 mm  $\times$  7 mm, 48-lead LFCSP

### APPLICATIONS

Multiband/multistandard cellular base station diversity receivers

Wideband radio link diversity downconverters

Multimode cellular extenders and picocells

### FUNCTIONAL BLOCK DIAGRAM

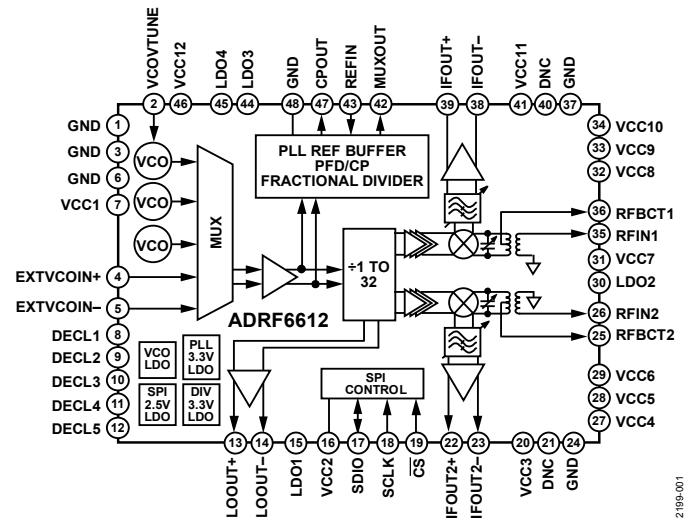


Figure 1.

### GENERAL DESCRIPTION

The [ADRF6612](#) is a dual radio frequency (RF) mixer and intermediate frequency (IF) amplifier with an integrated phase-locked loop (PLL) and voltage controlled oscillators (VCOs). The [ADRF6612](#) uses revolutionary broadband square wave limiting local oscillator (LO) amplifiers to achieve an unprecedented RF bandwidth of 700 MHz to 3000 MHz. Unlike narrow-band sine wave LO amplifier solutions, the LO can be applied above or below the RF input over an extremely wide bandwidth. Energy storage elements are not utilized in the LO amplifier, thus dc current consumption also decreases with decreasing LO frequency.

The [ADRF6612](#) utilizes highly linear, doubly balanced passive mixer cores with integrated RF and LO balancing circuits to allow single-ended operation. Integrated RF baluns allow optimal performance over the 700 MHz to 3000 MHz RF input frequency. The balanced passive mixer arrangement provides outstanding LO to RF and LO to IF leakages, excellent RF to IF isolation, and excellent intermodulation performance over the full RF bandwidth.

The balanced mixer cores provide extremely high input linearity, allowing the device to be used in demanding

wideband applications where in band blocking signals may otherwise result in the degradation of dynamic range. Noise performance under blocking is comparable to narrow-band passive mixer designs. High linearity IF buffer amplifiers follow the passive mixer cores, yielding typical power conversion gains of 9 dB, and can be matched to a wide range of output impedances.

The PLL architecture supports both integer-N and fractional-N operation and can generate the entire LO frequency range of 200 MHz to 2700 MHz using an external reference input frequency anywhere in the range of 12 MHz to 320 MHz. An external loop filter provides flexibility in trading off phase noise vs. acquisition time. To reduce fractional spurs in fractional-N mode, a sigma-delta ( $\Sigma$ - $\Delta$ ) modulator controls the post-VCO programmable divider. The VCO consists of multiple VCO cores.

All features of the [ADRF6612](#) are controlled via a 3-wire SPI resulting in optimum performance and minimum external components.

The [ADRF6612](#) is fabricated using a BiCMOS, high performance IC process. The device is available in a 7 mm  $\times$  7 mm, 48-lead LFCSP package and operates over a  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range. An evaluation board is available.

# ADRF6612\* Product Page Quick Links

Last Content Update: 08/30/2016

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## Evaluation Kits

- ADRF6612 Evaluation Board

## Documentation

### Data Sheet

- ADRF6612: 700 MHz to 3000MHz Dual Passive Receive Mixer with Integrated PLL and VCO Data Sheet

### User Guides

- UG-968: Evaluating the ADRF6612/ADRF6614, 700 MHz to 3000 MHz Rx Dual Mixer with Integrated Fractional-N PLL and VCO

## Reference Materials

### Press

- Analog Devices Introduces High-Performance RF ICs for Multi-band Base Stations and Microwave Point-to-Point Radios

## Design Resources

- ADRF6612 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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## REVISION HISTORY

### 5/2016—Rev. 0 to Rev. A

Changes to Table 19 .....	32
Changes to Address: 0x22, Reset: 0x000A, Name: VCO_CTRL1 Section and Table 34 .....	45
Updated Outline Dimensions .....	57
Changes to Ordering Guide .....	57

### 12/2014—Revision 0: Initial Version

## SPECIFICATIONS

### RF SPECIFICATIONS

$T_A = 25^\circ\text{C}$ ,  $f_{\text{RF}} = 1900\text{ MHz}$ ,  $f_{\text{LO}} = 1697\text{ MHz}$ ,  $Z_O = 50\ \Omega$ , frequency of the reference ( $f_{\text{REF}} = 122.88\text{ MHz}$ ,  $f_{\text{REF}}$  power = 4 dBm,  $f_{\text{PFD}} = 1.536\text{ MHz}$ , low-side LO injection, optimum RF balun (RFB) and low-pass filter (LPF) settings, unless otherwise noted.

**Table 1. High Performance Mode**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INTERFACE					
Return Loss	Tunable to >20 dB broadband via serial port		17.9		dB
Input Impedance			50		$\Omega$
RF Frequency Range ( $f_{\text{RF}}$ )		700		3000	MHz
IF OUTPUT INTERFACE					
Output Impedance	Differential impedance, $f = 200\text{ MHz}$		300  1.5		$\Omega$   pF
IF Frequency Range		40		500	MHz
DC Bias Voltage <sup>1</sup>	Externally generated		IFOUTx $\pm$		V
EXTERNAL LO INPUT					
External LO Power Input	External VCO input supports divide by 1, 2, 4, 8, 16, and 32 Low-side or high-side LO, internally or externally generated	−5	0	+5	dBm
Return Loss			−11		dB
Input Impedance			50		$\Omega$
External VCO Input Frequency		250		5700	MHz
LO Frequency Range		250		2850	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	4:1 IF port transformer and printed circuit board (PCB) loss removed		9.0		dB
Voltage Conversion Gain	$Z_{\text{SOURCE}} = 50\ \Omega$ , differential $Z_{\text{LOAD}} = 200\ \Omega$		15.0		dB
SSB Noise Figure			11.3		dB
IF Output Phase Noise Under Blocking	10 dBm blocker present 10 MHz above desired RF input, $f_{\text{RF}} = 1900\text{ MHz}$ , $f_{\text{BLOCK}} = 1910\text{ MHz}$ , $f_{\text{LO}} = 1697\text{ MHz}$ , IF = 203 MHz, IF <sub>BLOCKER</sub> = 213 MHz		−153		dBc/Hz
Input Third-Order Intercept (IIP3)	$f_{\text{RF}1} = 1900\text{ MHz}$ , $f_{\text{RF}2} = 1901\text{ MHz}$ , $f_{\text{LO}} = 1697\text{ MHz}$ , each RF tone at −10 dBm		30		dBm
Input Second-Order Intercept (IIP2)	$f_{\text{RF}1} = 1900\text{ MHz}$ , $f_{\text{RF}2} = 1950\text{ MHz}$ , $f_{\text{LO}} = 1697\text{ MHz}$ , each RF tone at −10 dBm		60		dBm
Input 1 dB Compression Point (P1dB)			10.6		dBm
LO to IF Output Leakage	Unfiltered IF output		−35		dBm
LO to RF Input Leakage			−45		dBm
RF to IF Output Isolation			−22		dB
IF/2 Spurious	−10 dBm input power		−72		dBc
IF/3 Spurious	−10 dBm input power		−69		dBc
POWER INTERFACE					
VCC12, VCC7, VCC2, VCC1		3.55	3.7	3.85	V
Supply Voltage					
Quiescent Current			260		mA
VCC3, VCC4, VCC5, VCC6, VCC8, VCC9, VCC10, VCC11, IFOUT1+, IFOUT1−, IFOUT2+, IFOUT2−		3.55	5	5.25	V
Supply Voltage					
Quiescent Current			214		mA
LO OUTPUT (LOOUT+, LOOUT−)					
Frequency Range	Adjustable via SPI in four steps, in 50 $\Omega$ balanced load	200		2700	MHz
Output Level		−5		+7	dBm
Output Impedance			50		$\Omega$

<sup>1</sup> Supply voltage must be applied from the external circuit through choke inductors.

$T_A = 25^\circ\text{C}$ ,  $f_{RF} = 1900\text{ MHz}$ ,  $f_{LO} = 1697\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $f_{REF} = 122.88\text{ MHz}$ ,  $f_{REF}\text{ power} = 4\text{ dBm}$ ,  $f_{PFD} = 1.536\text{ MHz}$ , low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

Table 2. High Efficiency Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
Power Conversion Gain	4:1 IF port transformer and PCB loss removed		8.7		dB
Voltage Conversion Gain	$Z_{SOURCE} = 50\ \Omega$ , differential $Z_{LOAD} = 200\ \Omega$		14.7		dB
SSB Noise Figure			10.7		dB
Input Third-Order Intercept (IIP3)	$f_{RF1} = 1900\text{ MHz}$ , $f_{RF2} = 1901\text{ MHz}$ , $f_{LO} = 1697\text{ MHz}$ , each RF tone at $-10\text{ dBm}$		20.5		dBm
Input Second-Order Intercept (IIP2)	$f_{RF1} = 1900\text{ MHz}$ , $f_{RF2} = 1950\text{ MHz}$ , $f_{LO} = 1697\text{ MHz}$ , each RF tone at $-10\text{ dBm}$		53		dBm
Input 1 dB Compression Point (P1dB)			8.2		dBm
LO to IF Output Leakage	Unfiltered IF output		-45.0		dBm
LO to RF Input Leakage			-52.0		dBm
RF to IF Output Isolation			-22.8		dB
IF/2 Spurious	$-10\text{ dBm}$ input power		-58		dBc
IF/3 Spurious	$-10\text{ dBm}$ input power		-58		dBc
<b>POWER INTERFACE</b>					
VCC12, VCC7, VCC2, VCC1					
Supply Voltage		3.55	3.7	3.85	V
Quiescent Current			260		mA
VCC3, VCC4, VCC5, VCC6, VCC8, VCC9, VCC10, VCC11, IFOUT1+, IFOUT1-, IFOUT2+, IFOUT2-					
Supply Voltage		3.55	3.7	5.25	V
Quiescent Current			210		mA

## SYNTHESIZER/PLL SPECIFICATIONS

High performance mode,  $T_A = 25^\circ\text{C}$ , measured on LO output,  $f_{LO} = 1700\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $f_{REF} = 122.88\text{ MHz}$ ,  $f_{PFD} = 1.536\text{ MHz}$ ,  $f_{REF}\text{ power} = 4\text{ dBm}$ ,  $CSCALE = 8\text{ mA}$ ,  $bleed = 0\ \mu\text{A}$ ,  $ABLDLY = 0.9\text{ ns}$ , integer mode loop filter, unless otherwise noted.

Table 3. Integer Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>SYNTHESIZER SPECIFICATIONS</b>					
Frequency Range	Synthesizer specifications referenced to $1 \times \text{LO}$	200		2700	MHz
Figure of Merit (FOM) <sup>1</sup>	Internally generated LO		-223		dBc/Hz/Hz
Phase and Frequency Detector (PFD)	$P_{REFIN} = 6.5\text{ dBm}$	0.8		70	MHz
Frequency ( $f_{PFD}$ )					
Reference Spurs	$f_{PFD} = 1.536\text{ MHz}$				
	$1 \times f_{PFD}$		-105		dBc
	$4 \times f_{PFD}$		-105		dBc
	$>4 \times f_{PFD}$		-90		dBc
<b>CHARGE PUMP</b>					
Pump Current	Programmable to $250\ \mu\text{A}$ , $500\ \mu\text{A}$ , ..., $8\text{ mA}$		8	8.75	mA
Output Compliance Range		0.7		2.5	V
<b>REFERENCE CHARACTERISTICS</b>					
REFIN Input Frequency	REFIN, MUXOUT pins	12		320	MHz
REFIN Input Capacitance			4		pF
Reference Divider Value	Programmable to 0.5, 1, 2, 3, ..., 2047	0.5		2047	
MUXOUT Output Level	VOL (lock detect output selected)			0.25	V
	VOH (lock detect output selected)	2.7			V
MUXOUT Duty Cycle	Reference output selected		50		%

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCO_0					
Phase Noise, Locked	$f_{LO} = 5.1$ GHz				
	1 kHz offset		–87		dBc/Hz
	50 kHz offset		–94.9		dBc/Hz
	100 kHz offset		–103.3		dBc/Hz
	1 MHz offset		–132.9		dBc/Hz
	10 MHz offset		–154.1		dBc/Hz
	40 MHz offset		–155.2		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.87		°rms
VCO_1					
Phase Noise, Locked	$f_{LO} = 4.45$ GHz				
	1 kHz offset		–90		dBc/Hz
	50 kHz offset		–98.4		dBc/Hz
	100 kHz offset		–106.5		dBc/Hz
	1 MHz offset		–136.1		dBc/Hz
	10 MHz offset		–154.8		dBc/Hz
	40 MHz offset		–155.5		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.63		°rms
VCO_2					
Phase Noise, Locked	$f_{LO} = 3.8$ GHz				
	1 kHz offset		–90		dBc/Hz
	50 kHz offset		–98.1		dBc/Hz
	100 kHz offset		–109.8		dBc/Hz
	1 MHz offset		–137.1		dBc/Hz
	10 MHz offset		–155.7		dBc/Hz
	40 MHz offset		–156.2		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.61		°rms
VCO_3					
Phase Noise, Locked	$f_{LO} = 3.2$ GHz				
	1 kHz offset		–89		dBc/Hz
	50 kHz offset		–97.2		dBc/Hz
	100 kHz offset		–107		dBc/Hz
	1 MHz offset		–136.2		dBc/Hz
	10 MHz offset		–155.7		dBc/Hz
	40 MHz offset		–157.3		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.64		°rms

<sup>1</sup> The FOM is computed as phase noise (dBc/Hz) – 10Log10( $f_{PFD}$ ) – 20Log10( $f_{LO}/f_{PFD}$ ). The FOM was measured across the full LO range, with  $f_{REF} = 122.88$  MHz and  $f_{REF}$  power = 6.5 dBm with a 1.536 MHz  $f_{PFD}$ . The FOM was computed at 50 kHz offset.

High performance mode,  $T_A = 25^\circ\text{C}$ , measured on LO output,  $f_{LO} = 1700\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $f_{REF} = 122.88\text{ MHz}$ ,  $f_{PPD} = 30.72\text{ MHz}$ ,  $f_{REF}\text{ power} = 4\text{ dBm}$ ,  $CSCALE = 250\ \mu\text{A}$ ,  $bleed = 93.75\ \mu\text{A}$ ,  $ABLDLY = 0\text{ ns}$ , fractional mode loop filter, unless otherwise noted.

Table 4. Fractional Mode

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to $1 \times \text{LO}$				
FOM <sup>1</sup>	$P_{REFIN} = 6.5\text{ dBm}$		219		dBc/Hz/Hz
REFERENCE CHARACTERISTICS	REFIN, MUXOUT pins				
VCO_0					
Phase Noise, Locked	$f_{LO} = 2.55\text{ GHz}$				
	1 kHz offset		-92.5		dBc/Hz
	50 kHz offset		-97.4		dBc/Hz
	100 kHz offset		-109.7		dBc/Hz
	1 MHz offset		-137.6		dBc/Hz
	10 MHz offset		-153.6		dBc/Hz
	40 MHz offset		-155.5		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.36		°rms
VCO_1					
Phase Noise, Locked	$f_{LO} = 2.22\text{ GHz}$				
	1 kHz offset		-93.6		dBc/Hz
	50 kHz offset		-101.8		dBc/Hz
	100 kHz offset		-112.5		dBc/Hz
	1 MHz offset		-140.5		dBc/Hz
	10 MHz offset		-154.3		dBc/Hz
	40 MHz offset		-155.3		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.32		°rms
VCO_2					
Phase Noise, Locked	$f_{LO} = 1.9\text{ GHz}$				
	1 kHz offset		-94.2		dBc/Hz
	50 kHz offset		-101.7		dBc/Hz
	100 kHz offset		-112.4		dBc/Hz
	1 MHz offset		-141.3		dBc/Hz
	10 MHz offset		-155.8		dBc/Hz
	40 MHz offset		-156.8		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.32		°rms
VCO_3					
Phase Noise, Locked	$f_{LO} = 1.6\text{ GHz}$				
	1 kHz offset		-93.1		dBc/Hz
	50 kHz offset		-99.8		dBc/Hz
	100 kHz offset		-110.9		dBc/Hz
	1 MHz offset		-140.2		dBc/Hz
	10 MHz offset		-155.7		dBc/Hz
	40 MHz offset		-157.2		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.33		°rms

<sup>1</sup> The FOM is computed as phase noise (dBc/Hz) -  $10\log_{10}(f_{PPD}) - 20\log_{10}(f_{LO}/f_{PPD})$ . The FOM was measured across the full LO range, with  $f_{REF} = 122.88\text{ MHz}$  and  $f_{REF}\text{ power} = 6.5\text{ dBm}$  with a  $30.72\text{ MHz } f_{PPD}$ . The FOM was computed at 45 kHz offset.

**VCO SPECIFICATIONS, OPEN-LOOP**

High performance mode,  $T_A = 25^\circ\text{C}$ , measured on LO output, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCO_0 PHASE NOISE	$f_{\text{VCO}} = 5.15 \text{ GHz}$				
	1 kHz offset		−50		dBc/Hz
	50 kHz offset		−104.4		dBc/Hz
	100 kHz offset		−112.6		dBc/Hz
	1 MHz offset		−137.7		dBc/Hz
	10 MHz offset		−154		dBc/Hz
	40 MHz offset		−155.1		dBc/Hz
VCO_1 PHASE NOISE	$f_{\text{VCO}} = 4.3 \text{ GHz}$				
	1 kHz offset		−54		dBc/Hz
	50 kHz offset		−106.1		dBc/Hz
	100 kHz offset		−115		dBc/Hz
	1 MHz offset		−138.9		dBc/Hz
	10 MHz offset		−155.8		dBc/Hz
	40 MHz offset		−155.2		dBc/Hz
VCO_2 PHASE NOISE	$f_{\text{VCO}} = 3.8 \text{ GHz}$				
	1 kHz offset		−53.6		dBc/Hz
	50 kHz offset		−106.6		dBc/Hz
	100 kHz offset		−114.6		dBc/Hz
	1 MHz offset		−140.8		dBc/Hz
	10 MHz offset		−155.4		dBc/Hz
	40 MHz offset		−156.3		dBc/Hz
VCO_3 PHASE NOISE	$f_{\text{VCO}} = 3.2 \text{ GHz}$				
	1 kHz offset		−48.5		dBc/Hz
	50 kHz offset		−106		dBc/Hz
	100 kHz offset		−115.3		dBc/Hz
	1 MHz offset		−140.2		dBc/Hz
	10 MHz offset		−157.7		dBc/Hz
	40 MHz offset		−156.3		dBc/Hz



## LOGIC INPUT AND POWER SPECIFICATIONS

$T_A = 25^\circ\text{C}$ ,  $f_{RF} = 1900\text{ MHz}$ ,  $f_{LO} = 1697\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $f_{REF} = 122.88\text{ MHz}$ ,  $f_{REF}\text{ power} = 4\text{ dBm}$ ,  $f_{PFD} = 1.536\text{ MHz}$ , low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS	SCLK, SDIO, $\overline{CS}$				
Input High Voltage, $V_{IH}$		1.4		3.3	V
Input Low Voltage, $V_{IL}$		0		0.7	V
Input Current, $I_{INH}/I_{INL}$			0.1		$\mu\text{A}$
POWER SUPPLIES					
High Performance Mode					
Voltage Range					
VCC3, VCC4, VCC5, VCC6, VCC8, VCC9, VCC10, VCC11, IFOUT1+, IFOUT1-, IFOUT2+, IFOUT2-, VCC12, VCC7, VCC2, VCC1		4.75	5	5.25	V
Power Dissipation	Internal LO mode (internal PLL)	3.55	3.7	5.25	W
	External LO output enabled		2.7		W
	External LO output disabled		2.5		W
High Efficiency Mode					
Voltage Range					
VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, VCC9, VCC10, VCC11, VCC12, IFOUT1+, IFOUT1-, IFOUT2+, IFOUT2-		3.55	3.7	3.85	V
Power Dissipation	Internal LO mode (internal PLL)				
	External LO output enabled		2.0		W
	External LO output disabled		1.8		W

## DIGITAL LOGIC SPECIFICATIONS

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Input Voltage High	$V_{IH}$		1.4			V
Input Voltage Low	$V_{IL}$				0.70	V
Output Voltage High	$V_{OH}$	$I_{OH} = -100 \mu A$	2.3			V
Output Voltage Low	$V_{OL}$	$I_{OL} = 100 \mu A$			0.2	V
Serial Clock Period	$t_{CLK}$		38			ns
Setup Time Between Data and Rising Edge of SCLK	$t_{DS}$		8			ns
Hold Time Between Data and Rising Edge of SCLK	$t_{DH}$		8			ns
Setup Time Between Falling Edge of $\overline{CS}$ and SCLK	$t_S$		10			ns
Hold Time Between Rising Edge of $\overline{CS}$ and SCLK	$t_H$		10			ns
Minimum Period for SCLK to Be in a Logic High State	$t_{HIGH}$		10			ns
Minimum Period for SCLK to Be in a Logic Low State	$t_{LOW}$		10			ns
Maximum Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	$t_{ACCESS}$				231	ns
Maximum Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance	$t_Z$				5	ns

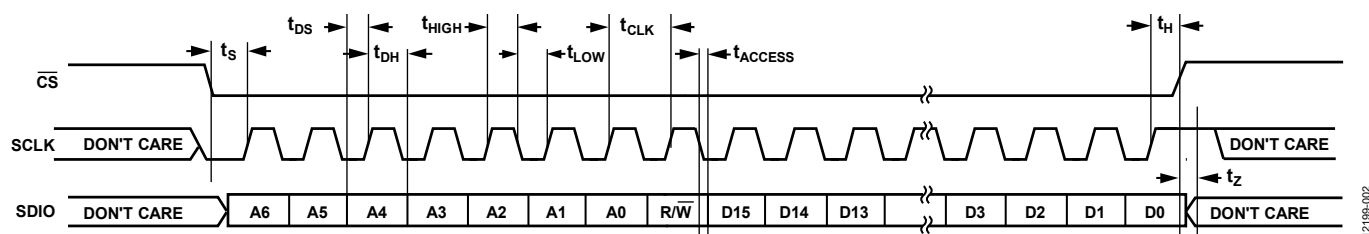


Figure 2. Setup and Hold Timing Measurements

12199-002

## ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Supply Voltage (VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7, VCC8, VCC9, VCC10, VCC11, VCC12, IFOUT1+, IFOUT1–, IFOUT2+, IFOUT2–)	–0.5 V to +5.5 V
Digital Input/Output (SCLK, SDIO, $\overline{CS}$ )	–0.3 V to +3.6 V
RFINx	20 dBm
EXTVCOIN+, EXTVCOIN–	13 dBm
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JC}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 9. Thermal Resistance

Package Type	$\theta_{JC}$	Unit
48-Lead LFCSP	1.62	°C/W

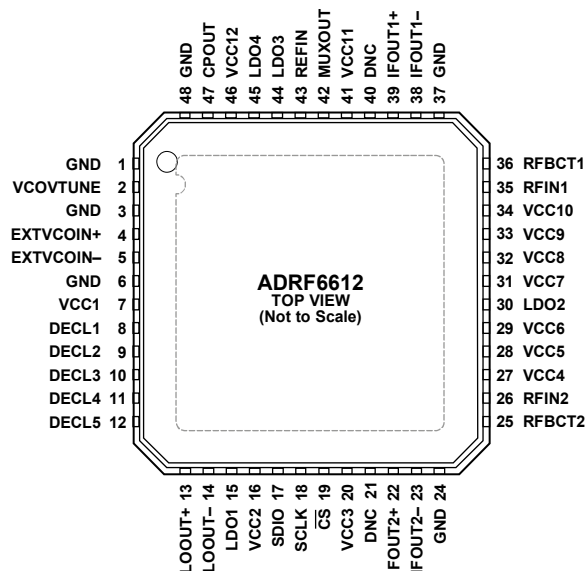
## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. DNC = DO NOT CONNECT.
2. THE EXPOSED PAD MUST BE CONNECTED TO A GROUND PLANE WITH LOW THERMAL IMPEDANCE.

12196-003

Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Common Ground Connection for External Loop Filter.
2	VCOVTUNE	Control Voltage for Internal VCO.
3, 6	GND	Common Ground for External VCO.
4, 5	EXTVCoin+, EXTVCoin-	Inputs from External VCO to Internal Divider.
7	VCC1	3.7 V VCO Supply.
8, 9	DECL1, DECL2	LDO Output Decouplers for VCO.
10, 11	DECL3, DECL4	External Decouplers for VCO Buffer.
12	DECL5	External Decoupler for VCO Circuitry.
13, 14	LOOUT+, LOOUT-	Differential Outputs of Internally Generated LO.
15	LDO1	External Decoupling for Internal 2.5 V SPI Port LDO.
16	VCC2	3.7 V Supply for Programmable SPI Port.
17	SDIO	Serial Data Input/Output for Programmable SPI Port.
18	SCLK	Clock for Programmable SPI Port.
19	CS	SPI Chip Select, Asserted Low.
20, 41	VCC3, VCC11	5 V Biases for Channel 1 and Channel 2 IF.
21, 40	DNC	Do Not Connect. Do not connect this pin externally.
22, 23	IFOUT2+, IFOUT2-	Channel 2 Differential IF Outputs.
24, 37	GND, GND	Ground Connections for Channel 1 and Channel 2 IF Stage.
25	RFBCT2	Balun Center Tap Connection for Channel 2 RF Input.
26	RFIN2	Channel 2 RF Input.
27, 28, 29	VCC4, VCC5, VCC6	5 V Supplies for Mixer LO Amplifiers.
30	LDO2	External Decoupling for Internal 3.3 V PLL/Divider LDO.
31	VCC7	3.7 V Supply for Mixer LO Divider Chain.
32, 33, 34	VCC8, VCC9, VCC10	5 V Supplies for Mixer LO Amplifiers.
35	RFIN1	Channel 1 RF Input.
36	RFBCT1	Balun Center Tap Connection for Channel 1 RF Input.
38, 39	IFOUT1-, IFOUT1+	Channel 1 Differential IF Outputs.
42	MUXOUT	Internal Multiplexer Output.

Pin No.	Mnemonic	Description
43	REFIN	Reference Input for Internal PLL (Single-Ended, CMOS).
44	LDO3	External Decoupling for Internal 2.5 V PLL LDO.
45	LDO4	External Decoupling for Internal 3.3 V PLL LDO.
46	VCC12	3.7 V Supply for Internal PLL.
47	CPOUT	Charge Pump Output.
48	GND	Common Ground for External Charge Pump.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

## TYPICAL PERFORMANCE CHARACTERISTICS

### MIXER, HIGH PERFORMANCE MODE

$T_A = 25^\circ\text{C}$ ,  $f_{RF} = 1900\text{ MHz}$ ,  $f_{LO} = 1697\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $f_{REF} = 122.88\text{ MHz}$ ,  $f_{REF}$  power = 4 dBm, low-side LO injection, optimum RFB and LPF settings, unless otherwise noted. For integer mode:  $f_{PFD} = 1.536\text{ MHz}$ ,  $CSCALE = 8\text{ mA}$ , bleed = 0  $\mu\text{A}$ ,  $ABLDLY = 0.9\text{ ns}$ . For fractional mode:  $f_{PFD} = 30.72\text{ MHz}$ ,  $CSCALE = 250\ \mu\text{A}$ , bleed = 93.75  $\mu\text{A}$ ,  $ABLDLY = 0.0\text{ ns}$ .

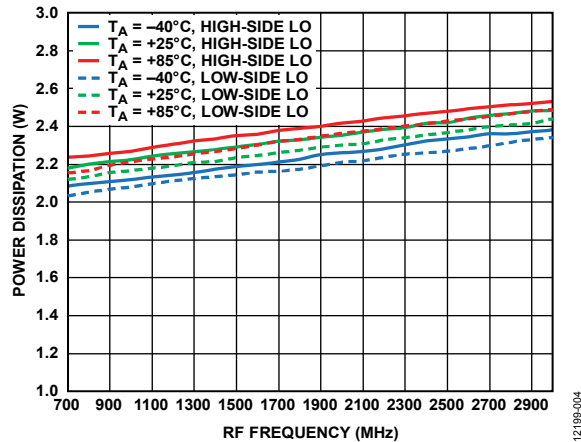


Figure 4. Power Dissipation vs. RF Frequency over Three Temperatures

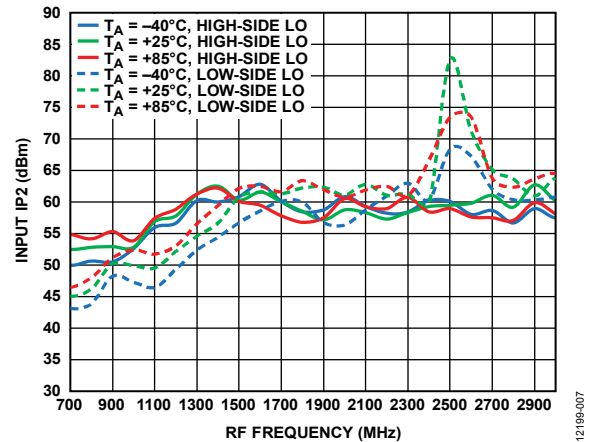


Figure 7. Input IP2 vs. RF Frequency over Three Temperatures

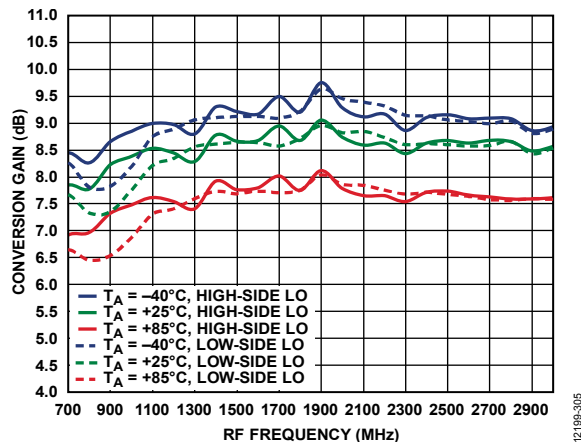


Figure 5. Power Conversion Gain vs. RF Frequency over Three Temperatures, IF Balun and Board Loss Removed

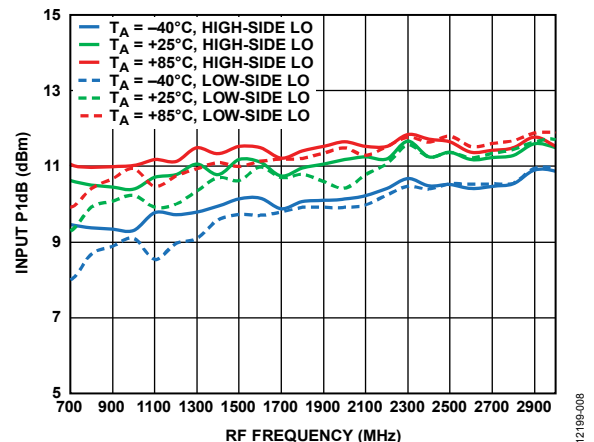


Figure 8. Input P1dB vs. RF Frequency over Three Temperatures

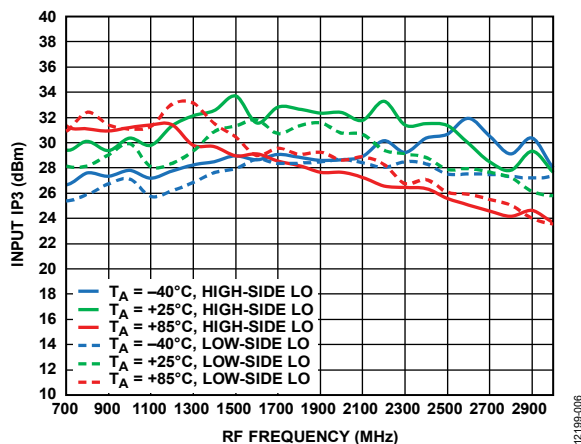


Figure 6. Input IP3 vs. RF Frequency over Three Temperatures

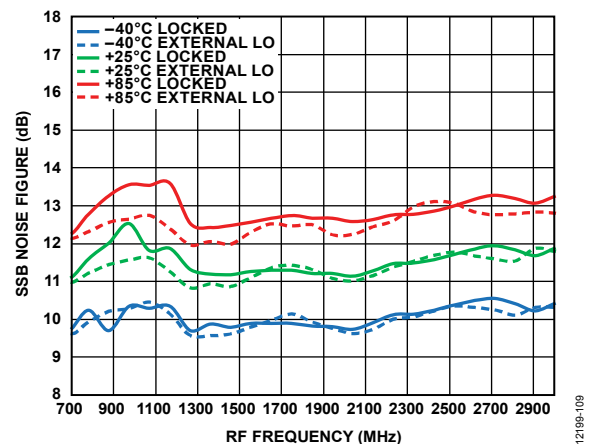


Figure 9. SSB Noise Figure vs. RF Frequency over Three Temperatures

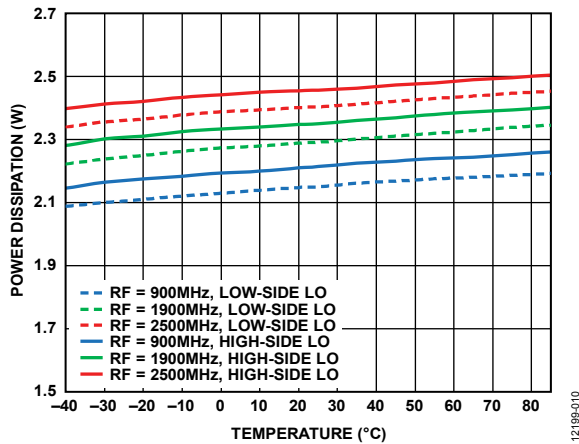


Figure 10. Power Dissipation vs. Temperature for Three RF Frequencies

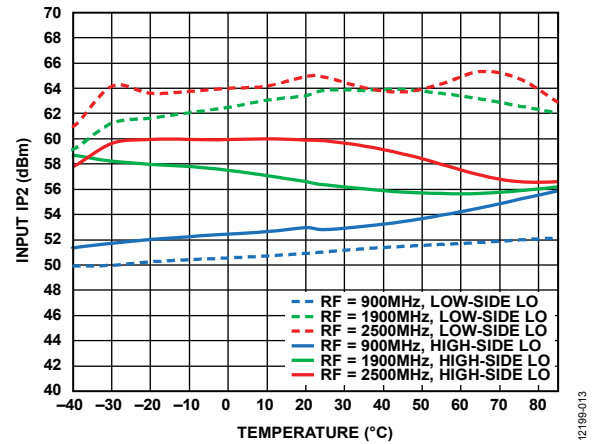


Figure 13. Input IP2 vs. Temperature for Three RF Frequencies

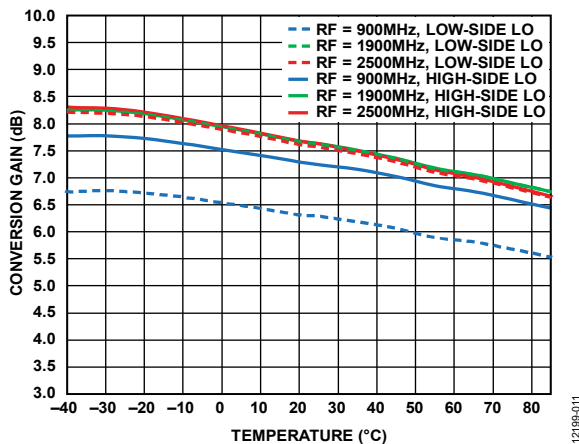


Figure 11. Power Conversion Gain vs. Temperature for Three RF Frequencies

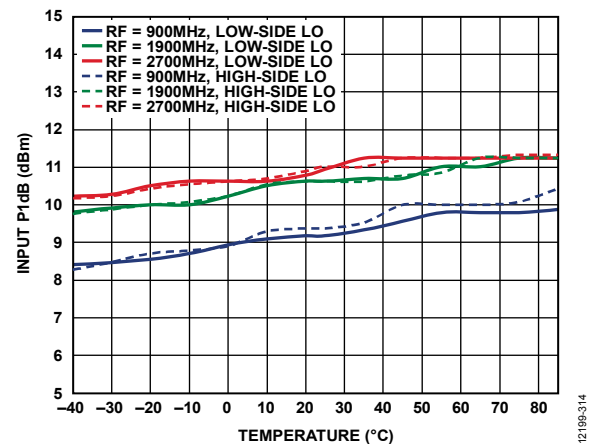


Figure 14. Input P1dB vs. Temperature for Three RF Frequencies

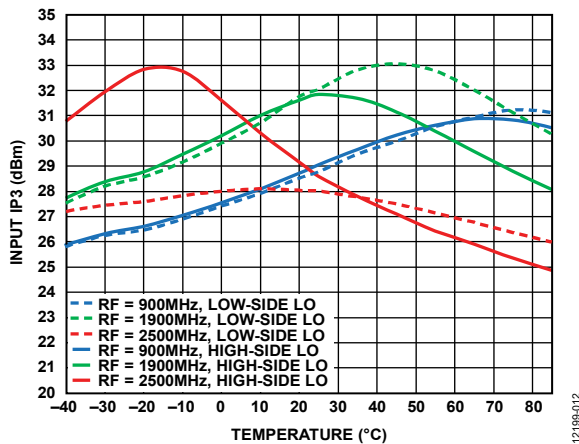


Figure 12. Input IP3 vs. Temperature for Three RF Frequencies

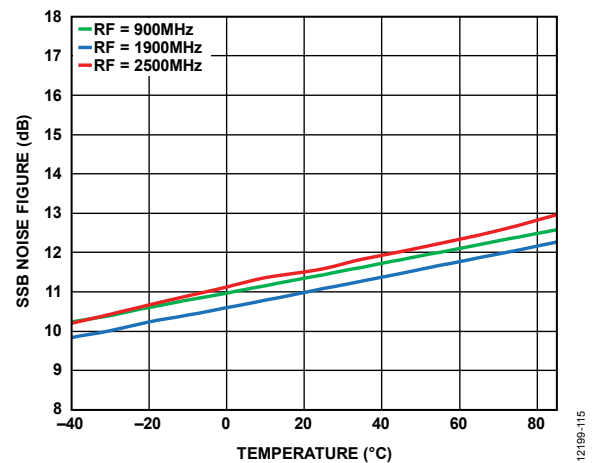


Figure 15. SSB Noise Figure vs. Temperature for Three RF Frequencies

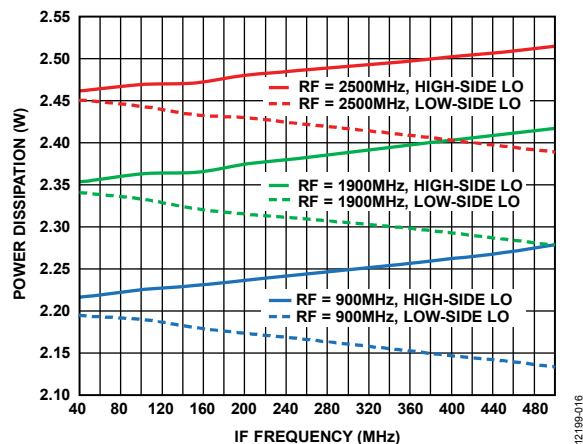


Figure 16. Power Dissipation vs. IF Frequency for Three RF Frequencies

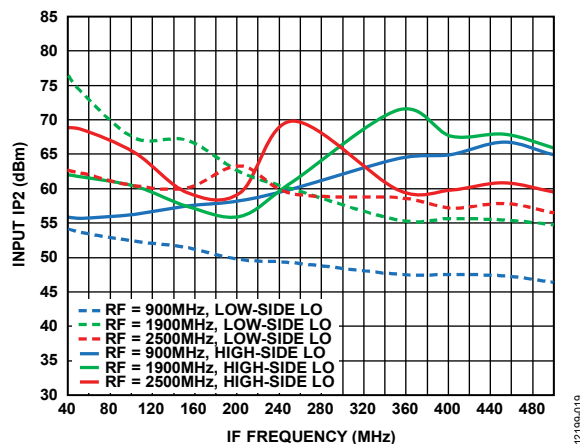


Figure 19. Input IP2 vs. IF Frequency for Three RF Frequencies

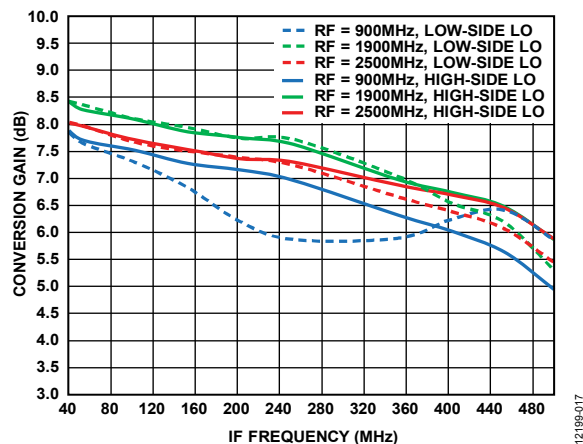


Figure 17. Power Conversion Gain vs. IF Frequency for Three RF Frequencies

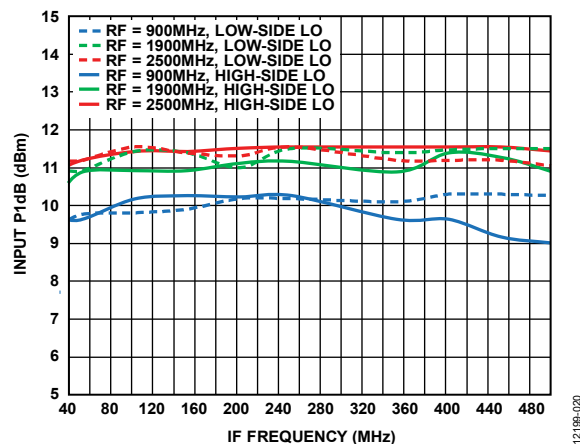


Figure 20. Input P1dB vs. IF Frequency for Three RF Frequencies

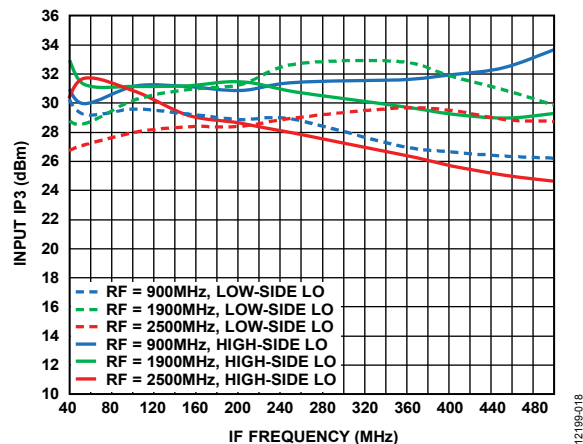


Figure 18. Input IP3 vs. IF Frequency for Three RF Frequencies

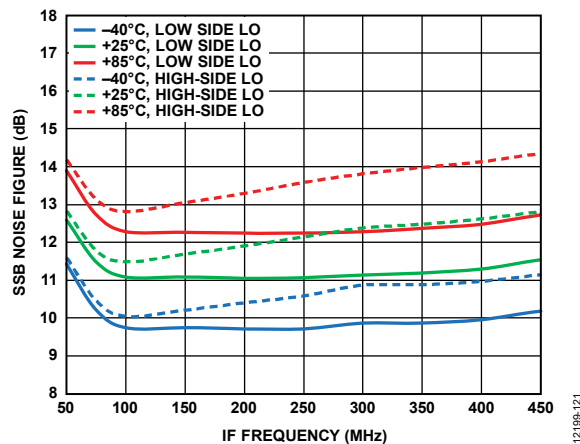


Figure 21. SSB Noise Figure vs. IF Frequency for Three RF Frequencies



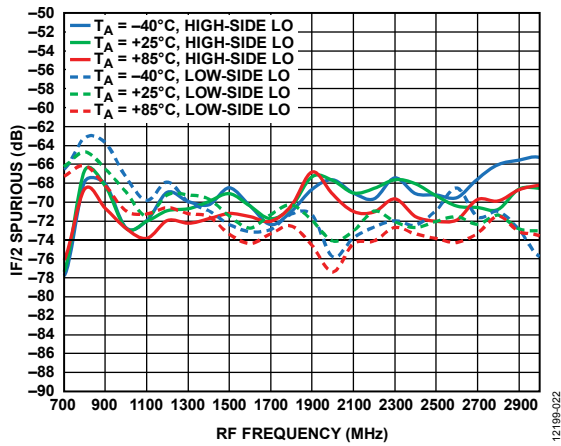


Figure 22. IF/2 Spurious vs. RF Frequency over Three Temperatures

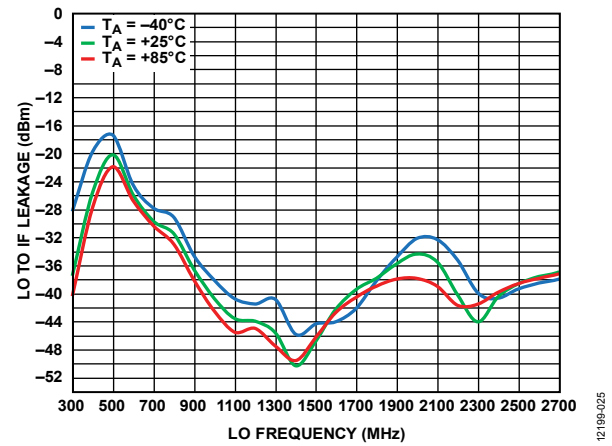


Figure 25. LO to IF Leakage vs. LO Frequency over Three Temperatures

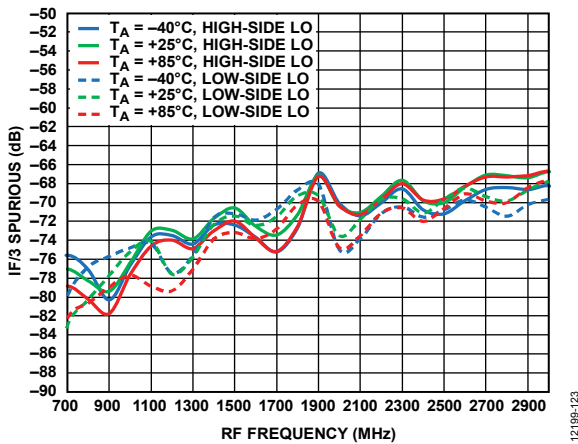


Figure 23. IF/3 Spurious vs. RF Frequency over Three Temperatures

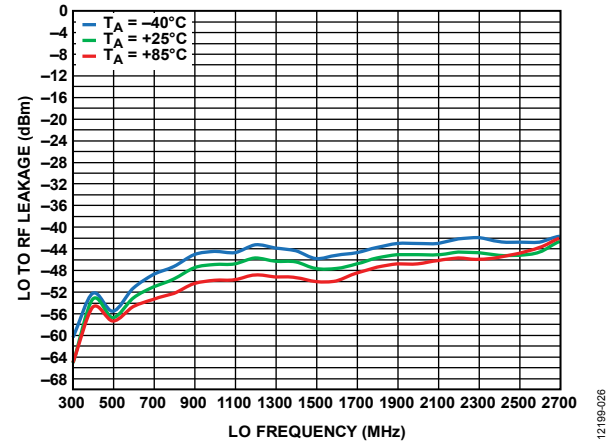


Figure 26. LO to RF Leakage vs. LO Frequency over Three Temperatures

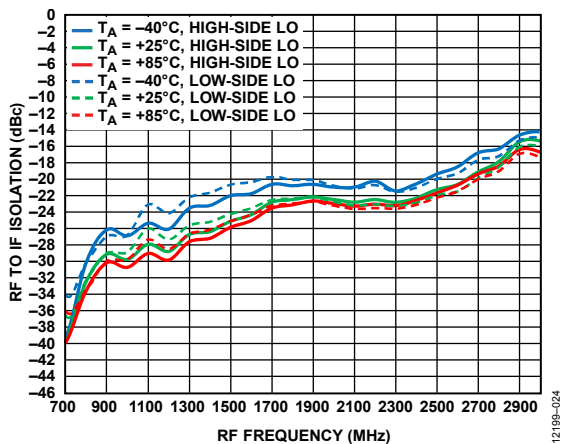


Figure 24. RF to IF Isolation vs. RF Frequency over Three Temperatures

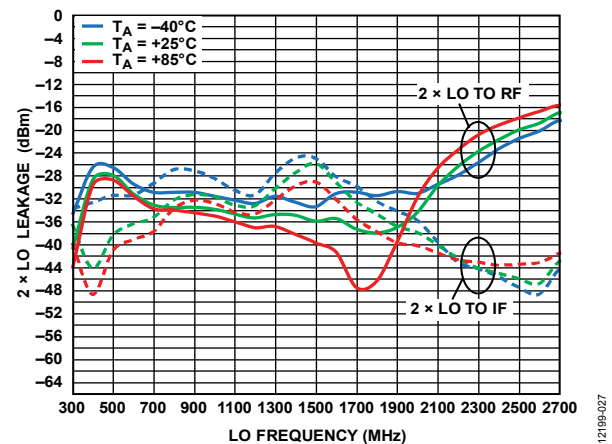


Figure 27. 2 x LO Leakage vs. LO Frequency (2 x LO to RF and 2 x LO to IF)

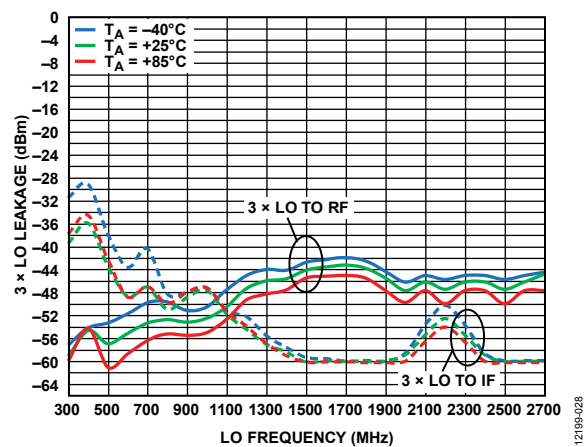


Figure 28.  $3 \times$  LO Leakage vs. LO Frequency  
( $3 \times$  LO to RF and  $3 \times$  LO to IF)

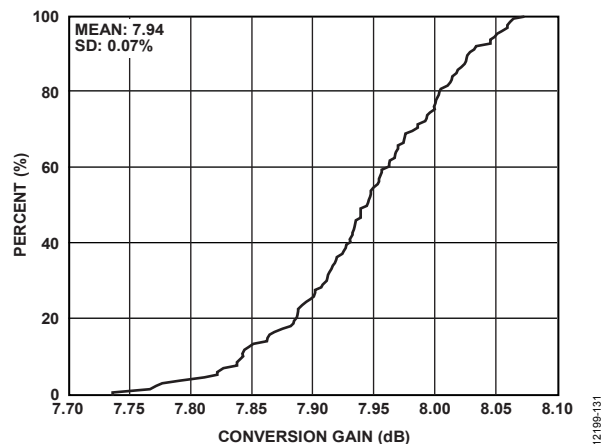


Figure 31. Conversion Gain Distribution

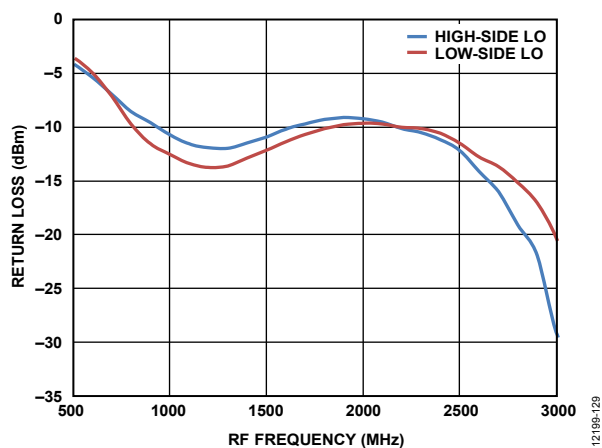


Figure 29. RF Port Return Loss, Fixed IF LO Return Loss

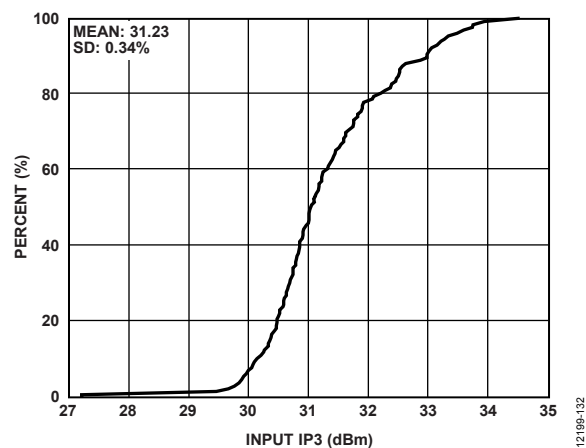


Figure 32. Input IP3 Distribution

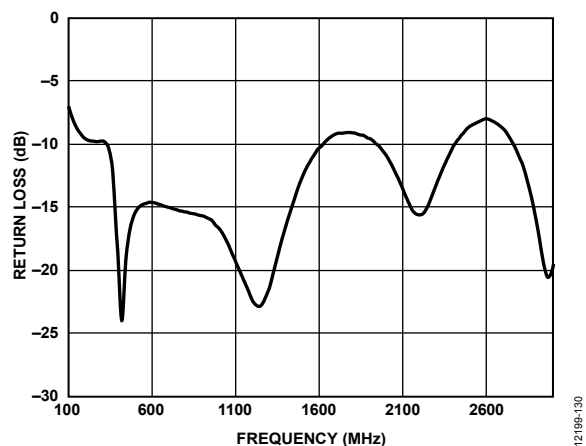


Figure 30. LO Return Loss

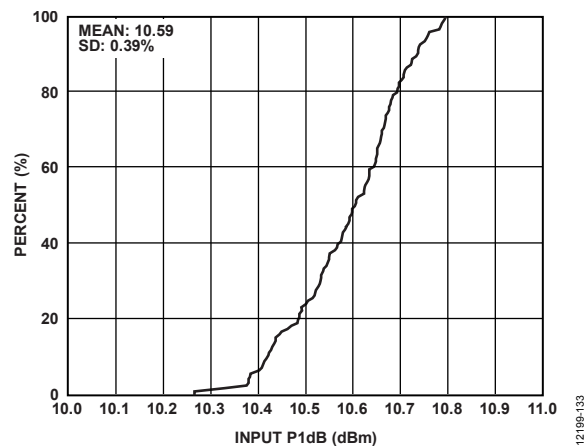


Figure 33. Input P1dB Distribution

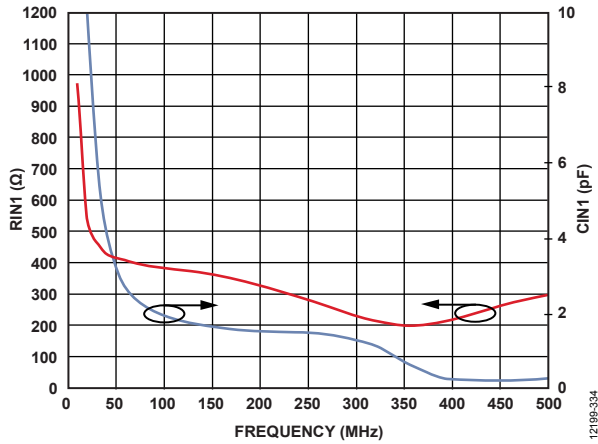


Figure 34. IF Output Impedance (R Parallel C Equivalent)

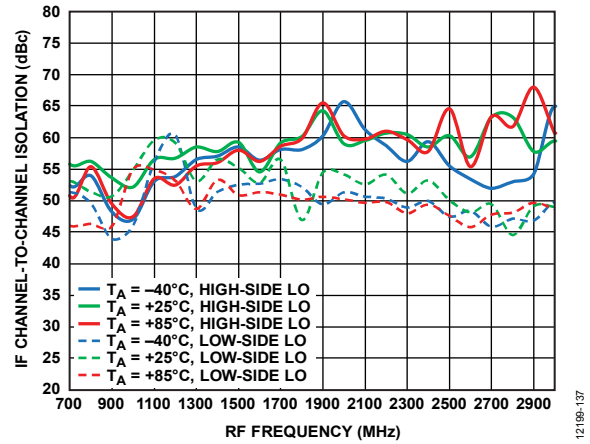


Figure 37. IF Channel-to-Channel Isolation vs. RF Frequency over Three Temperatures

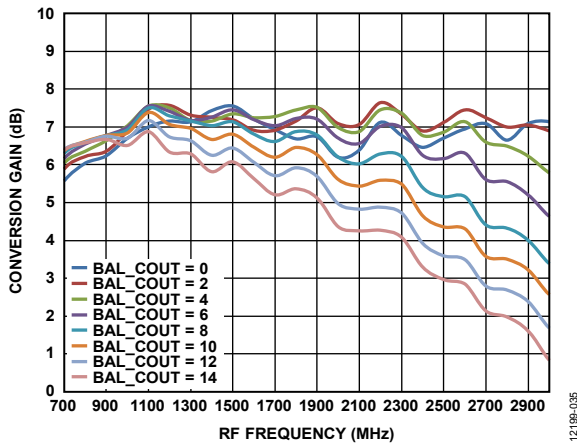


Figure 35. Conversion Gain vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

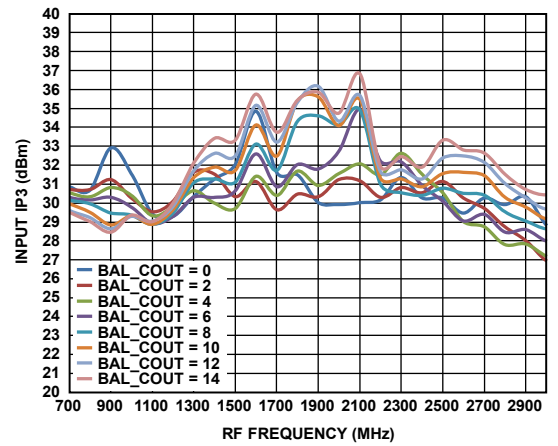


Figure 38. Input IP3 vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

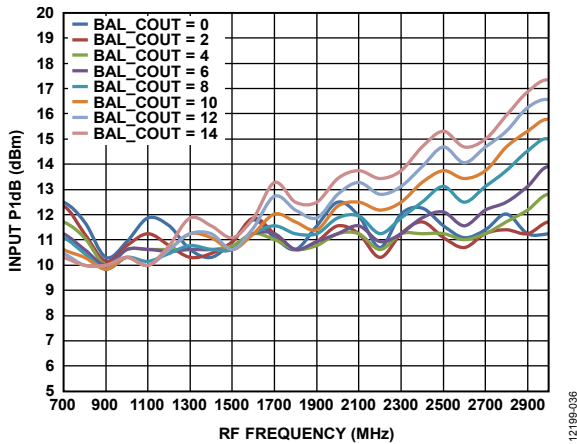


Figure 36. Input P1dB vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

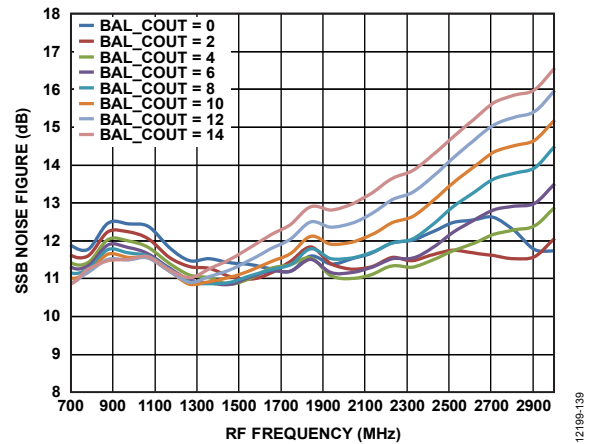


Figure 39. SSB Noise Figure vs. RF Frequency for All RFB Settings, VGS and LPF Use Optimum Settings

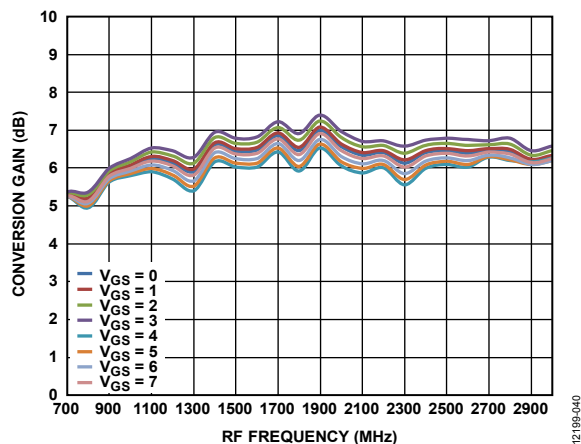


Figure 40. Conversion Gain vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

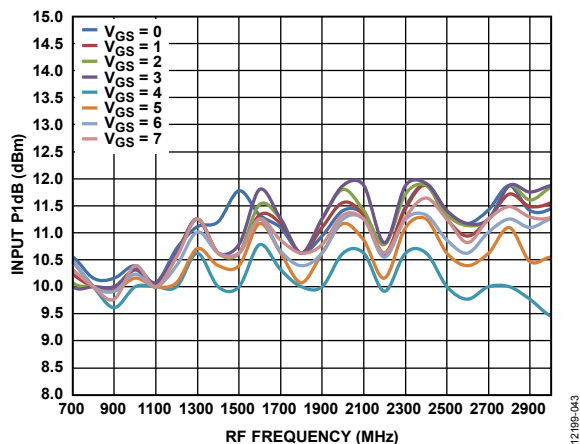


Figure 43. Input P1dB vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

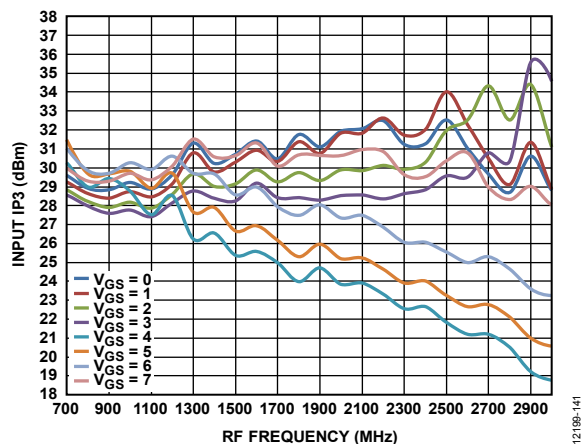


Figure 41. Input IP3 vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

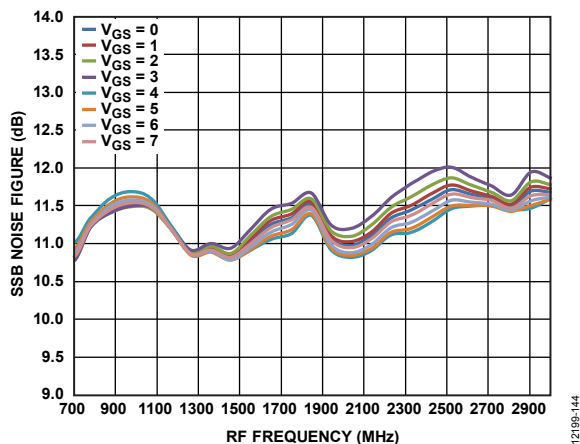


Figure 44. SSB Noise Figure vs. RF Frequency for All VGS Settings, RFB and LPF Use Optimum Settings

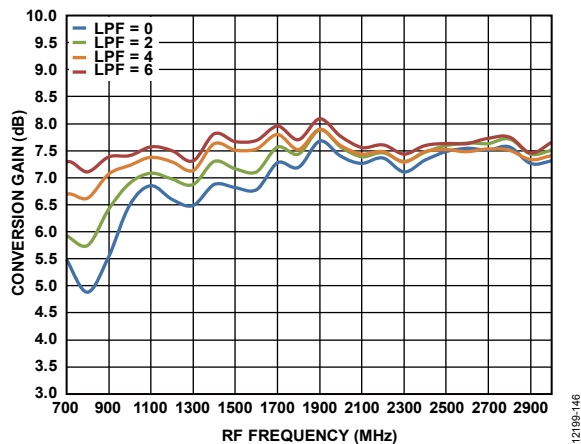


Figure 42. Conversion Gain vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

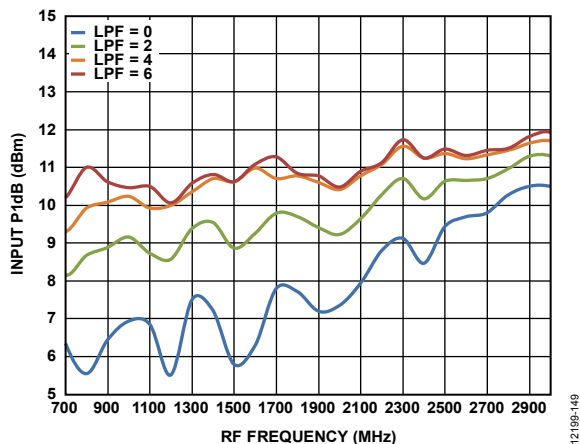


Figure 45. Input P1dB vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

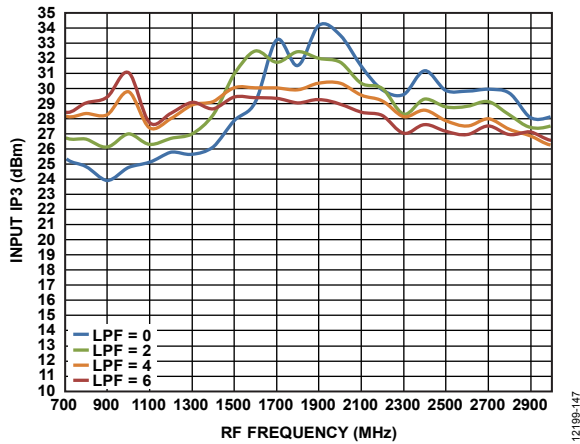


Figure 46. Input IP3 vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

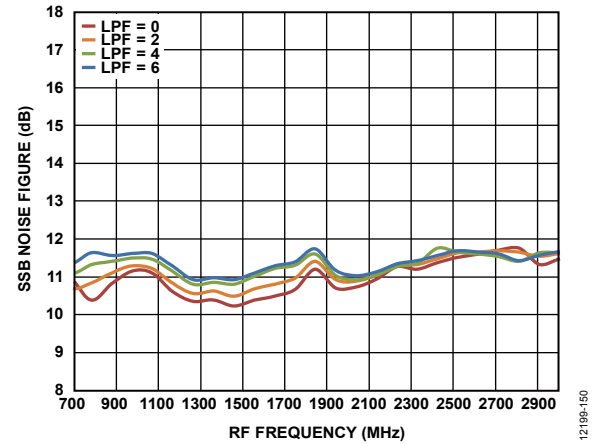


Figure 49. SSB Noise Figure vs. RF Frequency for All LPF Settings, RFB and VGS Use Optimum Settings

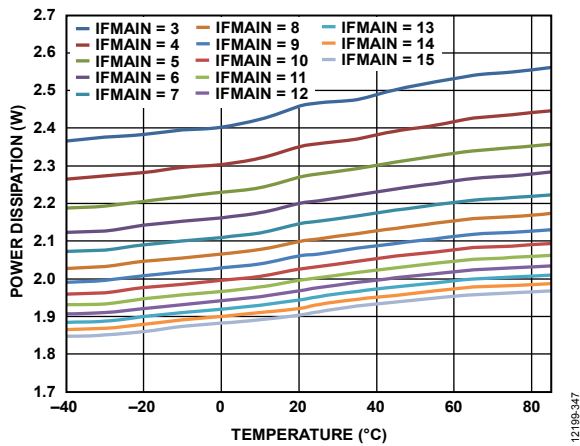


Figure 47. Power Dissipation vs. Temperature for IF Main Settings

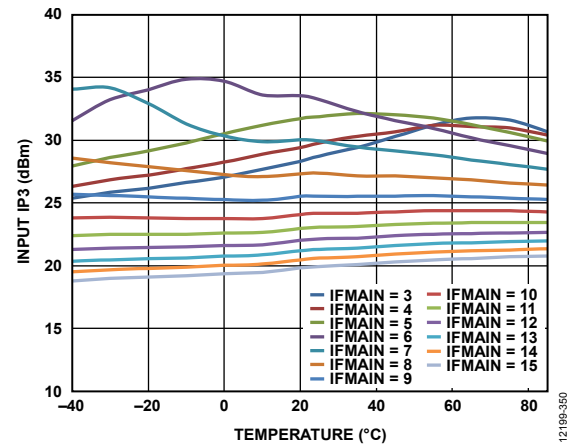


Figure 50. Input IP3 vs. Temperature for IF Main Settings

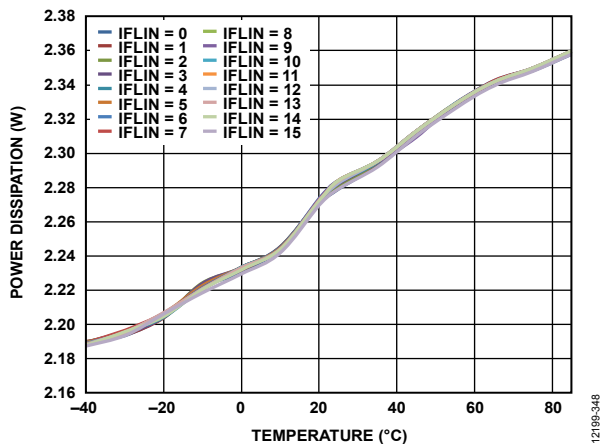


Figure 48. Power Dissipation vs. Temperature for IF LIN Settings

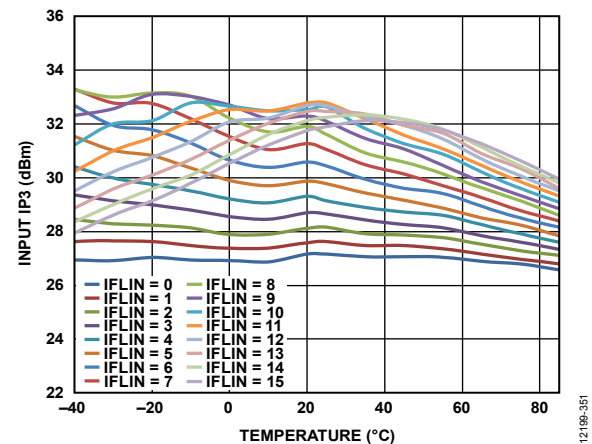


Figure 51. Input IP3 vs. Temperature for IF LIN Settings

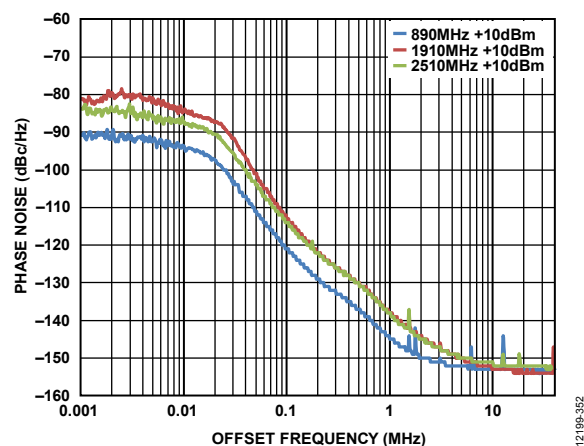


Figure 52. Phase Noise at IF Output vs. Offset Frequency with 10 dBm Blocker in Integer Mode

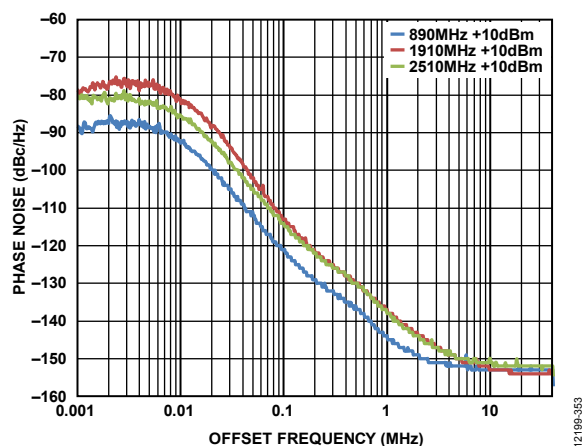


Figure 53. Phase Noise at IF Output vs. Offset Frequency with 10 dBm Blocker in Fractional Mode

**MIXER, HIGH EFFICIENCY MODE**

$T_A = 25^\circ\text{C}$ ,  $f_{RF} = 1900\text{ MHz}$ ,  $f_{LO} = 1697\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $f_{REF} = 122.88\text{ MHz}$ ,  $f_{REF}\text{ power} = 4\text{ dBm}$ ,  $f_{PFD} = 1.536\text{ MHz}$ , low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

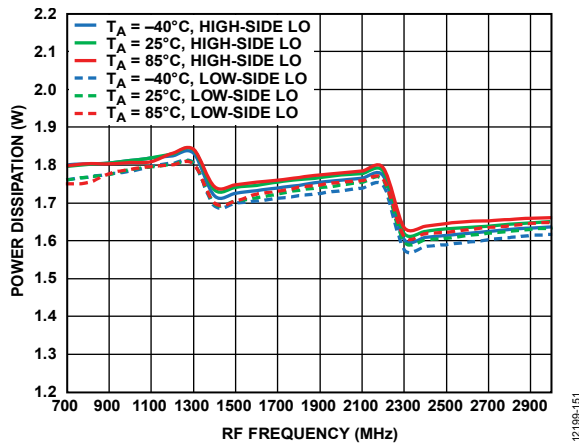


Figure 54. Power Dissipation vs. RF Frequency over Three Temperatures

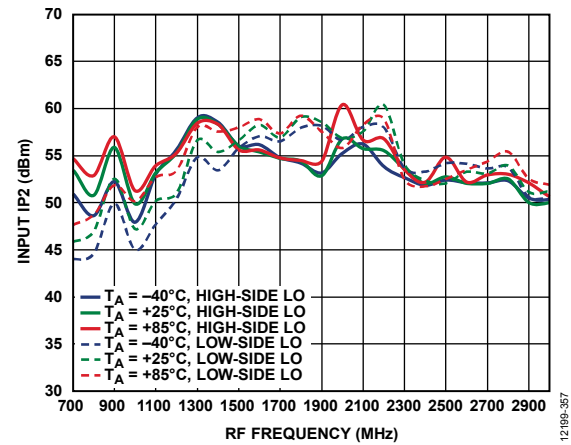


Figure 57. Input IP2 vs. RF Frequency over Three Temperatures

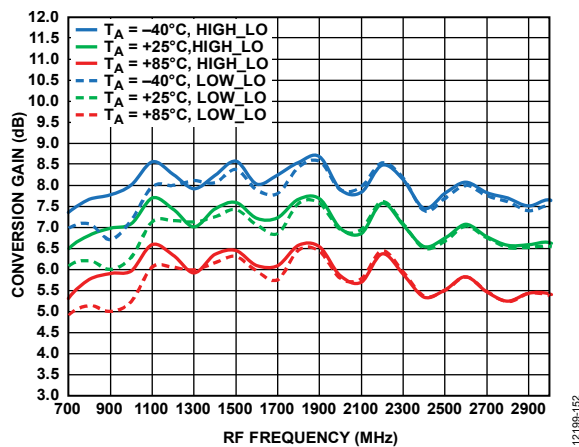


Figure 55. Conversion Gain vs. RF Frequency over Three Temperatures

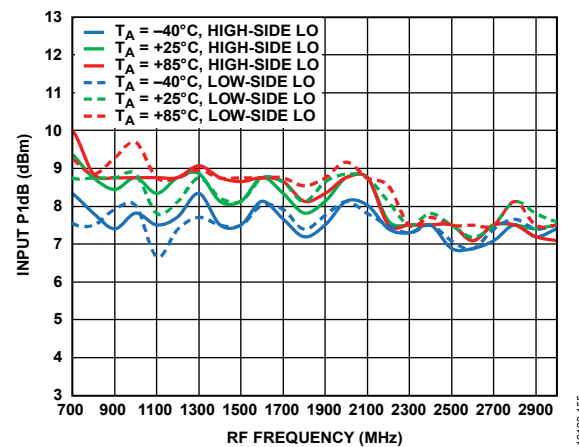


Figure 58. Input P1dB vs. RF Frequency over Three Temperatures

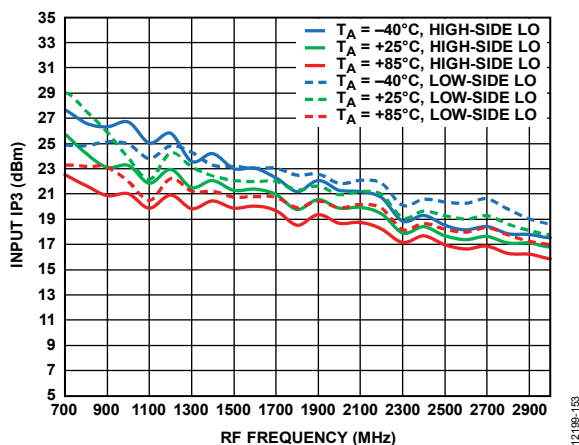


Figure 56. Input IP3 vs. RF Frequency over Three Temperatures

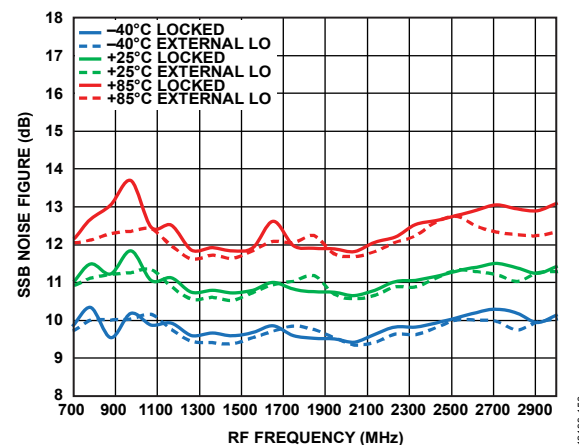


Figure 59. SSB Noise Figure vs. RF Frequency over Three Temperatures

## SYNTHESIZER

$V_S$  = high performance mode,  $T_A = 25^\circ\text{C}$ , measured on LO output,  $f_{LO} = 1700\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $f_{REF} = 122.88\text{ MHz}$ ,  $f_{PDF} = 1.536\text{ MHz}$ ,  $f_{REF}$  power = 4 dBm, integer mode loop filter, unless otherwise noted.

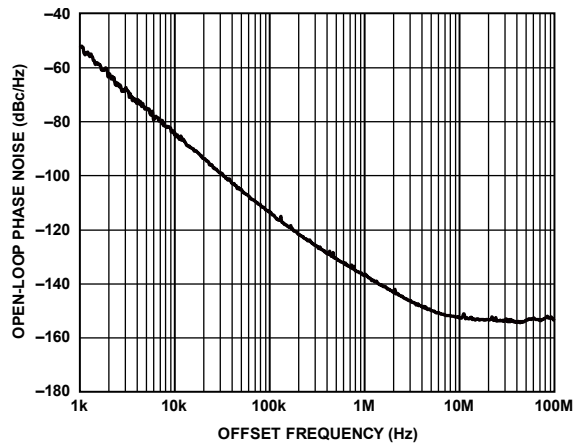


Figure 60. VCO\_0 Open-Loop Phase Noise vs. Offset Frequency,  $f_{VCO_0} = 5.1\text{ GHz}$ , Divide by Two Selected, VCOVTUNE = 1.5 V

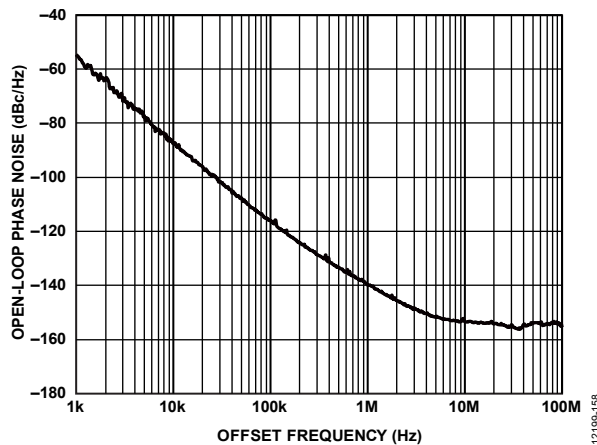


Figure 61. VCO\_1 Open-Loop Phase Noise vs. Offset Frequency,  $f_{VCO_1} = 4.5\text{ GHz}$ , Divide by Two Selected, VCOVTUNE = 1.5 V

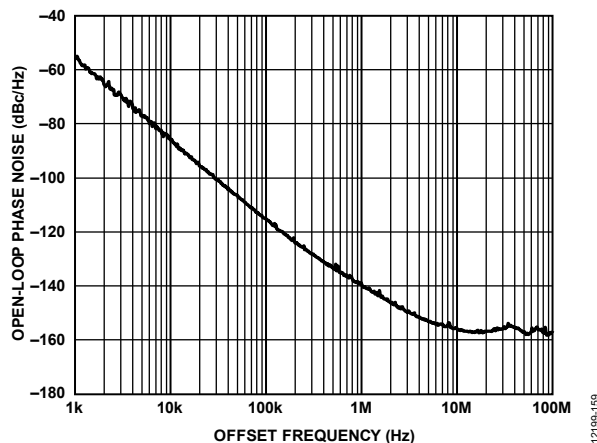


Figure 62. VCO\_2 Open-Loop Phase Noise vs. Offset Frequency,  $f_{VCO_2} = 3.8\text{ GHz}$ , Divide by Two Selected, VCOVTUNE = 1.5 V

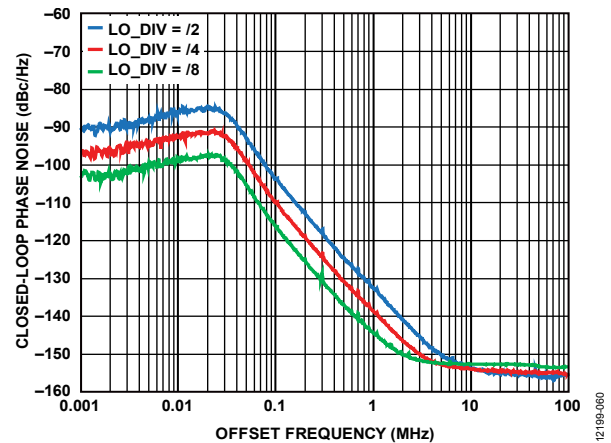


Figure 63. VCO\_0 Closed-Loop Phase Noise for Various LO\_DIV Dividers vs. Offset Frequency,  $f_{VCO_0} = 5.1\text{ GHz}$

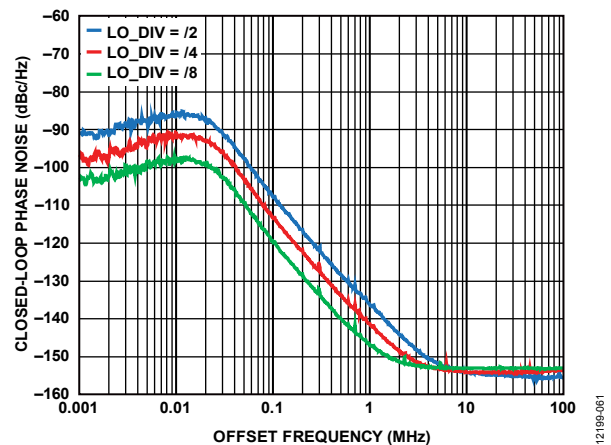


Figure 64. VCO\_1 Closed-Loop Phase Noise for Various LO\_DIV Dividers vs. Offset Frequency,  $f_{VCO_1} = 4.5\text{ GHz}$

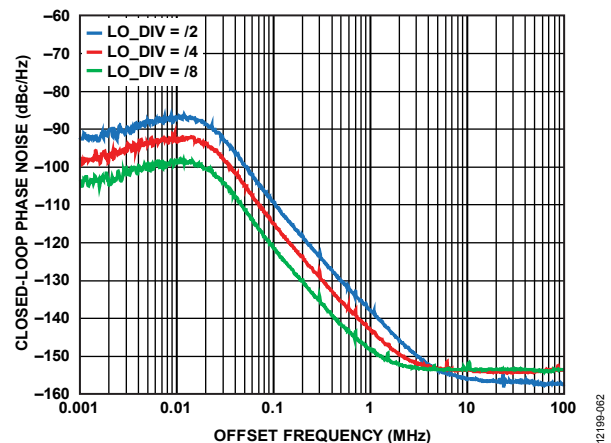


Figure 65. VCO\_2 Closed-Loop Phase Noise for Various LO\_DIV Dividers vs. Offset Frequency,  $f_{VCO_2} = 3.8\text{ GHz}$



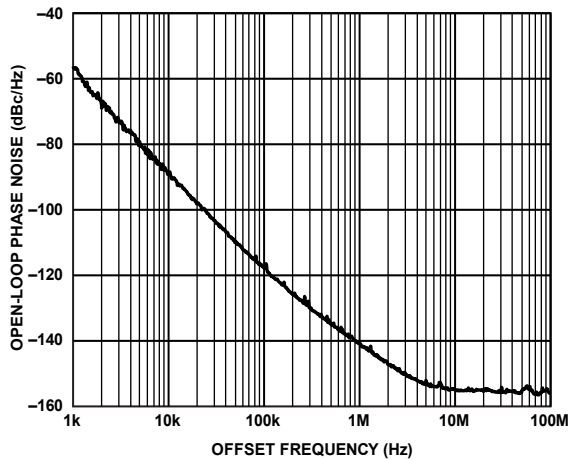


Figure 66. VCO\_3 Open-Loop Phase Noise vs. Offset Frequency,  $f_{VCO\_3} = 3.2$  GHz, Divide by Two Selected, VCOVTUNE = 1.5 V

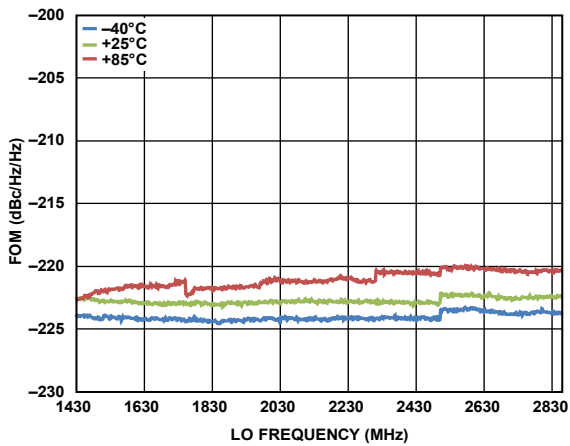


Figure 67. PLL Figure of Merit (FOM) vs. LO Frequency, Integer Mode

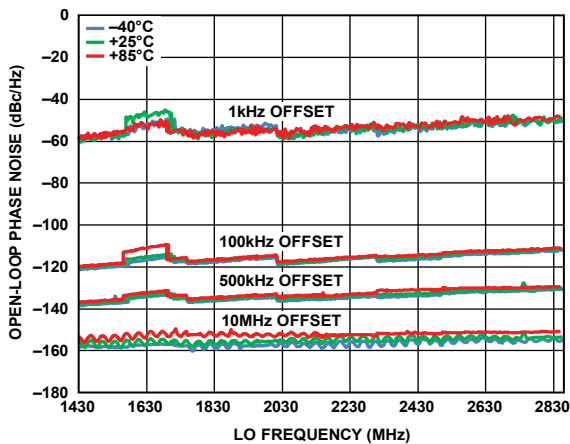


Figure 68. Open-Loop Phase Noise vs. LO Frequency, Divide by Two Selected

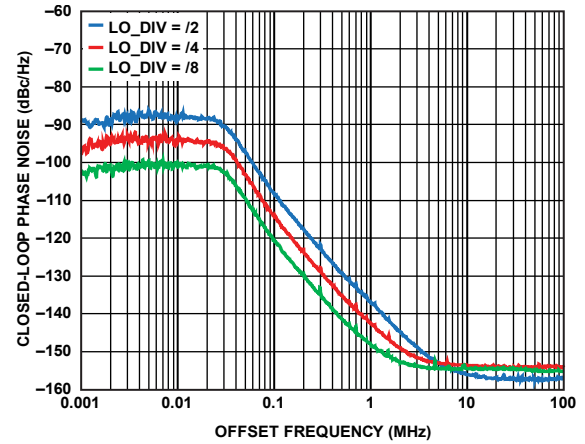


Figure 69. VCO\_3 Closed-Loop Phase Noise for Various LO\_DIV Dividers vs. Offset Frequency,  $f_{VCO\_3} = 3.2$  GHz

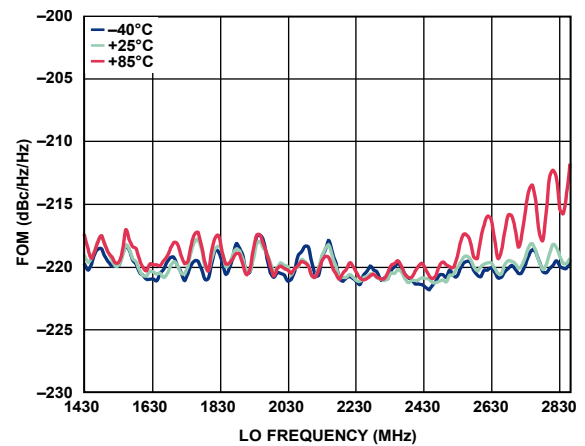


Figure 70. PLL Figure of Merit (FOM) vs. LO Frequency, Fractional Mode Offset = 45 kHz, Bleed = 125  $\mu$ A

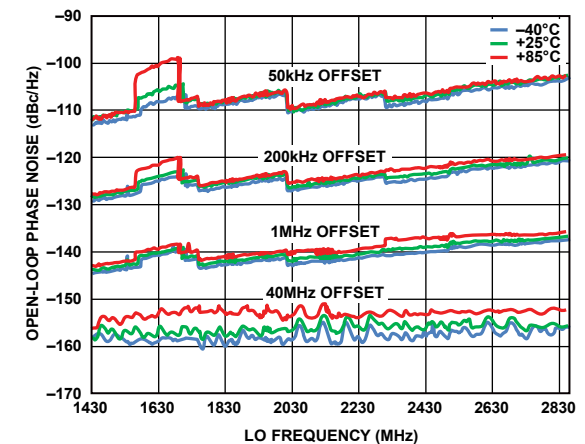


Figure 71. Open-Loop Phase Noise vs. LO Frequency, Divide by Two Selected

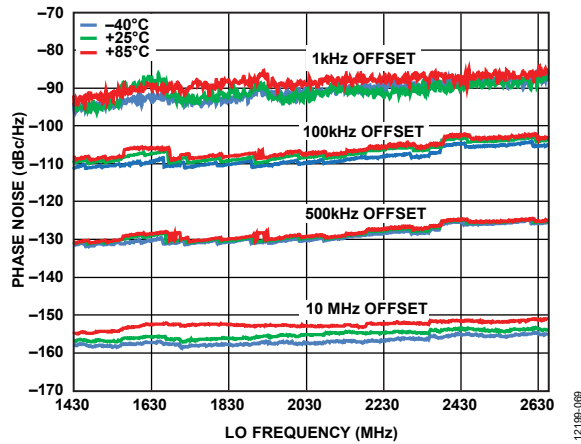


Figure 72. Integer Loop Filter Phase Noise, Divide by Two Selected, Offset = 1 kHz, 100 kHz, 500 kHz, and 10 MHz

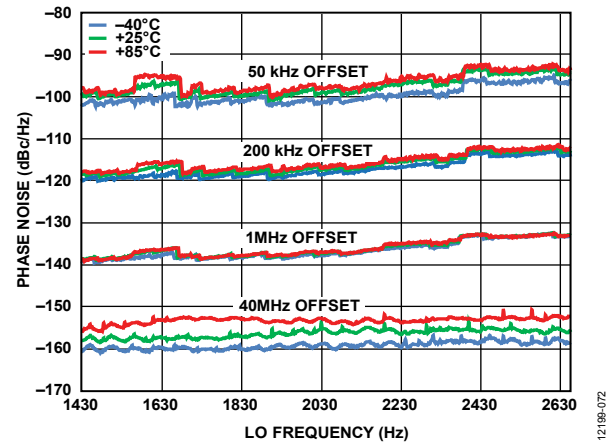


Figure 75. Integer Loop Filter Phase Noise, Divide by Two Selected, Offset = 50 kHz, 200 kHz, 1 MHz, and 40 MHz

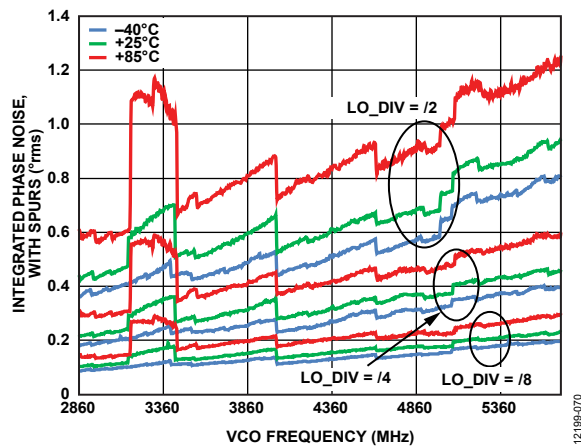


Figure 73. 10 kHz to 40 MHz Integrated Phase Noise vs. VCO Frequency, Divide by Two, Four, and Eight, Including Spurs

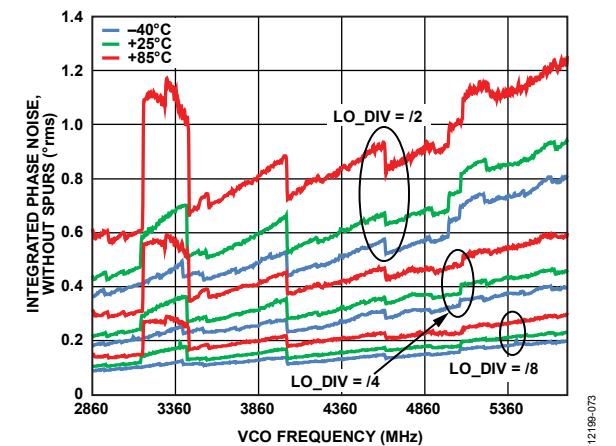


Figure 76. 10 kHz to 40 MHz Integrated Phase Noise vs. VCO Frequency, Divide by Two, Four, and Eight, Excluding Spurs

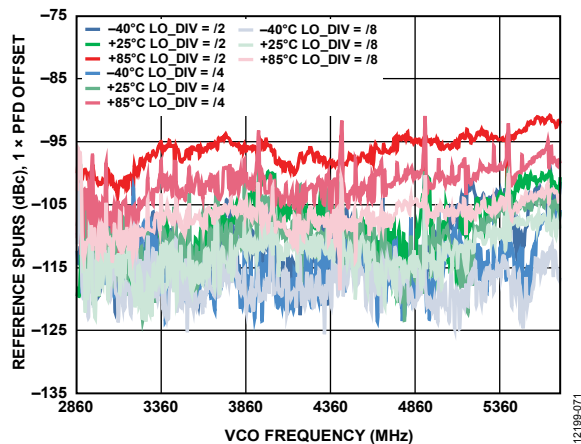


Figure 74.  $f_{PFD}$  Reference Spurs vs. VCO Frequency,  $1 \times PFD$  Offset, Measured at LO Output, Integer Mode

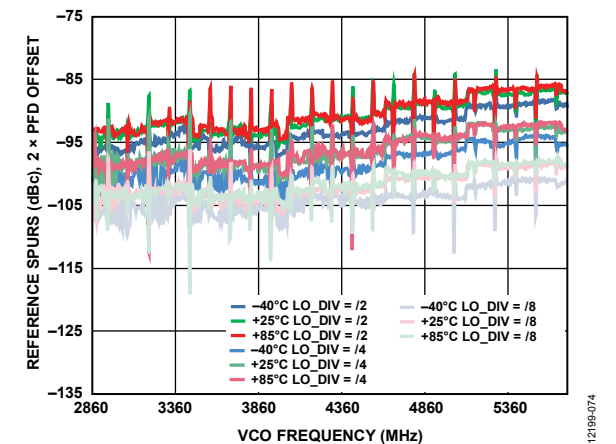


Figure 77.  $f_{PFD}$  Reference Spurs vs. VCO Frequency,  $2 \times PFD$  Offset, Measured at LO Output, Integer Mode

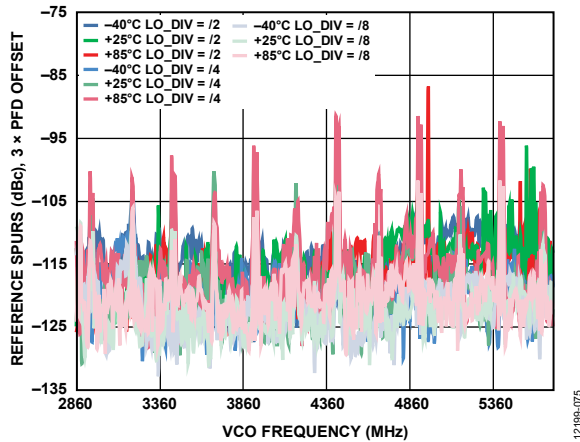


Figure 78.  $f_{PFD}$  Reference Spurs vs. VCO Frequency,  $3 \times$  PFD Offset, Measured at LO Output, Integer Mode

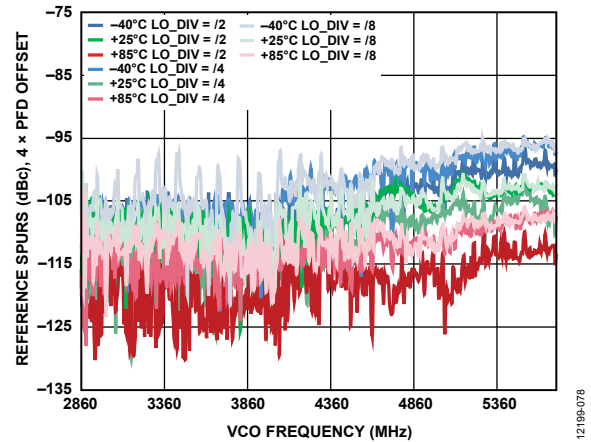


Figure 81.  $f_{PFD}$  Reference Spurs vs. VCO Frequency,  $4 \times$  PFD Offset, Measured at LO Output, Integer Mode

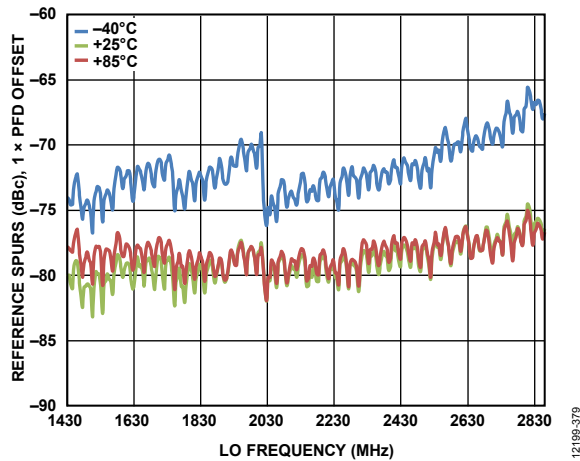


Figure 79.  $f_{PFD}$  Reference Spurs vs. LO Frequency,  $1 \times$  PFD Offset, Measured at LO Output, Fractional Mode

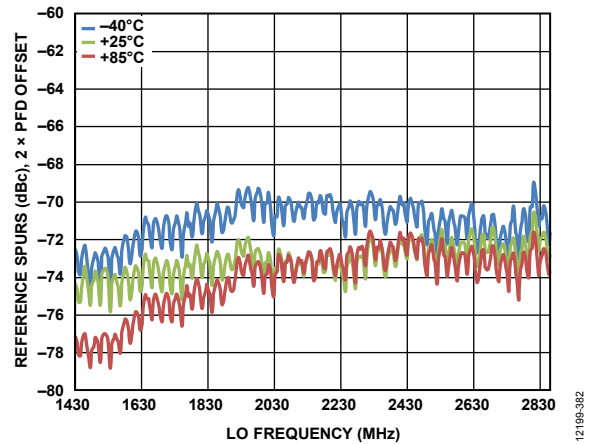


Figure 82.  $f_{PFD}$  Reference Spurs vs. LO Frequency,  $2 \times$  PFD Offset, Measured at LO Output, Fractional Mode

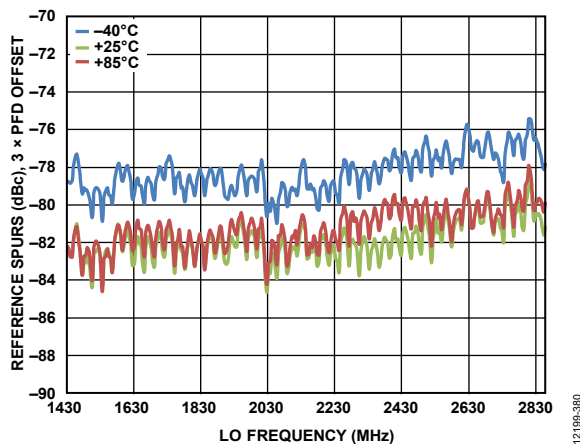


Figure 80.  $f_{PFD}$  Reference Spurs vs. LO Frequency,  $3 \times$  PFD Offset, Measured at LO Output, Fractional Mode

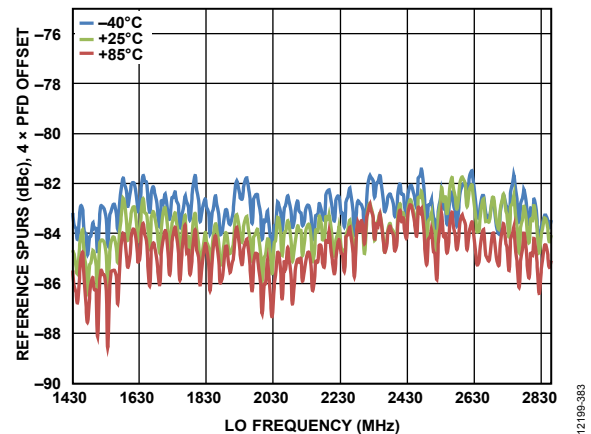


Figure 83.  $f_{PFD}$  Reference Spurs vs. LO Frequency,  $4 \times$  PFD Offset, Measured at LO Output, Fractional Mode

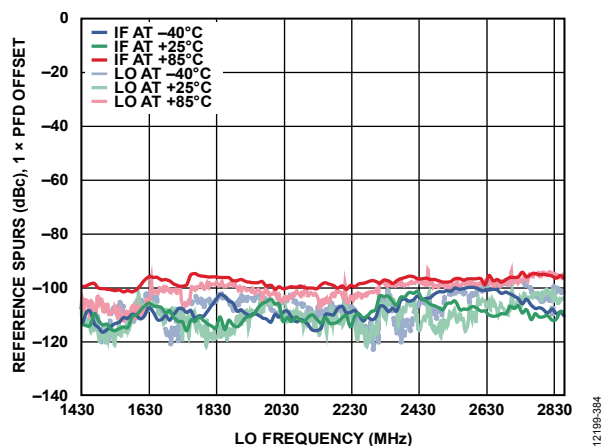


Figure 84.  $f_{PFD}$  Reference Spurs vs. LO Frequency, Divide by Two Selected,  $1 \times PFD$  Offset, Measured on LO Output and IF Output

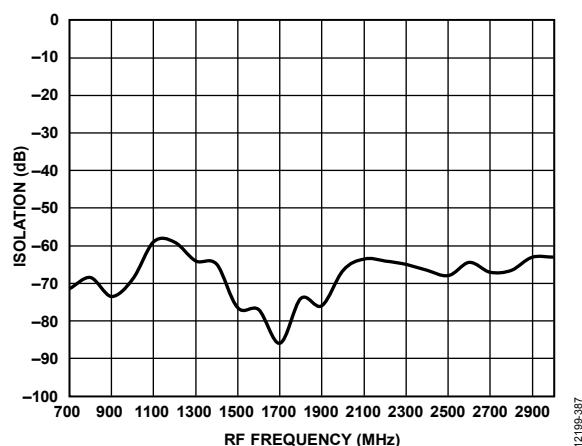


Figure 87. RF to LO Output Feedthrough,  $LO\_DRV\_LVL = 0$

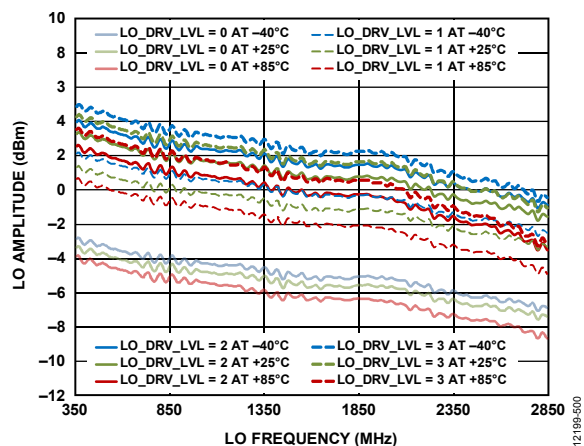


Figure 85. LO Amplitude vs. LO Frequency,  $LO\_DRV\_LVL = 0, 1, 2$ , and  $3$

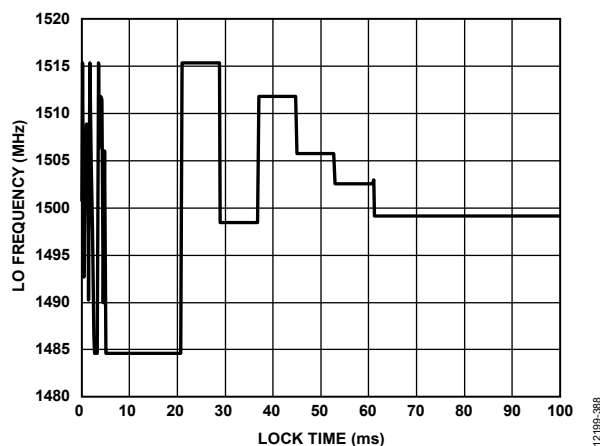


Figure 88. LO Frequency Settling Time, Integer Mode Loop Filter, Integer Mode

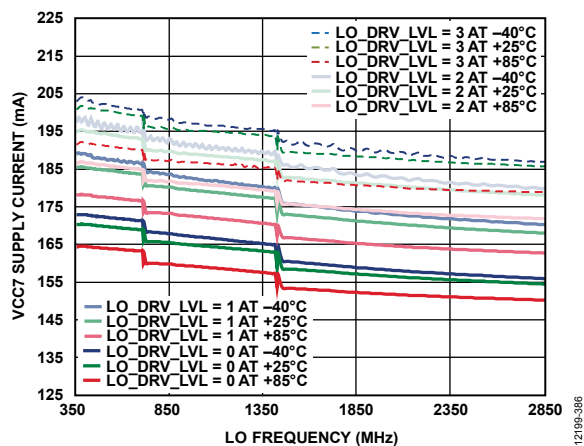


Figure 86. Supply Current for VCC7 vs. LO Frequency,  $LO\_DRV\_LVL = 0, 1, 2$ , and  $3$

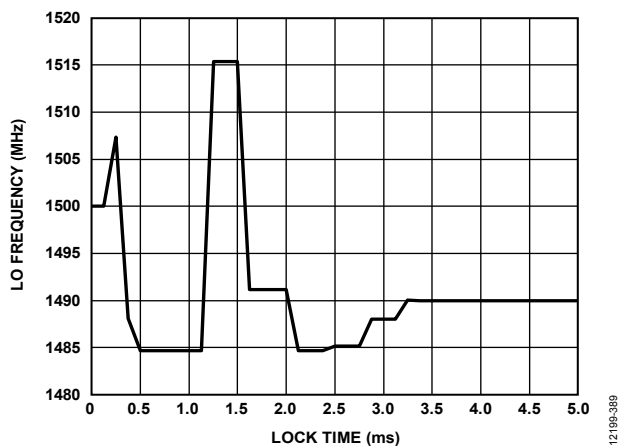


Figure 89. LO Frequency Settling Time, Fractional Loop Filter, Fractional Mode

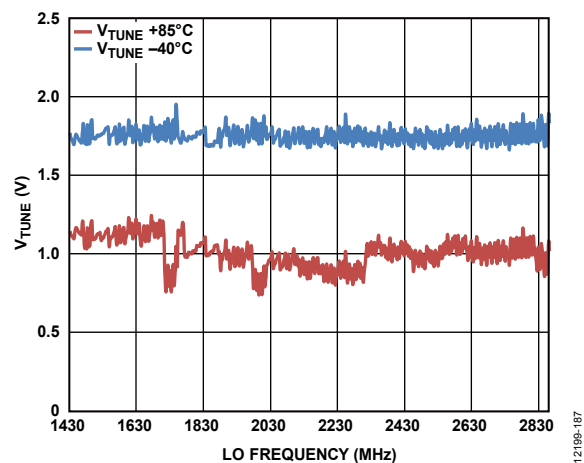


Figure 90. V<sub>TUNE</sub> vs. LO Frequency for Lock at Cold Drift to Hot

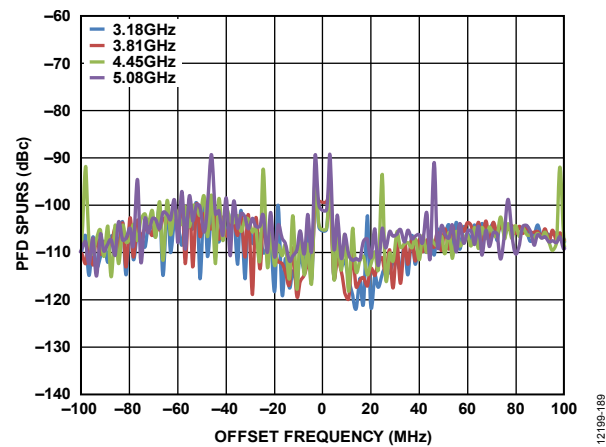


Figure 92. PFD Spurs vs. Offset Frequency for 4 VCOs, Integer Mode

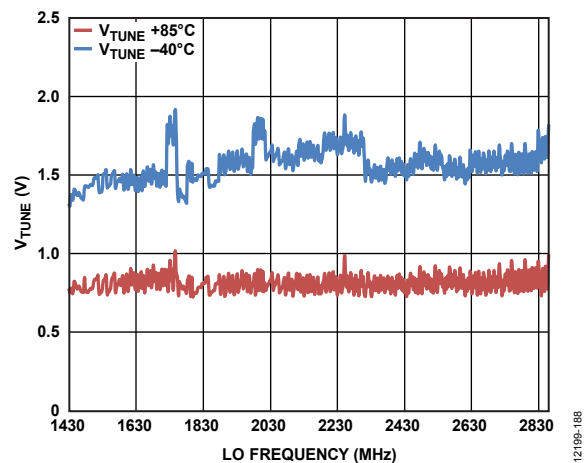


Figure 91. V<sub>TUNE</sub> vs. LO Frequency for Lock at Hot Drift to Cold

**SPURIOUS PERFORMANCE**

$(N \times f_{RF}) - (M \times f_{LO})$  spur measurements were made using the standard evaluation board. Mixer spurious products are measured in dBc from the IF output power level. Data was measured only for frequencies less than 6 GHz. Typical noise floor of the measurement system = -100 dBm.

**High Performance Mode**

$V_S$  = high performance mode,  $T_A$  = 25°C,  $Z_O$  = 50  $\Omega$ ,  $f_{REF}$  = 122.88 MHz,  $f_{REF}$  power = 4 dBm,  $f_{PFD}$  = 1.536 MHz, low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

**Table 11. RF = 900 MHz, LO = 697 MHz**

		M									
		0	1	2	3	4	5	6	7	8	9
N	0		-27.1	-32.1	-39.1	-27.0	-54.2	-48.5	-69.3	-65.6	
	1	-35.5	0.0	-52.5	-18.4	-56.6	-43.6	-66.7	-53.5	-87.4	-73.5
	2	-55.3	-68.9	-68.8	-73.4	-64.9	<-100	-68.3	<-100	-80.6	<-100
	3	-88.2	-88.4	<-100	-79.5	<-100	-94.1	<-100	<-100	<-100	<-100
	4	<-100	-56.6	<-100	<-100	<-100	<-100	<-100	<-100	<-100	<-100
	5	<-100	-43.6	<-100	<-100	<-100	<-100	<-100	<-100	<-100	<-100
	6	<-100	-66.7	<-100	<-100	<-100	<-100	<-100	<-100	<-100	<-100
	7		-53.5	<-100	<-100	<-100	<-100	<-100	<-100	<-100	<-100
	8			<-100	<-100	<-100	<-100	<-100	<-100	<-100	<-100
	9					<-100	<-100	<-100	<-100	<-100	<-100

**Table 12. RF = 1900 MHz, LO = 1697 MHz**

		M									
		0	1	2	3	4	5	6	7	8	9
N	0		-37.0	-31.2	-64.2						
	1	-30.2	0.0	-47.9	-52.1	-74.4					
	2	-70.8	-71.9	-81.6	-81.2	-67.2	<-100				
	3	<-100	<-100	-93.5	-75.2	<-100	<-100	<-100			
	4		<-100	<-100	<-100	<-100	<-100	<-100	<-100	<-100	
	5				<-100	<-100	<-100	<-100	<-100	<-100	<-100
	6					<-100	<-100	<-100	<-100	<-100	<-100
	7						<-100	<-100	<-100	<-100	<-100
	8							<-100	<-100	<-100	<-100
	9								<-100	<-100	<-100

**Table 13. RF = 2500 MHz, LO = 2297 MHz**

		M									
		0	1	2	3	4	5	6	7	8	9
N	0		-40.7	-44.1							
	1	-29.0	0.0	-49.4	-58.7						
	2	-81.0	-87.3	-75.4	-79.0	-84.7					
	3		<-100	-91.9	-74.7	<-100	<-100				
	4			<-100	<-100	<-100	<-100	<-100			
	5				<-100	<-100	<-100	<-100	<-100	<-100	
	6					<-100	<-100	<-100	-92.5	<-100	<-100
	7							<-100	<-100	<-100	<-100
	8								<-100	<-100	<-100
	9									<-100	<-100

**High Efficiency Mode**

$V_S$  = high efficiency mode,  $T_A = 25^\circ\text{C}$ ,  $Z_O = 50\ \Omega$ ,  $f_{\text{REF}} = 122.88\ \text{MHz}$ ,  $f_{\text{REF}} \text{ power} = 4\ \text{dBm}$ ,  $f_{\text{PFD}} = 1.536\ \text{MHz}$ , low-side LO injection, optimum RFB and LPF settings, unless otherwise noted.

**Table 14. RF = 900 MHz, LO = 697 MHz**

		M									
		0	1	2	3	4	5	6	7	8	9
N	0		−30.4	−34.1	−46.7	−29.6	−57.4	−51.2	−74.7	−62.7	
	1	−37.7	0.0	−52.6	−19.2	−61.6	−44.3	−64.0	−53.6	−91.8	−73.2
	2	−70.3	−66.4	−68.8	−71.9	−59.9	−93.0	−67.8	<−100	−79.0	<−100
	3	−86.4	−81.0	−96.4	−74.7	<−100	−85.0	<−100	<−100	<−100	<−100
	4	<−100	<−100	−97.9	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	5	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	6	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	7		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	8			<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	9					<−100	<−100	<−100	<−100	<−100	<−100

**Table 15. RF = 1900 MHz, LO = 1697 MHz**

		M									
		0	1	2	3	4	5	6	7	8	9
N	0		−41.4	−35.1	−69.0						
	1	−30.5	0.0	−46.9	−52.2	−74.4					
	2	−71.5	−67.7	−74.6	−71.3	−63.6	<−100				
	3	<−100	<−100	−89.9	−67.7	<−100	<−100	<−100			
	4		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100
	6					<−100	<−100	<−100	<−100	<−100	<−100
	7						<−100	<−100	<−100	<−100	<−100
	8							<−100	<−100	<−100	<−100
	9								<−100	<−100	<−100

**Table 16. RF = 2500 MHz, LO = 2297 MHz**

		M									
		0	1	2	3	4	5	6	7	8	9
N	0		−42.3	−48.6							
	1	−29.1	0.0	−48.6	−59.4						
	2	−75.6	−88.8	−71.6	−70.8	−77.0					
	3		−59.4	−86.2	−66.9	<−100	<−100				
	4			−77.0	<−100	<−100	<−100	<−100			
	5				<−100	<−100	<−100	<−100	<−100	<−100	
	6					<−100	<−100	<−100	<−100	<−100	<−100
	7							<−100	<−100	<−100	<−100
	8								<−100	<−100	<−100
	9									<−100	<−100

## CIRCUIT DESCRIPTION

The [ADRF6612](#) consists of two primary components: the RF subsystem and the LO subsystem. The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance device with excellent electrical, mechanical, and thermal properties. The wideband frequency response and flexible frequency programming simplifies the receiver design, saves on-board space, and minimizes the need for external components.

The RF subsystem consists of an integrated, tunable, low loss RF balun, a double balanced, passive MOSFET mixer, a tunable sum termination network, and an IF amplifier.

The LO subsystem consists of a multistage, limiting LO amplifier. The purpose of the LO subsystem is to provide a large, fixed amplitude, balanced signal to drive the mixer independent of the level of the LO input. A schematic of the device is shown in Figure 94.

### RF SUBSYSTEM

The single-ended, 50  $\Omega$  RF input is internally transformed to a balanced signal using a tunable, low loss, unbalanced-to-balanced (balun) transformer. This transformer is made possible by an extremely low loss metal stack, which provides both excellent balance and dc isolation for the RF port. Although the port can be dc connected, it is recommended to use a blocking capacitor to avoid running excessive dc current through the device. The RF balun can easily support an RF input frequency range of 700 MHz to 3000 MHz. This balun is tuned over the frequency range by a SPI controlled switched capacitor network at the output of the RF balun.

The resulting balanced RF signal is applied to a passive mixer that commutates the RF input in accordance with the output of the LO subsystem. The passive mixer is a balanced, low loss switch that adds minimum noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

The IF amplifier is a balanced feedback design that simultaneously provides the desired gain, noise figure, and input impedance that is required to achieve the overall performance. The balanced open-collector output of the IF amplifier, with an impedance modified by the feedback within the amplifier, permits the output to be connected directly to a high impedance filter, a differential amplifier, or an analog-to-digital converter (ADC) input while providing optimum second-order intermodulation suppression. The differential output impedance of the IF amplifier is approximately 200  $\Omega$ . If operation in a 50  $\Omega$  system is desired, the output can be transformed to 50  $\Omega$  by using a 4:1 transformer or an LC impedance matching network.

### EXTERNAL LO GENERATION

The [ADRF6612](#) LO can be generated by an externally applied source or by using the internal PLL synthesizer.

To select the external LO mode, write the value 011 to Register 0x22, Bits[2:0] and apply the differential LO signal to Pin 4 (EXTVCOIN+) and Pin 5 (EXTVCOIN-).

Internal dividers allow the externally applied LO signal to be divided before this signal arrives at the mixer LO input. The divider value is set by Register 0x21, Bits[5:3] and has possible values of 1, 2, 4, and 8. With the divider set to 1, the externally applied LO input frequency range is 250 MHz to 2850 MHz. When using a divider value of other than 1, the maximum externally applied LO frequency is 5700 MHz.

The external LO input pins present a broadband differential 50  $\Omega$  input impedance. The EXTVCOIN+ and EXTVCOIN- input pins must be ac-coupled. When not in use, EXTVCOIN+ and EXTVCOIN- can be left unconnected.

### INTERNAL LO GENERATION

#### Reference Input Circuitry

The [ADRF6612](#) includes an on-chip PLL for LO synthesis. The PLL, shown in Figure 93, consists of a reference input and input dividers, a PFD, a charge pump, VCOs, and a programmable fractional/integer divider with a 2 $\times$  prescaler.

The reference path takes in a reference clock and divides it by a factor of 1 to 8191 before passing it to the PFD. The PFD compares this signal to the divided down signal from the VCO. Depending on the PFD polarity selected, the PFD sends an up or down signal to the charge pump if the VCO signal is slow or fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (VCOVTUNE).

In band (within the band of the loop filter) phase noise performance is typically limited by the reference source. Due to the inherent phase noise reduction when performing frequency division, improved in band phase noise performance can be achieved with higher reference divide values. However, the divide chain adds its own small amount of phase noise, so there is a limit on how much improvement can be gained by increasing the divider value.



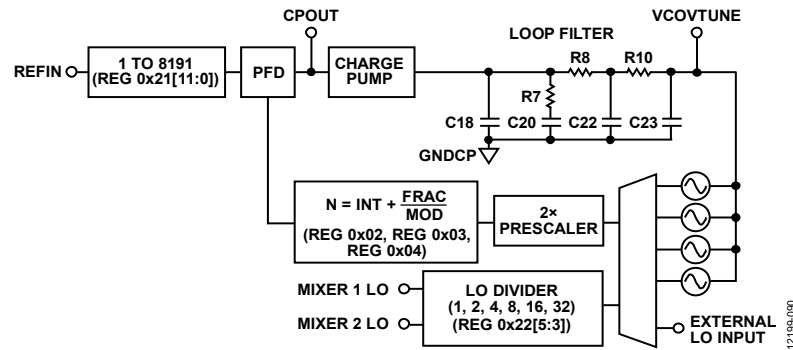


Figure 93. LO Generation Block Diagram

## Loop Filters

Defining a loop filter for the [ADRF6612](#) depends on several dynamics, these being the PLL REFIN and PFD frequency and desired PFD and fractional spur levels. Higher reference and PFD frequencies spread the PFD spurs over a wider bandwidth (wider separation between spurs), but also lead to higher levels of spurs coupling through the reference divider chain. Lower reference and PFD frequencies lower the spacing between PFD spurs, but the spur levels can be significantly improved by using lower frequencies. At lower PFD frequencies, it may also be possible to achieve the desired synthesizer frequency step size using the integer divider mode, therefore eliminating the risk of fractional spurs. Table 17 shows the recommended loop filter components and dynamic loop settings when using integer mode and PFD frequencies at less than 10 MHz.

### Table 17. Integer Mode Loop Filter Components and PLL Dynamic Settings

Loop Filter Components	PLL Dynamic Settings
C18	1500 pF
R7	910 $\Omega$
C20	33 nF
R8	1.8 k $\Omega$
C22	560 pF
R10	20 k $\Omega$
C23	39 pF
CSCALE	8000 $\mu$ A
Bleed Current	0 $\mu$ A
ABDLY	0.9 nS

If a smaller frequency step size is desired, the [ADRF6612](#) can be used in fractional mode. The 16-bit FRAC\_DIV and MOD\_DIV values available in the [ADRF6612](#) mean that small step sizes can be achieved with high PFD frequencies. PFD spurs may be higher in amplitude, but are spaced further apart. Fractional spurs may be present as well.

**Table 18. Fractional Mode Loop Filter Components and PLL Dynamic Settings**

Loop Filter Components	PLL Dynamic Settings
C18	1000 pF
R7	700 $\Omega$
C20	33 nF
R8	1.8 k $\Omega$
C22	560 pF
R10	20 k $\Omega$
C23	39 pF
CSCALE	500 $\mu$ A
Bleed Current	93.75 $\mu$ A
ABDLY	0 nS

### VCOs and Dividers

The [ADRF6612](#) has four internal VCOs. Considering the range of these VCOs, the fixed 2× prescaler after the VCO, and the LO\_DIV (1, 2, 4, 8, 16, and 32) range, the total LO range allows RF generation of 200 MHz to 2700 MHz.

### Table 19. VCO Range

VCO_SEL (Register 0x22, Bits[2:0]) <sup>1</sup>	Frequency Range (GHz) <sup>1</sup>
000	VCO_0 = 4.6 to 5.7
001	VCO_1 = 4.02 to 4.6
010	VCO_2 = 3.5 to 4.02
011	VCO_3 = 2.85 to 3.5

<sup>1</sup> For VCO\_0, VCO\_1, VCO\_2, and VCO\_3, set VTUNE\_DAC\_SLOPE (Register 0x49, Bits[13:9]) = 11 (decimal), VTUNE\_DAC\_OFFSET (Register 0x49, Bits[8:0]) = 184 (decimal), VCO\_LDO\_R2 (Register 0x22, Bits[11:8]) = 0 (decimal), and VCO\_LDO\_R4 (Register 0x22, Bits[15:12]) = 5 (decimal).

The N-divider divides down the differential VCO signal to the PFD frequency. The N-divider can be configured for fractional mode or integer mode by addressing the DIV\_MODE bit (Register 0x02, Bit 15). The default configuration is set for fractional mode.

The following equations can be used to determine the N value and the PLL frequency:

$$f_{PFD} = \frac{f_{VCO}}{2 \times N}$$

$$N = INT + \frac{FRAC}{MOD}$$

$$f_{LO} = \frac{f_{PFD} \times 2 \times N}{LO\_DIVIDER}$$

where:

$f_{PFD}$  is the phase frequency detector frequency.

$f_{VCO}$  is the voltage controlled oscillator frequency.

N is the fractional divide ratio.

INT is the integer divide ratio programmed in Register 0x02.

FRAC is the fractional divide ratio programmed in Register 0x03.

MOD is the modulus divide ratio programmed in Register 0x04.

$f_{LO}$  is the LO frequency going to the mixer core when the loop is locked.

LO\_DIVIDER is the final divider block that divides the VCO frequency down by 1, 2, 4, or 8 before it reaches the mixer (see Table 20). This control is located in the LO\_DIV bits (Register 0x22, Bits[5:3]).

**Table 20. LO Divider**

LO_DIV (Register 0x22, Bits[5:3])	LO_DIVIDER
00	1
01	2
10	4
11	8

The lock detect signal is available as one of the selectable outputs through the MUXOUT pin; a logic high indicates that the loop is locked. The MUXOUT pin is controlled by the REF\_MUX\_SEL bits (Register 0x21, Bits[14:13]); the PLL lock detect signal is the default configuration.

To ensure that the PLL locks to the desired frequency, follow the proper write sequence of the PLL registers. The PLL registers must be configured accordingly to achieve the desired frequency, and the last writes must be to Register 0x02 (INT\_DIV in Table 25),

Register 0x03 (FRAC\_DIV in Table 25), or Register 0x04 (MOD\_DIV in Table 25). When one of these registers is programmed, an internal VCO calibration is initiated, which is the last step in locking the PLL.

The time it takes to lock the PLL after the last register is written can be broken down into two parts: VCO band calibration and loop settling.

After the last register is written, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration takes approximately 5120 PFD cycles. For a 40 MHz  $f_{PFD}$ , this corresponds to 128  $\mu$ s. After calibration is complete, the feedback action of the PLL causes the VCO to eventually lock to the correct frequency. The speed with which this locking occurs depends on the nonlinear cycle-slipping behavior, as well as the small-signal settling of the loop. For an accurate estimation of the lock time, download the [ADIsimPLL™](#) tool, which correctly captures these effects. In general, higher bandwidth loops tend to lock faster than lower bandwidth loops.

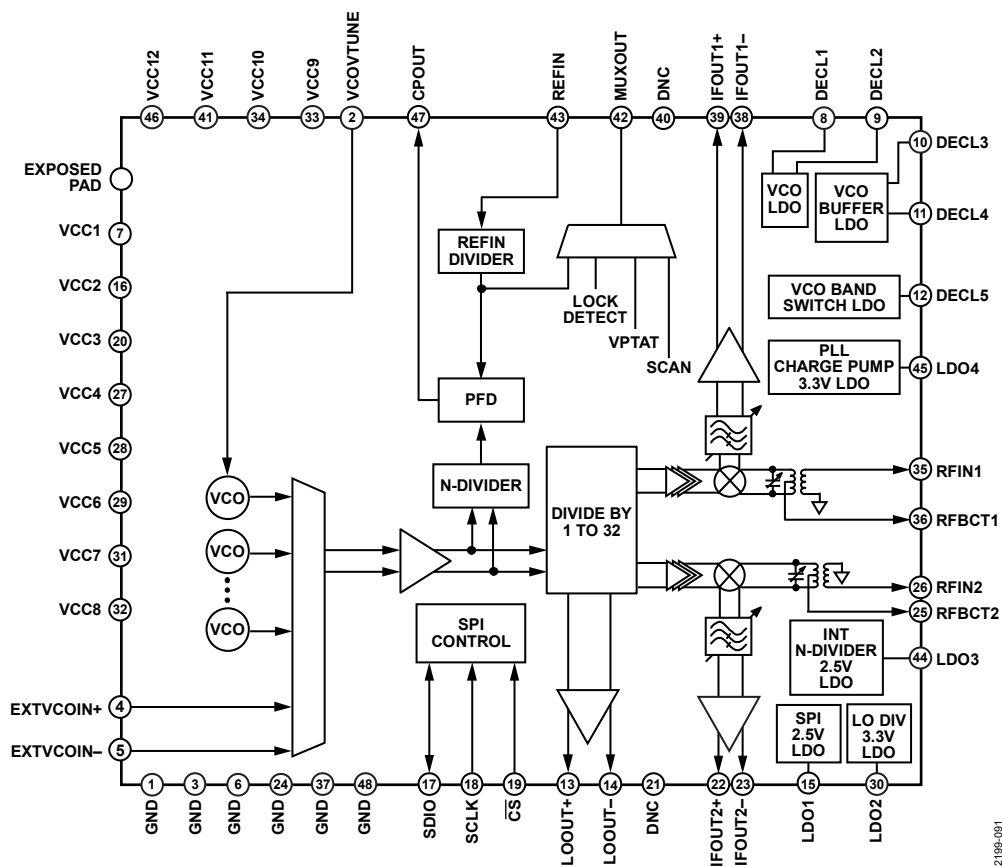
#### Additional LO Controls

To access the LO signal going to the mixer core through the LOOUT+ and LOOUT– pins (Pin 13 and Pin 14), enable the LO\_DRV\_EN bit in Register 0x01, Bit 7. This setting offers direct monitoring of the LO signal to the mixer for debug purposes; or the LO signal can be used to daisy-chain many devices synchronously. One [ADRF6612](#) can serve as the master where the LO signal is sourced, and the subsequent slave devices share the same LO signal from the master. This flexibility substantially eases the LO requirements of a system with multiple LOs.

The LO output drive level is controlled by the LO\_DRV\_LVL bits (Register 0x22, Bits[7:6]). Table 21 shows the available drive levels.

**Table 21. LO Drive Levels**

LO_DRV_LVL (Register 0x22, Bits[7:6])	Amplitude (dBm)
00	–4
01	0.5
10	3
11	4.5



12109-091

Figure 94. Simplified Schematic

## BASIC CONNECTIONS PIN DESCRIPTION

Table 22. Basic Connections

Pin No.	Mnemonic	Description	Basic Connection
5 V Power			Decouple to GND with a 10 $\mu$ F, a 0.1 $\mu$ F, and a 10 pF capacitor as close to the pin as possible.
7	VCC1	5 V VCO supply	
16	VCC2	5 V supply for SPI port	
20, 41	VCC3, VCC11	5 V biases for IF Channel 2 and IF Channel 1	
27, 28, 29, 32, 33, 34	VCC4, VCC5, VCC6, VCC8, VCC9, VCC10	5 V supplies for mixer LO amplifier	
31	VCC7	5 V supply for mixer LO divider chain	
46	VCC12	5 V supply for internal PLL	
Internal LDO Nodes			Decouple to GND with a 10 $\mu$ F and a 100 pF capacitor, as close to the pin as possible.
8, 9	DECL1, DECL2	VCO LDO outputs	
10, 11, 12	DECL3, DECL4, DECL5	External decoupling for VCO circuitry	
15	LDO1	External decoupling for internal 2.5 V SPI LDO	
30	LDO2	External decoupling for internal 3.3 V PLL/divider LDO	
44	LDO3	External decoupling for internal 2.5 V PLL LDO	
45	LDO4	External decoupling for internal 3.3 V PLL LDO	
GND			Connect directly to the PCB ground through a low impedance connection.
1	GND	External loop filter ground	
3, 6	GND	Common ground for external loop filter	
24, 37	GND	If stage, Channel 2 and Channel 1 ground	
48	GND	External charge pump ground	
SPI			
17	SDIO	SPI port data input/output	
18	SCLK	SPI port clock	
19	$\overline{CS}$	SPI port chip select	
RF, Mixer, IF Path			
4, 5	EXTVCOIN+, EXTVCOIN–	External VCO or LO inputs	DC block with 100 pF capacitors.
13, 14	LOOUT+, LOOUT–	Differential LO outputs	DC block with 100 pF capacitors.
22, 23	IFOUT2+, IFOUT2–	Channel 2 differential IF outputs	Bias to 5 V supply with 330 nH inductors and dc block with 150 pF capacitors.
25	RFBCT2	Internal mixer bias control for Channel 2 RF input	Decouple to GND with a 10 pF and a 10 nF capacitor, as close to the pin as possible.
26	RFIN2	Channel 2 single-ended RF input	DC block with a 22 pF capacitor.
36	RFBCT1	Internal mixer bias control for Channel 1 RF input	Decouple to GND with a 10 pF and a 10 nF capacitor, as close to the pin as possible.
35	RFIN1	Channel 1 single-ended RF input	DC block with a 22 pF capacitor.
38, 39	IFOUT1–, IFOUT1+	Channel 1 differential IF outputs	Bias to 5 V supply with 330 nH inductors and dc block with 150 pF capacitors.
PLL/VCO			
2	VCOVTUNE	Control voltage for internal VCO	Output from external loop filter.
43	REFIN	External reference for internal PLL	
47	CPOUT	Charge pump output	Input to external loop filter.
Other			
42	MUXOUT	Output for various internal analog signals, including PLL lock detect and VPTAT	Can be read directly from the pin; the user must be careful of loading effects, not a low impedance output.
21, 40	DNC	Do not connect	

## MIXER OPTIMIZATION

### RF INPUT BALUN INSERTION LOSS OPTIMIZATION

At lower input frequencies, more capacitance is needed. This increase is achieved by programming higher codes into BAL\_COUT. At high frequencies, less capacitance is required; therefore, lower BAL\_COUT codes are appropriate.

As shown in Figure 96 and Figure 97, this tuning range can be further optimized by adding capacitance across the RF input in conjunction with tuning BAL\_COUT. This can help to increase the low frequency range of the device significantly.

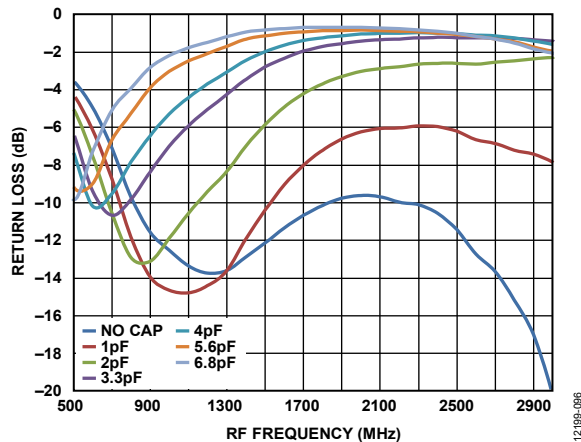


Figure 96. Return Loss; Optimum COUT vs. Tuning Capacitor on RFIN Using a High Side LO

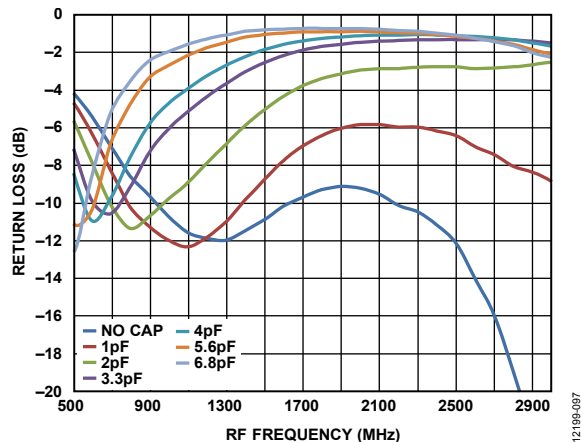


Figure 97. Return Loss; Optimum COUT vs. Tuning Capacitor on RFIN Using a Low Side LO

### IIP3 OPTIMIZATION

In applications in which performance is critical, the ADRF6612 offers IIP3 optimization. The IF amplifier bias current can be reduced to trade performance vs. power consumption. This saves on the overall power at the expense of degraded performance.

Figure 98 to Figure 101 show the IIP3 sweeps for all combinations of IFA main bias and linearity bias. The IIP3 vs. IFA main bias and linearity bias figures show both a surface and a contour plot in one figure. The contour plot is located directly underneath the surface plot. The best approach for reading the figure is to localize the

peaks on the surface plot, which indicate maximum IIP3, and to follow the same color pattern to the contour plot to determine the optimized IFA main bias and linearity bias settings.

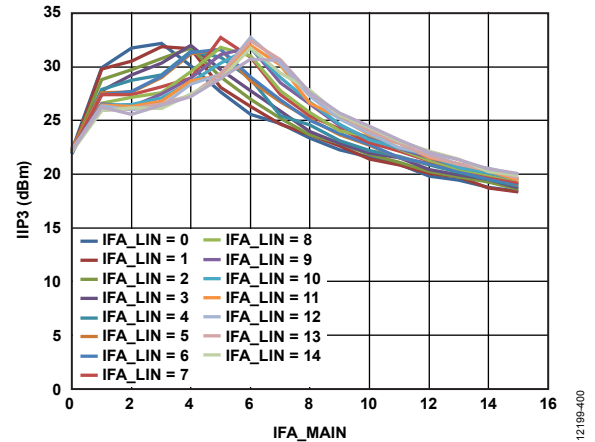


Figure 98. IIP3 vs. Main (IFA\_MAIN) and Linearity Bias (IFA\_LIN) Level at IF Frequency = 50 MHz

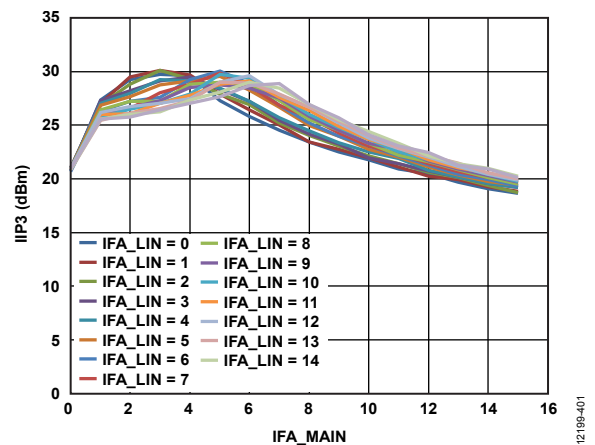


Figure 99. IIP3 vs. Main (IFA\_MAIN) and Linearity Bias (IFA\_LIN) Level at IF Frequency = 100 MHz

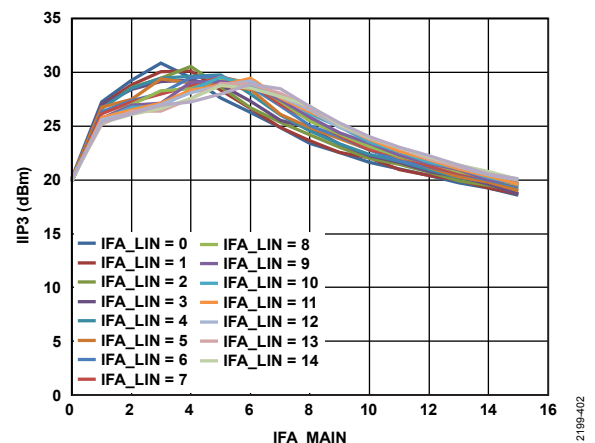


Figure 100. IIP3 vs. Main (IFA\_MAIN) and Linearity Bias (IFA\_LIN) Level at IF Frequency = 150 MHz

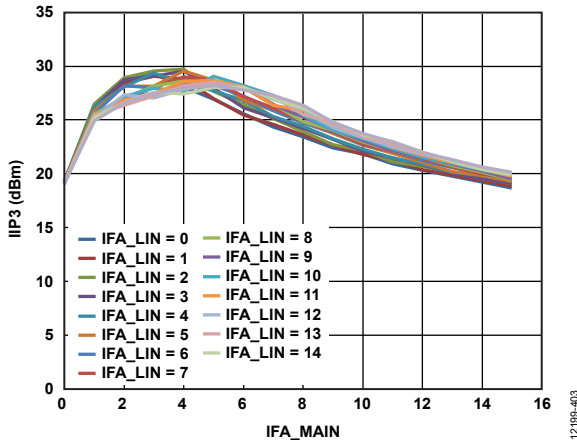


Figure 101. IIP3 vs. Main (IFA\_MAIN) and Linearity Bias (IFA\_LIN) Level at IF Frequency = 200 MHz

## VGS PROGRAMMING

The [ADRF6612](#) allows programmability for internal gate-to-source voltages for optimizing mixer performance over the desired frequency bands. The [ADRF6612](#) default VGS setting is 0. Both channels of the [ADRF6612](#) are programmed together using the same VGS setting. Power conversion gain, input IP3 NF, and input P1dB can be optimized, as shown in Figure 40, Figure 41, Figure 43, and Figure 44.

## LOW-PASS FILTER PROGRAMMING

The [ADRF6612](#) allows programmability for the low-pass filter terminating the mixer output. This filter helps to block sum term mixing products at the expense of some noise figure and gain and can significantly increase input IP3. The [ADRF6612](#) default LPF setting is 0. Both channels of the [ADRF6612](#) are programmed together using the same LPF settings. Power conversion gain, input IP3, NF, and input P1dB can be optimized, as shown in Figure 42, Figure 45, Figure 46, and Figure 49.

Table 23. Recommended Optimum Settings for High Performance Mode (in Decimal)

RF Frequency (MHz)	LO Frequency (MHz)	IFA_MAINBIAS	IFA_LINBIAS	BAL_COUT	LPF	VGS
700	497	5	11	14	4	0
800	597	5	11	14	4	0
900	697	5	11	10	4	0
1000	797	5	11	10	4	0
1100	897	5	15	10	4	0
1200	997	5	15	10	4	0
1300	1097	5	15	10	4	0
1400	1197	5	15	6	4	0
1500	1297	5	15	6	4	0
1600	1397	5	15	4	4	0
1700	1497	5	15	4	4	0
1800	1597	5	15	4	4	0
1900	1697	5	15	4	4	0
2000	1797	5	15	4	4	0
2100	1897	5	15	4	4	0
2200	1997	5	15	4	4	0
2300	2097	5	15	2	4	0
2400	2197	5	15	2	4	0
2500	2297	5	15	2	4	0
2600	2397	5	15	2	4	0
2700	2497	5	15	2	4	0
2800	2597	5	15	2	4	0
2900	2697	5	15	0	4	0
3000	2797	5	15	0	4	0

Table 24. Recommended Optimum Settings for High Efficiency Mode (in Decimal)

RF Frequency (MHz)	LO Frequency (MHz)	IFA_MAINBIAS	IFA_LINBIAS	BAL_COUT	LPF	VGS
700	497	5	15	14	4	0
800	597	5	15	14	4	0
900	697	5	15	10	4	0
1000	797	5	15	10	4	0
1100	897	5	15	10	4	0
1200	997	5	15	10	4	0
1300	1097	5	15	10	4	0
1400	1197	7	15	6	4	0
1500	1297	7	15	6	4	0
1600	1397	7	15	4	4	0
1700	1497	7	15	4	4	0
1800	1597	7	15	4	4	0
1900	1697	7	15	4	4	0
2000	1797	7	15	4	4	0
2100	1897	7	15	4	4	0
2200	1997	7	15	4	4	0
2300	2097	13	15	2	4	0
2400	2197	13	15	2	4	0
2500	2297	13	15	2	4	0
2600	2397	13	15	2	4	0
2700	2497	13	15	2	4	0
2800	2597	13	15	2	4	0
2900	2697	13	15	0	4	0
3000	2797	13	15	0	4	0

## REGISTER SUMMARY

Table 25. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW							
0x00	SOFT_RESET	[15:8] [7:0]	SOFT_RESET[15:8] SOFT_RESET[7:0]								0x0000	R							
0x01	ENABLES	[15:8] [7:0]	LO_LDO_EN	LO2_ENP	BALUN_EN	LO1_ENP	DIV2P5_EN	PWRUPRX		LO_PATH_EN	0x0000	RW							
			LO_DRV_EN	VCODBUF_LDO_EN	REF_BUF_EN	VCO_EN	DIV_EN	CP_EN	VCO_LDO_EN	LDO_3P3_EN									
0x02	INT_DIV	[15:8] [7:0]	DIV_MODE	INT_DIV[14:8] INT_DIV[7:0]							0x0058	RW							
0x03	FRAC_DIV	[15:8] [7:0]	FRAC_DIV[15:8] FRAC_DIV[7:0]								0x0250	RW							
0x04	MOD_DIV	[15:8] [7:0]	MOD_DIV[15:8] MOD_DIV[7:0]								0x0600	RW							
0x10	IF_BIAS	[15:8] [7:0]	IFA_LIN_HIEFFP	IFA_MAIN_HIEFFP	IFA_LINSLOPE		IFA_MAINSLOPE		IFA_LINBIAS[3:2]		0x02B5	RW							
			IFA_LINBIAS[1:0]		IFA_LINBIAS_EN		IFA_MAINBIAS			IFA_MAINBIAS_EN									
0x20	CP_CTRL	[15:8] [7:0]	UNUSED		CSCALE BLEED_POLARITY							0x0026	RW						
			BLEED_POLARITY		BLEED														
0x21	PFD_CTRL1	[15:8] [7:0]	UNUSED	REF_MUX_SEL		PFD_POLARITY	REFSEL[11:8] REFSEL[7:0]					0x0003	RW						
0x22	VCO_CTRL1	[15:8] [7:0]	VCO_LDO_R4 LO_DRV_LVL				LO_DIV		VCO_LDO_R2 VCO_SEL				0x000A	RW					
0x30	BALUN_CTRL	[15:8] [7:0]	UNUSED		VGS			LPF					0x0000	RW					
			BAL_COUT				RESERVED												
0x40	PFD_CTRL2	[15:8] [7:0]	UNUSED ABLDLY[2:0]						CPCTRL		ABLDLY[3] CLKEDGE		0x0010	RW					
			ABLDLY[2:0]						CPCTRL		CLKEDGE								
0x42	DITH_CTRL1	[15:8] [7:0]	UNUSED[11:4] UNUSED[3:0]				DITH_EN		DITH_MAG		DITH_VAL_H		0x000E	RW					
			UNUSED[3:0]				DITH_EN		DITH_MAG		DITH_VAL_H								
0x43	DITH_CTRL2	[15:8] [7:0]	DITH_VAL_L[15:8] DITH_VAL_L[7:0]									0x0001	RW						
0x44	SYNTH_FCNTN_CTRL	[15:8] [7:0]	UNUSED[9:2] UNUSED[1:0]						DIV_SDM_DIS		VCOCNT_CG_DIS		BANDCAL_CG_DIS		SDM_CG_DIS	SDM_DIVD_CLR	BANDCAL_DIVD_CLR	0x0000	RW
			UNUSED[1:0]						DIV_SDM_DIS		VCOCNT_CG_DIS		BANDCAL_CG_DIS		SDM_CG_DIS	SDM_DIVD_CLR	BANDCAL_DIVD_CLR		
0x45	VCO_CTRL2	[15:8] [7:0]	UNUSED VCO_BAND_SRC								BAND				0x0020	RW			
			VCO_BAND_SRC		BAND														
0x46	VCO_CTRL3	[15:8] [7:0]	UNUSED VCO_CNTR_DONE								VCO_BAND				0x0000	RW			
			VCO_CNTR_DONE		VCO_BAND														
0x47	VCO_CNTR_CTRL	[15:8] [7:0]	UNUSED[11:4] UNUSED[3:0]						VCO_CNTR_REFCNT		VCO_CNTR_CLR		VCO_CNTR_EN		0x0000	RW			
			UNUSED[3:0]						VCO_CNTR_REFCNT		VCO_CNTR_CLR		VCO_CNTR_EN						
0x48	VCO_CNTR_RB	[15:8] [7:0]	VCO_CNTR_RB[15:8] VCO_CNTR_RB[7:0]									0x0000	R						
0x49	VTUNE_DAC_CTRL	[15:8] [7:0]	UNUSED		VTUNE_DAC_SLOPE VTUNE_DAC_OFFSET[7:0]						VTUNE_DAC_OFFSET[8]		0x0000	RW					
			UNUSED		VTUNE_DAC_SLOPE						VTUNE_DAC_OFFSET[8]								
0x4A	VCO_BUF_LDO	[15:8] [7:0]	UNUSED VCODBUF_LDO_R4								VCODBUF_LDO_R2				0x0000	RW			
			VCODBUF_LDO_R4				VCODBUF_LDO_R2												
0x7C	VARIATION1	[15:8] [7:0]	IS_RESET	VCO_SW_CAL	VARIANT BE_VER				FE_VER				0x0000	R					
			IS_RESET		VCO_SW_CAL		VARIANT				FE_VER								
0x7D	VARIATION2	[15:8] [7:0]	SIF_VER				PART_ID[11:8] PART_ID[7:0]					0x2001	R						
			SIF_VER				PART_ID[11:8]												
0x7E	VARIATION3	[15:8] [7:0]	IS_RESET	VCO_SW_CAL	VARIANT BE_VER				FE_VER				0x0001	R					
			IS_RESET		VCO_SW_CAL		VARIANT				FE_VER								
0x7F	VARIATION4	[15:8] [7:0]	SIF_VER				PART_ID[11:8] PART_ID[7:0]					0x2001	R						
			SIF_VER				PART_ID[11:8]												



## REGISTER DETAILS

Address: 0x00, Reset: 0x0000, Name: SOFT\_RESET

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[15:0] SOFT\_RESET (R)  
SOFT RESET

0: any write to this register will  
assert soft reset command

Table 26. Bit Descriptions for SOFT\_RESET

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SOFT_RESET	0	Soft reset bit Any write to this register will assert soft reset command	0x0 0x0	R R

Address: 0x01, Reset: 0x0000, Name: ENABLES

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[15] LO\_LDO\_EN (RW)  
Power up LO LDO

[14] LO2\_ENP (RW)  
LO 2 enable

[13] BALUN\_EN (RW)  
Input Balun enable

[12] LO1\_ENP (RW)  
LO 1 enable

[11] DIV2P5\_EN (RW)  
enable dividers 2.5V LDO

[10:9] PWRUPRX (RW)  
Power up Rx  
0x0: Power down both mixer channels  
0x1: Power up mixer channel 1  
0x2: Power up mixer channel 2  
0x3: Power up both mixer channels

[8] LO\_PATH\_EN (RW)  
External LO path enable

[0] LDO\_3P3\_EN (RW)  
Power up 3.3V LDO

[1] VCO\_LDO\_EN (RW)  
Power up VCO LDO

[2] CP\_EN (RW)  
Power up charge pump

[3] DIV\_EN (RW)  
Power up dividers

[4] VCO\_EN (RW)  
Power up VCOs

[5] REF\_BUF\_EN (RW)  
Reference buffer enable

[6] VCOBUF\_LDO\_EN (RW)  
VCO buffer LDO enable

[7] LO\_DRV\_EN (RW)  
LO driver enable

Table 27. Bit Descriptions for ENABLES

Bits	Bit Name	Settings	Description	Reset	Access
15	LO_LDO_EN		Power up LO LDO	0x0	RW
14	LO2_ENP		LO 2 enable	0x0	RW
13	BALUN_EN		Input Balun enable	0x0	RW
12	LO1_ENP		LO 1 enable	0x0	RW
11	DIV2P5_EN		Enable dividers 2.5 V LDO	0x0	RW
[10:9]	PWRUPRX	0x0 0x1 0x2 0x3	Power up Rx Power down both mixer channels Power up mixer Channel 1 Power up mixer Channel 2 Power up both mixer channels	0x0	RW
8	LO_PATH_EN		External LO path enable	0x0	RW
7	LO_DRV_EN		LO driver enable	0x0	RW

Bits	Bit Name	Settings	Description	Reset	Access
6	VCOBUF_LDO_EN		VCO buffer LDO enable	0x0	RW
5	REF_BUF_EN		Reference buffer enable	0x0	RW
4	VCO_EN		Power up VCOs	0x0	RW
3	DIV_EN		Power up dividers	0x0	RW
2	CP_EN		Power up charge pump	0x0	RW
1	VCO_LDO_EN		Power up VCO LDO	0x0	RW
0	LDO_3P3_EN		Power up 3.3 V LDO	0x0	RW

Address: 0x02, Reset: 0x0058, Name: INT\_DIV

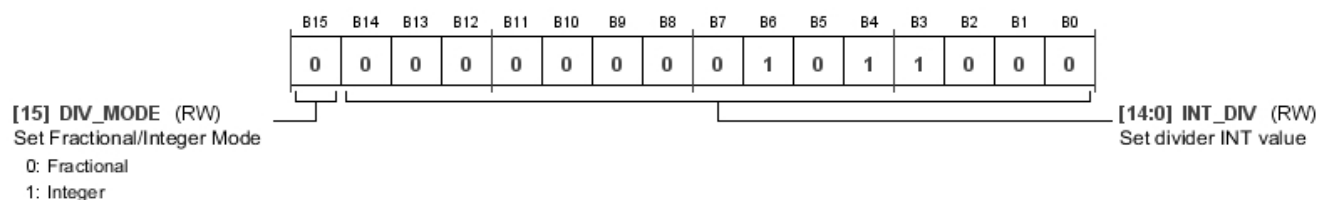


Table 28. Bit Descriptions for INT\_DIV

Bits	Bit Name	Settings	Description	Reset	Access
15	DIV_MODE	0 1	Set fractional/integer mode Fractional Integer	0x0	RW
[14:0]	INT_DIV		Set divider INT value	0x58	RW

Address: 0x03, Reset: 0x0250, Name: FRAC\_DIV



Table 29. Bit Descriptions for FRAC\_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	FRAC_DIV		Set divider FRAC value	0x250	RW

Address: 0x04, Reset: 0x0600, Name: MOD\_DIV

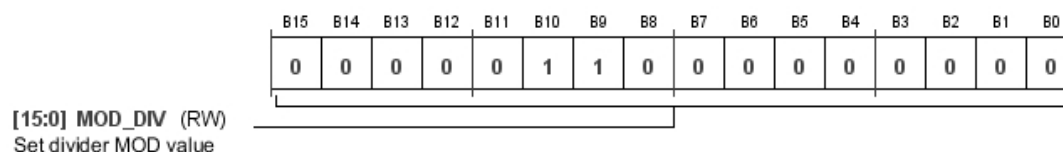


Table 30. Bit Descriptions for MOD\_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	MOD_DIV		Set divider MOD value	0x600	RW

Address: 0x10, Reset: 0x02B5, Name: IF\_BIAS

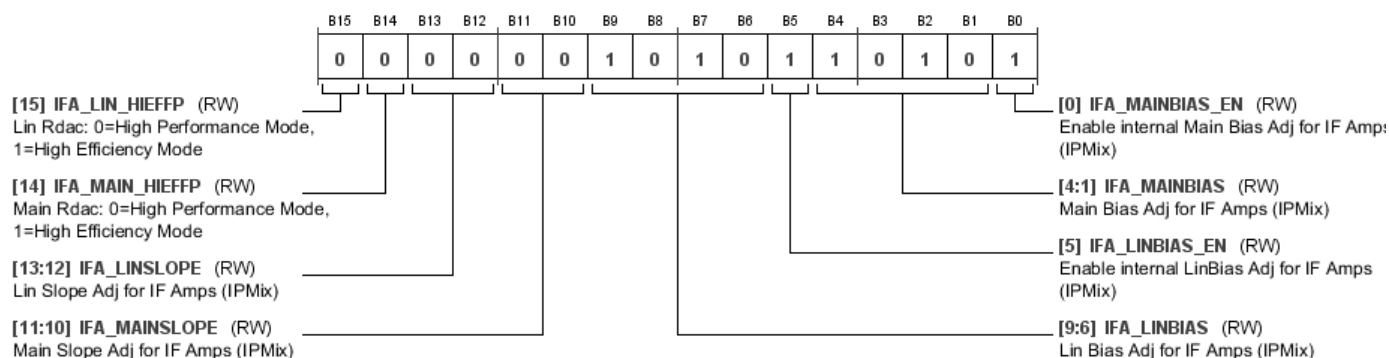


Table 31. Bit Descriptions for IF\_BIAS

Bits	Bit Name	Settings	Description	Reset	Access
15	IFA_LIN_HIEFFP		Linearity RDAC: 0 = high performance mode, 1 = high efficiency mode	0x0	RW
14	IFA_MAIN_HIEFFP		Main RDAC: 0 = high performance mode, 1 = high efficiency mode	0x0	RW
[13:12]	IFA_LINSLOPE		Linearity Slope Adj for IF amps (IPMix)	0x0	RW
[11:10]	IFA_MAINSLOPE		Main Slope Adj for IF amps (IPMix)	0x0	RW
[9:6]	IFA_LINBIAS		Linearity Bias Adj for IF amps (IPMix)	0xa	RW
5	IFA_LINBIAS_EN		Enable internal Linearity Bias Adj for IF amps (IPMix)	0x1	RW
[4:1]	IFA_MAINBIAS		Main Bias Adj for IF Amps (IPMix)	0xa	RW
0	IFA_MAINBIAS_EN		Enable internal Main Bias Adj for IF amps (IPMix)	0x1	RW

Address: 0x20, Reset: 0x0026, Name: CP\_CTRL

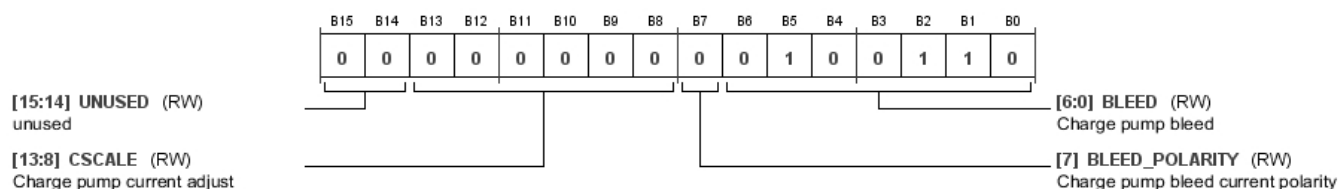


Table 32. Bit Descriptions for CP\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	UNUSED		Unused	0x0	RW
[13:8]	CSCALE		Charge pump current adjust	0x0	RW
7	BLEED_POLARITY		Charge pump bleed current polarity	0x0	RW
[6:0]	BLEED		Charge pump bleed	0x26	RW

Address: 0x21, Reset: 0x0003, Name: PFD\_CTRL1

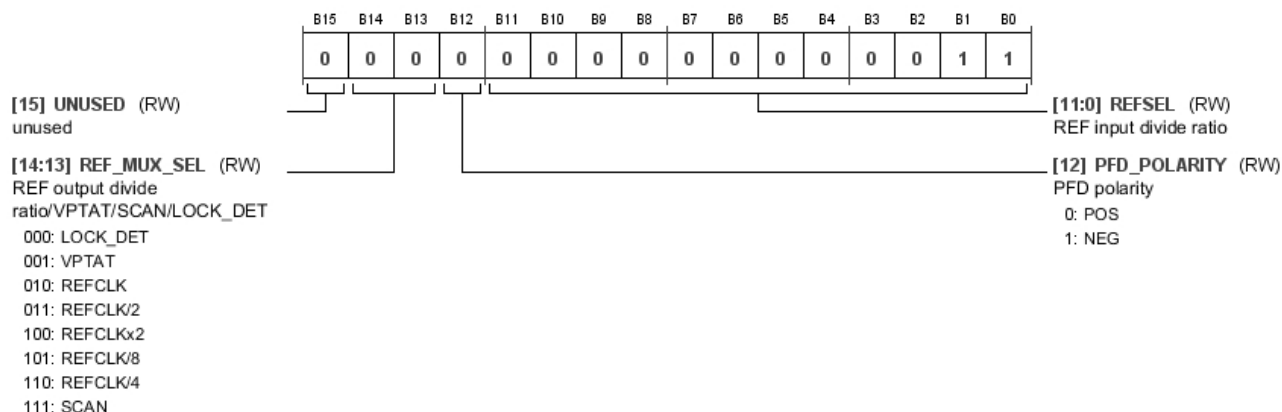


Table 33. Bit Descriptions for PFD\_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
15	UNUSED		Unused	0x0	RW
[14:13]	REF_MUX_SEL	000 LOCK_DET 001 VPTAT 010 REFCLK 011 REFCLK/2 100 REFCLKx2 101 REFCLK/8 110 REFCLK/4 111 SCAN	REF output divide ratio/VPTAT/SCAN/LOCK_DET	0x0	RW
12	PFD_POLARITY	0 POS 1 NEG	PFD polarity	0x0	RW
[11:0]	REFSEL		REF input divide ratio	0x3	RW

Address: 0x22, Reset: 0x000A, Name: VCO\_CTRL1

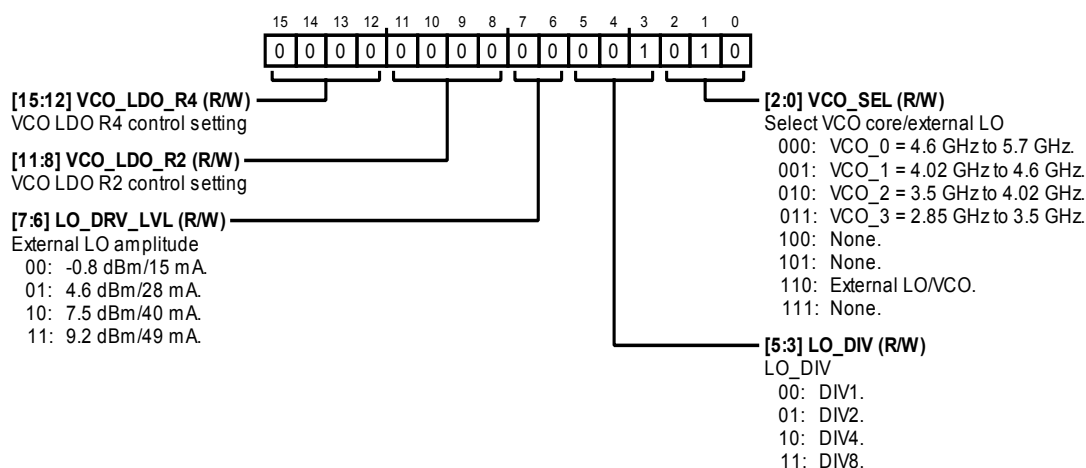


Table 34. Bit Descriptions for VCO\_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	VCO_LDO_R4		VCO LDO R4 control setting	0x0	RW
[11:8]	VCO_LDO_R2		VCO LDO R2 control setting	0x0	RW
[7:6]	LO_DRV_LVL	00 01 10 11	External LO amplitude -0.8 dBm/15 mA 4.6 dBm/28 mA 7.5 dBm/40 mA 9.2 dBm/49 mA	0x0	RW
[5:3]	LO_DIV	00 01 10 11	LO_DIV DIV1 DIV2 DIV4 DIV8	0x1	RW
[2:0]	VCO_SEL	000 001 010 011 100 101 110 111	Select VCO core/external LO VCO_0 = 4.6 GHz to 5.7 GHz VCO_1 = 4.02 GHz to 4.6 GHz VCO_2 = 3.5 GHz to 4.02 GHz VCO_3 = 2.85 GHz to 3.5 GHz None None External LO/VCO None	0x2	RW

Address: 0x30, Reset: 0x0000, Name: BALUN\_CTRL

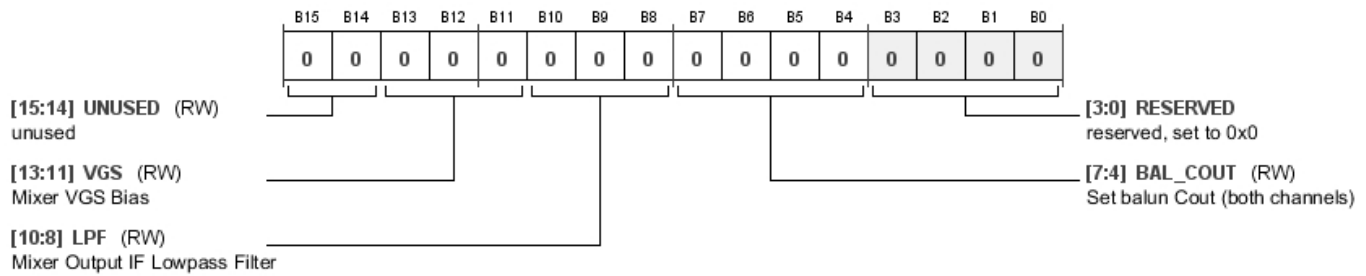


Table 35. Bit Descriptions for BALUN\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	UNUSED		Unused	0x0	RW
[13:11]	VGS		Mixer VGS bias	0x0	RW
[10:8]	LPF		Mixer output IF low-pass filter	0x0	RW
[7:4]	BAL_COUT		Set balun C <sub>OUT</sub> (both channels)	0x0	RW
[3:0]	RESERVED		Reserved, set to 0x0	0x0	RW

Address: 0x40, Reset: 0x0010, Name: PFD\_CTRL2

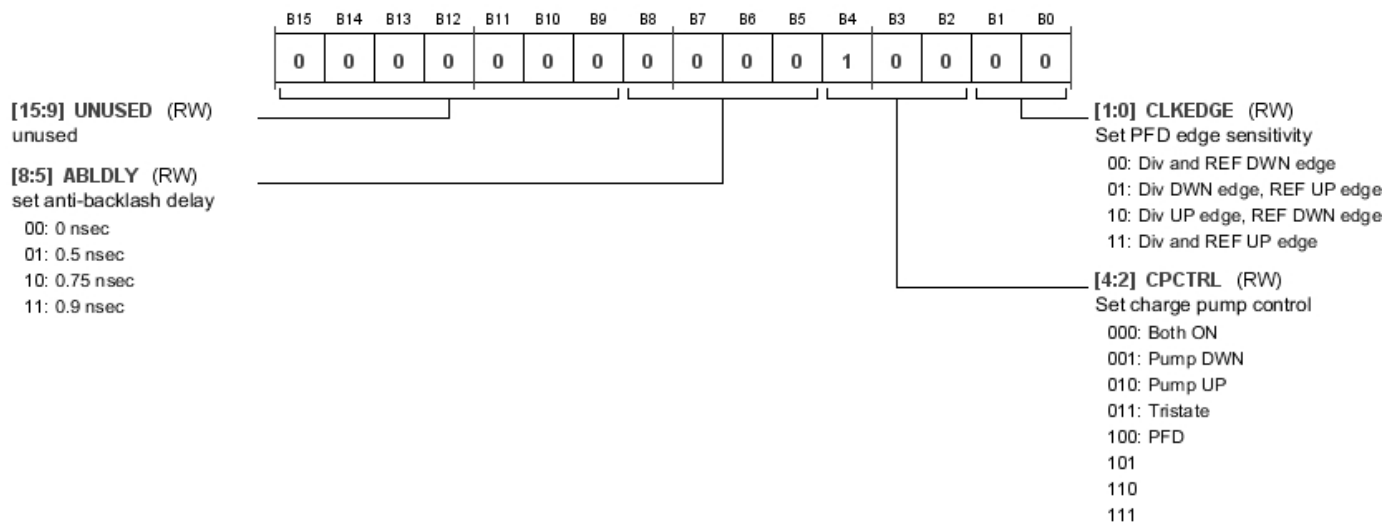


Table 36. Bit Descriptions for PFD\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	UNUSED		Unused	0x0	RW
[8:5]	ABLDLY	00 0 ns 01 0.5 ns 10 0.75 ns 11 0.9 ns	Set antibacklash delay	0x0	RW

Bits	Bit Name	Settings	Description	Reset	Access
[4:2]	CPCTRL	000 Both ON 001 Pump DWN 010 Pump UP 011 Tristate 100 PFD 101 110 111	Set charge pump control	0x4	RW
[1:0]	CLKEDGE	00 Div and REF DWN edge 01 Div DWN edge, REF UP edge 10 Div UP edge, REF DWN edge 11 Div and REF UP edge	Set PFD edge sensitivity	0x0	RW

Address: 0x42, Reset: 0x000E, Name: DITH\_CTRL1

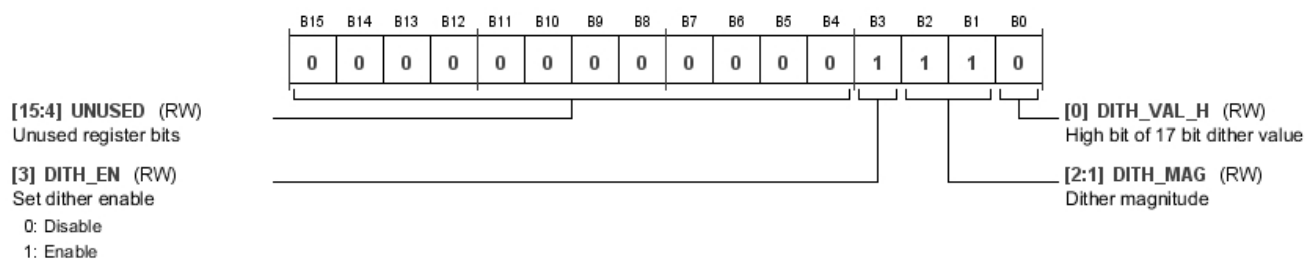


Table 37. Bit Descriptions for DITH\_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	UNUSED		Unused register bits	0x0	RW
3	DITH_EN	0 Disable 1 Enable	Set dither enable	0x1	RW
[2:1]	DITH_MAG		Dither magnitude	0x3	RW
0	DITH_VAL_H		High bit of 17 bit dither value	0x0	RW

Address: 0x43, Reset: 0x0001, Name: DITH\_CTRL2

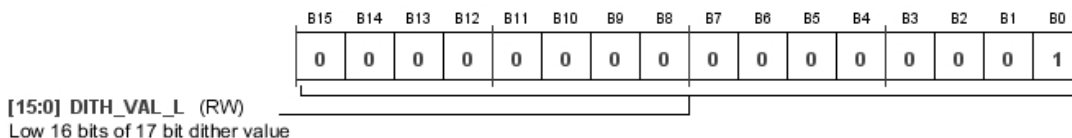


Table 38. Bit Descriptions for DITH\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DITH_VAL_L		Low 16 bits of 17 bit dither value	0x1	RW

Address: 0x44, Reset: 0x0000, Name: SYNTH\_FCNTN\_CTRL

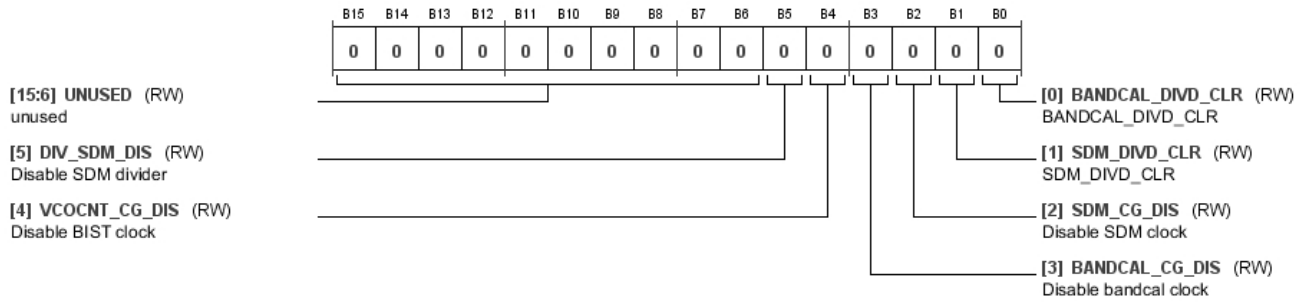


Table 39. Bit Descriptions for SYNTH\_FCNTN\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[15:6]	UNUSED		Unused	0x0	RW
5	DIV_SDM_DIS		Disable SDM divider	0x0	RW
4	VCOCNT_CG_DIS		Disable BIST clock	0x0	RW
3	BANDCAL_CG_DIS		Disable bandcal clock	0x0	RW
2	SDM_CG_DIS		Disable SDM clock	0x0	RW
1	SDM_DIVD_CLR		SDM_DIVD_CLR	0x0	RW
0	BANDCAL_DIVD_CLR		BANDCAL_DIVD_CLR	0x0	RW

Address: 0x45, Reset: 0x0020, Name: VCO\_CTRL2

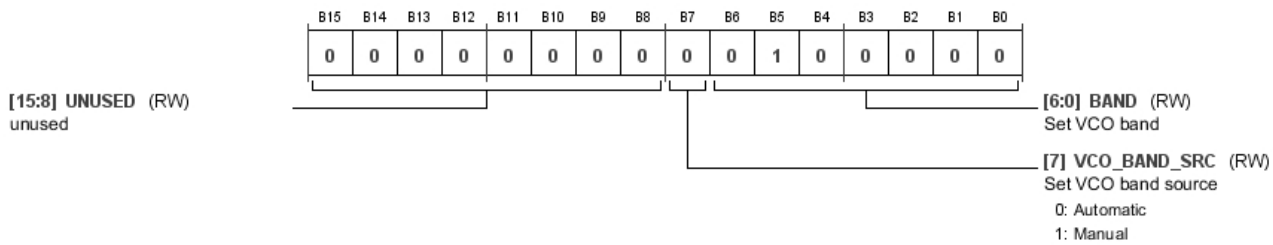


Table 40. Bit Descriptions for VCO\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	UNUSED		Unused	0x0	RW
7	VCO_BAND_SRC	0 1	Set VCO band source Automatic Manual	0x0	RW
[6:0]	BAND		Set VCO band	0x20	RW



Address: 0x46, Reset: 0x0000, Name: VCO\_CTRL3

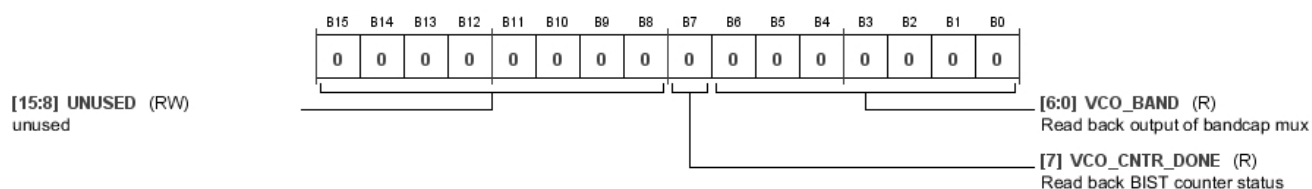


Table 41. Bit Descriptions for VCO\_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	UNUSED		Unused	0x0	RW
7	VCO_CNTR_DONE		Read back BIST counter status	0x0	R
[6:0]	VCO_BAND		Read back output of bandcap mux	0x0	R

Address: 0x47, Reset: 0x0000, Name: VCO\_CNTR\_CTRL

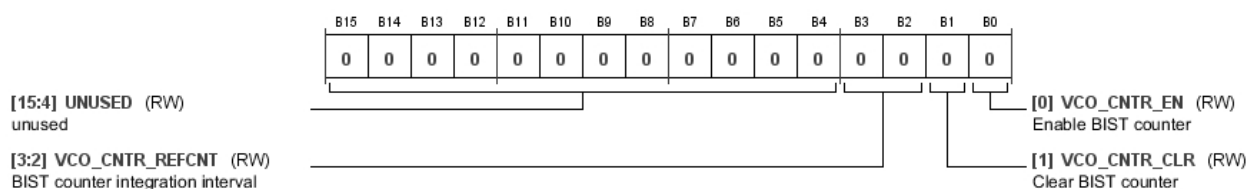


Table 42. Bit Descriptions for VCO\_CNTR\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	UNUSED		Unused	0x0	RW
[3:2]	VCO_CNTR_REFCNT		BIST counter integration interval	0x0	RW
1	VCO_CNTR_CLR		Clear BIST counter	0x0	RW
0	VCO_CNTR_EN		Enable BIST counter	0x0	RW

Address: 0x48, Reset: 0x0000, Name: VCO\_CNTR\_RB

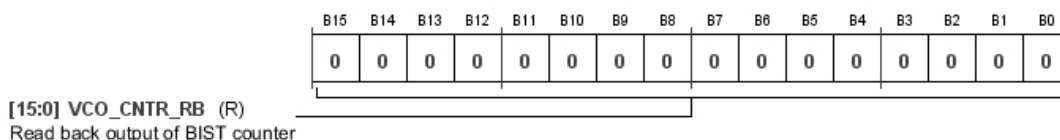


Table 43. Bit Descriptions for VCO\_CNTR\_RB

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	VCO_CNTR_RB		Read back output of BIST counter	0x0	R

Address: 0x49, Reset: 0x0000, Name: VTUNE\_DAC\_CTRL

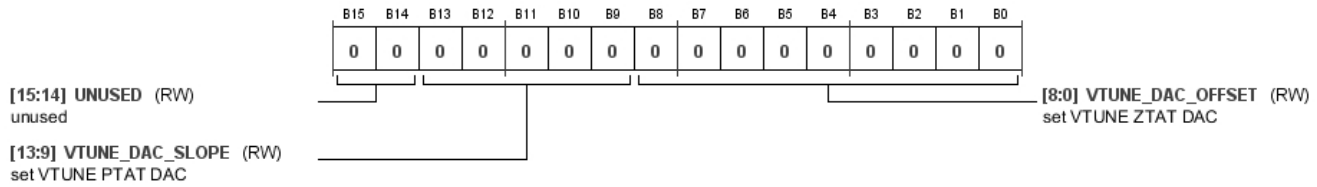


Table 44. Bit Descriptions for VTUNE\_DAC\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	UNUSED		Unused	0x0	RW
[13:9]	VTUNE_DAC_SLOPE		Set VTUNE PTAT DAC	0x0	RW
[8:0]	VTUNE_DAC_OFFSET		Set VTUNE ZTAT DAC	0x0	RW

Address: 0x4A, Reset: 0x0000, Name: VCO\_BUF\_LDO

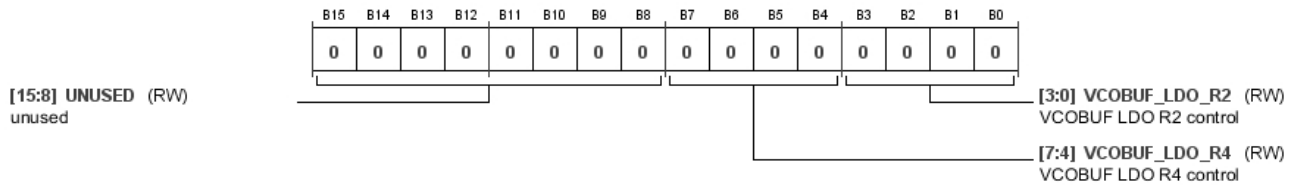


Table 45. Bit Descriptions for VCO\_BUF\_LDO

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	UNUSED		Unused	0x0	RW
[7:4]	VCOBUF_LDO_R4		VCOBUF LDO R4 control	0x0	RW
[3:0]	VCOBUF_LDO_R2		VCOBUF LDO R2 control	0x0	RW

Address: 0x7C, Reset: 0x0000, Name: VARIATION1

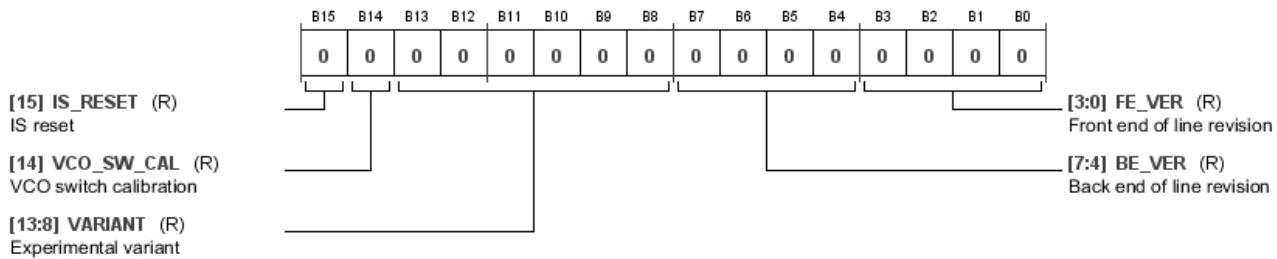


Table 46. Bit Descriptions for VARIATION1

Bits	Bit Name	Settings	Description	Reset	Access
15	IS_RESET		IS reset	0x0	R
14	VCO_SW_CAL		VCO switch calibration	0x0	R
[13:8]	VARIANT		Experimental variant	0x0	R
[7:4]	BE_VER		Back end of line revision	0x0	R
[3:0]	FE_VER		Front end of line revision	0x0	R

Address: 0x7D, Reset: 0x2001, Name: VARIATION2

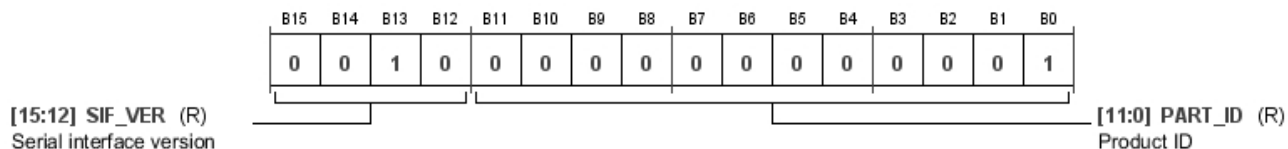


Table 47. Bit Descriptions for VARIATION2

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	SIF_VER		Serial interface version	0x2	R
[11:0]	PART_ID		Product ID	0x1	R

Address: 0x7E, Reset: 0x0001, Name: VARIATION3

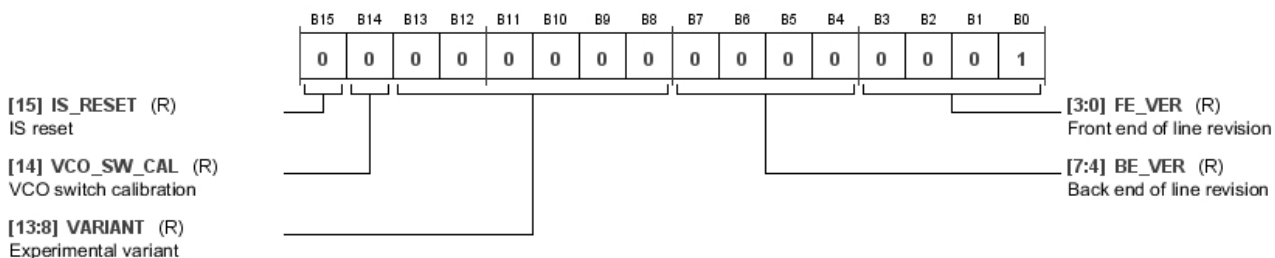


Table 48. Bit Descriptions for VARIATION3

Bits	Bit Name	Settings	Description	Reset	Access
15	IS_RESET		IS reset	0x0	R
14	VCO_SW_CAL		VCO switch calibration	0x0	R
[13:8]	VARIANT		Experimental variant	0x0	R
[7:4]	BE_VER		Back end of line revision	0x0	R
[3:0]	FE_VER		Front end of line revision	0x1	R

Address: 0x7F, Reset: 0x2001, Name: VARIATION4

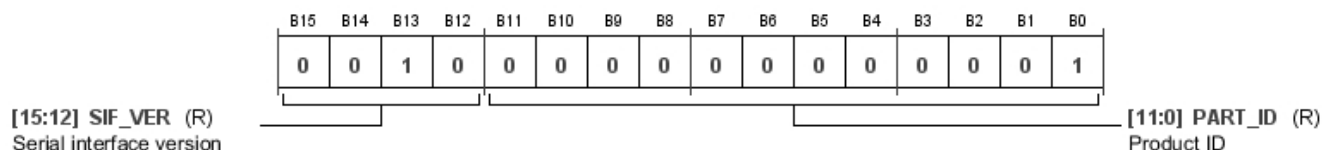


Table 49. Bit Descriptions for VARIATION4

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	SIF_VER		Serial interface version	0x2	R
[11:0]	PART_ID		Product ID	0x1	R

## APPLICATIONS INFORMATION

The ADRF6612 mixer is designed to downconvert radio frequencies (RF) primarily between 700 MHz and 2800 MHz to lower intermediate frequencies (IF) between 30 MHz and 450 MHz. Figure 95 depicts the basic connections of the mixer.

It is recommended to ac couple the RF and LO input ports to prevent nonzero dc voltages from damaging the RF balun or LO input circuit. A RFIN capacitor value of 22 pF is recommended.

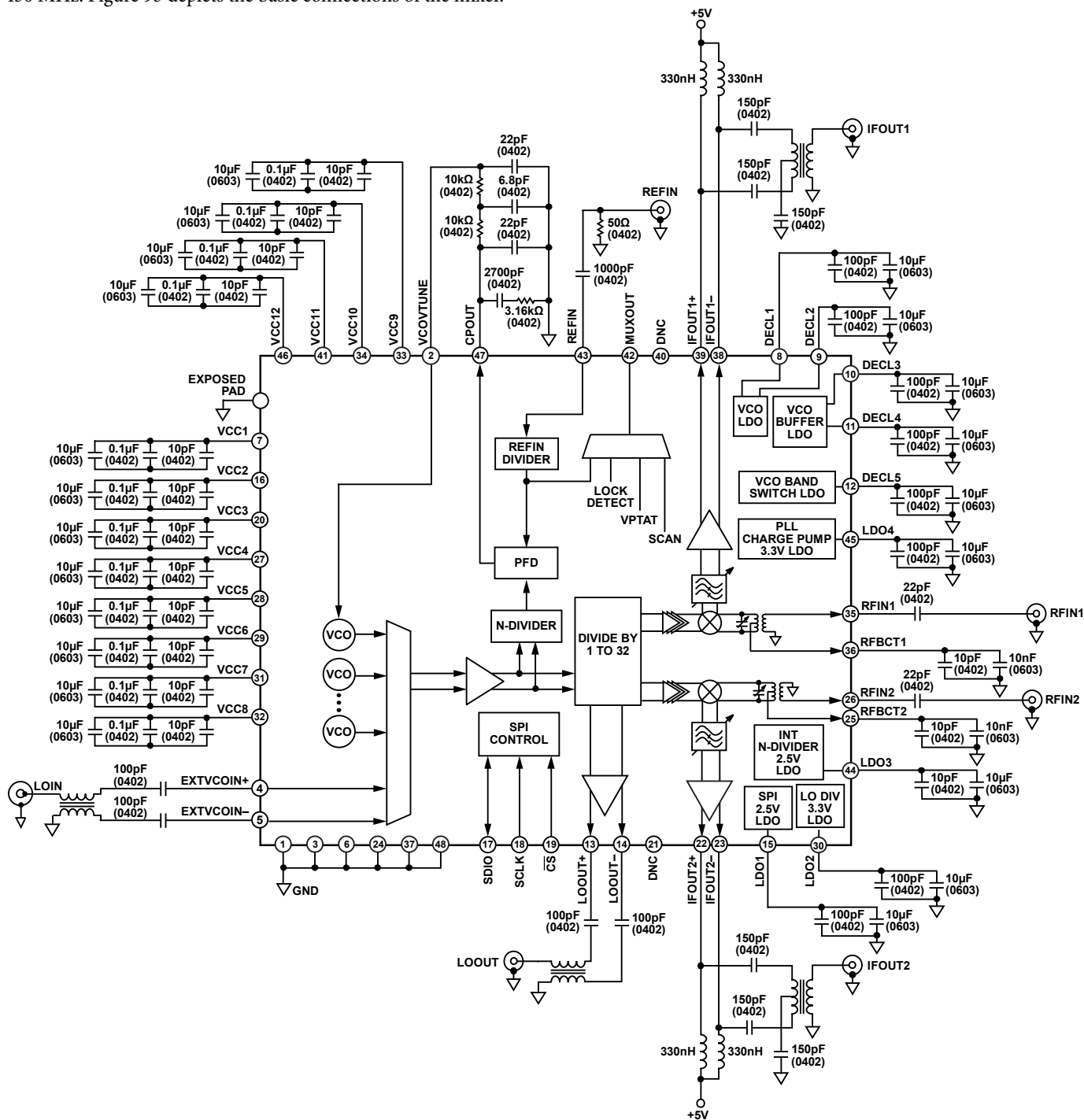
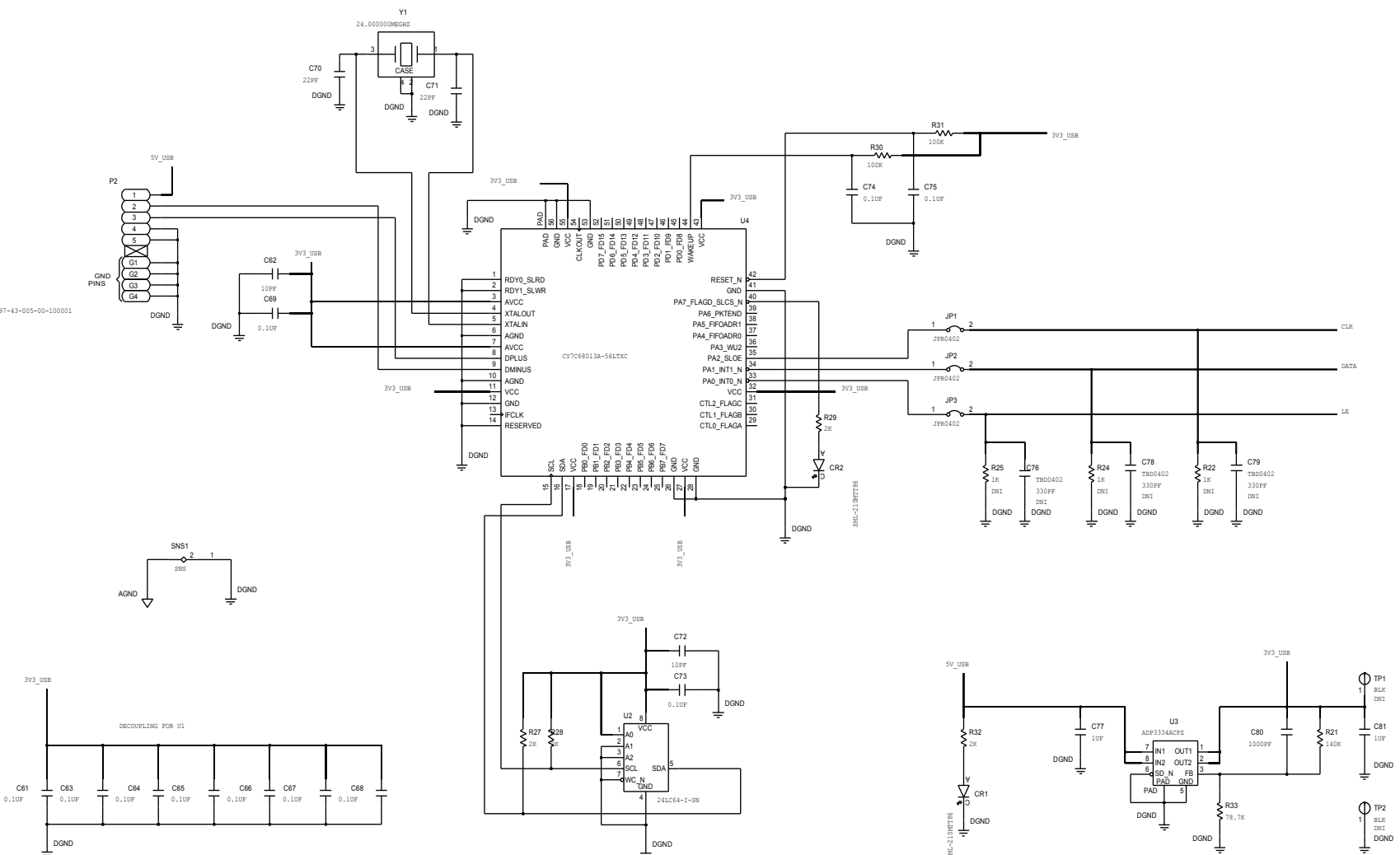


Figure 95. Basic Connections Diagram





*Figure 103. Evaluation Board, Legacy USB Interface*

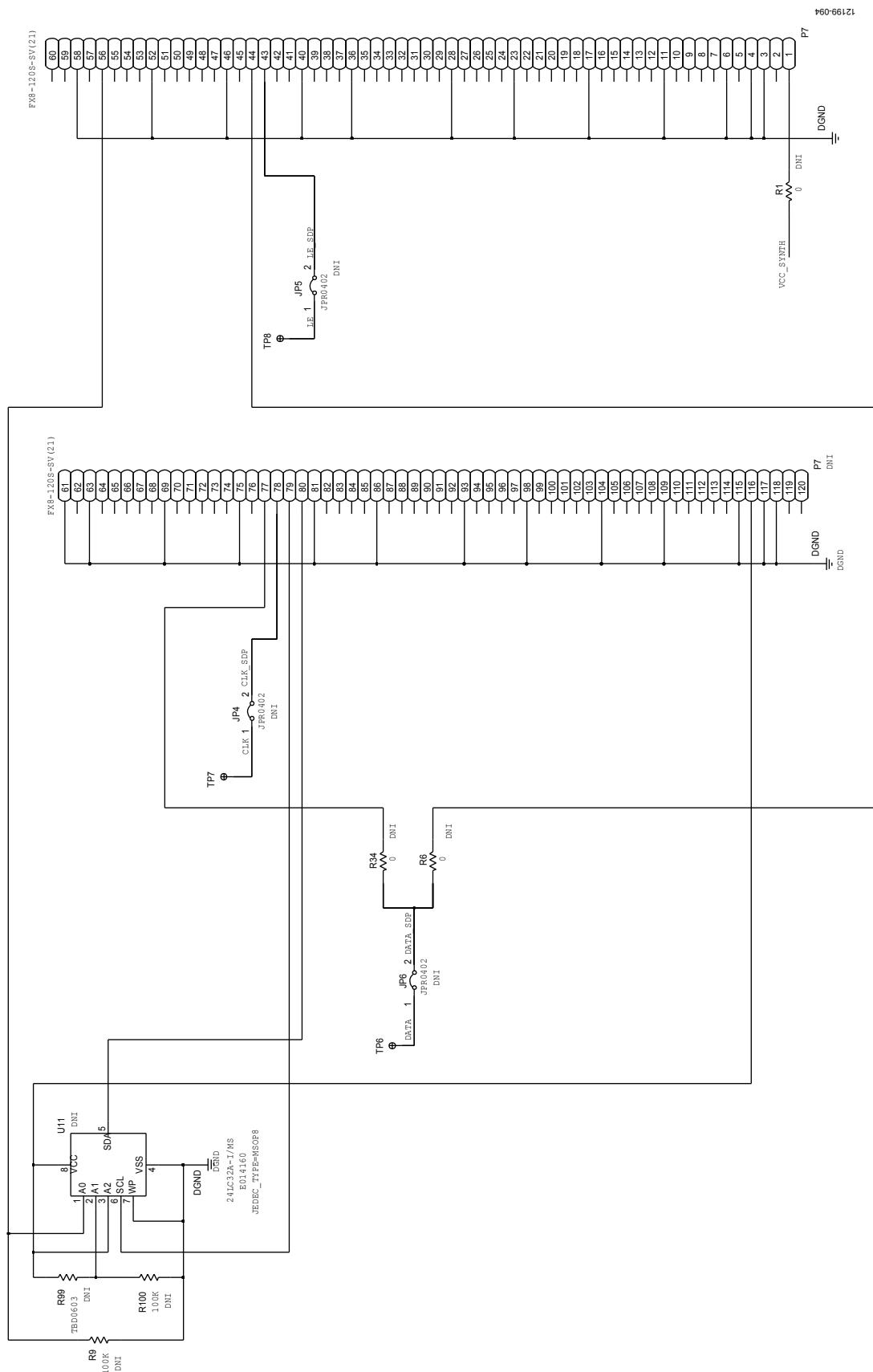


Figure 104. Evaluation Board, ADI SDP-S USB Interface

Table 50. Evaluation Board Configuration

Components	Description	Default Conditions
C1, C2, C8, C11, C12, C13, C14, C15, C18, C19, C20, C23, C26, C27	Power supply decoupling. Nominal supply decoupling consists of a 0.1 $\mu$ F capacitor to ground in parallel with a 10 pF capacitor to ground positioned as close to the device as possible.	C1, C2, C26, C27 = 0.1 $\mu$ F (size 0402), C8, C11, C12, C13, C14, C15, C18, C19, C20, C23 = 10 pF (size 0402)
C6, C7, C24, C25	RF input interface. The input channels are ac-coupled through C6 and C24. C7 and C25 provide bypassing for the center tap of the RF input baluns.	C6, C24 = 22 pF (size 0402), C7, C25 = 22 pF (size 0402)
C3, C4, C5, C28, C29, C30, L1, L2, L3, L4, R20, R21, R22, R23, T1, T2	IF output interface. The open-collector IF output interfaces are biased through pull-up choke inductors L1, L2, L3, and L4. T1 and T2 are 4:1 impedance transformers used to provide single-ended IF output interfaces, with C5 and C30 providing center-tap bypassing. Remove R21 and R22 for balanced output operation.	C3, C4, C5, C28, C29, C30 = 120 pF (size 0402), L1, L2, L3, L4 = 470 nH (size 0603), R20, R23 = open, R21, R22 = 0 $\Omega$ (size 0402), T1, T2 = TC4-1W+ (Mini-Circuits®)
C17	LO interface. C17 provides ac coupling for the LOIP local oscillator input.	C17 = 22 pF (size 0402)
R1, R2	Bias control. R1 and R2 set the bias point for the internal IF amplifier.	R1, R2 = 910 $\Omega$ (size 0402)

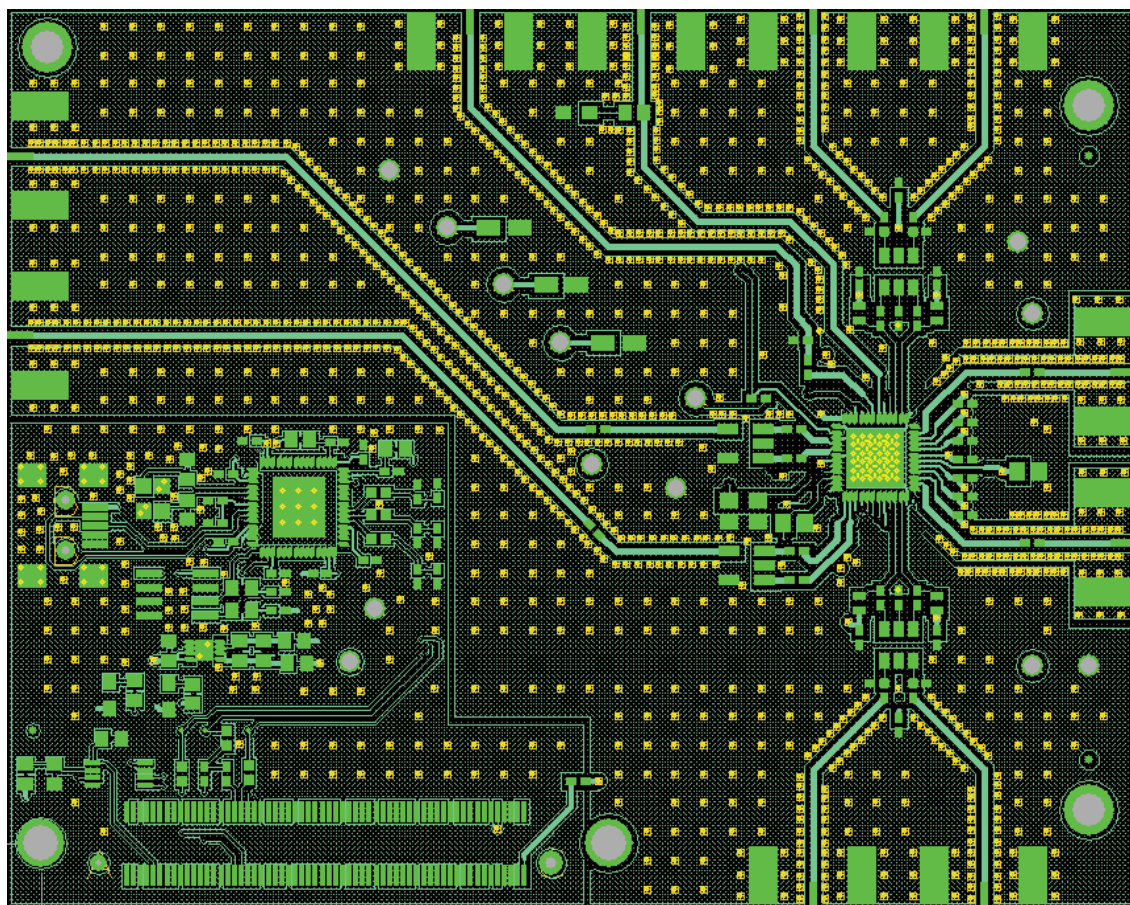
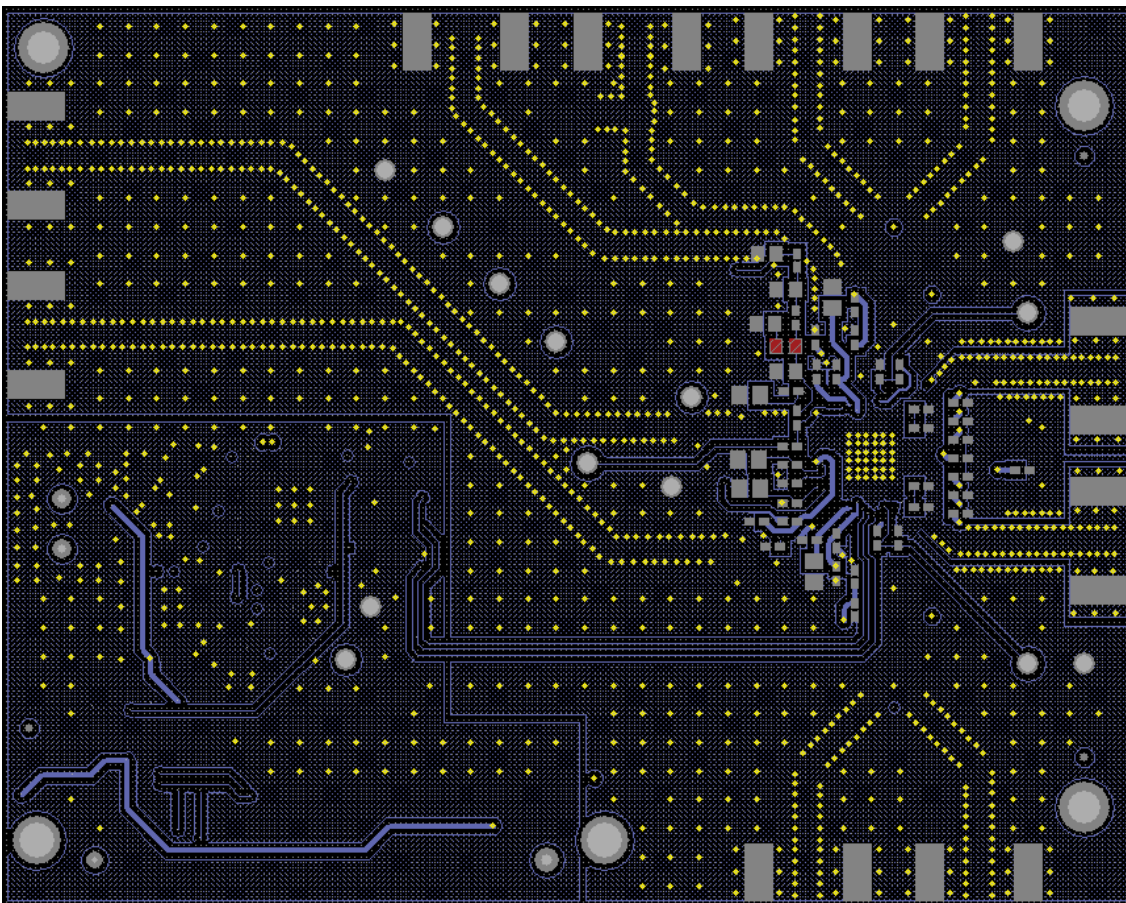


Figure 105. Evaluation Board, Top Layer

12199-205

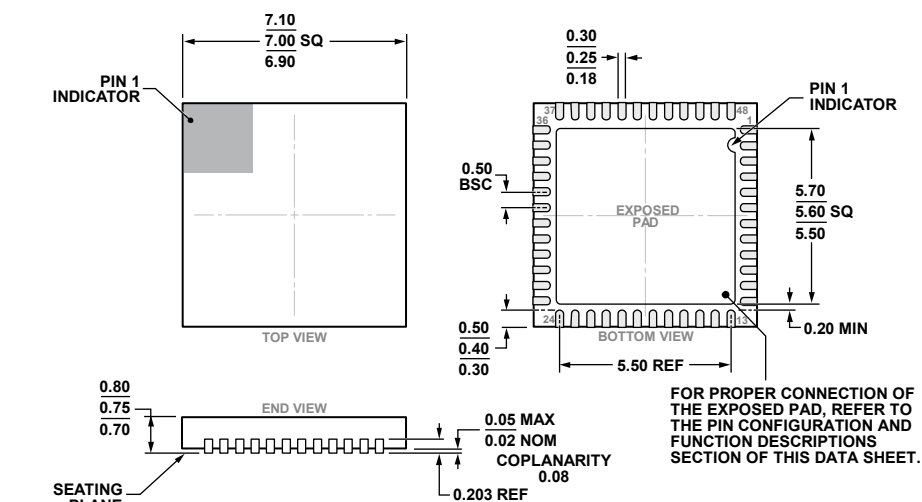




12199-206

Figure 106. Evaluation Board, Bottom Layer

## OUTLINE DIMENSIONS



## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADRF6612ACPZ-R7	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
ADRF6612-EVALZ		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.