CSE3666

Homework 9

Firm deadline: By the end of Wed, 4/24/2024.

Total Points: 100

An Excel file in XLSX format is provided. Put answers in the file and submit it in HuskyCT/ Gradescope.

The file has multiple sheets. Pay attention to the sheet names. Do not add or remove cells and do not change the filename.

The submitted file will be automatically graded. Please check the feedback from the auto grader. We will not grade submission manually. Therefore, it is important to make attempts early and correct mistakes in your work.

HW9 solutions will not be provided.

Solving homework questions is important to learning and preparation for the final exam. It is not enough to just know the correct answers or memorize the steps.

Assume 32-bit addresses in all problems.

Round answers to the nearest hundredths, *if necessary*, unless otherwise stated. For example, enter 0.5 for a half, 0.33 for a third, and 0.67 for two thirds. Enter percentages, enter 1.23% for 1.234% and 1.24% for 1.235%. Note that for the auto grader (and almost all applications), 1.24% is the same as 0.0124.

1. Cache operation.

In this problem, we assume the highest 20 bits of addresses are the same so we ignore them in this question.

Consider a cache that has 8 blocks. There are 5 bits in the block offset.

a. Initially, all the blocks in the cache are valid. The tags are provided in the table. Fill out cells H2:I9 with the highest address and the lowest address of data in each block stored in cache. The addresses in cache block 0 are provided as an example. Note that a real cache does not store these addresses. However, keeping track of addresses, instead of data, is more helpful for us to learn the cache operation.

b. The addresses in a sequence of memory reads are provided in column A. For each address, find out the tag, the cache index, the block offset, and whether the access is a miss or a hit (0 for miss and 1 for hit). Fields in the first address are provided as an example. Also, show the cache contents after each read. It is easier to copy the cache contents before the access and make changes, if needed.

2. Cache organization.

Consider a direct-mapped cache of 256 KiB. The block size is 64 bytes. Each block has two status bits.

Answer the questions in the spreadsheet.

3. Cache organization.

Consider a direct-mapped cache. The bits in an address are used in the following way when accessing the cache. The number of bits in cache index is 8 and the number of bits in the block offset is 5.

One status bit for each block indicates if a block is valid.

Answer the questions in the spreadsheet.

4. Cache performance.

Suppose a computer system has a 5-stage RISC-V processor, and separate data and instruction caches. The hit time of both caches is one cycle. The miss penalty of both caches is 80 cycles.

When the processor runs an application, the miss rate of the data cache is 10% and the miss rate of the instruction cache is 5%.

35% of the instruction executed in an application are memory accesses.

The CPI of the application is 1.6 without memory stalls.

Answer the questions in the spreadsheet. A system that has a perfect memory does not stall due to memory accesses.

5. Application.

Applications that have "streaming" workloads bring in large amounts of data but do not reuse much of it. Consider a streaming application that mainly uses an array of 1M (2^{20}) half words as working data set and accesses the elements in the array sequentially, starting from 0.

```
short int D[1024*1024]; // a short int is a half word
// access pattern is D[0], D[1], D[2], and so on
```

Assume the system has a 64KiB direct-mapped cache with 32-byte blocks. The starting address of the array is a multiple of 256. Ignore other memory references.

Answer the questions in the spreadsheet.