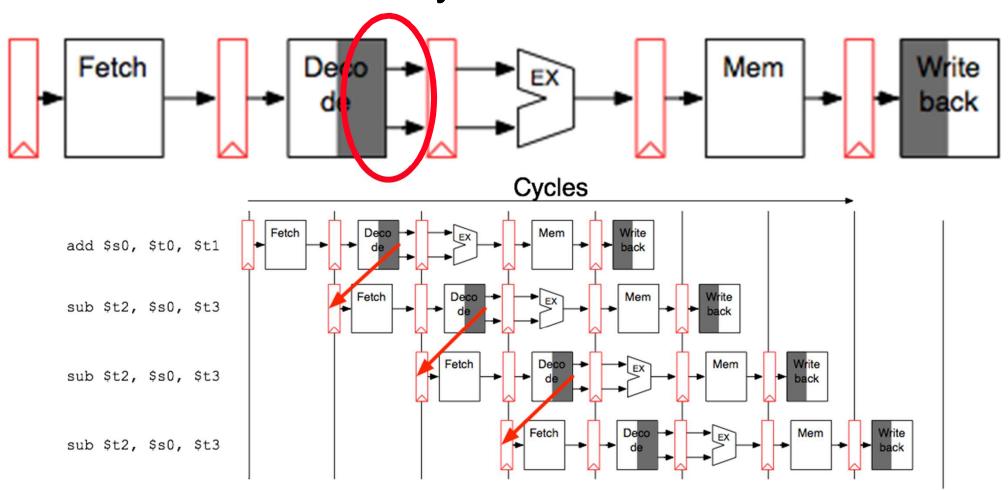
Key Points: Control Hazards

- Control hazards occur when we don't know what the next instruction is
- Caused by branches and jumps.
- Strategies for dealing with them
 - Stall
 - Guess!
 - Leads to speculation
 - Flushing the pipeline
 - Strategies for making better guesses
- Understand the difference between stall and flush

Computing the PC Normally

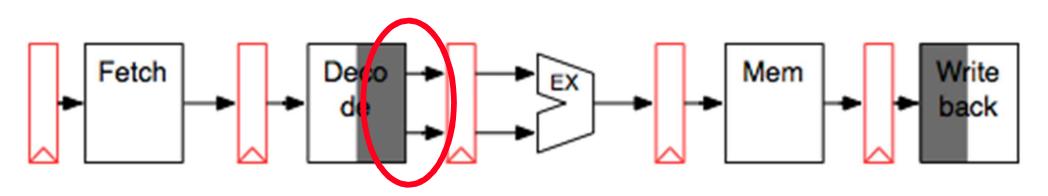
- Non-branch instruction
 - PC = PC + 4
- When is PC ready?



Fixing the Ubiquitous Control Hazard

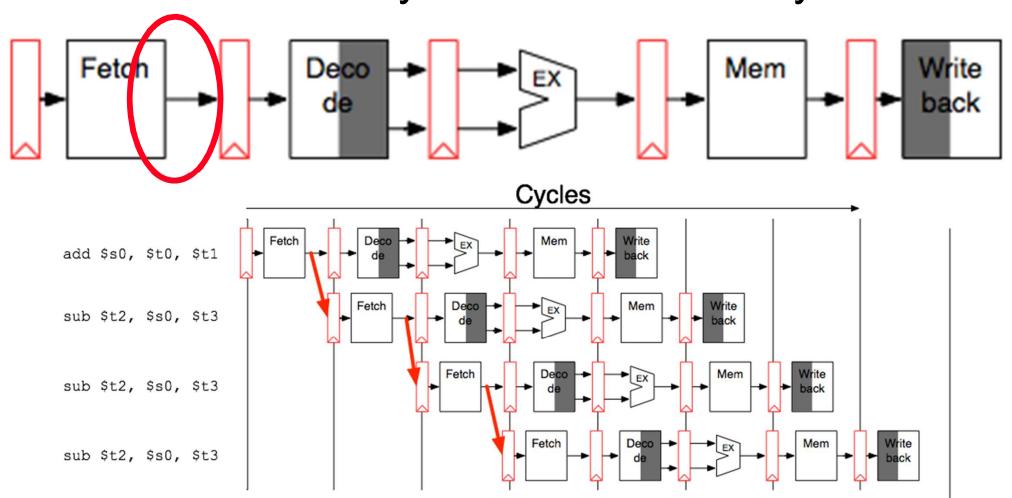
- We need to know if an instruction is a branch in the fetch stage!
- How can we accomplish this?

Solution: Partially decode the instruction in fetch (or even when you bring it into the I-Cache). You just need to know if it's a branch, a jump, or something else.



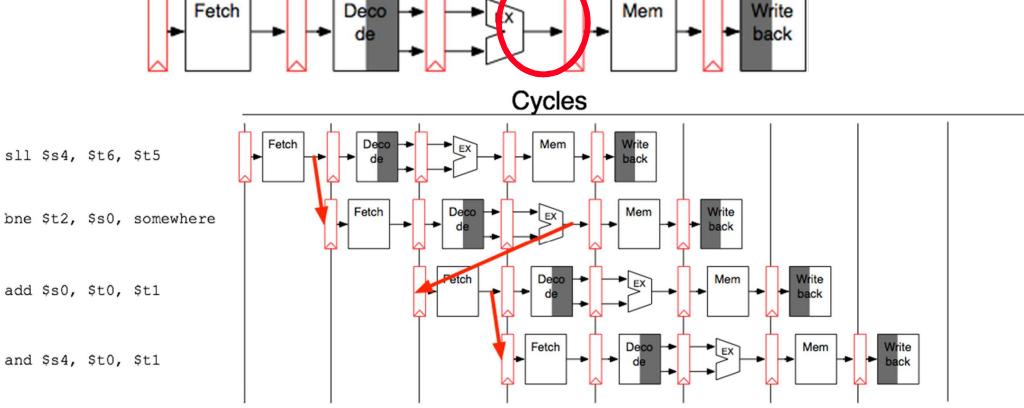
Computing the PC Normally

- Pre-decode in the fetch unit.
 - PC = PC + 4
- The PC is ready for the next fetch cycle.

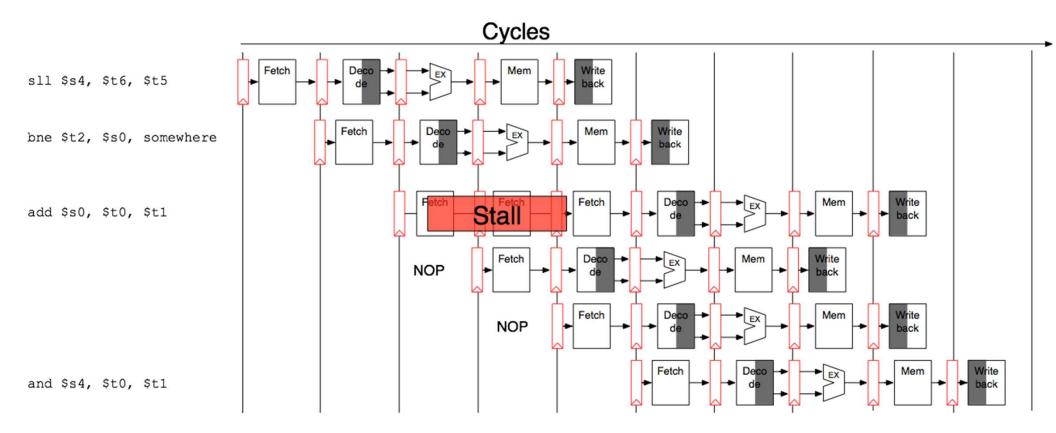


Computing the PC for Branches

- Branch instructions
 - bne \$s1, \$s2, offset
 - if (\$s1 != \$s2) { PC = PC + offset} else {PC = PC + 4;}
- When is the value ready?



Dealing with Branches: Option 0 -- stall



• What does this do to our CPI?

Option 1: The compiler

- Use "branch delay" slots.
- The next N instructions after a branch are always executed
- How big is N?
 - For jumps?
 - For branches?
- Good
 - Simple hardware
- Bad
 - N cannot change.

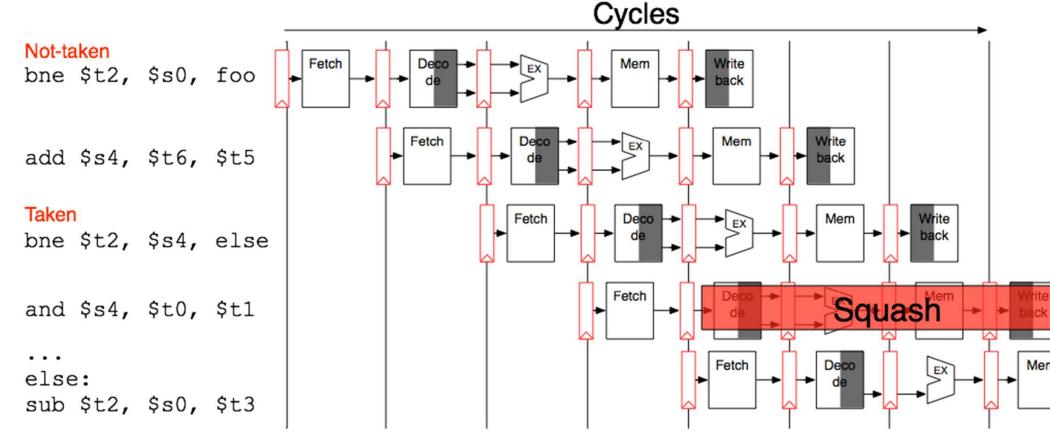
Delay slots.

Cycles Taken Fetch Mem Deco bne \$t2, \$s0, somewhere **Fetch** Deco add \$t2, \$s4, \$t1 **Branch** Delay Fetch Deco add \$s0, \$t0, \$t1 Fetch somewhere: sub \$t2, \$s0, \$t3

Option 2: Simple Prediction

- Can a processor tell the future?
- For non-taken branches, the new PC is ready immediately.
- Let's just assume the branch is not taken
- Also called "branch prediction" or "control speculation"
- What if we are wrong?
- Branch prediction vocabulary
 - Prediction -- a guess about whether a branch will be taken or not taken
 - Misprediction -- a prediction that turns out to be incorrect.
 - Misprediction rate -- fraction of predictions that are incorrect.

Predict Not-taken



- We start the add, and then, when we discover the branch outcome, we squash it.
 - Also called "flushing the pipeline"

Simple "static" Prediction

- "static" means before run time
- Many prediction schemes are possible
- Predict taken
 - Pros? Loops are commons
- Predict not-taken
 - Pros? Not all branches are for loops.
- Backward taken/Forward not taken
 - The best of both worlds!
 - Most loops have have a backward branch at the bottom, those will predict taken
 - Others (non-loop) branches will be not-taken.

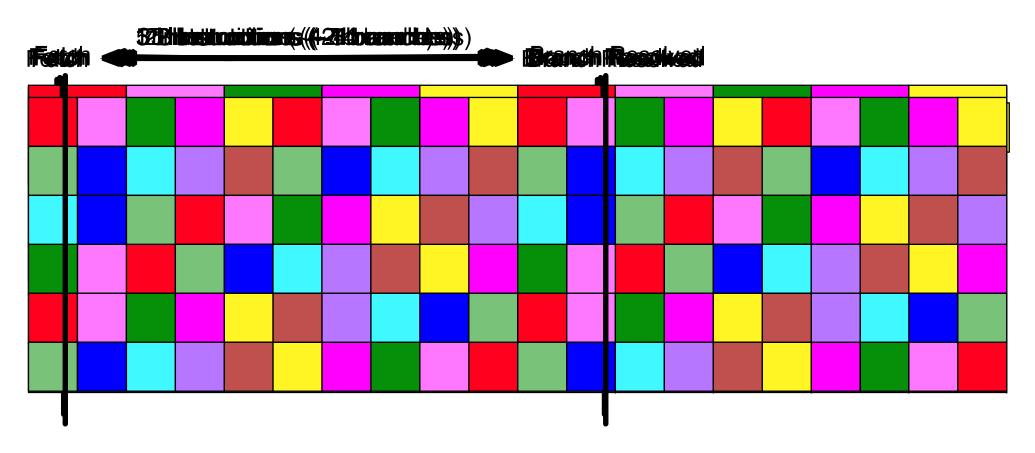
The Branch Misprediction Penalty

- The number of cycle between fetch and branch resolution is called the "branch delay penalty"
 - It is the number of instruction that get flushed on a misprediction.
 - It is the number of extra cycles the branch gets charged (i.e., the CPI for mispredicted branches goes up by the penalty for)

The Importance of Pipeline depth

- There are two important parameters of the pipeline that determine the impact of branches on performance
 - Branch decode time -- how many cycles does it take to identify a branch (in our case, this is less than 1)
 - Branch resolution time -- cycles until the real branch outcome is known (in our case, this is 2 cycles)

BTFNT is not nearly good enough!



- 14 branches @ 80% accuracy = .8^14 =4.3%
- 14 branches @ 90% accuracy = .9^14 = 22%
- 14 branches @ 95% accuracy = .95^14 =49%
- 14 branches @ 99% accuracy = .99^14 =86%

Pentium 4 pipeline

- Branches take 19 cycles to resolve
- Identifying a branch takes 4 cycles.
- Stalling is not an option.
- 80% branch prediction accuracy is also not an option.
- Not quite as bad now, but BP is still very important.
- Wait, it gets worse!!!!

1	2	3	4	5	6	7	8	9	10
TC N	xt IP	TC F	etch	Drive	Alloc	Rer	name	Que	Sch

11	12	13	14	15	16	17	18	19	20
Sch	Sch	Disp	Disp	RF	RF	Ex	Flgs	Br Ck	20 Drive

Dynamic Branch Prediction

- Long pipes demand higher accuracy than static schemes can deliver.
- Instead of making the the guess once (i.e. statically), make it every time we see the branch.
- Many ways to predict dynamically
 - We will focus on predicting future behavior based on past behavior

Predictable control

- Use previous branch behavior to predict future branch behavior.
- When is branch behavior predictable?

Predictable control

- Use previous branch behavior to predict future branch behavior.
- When is branch behavior predictable?
 - Loops -- for(i = 0; i < 10; i++) {} 9 taken branches, 1 not-taken branch. All 10 are pretty predictable.
 - Run-time constants
 - Foo(int v,) { for (i = 0; i < 1000; i++) {if (v) $\{...\}$ }.
 - The branch is always taken or not taken.
 - Corollated control
 - a = 10; b = <something usually larger than a >
 - if (a > 10) {}
 - if (b > 10) {}
 - Function calls
 - LibraryFunction() -- Converts to a jr (jump register) instruction, but it's always the same.
 - BaseClass * t; // t is usually a of sub class, SubClass
 - t->SomeVirtualFunction() // will usually call the same function

Dynamic Predictor 1: The Simplest Thing

- Predict that this branch will go the same way as the previous branch did.
- Pros?

Dead simple. Keep a bit in the fetch stage that is the direction of the last branch. Works ok for simple loops. The compiler might be able to arrange things to make it work better.

Cons?

An unpredictable branch in a loop will mess everything up. It can't tell the difference between branches.

Accuracy of 1-bit counter

Consider the following code:

```
i = 0;
do {
   if( i % 3 != 0)  // Branch Y, taken if i % 3 == 0
       a[i] *= 2;
   a[i] += i;
} while ( ++i < 100) // Branch X</pre>
```

What is the prediction accuracy of branch Y using 1-bit predictors (if all counters start with 0/not taken). Choose the

most close one.

Λ	0%	/
А.	U7	0

B. 33%

C. 67%

D. 100%

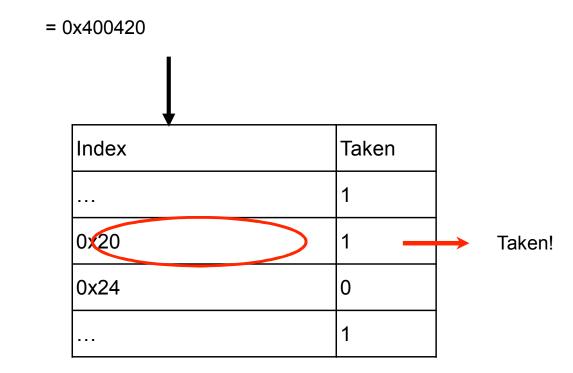
i	branch	Last branch (x) bit	Actual (y)
0	Υ	Т	Т
1	Υ	Т	NT
2	Υ	Т	NT
3	Υ	Т	Т
4	Υ	Т	NT
5	Υ	Т	NT
6	Υ	Т	Т
7	Υ	Т	NT

The 1-bit Predictor

- Predict this branch will go the same way as the result of the last time this branch executed
 - 1 for taken, 0 for not takens

PC

How big should this table be?



What about conflicts?

Accuracy of 1-bit counter

Consider the following code:

```
i = 0;
do {
   if( i % 3 != 0)  // Branch Y, taken if i % 3 == 0
       a[i] *= 2;
   a[i] += i;
} while ( ++i < 100) // Branch X</pre>
```

What is the prediction accuracy of branch Y using 1-bit predictors (if all counters start with 0/not taken). Choose the most close one.

Assume unlimited BTB entries.

A. 0% B. 33%

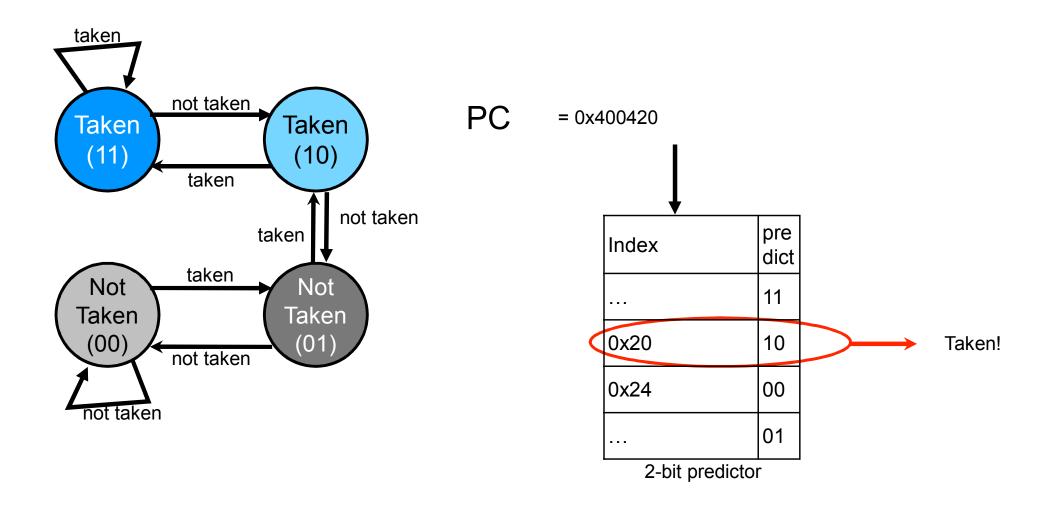
C. 67%

D. 100%

i	branch	predict	actual
0	Υ	NT	Т
1	Υ	Т	NT
2	Υ	NT	NT
3	Υ	NT	Т
4	Υ	Т	NT
5	Υ	NT	NT
6	Υ	NT	Т
7	Υ	Т	NT

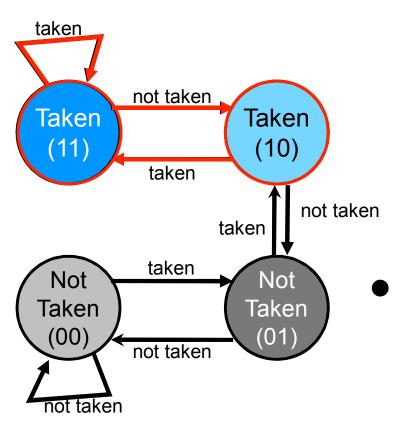
2-bit counter

- A 2-bit counter for each branch
- If the prediction in taken states, fetch from target PC, otherwise, use PC+4



Performance of 2-bit counter

2-bit state machine for each branch



```
for(i = 0; i < 10; i++)
{
    sum += a[i];
}
```

90% prediction rate!

- Application: 80% ALU, 20% Branch, and branch resolved in EX stage, average CPI?
- \bullet 1+20%*(1-90%)*2 = 1.04

Accuracy of 2-bit counter

Consider the following code:

```
i = 0;
do {
   if( i % 3 != 0)  // Branch Y, taken if i % 3 == 0
       a[i] *= 2;
   a[i] += i;
} while ( ++i < 100) // Branch X</pre>
```

What is the prediction accuracy of branch Y using 2-bit predictors (if all counters start with 00). Choose the closest one. Assume unlimited BTB entries.

A. 0%

B. 33%

C. 67%

D. 100%

i	branch	state	predict	actual
0	Υ	00	NT	Т
1	Υ	01	NT	NT
2	Υ	00	NT	NT
3	Υ	00	NT	Т
4	Υ	01	NT	NT
5	Υ	00	NT	NT
6	Υ	00	NT	Т
7	Υ	01	NT	NT

Make the prediction better

Consider the following code:

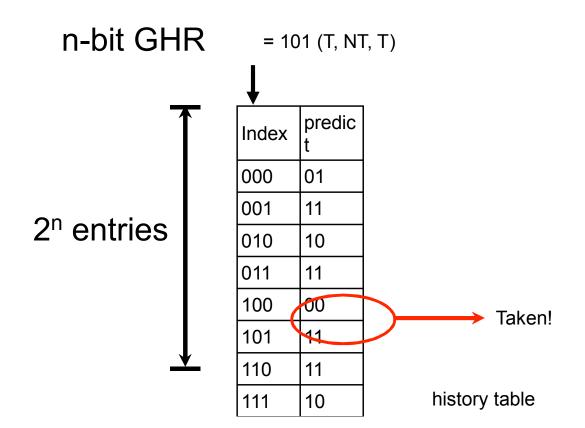
```
i = 0;
do {
   if( i % 3 != 0)  // Branch Y,
taken if i % 3 == 0
       a[i] *= 2;
   a[i] += i;
} while ( ++i < 100) // Branch X</pre>
```

Can we capture the pattern?

i	branch	result
0	Υ	Т
0	X Y X Y	Т
1	Υ	NT
1	X	Т
2	Υ	NT
i 0 0 1 1 2 2 3 3 4 4 5 5	X Y X Y X Y	Т
3	Υ	Т
3	X	Т
4	Υ	NT
4	X	Т
5	Υ	NT
5	X	Т
6 6	X Y X	Т
		Т
7	Υ	NT

Predict using history

- Instead of using the PC to choose the predictor, use a bit vector (global history register, GHR) made up of the previous branch outcomes.
- Each entry in the history table has its own counter.



Performance of global history predictor

Consider the following code:

```
i = 0;
do {
   if( i % 3 != 0)  // Branch Y,
taken if i % 3 == 0
        a[i] *= 2;
   a[i] += i;
// Branch Y
} while ( ++i < 100) // Branch X</pre>
```

Assume that we start with a 4-bit GHR= 0, all counters are 10.

Nearly perfect after this

				1		
i	?	GHR	ВНТ	prediction	actual	New BHT
0	Υ	0000	10	Т	Т	11
0	Х	0001	10	Т	Т	11
1	Υ	0011	10	Т	NT	01
1	Х	0110	10	Т	Т	11
2	Υ	1101	10	Т	NT	01
2	Х	1010	10	Т	Т	11
3	Υ	0101	10	Т	Т	11
3	Х	1011	10	Т	Т	11
4	Υ	0111	10	Т	NT	01
4	Х	1110	10	Т	Т	11
5	Υ	1101	01	NT	NT	00
5	Х	1010	11	Т	Т	11
6	Υ	0101	11	Т	Т	11
6	Х	1011	11	Т	Т	11
7	Υ	0111	01	NT	NT	00
7	Х	1110	11	Т	Т	11
8	Υ	1101	00	NT	NT	00
8	Х	1010	11	Т	Т	11
9	Υ	0101	11	Т	Т	11
9	Х	1011	11	Т	Т	11
10	Υ	0111	00	NT	NT	00

Accuracy of global history predictor

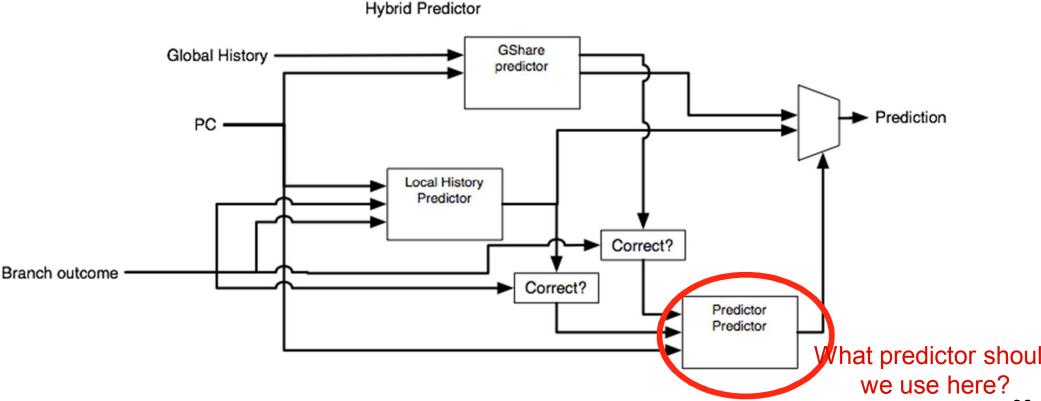
Consider the following code:

Which of predictor performs the best?

- A. Predict always taken
- B. Predict alway not-taken
- C. 1-bit predictor
- D. 2-bit predictor
- E. 4-bit global history with 2-bit counters

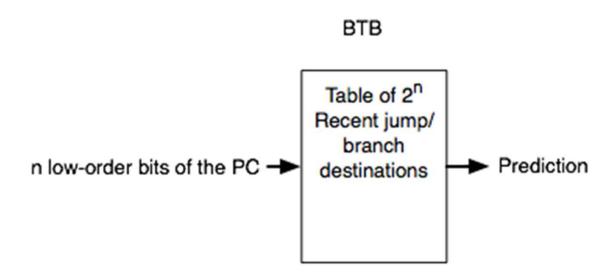
Other Ways of Identifying Branches

- How do we get the best of all possible worlds?
- Build them all, and have a predictor to decide which one to use on a given branch -- The Hybrid (or Tournament) Predictor
 - 2-bit predictor now has different states
 - Strongly prefer GShare, weakly prefer Gshare, weakly prefer local, strongly prefer local.



Predicting Function Invocations

- Branch Target Buffers (BTB)
 - Use a table, indexed by PC, that stores the last target of the jump.
 - When you fetch a jump, start executing at the address in the BTB.
 - Update the BTB when you find out the correct destination.
- The BTB is useful for predicting function calls and jump instructions (and some other things, as we will see shortly.)



Predicting Returns

- Function call returns are hard to predict
 - For every call site, the return address is different
 - The BTB will do a poor job, since it's based on PC
- Instead, maintain a "return stack predictor"
 - Keep a stack of return targets
 - jal pushes \$ra onto the stack
 - Fetch predicts the target for retn instruction by popping an address off the stack.
 - Doesn't work in MIPS, because there is no return instruction.

Return Address Predictor

