LANL Neuromorphic

Adam O'Brien
Cason Love

CONCEPT OF OPERATIONS

REVISION – 1
10 February 2023

CONCEPT OF OPERATIONS
FOR
LANL Neuromorphic

TEAM <20>

APPROVED BY:

Project Leader Date

Prof. Kalafatis Date

T/A Date

Change Record

Rev.	Date	Originator	Approvals	Description
-	2/10/2023	Cason Love	Adam O’Brien	Draft Release

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1. Executive Summary

The reason for designing the LANL Neuromorphic Chip is to demonstrate the potential of analog, specifically neuromorphic, processors. The circuit will take in human speech through a microphone and have one output wire that leads into the reservoir, or processor. The reservoir will take this input and calculate a series of algorithms and output this information to the matrix multiplication circuit, which will display whether the phrase was an activation phrase or not. The signal will be analog throughout the entire circuit, and this will display the advantages of neuromorphic circuits.

2. Introduction

The reason for creating the LANL Neuromorphic Chip is to display the power of analog, specifically neuromorphic, processors. To facilitate this exhibition, we will design a voice recognition circuit that has three parts as follows: microphone, reservoir, or processor, and finally the output, which will be in the form of a matrix multiplication circuit. The LANL Neuromorphic Chip will have a specific activation phrase and will take user speech as input, distinguishing whether the user has spoken the activation phrase or not and display an output for each outcome that is calculated. It has a multitude of possible implementations and is meant to be a demonstration of the power of our neuromorphic computing technology to chip manufacturers.

2.1. Background

Most computers of today use the von Neumann architecture, which is a system in which data is transferred back and forth between a central processor and memory through sequences of linear computations. While this architecture is great for performing calculations and executing written programs, it is not ideal for processing more abstract and organic data such as sound and images. The current answer to this dilemma is neuromorphic computing. Neuromorphic computing attempts to model the way the human brain processes information, allowing systems to learn and process abstract data much more efficiently.

Another problem with von Neumann architecture is the von Neumann bottleneck, which notes the limitations of computer speed to the speed of the processor retrieving data and instructions. In turn, most of the power is used for shuttling memory back and forth. Neuromorphic circuits solve this problem by allowing for much higher processing speeds at much lower power.

The LANL Neuromorphic chip aims to demonstrate the abilities of neuromorphic computing in voice recognition technology. The system will take in human speech and be able to recognize whether the input is a specified activation phrase. Our system will also be much more efficient and cost effective than current neuromorphic chips on the market, as they will be made of far fewer components. This system can have a multitude of applications, such as turning on another system, setting an alarm, etc.

2.2. Overview

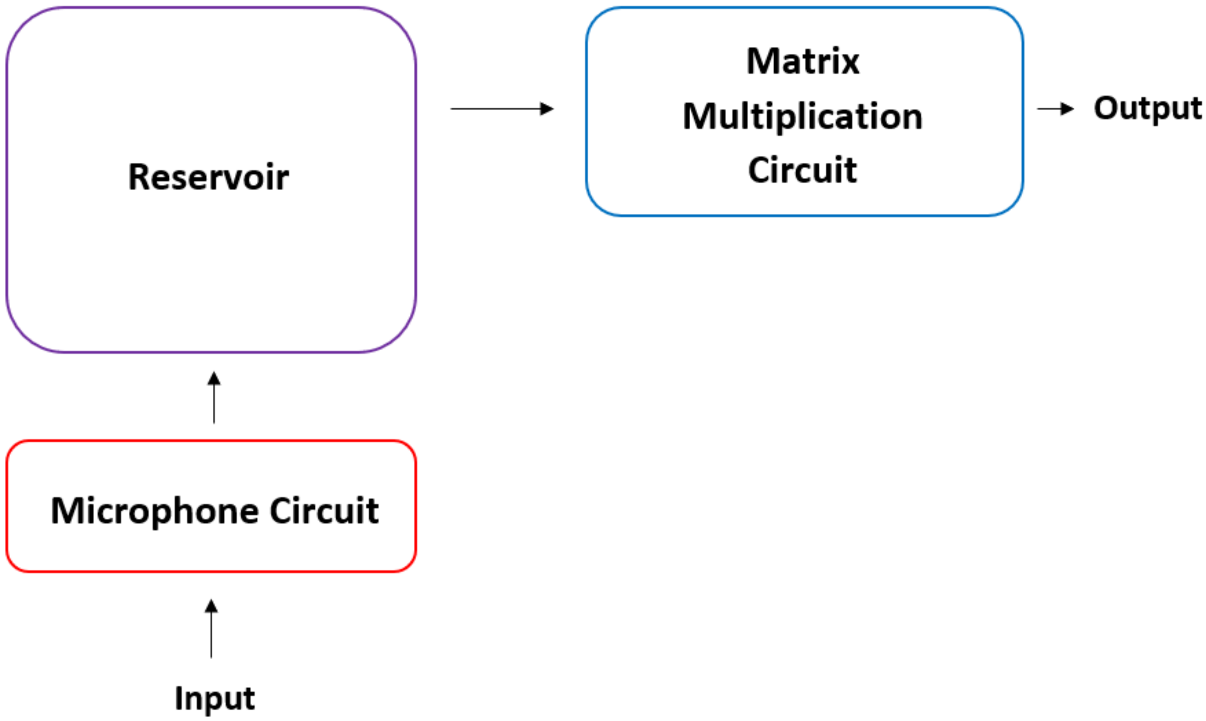

Figure 1: LANL Neuromorphic Chip System Block Diagram

Our system will demonstrate the power of neuromorphic computing through voice recognition technology. A small microphone will be used in the system to pick up user speech. The microphone circuit will amplify the input signal and deliver it to the reservoir, where most of the computing will be done. The reservoir is the learning environment of the chip and will comprise various subcircuits. Once the reservoir has mapped the input signal to a specific matrix output, it will be read by the matrix multiplication circuit. The matrix multiplication circuit will perform matrix multiplication on the output of the reservoir to determine whether the user speech was the specified activation phrase or not. Section 3.3 will describe each subsystem in greater detail.

2.3. Referenced Documents and Standards

Hof, Robert D. “Neuromorphic Chips.” *MIT Technology Review*, MIT Technology Review, 17 Sept. 2021, https://www.technologyreview.com/technology/neuromorphic-chips/.

Martinuzzi, Francesco. “A Brief Introduction to Reservoir Computing.” *Francesco Martinuzzi*, Xxxx, 26 May 2020, https://martinuzzifrancesco.github.io/posts/a-brief-introduction-to-reservoir-computing/#top.

“MT-079: Analog Multipliers.” *Analog*, Analog Devices, https://www.analog.com/media/en/training-seminars/tutorials/MT-079.pdf.

3. Operating Concept

3.1. Scope

The LANL Neuromorphic Chip is meant to be a system to demonstrate the power of neuromorphic computing through voice recognition. The system will be able to recognize a specific activation phrase from a user and will do so at greater speed and lower power compared to that of a traditional chip. It will also learn and train outputs on the singular chip, doing the work of what would require multiple traditional chips/processors. While it can have a multitude of applications, the LANL Neuromorphic Chip is ideal for processing human speech in smaller devices such as mobile phones and tablets.

3.2. Operational Description and Constraints

The LANL Neuromorphic Chip will operate by having a user speak into the microphone. If the user says the activation phrase, it will be signified in the output. The output will be visualized by two LEDs. If the user speaks into the microphone but does not say the activation phrase, the corresponding LED will light up, and vice versa. The system will only be made to recognize human speech, within the ranges of roughly 80 to 260 Hz.

3.3. System Description

- Microphone Circuit: This subsystem will take in user speech through a microphone. The circuit will then amplify this input signal for the Reservoir subsystem.

- Reservoir: This subsystem is a physical reservoir that will utilize reservoir computing to map the user input to a certain matrix output.

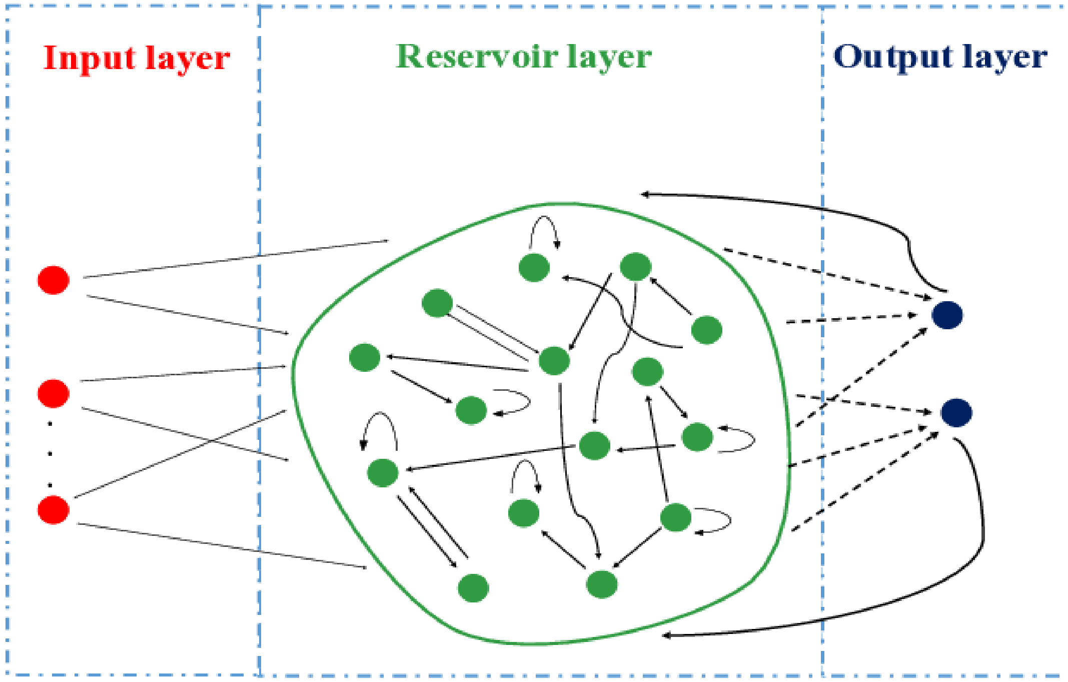

Figure 2: Diagram illustrating the concept of reservoir computing

Figure 2. depicts how reservoir computing works. Put simply, an input is given to the reservoir layer and passed through a series of non-linear units in recurrent loops. These units allow for the system to learn and store information. In this project, we will have the Reservoir recognize specific frequencies associated with the activation phrase. The circuitry for this subsystem will be built based on a pre-existing design created by Dr. Michael Saccone, the LANL lead on this project. The algorithms for reservoir computing have also been created by Dr. Saccone.

- Matrix Multiplication Circuit: This subsystem will perform matrix multiplication on the matrix output from the reservoir to determine whether the user input is the activation phrase. This is necessary as the Reservoir will produce multiple different outputs. The matrix multiplication on the Reservoir output will narrow it down to a binary output, i.e., a voltage range that either turns the LED on or a voltage range that does not turn the LED on. The idea behind the matrix multiplication is to have the Reservoir output 4 distinct voltage values, which this subsystem will perform addition and multiplication (dot product) on to produce the result.

3.4. Modes of Operations

This system will have a singular mode of operation, which will simply react to user speech. It will then discern whether the human speech was the specified activation phrase or not.

3.5. Users

Provide detail who will be using your system. Provide some user characteristics such as level of training required for installation, use, and who will benefit from your proposed system.

3.6. Support

Documentation on the system would be provided to users, showing how each subsystem works and how reservoir computing is utilized to create voice recognition hardware.

4. Scenario(s)

4.1. Activating Another Device

This system could be used to turn on another device. For example, the activation phrase can cause our system to supply a certain voltage to the output, which could be the necessary voltage to power on another device connected to the system. This is likely the most generic application of our system.

4.2. Embedded Within a Device

This system could be embedded within a device such as a mobile phone and be used to perform a task on the device using voice activation. For example, the activation phrase could be “Set Alarm”, and the device would set the alarm function on your mobile phone.

5. Analysis

5.1. *Summary of Proposed Improvements*

- The LANL Neuromorphic Circuit will be much more efficient due to its low power usage
- This system will be much better at processing abstract data - specifically human speech - than digital systems due to its ability to learn by imitating neurons in the human brain
- Much cheaper than using algorithms designed for voice recognition on traditional hardware, due to the significant decrease in required components.

5.2. *Disadvantages and Limitations*

The LANL Neuromorphic Circuit will possibly have limitations such as:

- Analog circuit components are bigger than digital counterparts
- Analog operations are more susceptible to noise, and the greater complexity of operations on the chip can increase the likelihood of miscalculations

5.3. *Alternatives*

- Pre-existing neuromorphic circuits in use already
- Digital computers can be trained to model neural networks

5.4. *Impact*

There are multiple impacts that can outcome from this project like:

- Showcase the advancement of analog processors to further the evolution of them
- Reducing the number of components may reduce production costs/time for companies, as well as decrease their carbon footprint
- Allowing all training of data/learning on the hardware will improve privacy for users, as there will not be a need for a cloud-based system; therefore, there will not be any digitized, personal data that can be exploited
- Reduced power consumption will allow for the system to be implemented in smaller devices, allowing for new devices/products to be created using this technology

LANL Neuromorphic
Adam O'Brien
Cason Love

FUNCTIONAL SYSTEM REQUIREMENTS

REVISION –1
22 February 2023

FUNCTIONAL SYSTEM REQUIREMENTS
FOR
LANL Neuromorphic

PREPARED BY:

Author Date

APPROVED BY:

Project Leader Date

Prof. Kalafatis Date

T/A Date

Change Record

Rev.	Date	Originator	Approvals	Description
-	2/22/23	Cason Love	Adam O'Brien	Draft Release

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1. Introduction

1.1. Purpose and Scope

The LANL Neuromorphic Circuit will exhibit the advancement in neuromorphic, analog circuits by computing organic tasks, such as voice recognition. This will be advantageous in terms of power required and training time of deep neural networks to replace traditional binary computers. The scope of this project reaches two distinct phases: Build an educational demo that can help build connections to form a market, and then design a satellite control chip to reach a vast, hidden market. Figure 1 displays the integration of subsystems into the full prototype.

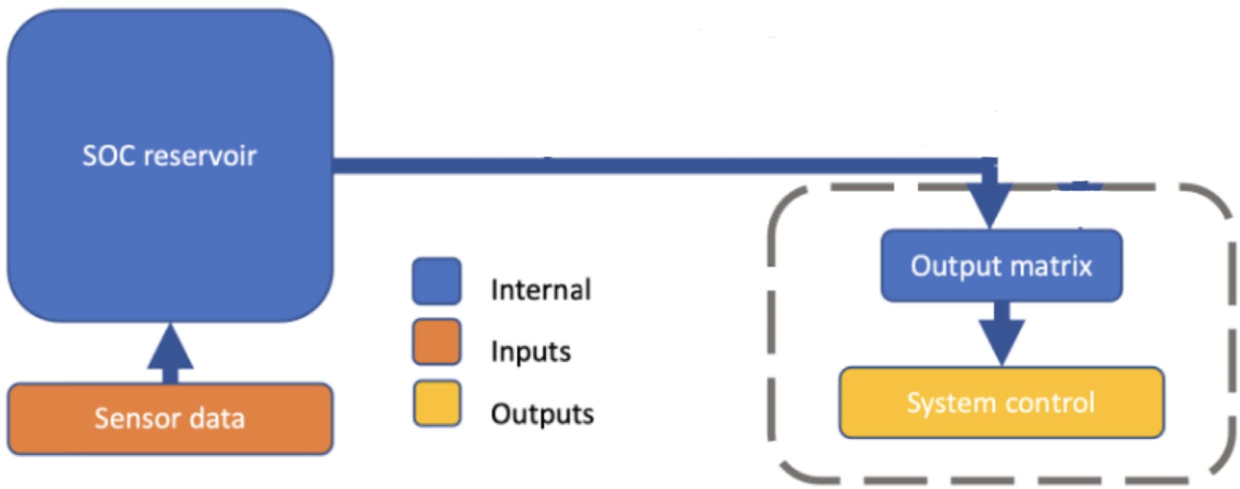

Figure 1. Functional System Diagram of LANL Neuromorphic Circuit

The system should receive power from a 1.5V battery. The microphone will take input from a human voice and will also feature a bandpass filter to solely allow human voice frequencies. The output from the filter will input into the reservoir which will compute whether the phrase is deemed as an activation phrase. The output from the reservoir will feed into the output matrix, which will compute the results from the reservoir and illuminate LEDs to signal the output, activation phrase or not an activation phrase.

1.2. Responsibility and Change Authority

The responsibility for making sure all requirements and specifications are met shall be with Cason Love, the team leader. All changes to the project shall be approved by Adam O’Brien, and Dr. Michael Saccone, the sponsor representing Los Alamos National Labs.

2. Applicable and Reference Documents

2.1. Applicable Documents

The following documents, of the exact issue UA741 and revision shown, form a part of this specification to the extent specified herein:

Document Number	Revision/Release Date	Document Title
SLOS094G	Revision – January 2018	UA741 General-Purpose Operational Amplifiers
U.S.Congress, United States Code: Copyright Office, 17 U.S.C. §§ 201-216. 1958	1958	Title 17.-Copyrights
US Congress, United States. Classification of Patents. June 1898	June 10, 1898	Classification of Patents

2.2. Reference Documents

The following documents are reference documents utilized in the development of this specification. These documents do not form a part of this specification and are not controlled by their reference herein.

Document Number	Revision/Release Date	Document Title
Pickett, Mathew. “Neuristor-based reservoir computing devices.” US20150379395A1. November 2015.	September 2015	Neuristor-based reservoir computing devices
Pino, Robinson. “Neuromorphic Computer.” US8275728B2. November 2009.	November 2009	Neuromorphic Computer

2.3. Order of Precedence

In the event of a conflict between the text of this specification and an applicable document cited herein, the text of this specification takes precedence without any exceptions.

All specifications, standards, exhibits, drawings, or other documents that are invoked as “applicable” in this specification are incorporated as cited. All documents that are referred to within an applicable report are for guidance and information only, except ICDs that have their relevant documents considered to be incorporated as cited.

3. Requirements

In the following section, “LANL Neuromorphic Chip” will solely refer to the entire system for which the proof of concept is being developed in the scope of this project. This includes the microphone, reservoir, and matrix multiplier output of the circuit. The term “microphone” will solely refer to the microphone circuit that will take input from the user. The term “reservoir” will solely refer to the processor of the processor that computes whether the used phrase is an activation phrase. The term “matrix multiplication” will solely refer to the output circuit that displays whether the phrase was an activation phrase.

3.1. System Definition

Provide a brief overview of the project, and then describe some of the main sub-systems of your proposed solution.

The LANL Neuromorphic Chip is a system capable of taking in a phrase from a user, computing whether the phrase was an activation phrase, and displaying the outcome. The system consists of three subsystems: the microphone circuit, reservoir, and matrix multiplication circuit, which are shown in Figure 2.

The microphone circuit subsystem

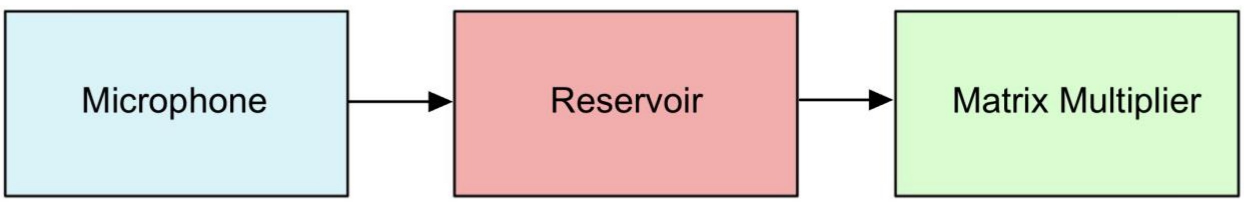

Figure 2. Block Diagram of System

Describe the block diagram, what are the subsystems, how do they interconnect. Someone reading this section should get a general idea of what you are building, why, and how it will solve the problem you are solving.

The microphone circuit will take in user speech through a microphone and amplify the signal for the reservoir. The reservoir subsystem is a physical reservoir that will utilize reservoir computing to map the user input to a certain matrix output. A different matrix output will be given depending on the user input, which will be in the form of four different voltage outputs. These will be fed to the matrix multiplier Circuit. This circuit will perform matrix multiplication on the four voltage outputs and produce two voltage outputs, i.e., a two by one vector. These two outputs will be fed to LEDs, which will signify the absence or presence of the activation phrase.

3.2. Characteristics

3.2.1. Functional / Performance Requirements

3.2.1.1. Activation Phrase Recognition

The LANL Neuromorphic Chip will be able to recognize a specific activation phrase from human speech.

> *Rationale: This is the core system performance requirement.*

3.2.2. Physical Characteristics

3.2.2.1. Mass

N/A

> *Rationale: No required mass specification.*

3.2.2.2. Volume Envelope

The PCB for the system is expected to be 8” x 8” x 1”.

> *Rationale: There is no required volume specification. This is a rough estimation.*

3.2.2.3. Mounting

N/A

3.2.3 Electrical Characteristics

3.2.3.1 Inputs

The LANL Neuromorphic Chip will have voltage supplied by a +1.5V 1A DC battery and user speech as inputs.

> *Rationale: The system will be designed to recognize an activation phrase from the user, and the battery will be used to power all circuits in the system with the help of amplification circuits.*

3.2.3.1.1 Power Consumption

The maximum peak power of the system shall not exceed 5 W.

> *Rationale: This is one of the appeals of neuromorphic computing, keeping the system low power.*

3.2.3.1.2 Input Voltage Level

The input voltage for the LANL Neuromorphic Chip shall be +1.5 VDC.

> *Rationale: A 1.5V 1A DC battery will be used to power the chip.*

3.2.3.1.3 Input Current Level

The input current for the LANL Neuromorphic Chip shall be 1A.

Rationale: A 1.5V 1A DC battery will be used to power the chip

3.2.3.2 Outputs

3.2.3.2.1 LED Output

The LANL Neuromorphic Chip will have two LED outputs, each corresponding to the absence or presence of the activation phrase.

Rationale: This will identify whether the system can differentiate between the activation phrase and other human speech.

3.2.4 Environmental Requirements

The LANL Neuromorphic Chip will be designed to be used at standard room conditions, low humidity.

Rationale: The LANL Neuromorphic Chip shall operate safely within another system that should handle any external/environmental factors

3.2.5 Failure Propagation

If there is to be any failure on the PCB, there will be an external test bench that can be used to help find and resolve the issue. Due to this being a research prototype, there is no current plan to implement failure protection on the final PCB.

4. Support Requirements

Documentation and design files pertaining to the LANL Neuromorphic Chip will be provided for support. Email addresses of team members will also be provided as additional support.

Appendix A: Acronyms and Abbreviations

A	Amp
LANL	Los Alamos National Lab
LED	Light-emitting Diode
PCB	Printed Circuit Board
V	Volt
W	Watt

LANL Neuromorphic
Adam O’Brien
Cason Love

INTERFACE CONTROL DOCUMENT

REVISION – 1
22 February 2023

INTERFACE CONTROL DOCUMENT
FOR
LANL Neuromorphic

PREPARED BY:

____
Author Date

APPROVED BY:

____
Project Leader Date

____
John Lusher II, P.E. Date

____
T/A Date

Change Record

Rev.	Date	Originator	Approvals	Description
-	2/22/23	Cason Love	Adam O’Brien	Draft Release

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1. Overview

Further detail on how the subsystems in the Concept of Operations and the Functional System Requests will be developed is provided in the Interface Control Document (ICD) for the entire LANL Neuromorphic Chip. The ICD will include physical descriptions of the individual components as well as information about how each circuit is designed, and its power ratings. To fulfill the objectives and specifications outlined in the FSR and ConOps documents, the document will also provide how the subsystems will interface with one another.

2. References and Definitions

2.1. References

MIL-STD-810F
Environmental Engineering Considerations and Laboratories Tests
1 Jan 2000
Change Notice 2
30 Aug 2002

Pickett, Mathew. "Neuristor-based reservoir computing devices." US20150379395A1.
November 2015.

Pino, Robinson. "Neuromorphic Computer." US8275728B2.
November 2009.

2.2. Definitions

W	Watt
A	Amp
Hz	Hertz
V	Volts
DC	Direct Current

3. Physical Interface

3.1. Weight

N/A

3.2. Dimensions

The PCB for the system is expected to be 8” x 8” x 1”.

3.3. Mounting Locations

N/A

4. Thermal Interface

The LANL Neuromorphic Chip system will be low power, with a maximum peak power no higher than 5 W. Therefore, a thermal interface will not be necessary for this system.

5. Electrical Interface

5.1. Primary Input Power

The system will be powered by a 1.5V 1A DC battery.

5.2. Polarity Reversal

N/A

5.3. Signal Interfaces

5.3.1 Microphone Signal

Human speech is used as input to the microphone, which will be filtered and amplified before being sent to the reservoir subsystem.

5.3.2 Reservoir Signal

The reservoir subsystem will produce four voltage outputs that will be fed to the matrix multiplication subsystem.

5.4. Audio Interfaces

An electric microphone will take speech from a user and input into the filter circuit, leaving signals from 80 Hz to 255Hz only.

6. Communications / Device Interface Protocols

6.1. Wireless Communications (WiFi)
N/A

6.2. Host Device
N/A

6.3. Video Interface
N/A

6.4. Device Peripheral Interface
N/A

Appendix B: Definition of Terms

Microphone Circuit	The circuit that will collect the signal from the user input.
Reservoir	The circuit that will map user input to a certain matrix output in the form of four voltage outputs.
Frequency Filter	The circuit that will filter out certain frequencies only leaving those of human voices.
Matrix Multiplication Circuit	The circuit that will compute matrix multiplication on the Reservoir outputs to determine the presence or absence of the activation phrase.

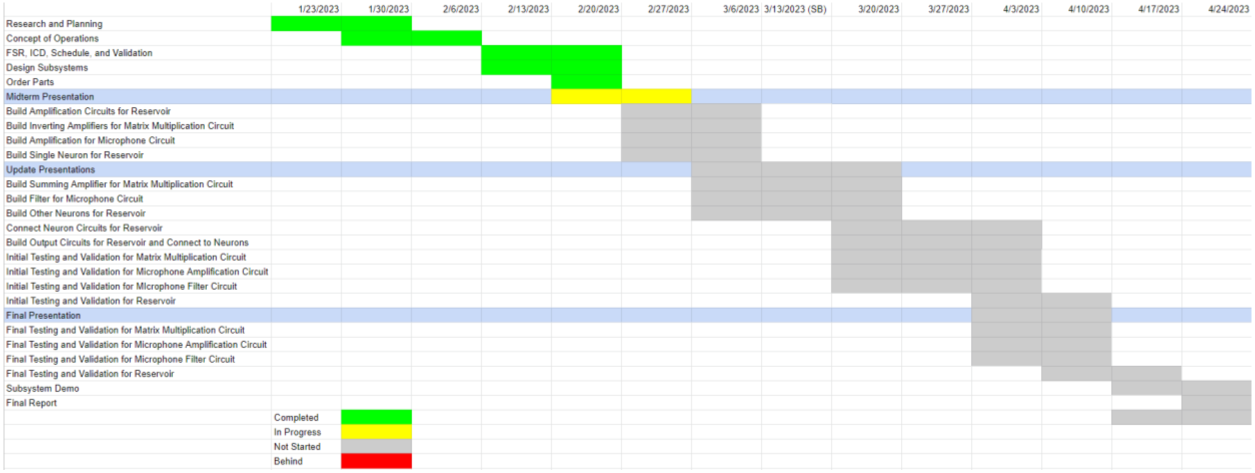
LANL Neuromorphic

Adam O'Brien
Cason Love

SCHEDULE

Work	End Date	Owner	Status	Date Completed
Concept of Operations	2/10/23	All	Completed	2/10/23
FSR, ICD, Schedule, and Validation	2/22/23	All	Completed	2/22/23
Design Subsystems	2/22/23	All	Completed	2/22/23
Order Parts	2/24/23	All	In Progress	
Midterm Presentation	3/1/23	All	In Progress	3/1/23
Build Amplification Circuits 1 – 6 for Reservoir	3/7/23	Cason	Not Started	
Build Amplification Circuits 7 – 9 for Reservoir	3/7/23	Adam	Not Started	
Build Inverting Amplifiers for MM Circuit	3/7/23	Adam	Not Started	
Build Amplification for Microphone Circuit	3/10/23	Cason	Not Started	
Build Filter for Microphone Circuit	3/10/23	Cason	Not Started	
Build Single Neuron for Reservoir	3/10/23	Adam	Not Started	
Update Presentations	3/22/23	All	Not Started	
Build Summing Amplifier for MM Circuit	3/24/23	Adam	Not Started	
Build Filter for Microphone Circuit	3/24/23	Cason	Not Started	
Build Other Neurons for Reservoir	3/24/23	All	Not Started	
Connect Neuron Circuits for Reservoir	3/31/23	All	Not Started	
Initial Testing and Validation for MM Circuit	4/7/2023	Adam	Not Started	
Initial Testing and Validation for Microphone Amplification Circuit	4/7/2023	Cason	Not Started	
Initial Testing and Validation for Microphone Filter Circuit	4/7/2023	Cason	Not Started	
Initial Testing and Validation for Reservoir	4/10/2023	All	Not Started	
Final Presentation	4/12/23	All	Not Started	
Final Testing and Validation for MM Circuit	4/14/2023	Adam	Not Started	
Final Testing and Validation for Microphone Amplification Circuit	4/14/2023	Cason	Not Started	
Final Testing and Validation for Microphone Filter Circuit	4/14/2023	Cason	Not Started	
Final Testing and Validation for Reservoir	4/23/2023	All	Not Started	
Subsystem Demo	4/25/23	All	Not Started	

Final Report	4/29/23	All	Not Started	



LANL Neuromorphic

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VALIDATION PLAN

Task	Result	Owner
Microphone Circuit outputs 20 V (Breadboard)		Cason
Microphone Circuit outputs 20 V (Perfboard)		Cason
Bandpass circuit filters frequencies outside range of 55 Hz - 260 Hz (Breadboard)		Cason
Bandpass circuit filters frequencies outside range of 55 Hz - 260 Hz (Perfboard)		Cason
Inverting Amplifier multiplies voltage as expected (gain value is still TBD) - (Breadboard)		Adam
Inverting Amplifier multiplies voltage as expected (gain value is still TBD) - (Perfboard)		Adam
Summing Amplifier produces correct sum of voltages (Breadboard)		Adam
Summing Amplifier produces correct sum of voltages (Perfboard)		Adam
Single Neuron Exhibits Nonharmonic Behavior		Adam
Single Neuron Fourier Transform Resembles 1/Frequency Behavior		Adam
Amplification Circuit 1 Outputs ~20.65 V		Cason
Amplification Circuit 2 Outputs ~40.14 V		Cason
Amplification Circuit 3 Outputs ~20.64 V		Cason
Amplification Circuit 4 Outputs ~20.15 V		Cason
Amplification Circuit 5 Outputs ~40.20 V		Cason
Amplification Circuit 6 Outputs ~20.63 V		Cason
Amplification Circuit 7 Outputs ~40.27 V		Adam
Amplification Circuit 8 Outputs ~20.48 V		Adam
Amplification Circuit 9 Outputs ~40.17 V		Adam
Other Neurons Exhibit Nonharmonic Behavior		All
Other Neurons Fourier Transform Resemble 1/Frequency Behavior		All
Neurons Do NOT Synchronize when connected		All
Voltage Outputs 1-2 Resemble Linear Behavior in LANL Simulation		Adam
Voltage Outputs 3-4 Resemble Linear Behavior in LANL Simulation		Cason