1. Description

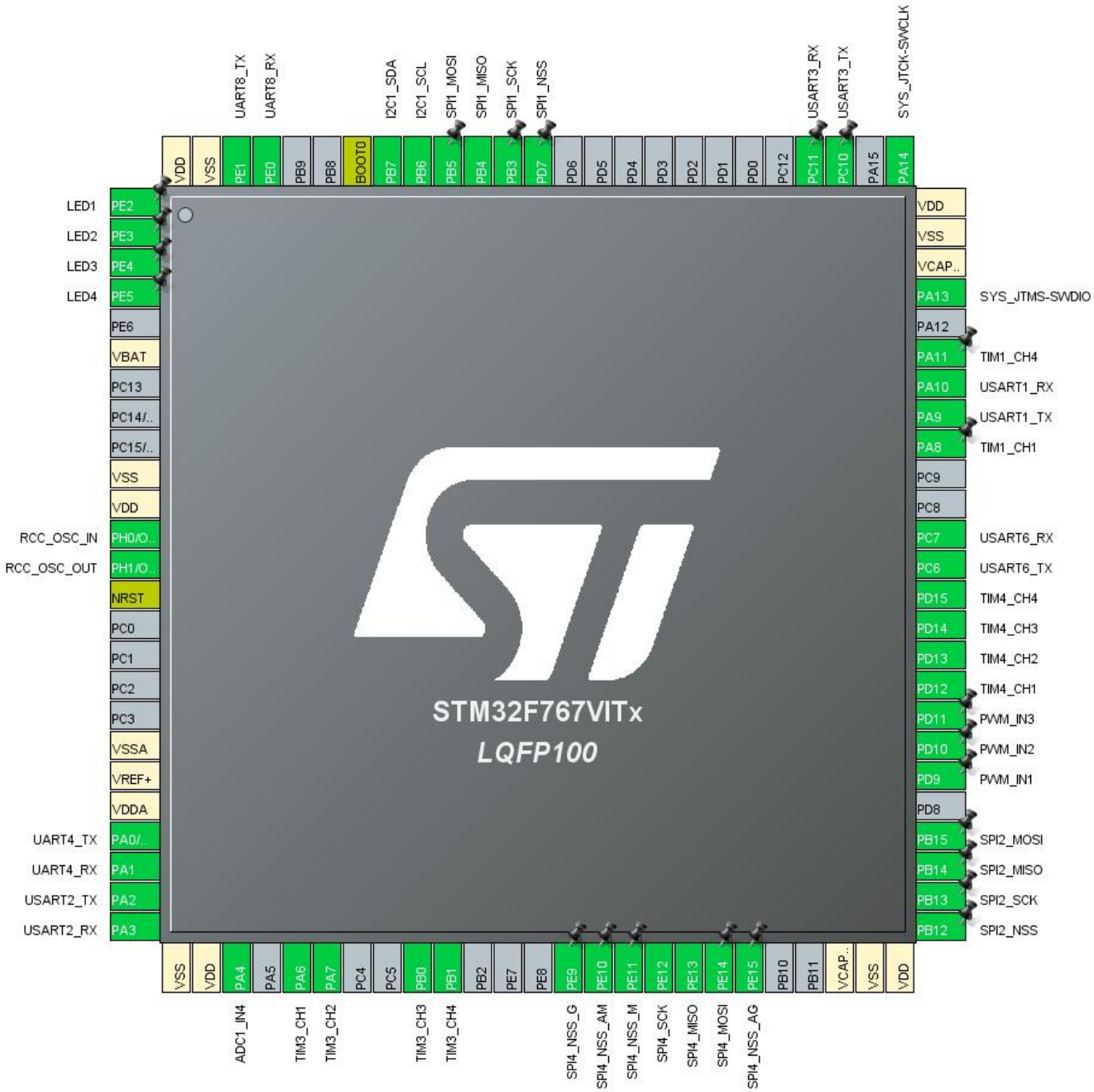
1.1. Project

Project Name	FlyControl
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	10/05/2019

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767VITx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



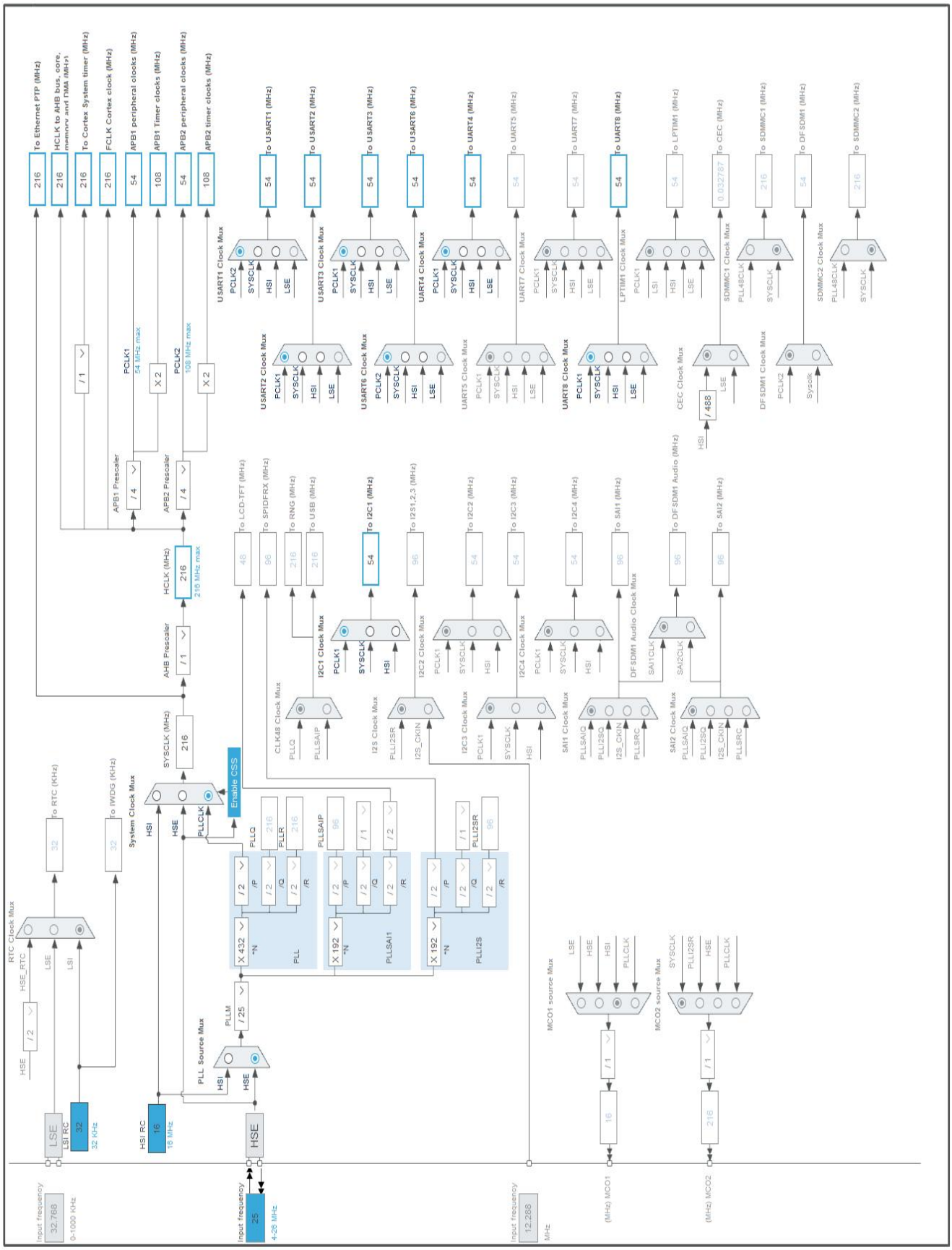
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	LED1
2	PE3 *	I/O	GPIO_Output	LED2
3	PE4 *	I/O	GPIO_Output	LED3
4	PE5 *	I/O	GPIO_Output	LED4
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0/OSC_IN	I/O	RCC_OSC_IN	
13	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
20	VREF+	Power		
21	VDDA	Power		
22	PA0/WKUP	I/O	UART4_TX	
23	PA1	I/O	UART4_RX	
24	PA2	I/O	USART2_TX	
25	PA3	I/O	USART2_RX	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	ADC1_IN4	
30	PA6	I/O	TIM3_CH1	
31	PA7	I/O	TIM3_CH2	
34	PB0	I/O	TIM3_CH3	
35	PB1	I/O	TIM3_CH4	
39	PE9 *	I/O	GPIO_Output	SPI4_NSS_G
40	PE10 *	I/O	GPIO_Output	SPI4_NSS_AM
41	PE11 *	I/O	GPIO_Output	SPI4_NSS_M
42	PE12	I/O	SPI4_SCK	
43	PE13	I/O	SPI4_MISO	
44	PE14	I/O	SPI4_MOSI	
45	PE15 *	I/O	GPIO_Output	SPI4_NSS_AG
48	VCAP_1	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	SPI2_NSS
52	PB13	I/O	SPI2_SCK	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	SPI2_MOSI	
56	PD9	I/O	GPIO_EXTI9	PWM_IN1
57	PD10	I/O	GPIO_EXTI10	PWM_IN2
58	PD11	I/O	GPIO_EXTI11	PWM_IN3
59	PD12	I/O	TIM4_CH1	
60	PD13	I/O	TIM4_CH2	
61	PD14	I/O	TIM4_CH3	
62	PD15	I/O	TIM4_CH4	
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
67	PA8	I/O	TIM1_CH1	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	TIM1_CH4	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	USART3_TX	
79	PC11	I/O	USART3_RX	
88	PD7 *	I/O	GPIO_Output	SPI1_NSS
89	PB3	I/O	SPI1_SCK	
90	PB4	I/O	SPI1_MISO	
91	PB5	I/O	SPI1_MOSI	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
97	PE0	I/O	UART8_RX	
98	PE1	I/O	UART8_TX	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	FlyControl
Project Folder	C:\Users\Ducted Fan\Desktop\ESKF.Note.code\code_test\FlyControl
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767VITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN4

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CORTEX_M7

7.2.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCLERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.3. GFXSIMULATOR

7.3.1. Simulator Graphic:

7.4. I2C1

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.6. SPI1

Mode: Full-Duplex Master

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**13.5 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.7. SPI2

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**13.5 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled

NSS Signal Type	Software

7.8. SPI4

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**6.75 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.9. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.10. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel4: PWM Generation CH4

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0

auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.11. TIM2

Clock Source : Internal Clock

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFFFFFF ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.12. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1

Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.13. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1

Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.14. TIM5

mode: Clock Source

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.15. UART4

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.16. UART8

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.17. USART1

Mode: Asynchronous

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.18. USART2

Mode: Asynchronous

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. USART3

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.20. USART6

Mode: Asynchronous

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.21. FREERTOS

Interface: CMSIS_V1

7.21.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled

QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	**Enabled ***
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.21.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled

vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI4	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE13	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PA0/WKUP	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI4_NSS_G
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI4_NSS_AM
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI4_NSS_M

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI4_NSS_AG
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_NSS
	PD9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	PWM_IN1
	PD10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	PWM_IN2
	PD11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	PWM_IN3
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_NSS

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
I2C1_RX	DMA1_Stream5	Peripheral To Memory	Low
I2C1_TX	DMA1_Stream7	Memory To Peripheral	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low
USART6_TX	DMA2_Stream6	Memory To Peripheral	Low
USART3_TX	DMA1_Stream3	Memory To Peripheral	Low
UART8_RX	DMA1_Stream6	Peripheral To Memory	Low
UART4_RX	DMA1_Stream2	Peripheral To Memory	Low
UART4_TX	DMA1_Stream4	Memory To Peripheral	Low
UART8_TX	DMA1_Stream0	Memory To Peripheral	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

I2C1_RX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable

Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_TX: DMA2_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART8_RX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_RX: DMA1_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART8_TX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream2 global interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream4 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
EXTI line[9:5] interrupts	true	5	0
USART1 global interrupt	true	5	0
USART2 global interrupt	true	5	0
USART3 global interrupt	true	5	0
EXTI line[15:10] interrupts	true	5	0
DMA1 stream7 global interrupt	true	5	0
TIM5 global interrupt	true	5	0
UART4 global interrupt	true	5	0
TIM7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream1 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
DMA2 stream6 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
USART6 global interrupt	true	5	0
UART8 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		

*** User modified value**

9. Software Pack Report