S.No	INSTRUCTION	OPERATION	OPCODE	Control Bits (Execute)
A) I	Flags and Machine Control Instructi	ons		
1.	CLR	[<rn>](n = 0, 1,7) \leftarrow 0 (all registers cleared)</rn>	00000000	WA _{RN}
2.	CLF	fl ← 0	00000011	CL _{FR}
В) І	Data Transfer Instructions			
3.	LDI <od></od>	[A] ← <od></od>	00000100	Ror, Wa
4.	STI	[((A]	00000101	R _A , W _{OR}
C) I	Logical Instructions			
5.	RTL <od></od>	Rotate [A] left by <od> bits</od>	00000110	WA
6.	RTR <od></od>	Rotate [A] Right by <od> bits</od>	00000111	WA
7.	CPI <od></od>	Compare [A] with <od></od>	00001000	WA
8.	ANI <od></od>	[A]← [A] & <od></od>	00001001	WA
9.	ORI <od></od>	[A]← [A] <od></od>	00001010	WA
10.	XRI <od></od>	[A]← [A] ^ <od></od>	00001 011	W _A
11.	CMA	[A] ← ~[A]	00001 100	WA
D) /	Arithmetic Instructions			
12.	ADI <od></od>	[A]←[A] + <od> with carry</od>	00001101	WA
13.	SBI <od></od>	[A]←[A]- <od> with borrow</od>	00001110	WA
E) I	Branch Control Instructions			
14.	JMP <ad></ad>	PC ← <ad></ad>	00010000	$I2_{PC}$, I_{SP} , R_{PC} , WR_S , RD_{AB} , W_{PC}
15.	JNC <ad></ad>	If Carry fl = 0, PC ← <ad></ad>	00010001	I2 _{PC} , I _{SP} , R _{PC} , WRs , RD _{AB} , W _{PC}
16.	JNZ <ad></ad>	If zero fl = 0, PC ← <ad></ad>	00010010	I2 _{PC} , I _{SP} , R _{PC} , WRs , RD _{AB} , W _{PC}
17.	JNS <ad></ad>	If sign fl = 0, PC ← <ad></ad>	00010011	I2 _{PC} , I _{SP} , R _{PC} , WRs , RD _{AB} , W _{PC}
18.	JC <ad></ad>	If Carry fl= 1, PC ← <ad></ad>	00010100	I2 _{PC} , I _{SP} , R _{PC} , WR _S , RD _{AB} , W _{PC}

19.	JZ <ad></ad>	If zero fl = 1, PC ← <ad></ad>	00010101	I2 _{PC} , I _{SP} , R _{PC} , WRs,
				RDAB, WPC
20.	JS <ad></ad>	If sign fl = 1, PC ← <ad></ad>	00010110	12 _{PC} , I _{SP} , R _{PC} , WR _S ,
				RD _{AB} , W _{PC}
21.	RET	PC ← <stack></stack>	00011000	RDs, W _{PC} , D _{SP}
		One Register Instructions		
A)	Logical Instructions			
22.	CPR <rn></rn>	if [A] < [<rn>]: carry flag is</rn>	01 000 <rn></rn>	R _{RN}
		set.		
		if [A] = [<rn>]: Sign flag is</rn>		
		set if [A] > [<rn>]: carry</rn>		
		and Sign flags are reset		
23.	AND <rn></rn>	[<rn>] ← [<rn>] & [A]</rn></rn>	01 001 <rn></rn>	R _{RN} , W _{RN}
24.	OR <rn></rn>	[<rn>] ← [<rn>] [A]</rn></rn>	01 010 <rn></rn>	R _{RN} , W _{RN}
25.	XOR <rn></rn>	[<rn>] ← [<rn>] ^ [A]</rn></rn>	01 011 <rn></rn>	R _{RN} , W _{RN}
26.	CMR <rn></rn>	[<rn>] ← ~[<rn>]</rn></rn>	01 100 <rn></rn>	R _{RN} , W _{RN}
В)	Arithmetic Instructions			
27.	ADIR <rn> <od></od></rn>	[<rn>] ← [<rn>] + <od></od></rn></rn>	01 101 <rn></rn>	R _{RN} , W _{RN}
28.	SBIR <rn> <od></od></rn>	[<rn>] ← [<rn>] - <od></od></rn></rn>	01 110 <rn></rn>	R _{RN} , W _{RN}
29.	ADD <rn></rn>	[<rn>] ← [<rn>] + [A]</rn></rn>	01 111 <rn></rn>	R _{RN} , W _{RN}
29.	ADD (III)	[<m>) ← [<m>) + [A]</m></m>	U IIII<	TRN, VVRN
C)	Data Transfer Instructions	f 1	10000 (77)	D W
30.	MVI <rn> <od></od></rn>	[<rn>] ← <od></od></rn>	10000 <rn></rn>	Ror, W _{RN}
31.	MOVD <rn></rn>	[<rn>] ← [A]</rn>	10001 <rn></rn>	R _A , W _{RN}
32.	MOVS <rn></rn>	[A] ←[<rn>]</rn>	10010 <rn></rn>	R _{RN} , W _A
		Two Register Instructions	1	
33.	STAR <rnp></rnp>	[[<rnp>]] ← [A]</rnp>	110 <rnp></rnp>	R _{RP} , A _{AR} , R _A , WR
34.	LDAR <rnp></rnp>	[A] ← [[<rnp>]]</rnp>	111 <rnp></rnp>	R _{RP} , A _{AR} , RD, W _A

Table : Instruction Set