

core 1

core 2

⋮

core  $n$

memoria

```
graph LR; C1[core 1] --- M[memoria]; C2[core 2] --- M; Dots[⋮]; Cn[core n] --- M;
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The diagram illustrates a system architecture where multiple processing units, labeled 'core 1', 'core 2', and 'core n', are connected to a single, shared memory component labeled 'memoria'. The connections are shown as lines originating from the right side of each core box and terminating at the left side of the vertical memory box. A vertical ellipsis between 'core 2' and 'core n' indicates that there are more than two cores in the system.