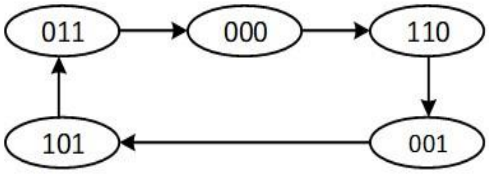
Proiect

Circuite integrate digitale

-Pop Catalin-Cornel-



r	clk	Action
0	x	Reset
1	↑	$Q^+ = D$
otherwise		Wait

Implementare:

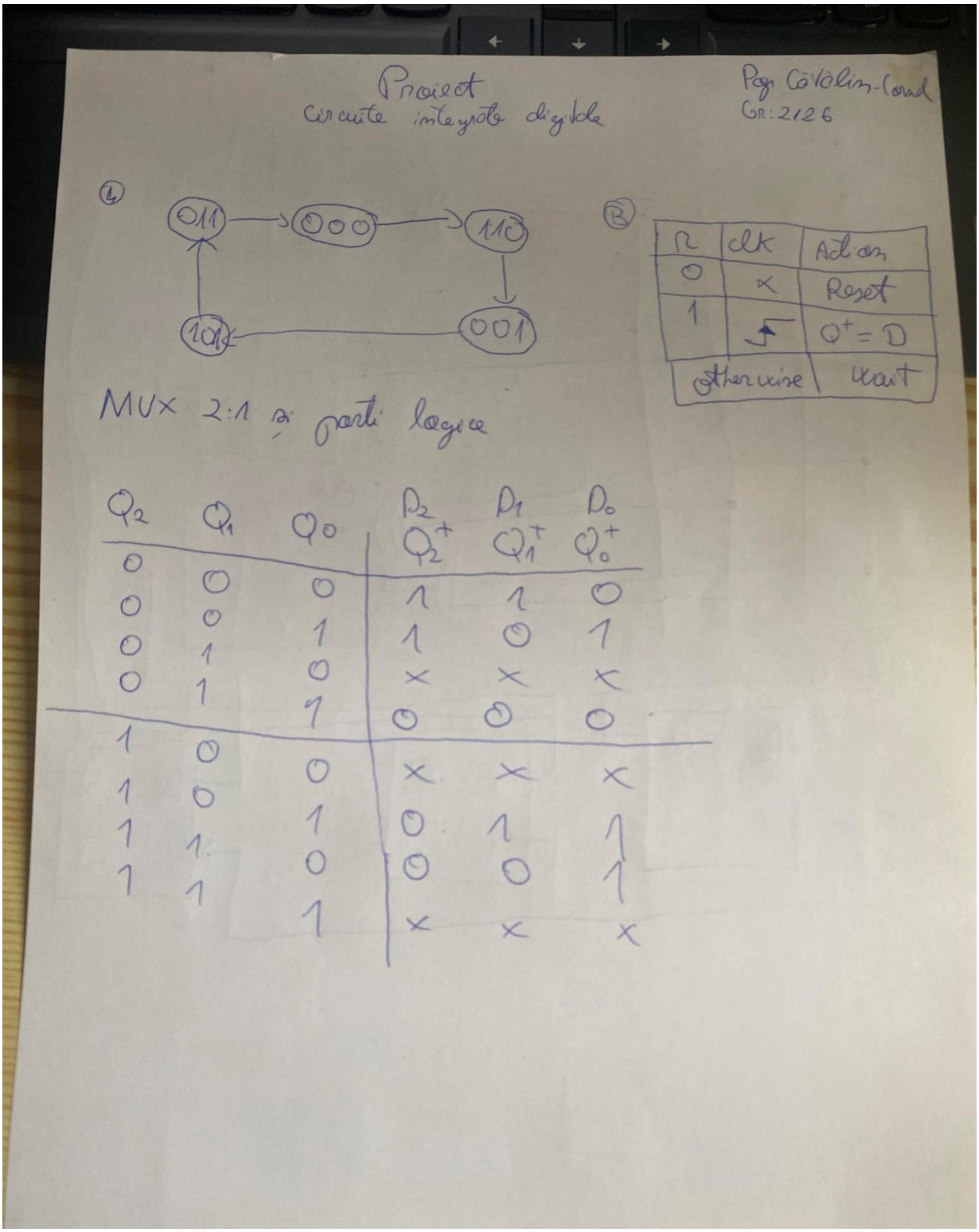
-MUX 2:1 cu Porti logice

Instructiuni implementare MUX:

-IF…ELSE

Q2	Q1	Q0	D2	D1	D0
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	x	x	x
0	1	1	0	0	0
1	0	0	x	x	x
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	x	x	x

1.Rezolvarea circuitului pe foaie



Proiect
Circuite integrate digitale

Pop Cătălin-Ionel
Gr: 2126

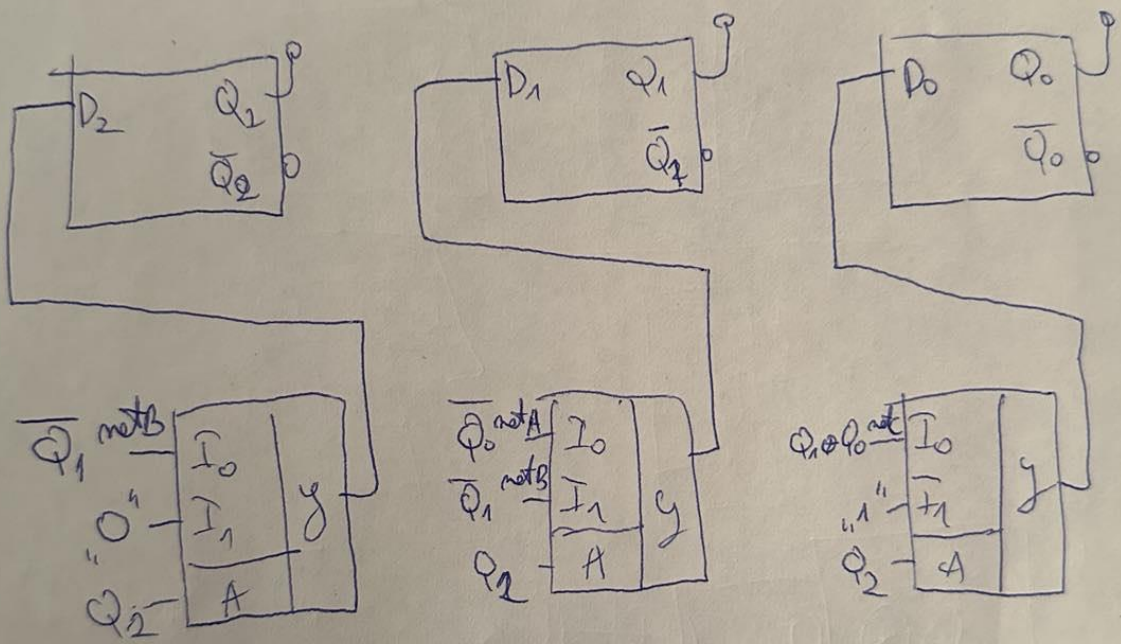
a)

b)

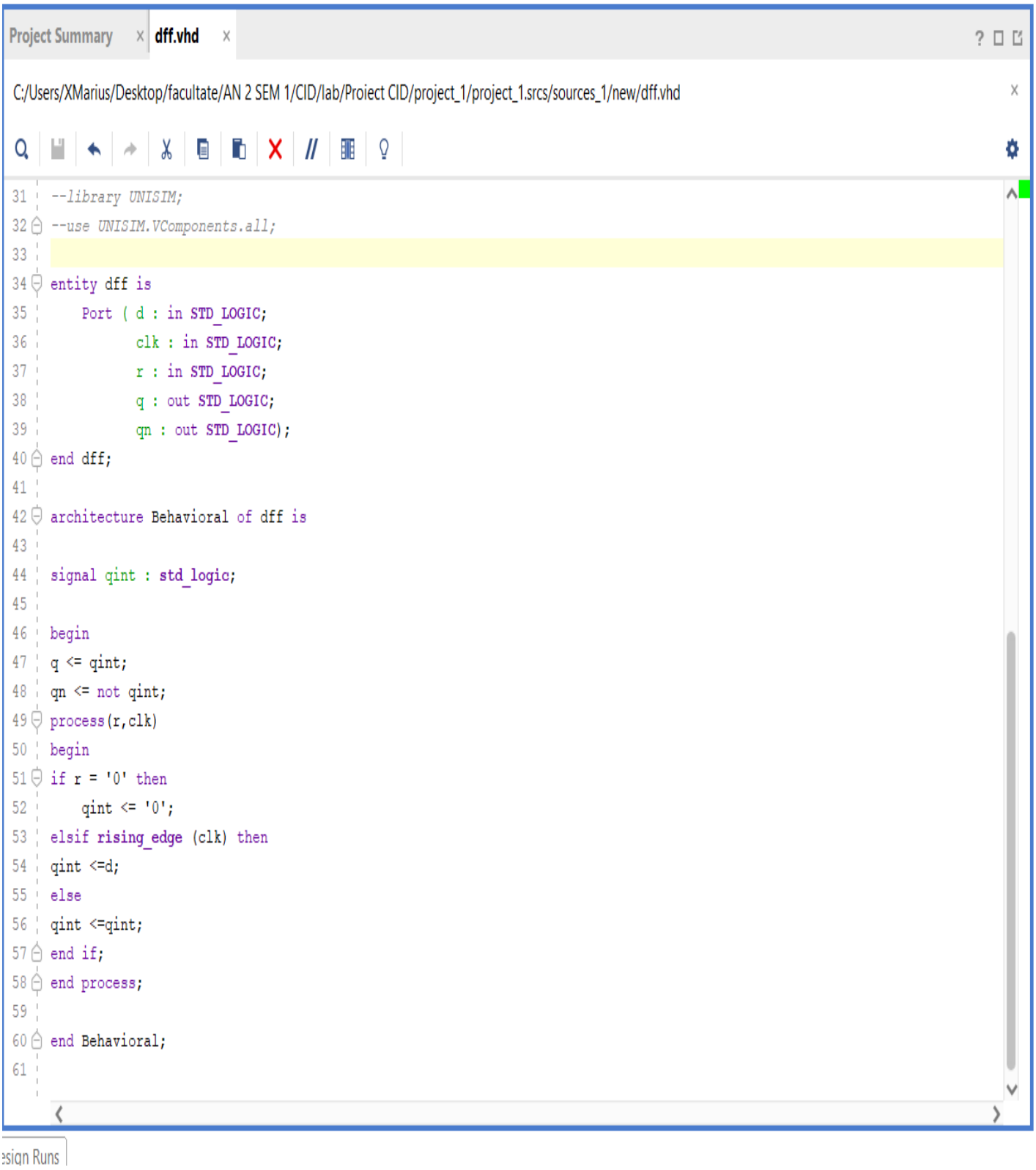
R	clk	Action
0	x	Reset
1	↓	$Q^+ = D$
otherwise		wait

MUX 2:1 și porți logice

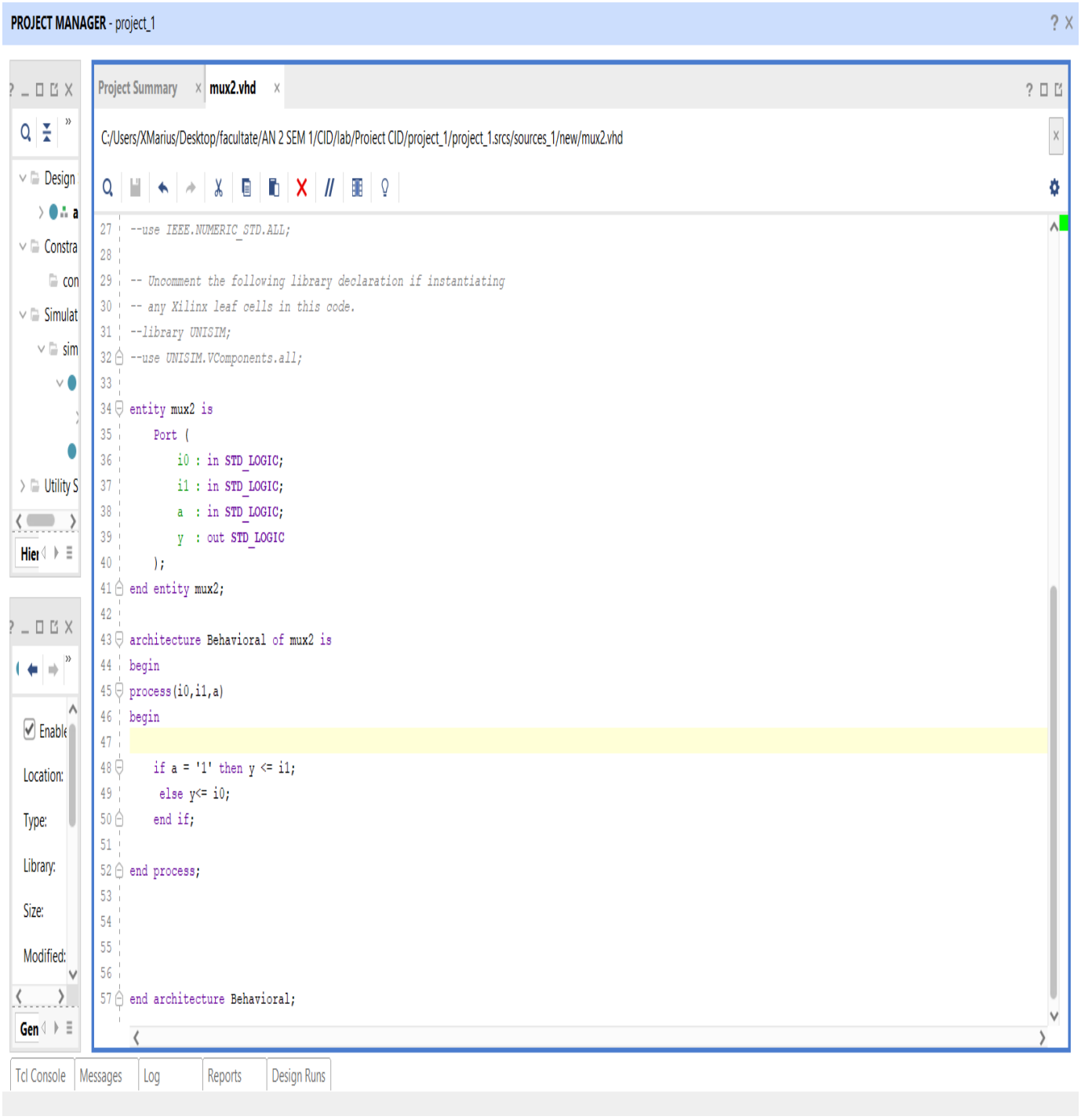
Q_2	Q_1	Q_0	D_2 / Q_2^+	D_1 / Q_1^+	D_0 / Q_0^+
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	x	x	x
0	1	1	0	0	0
1	0	0	x	x	x
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	x	x	x


D2
Q2
Q̄2
D1
Q1
Q̄1
D0
Q0
Q̄0
Q̄1 notB
"0"
Q2
I0
I1
A
y
Q̄0 notA
Q̄1 notB
Q2
Q1⊕Q0 not
"1"
Q2

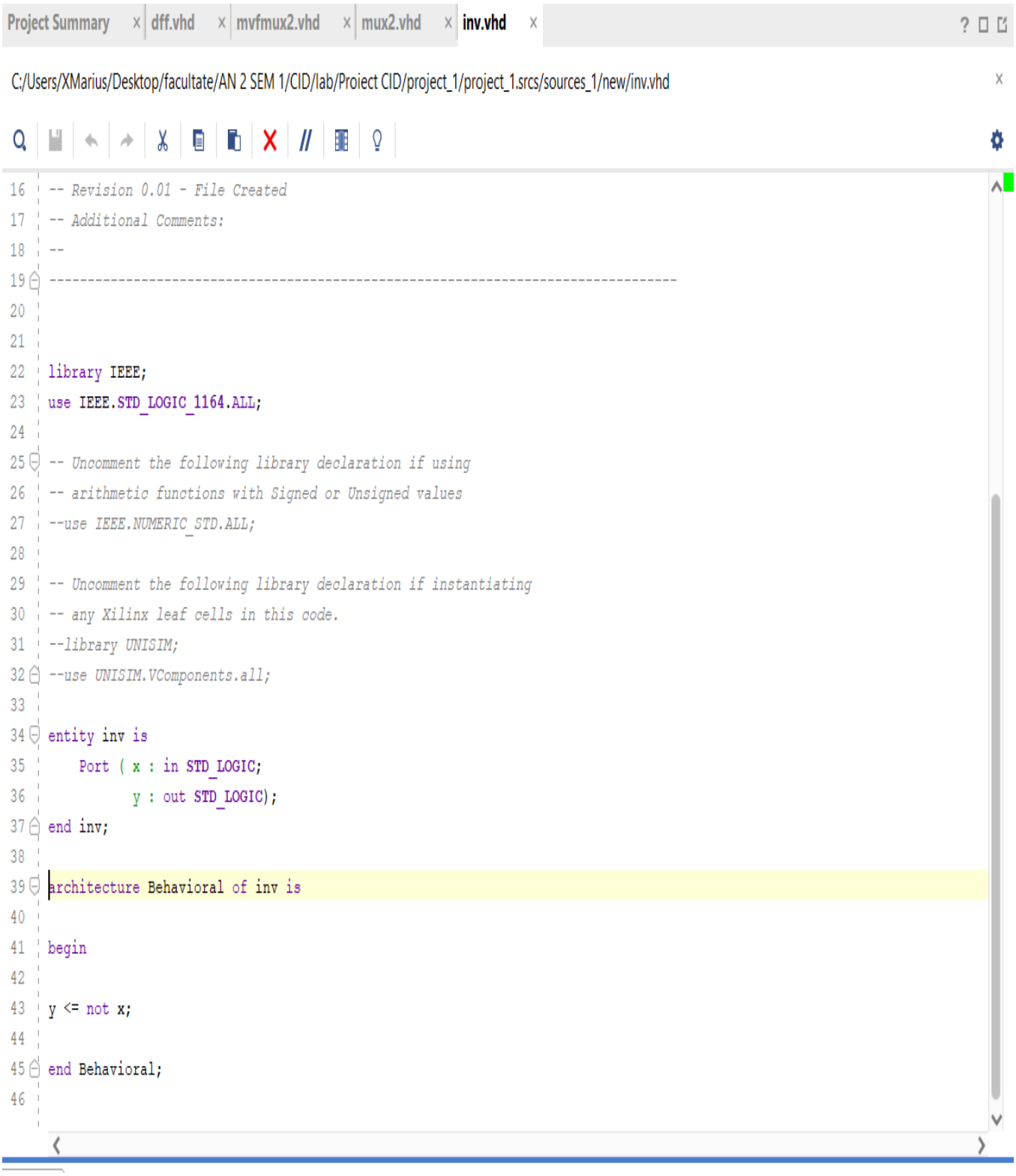
2.Implementarea sursei de design a Bistabilului D



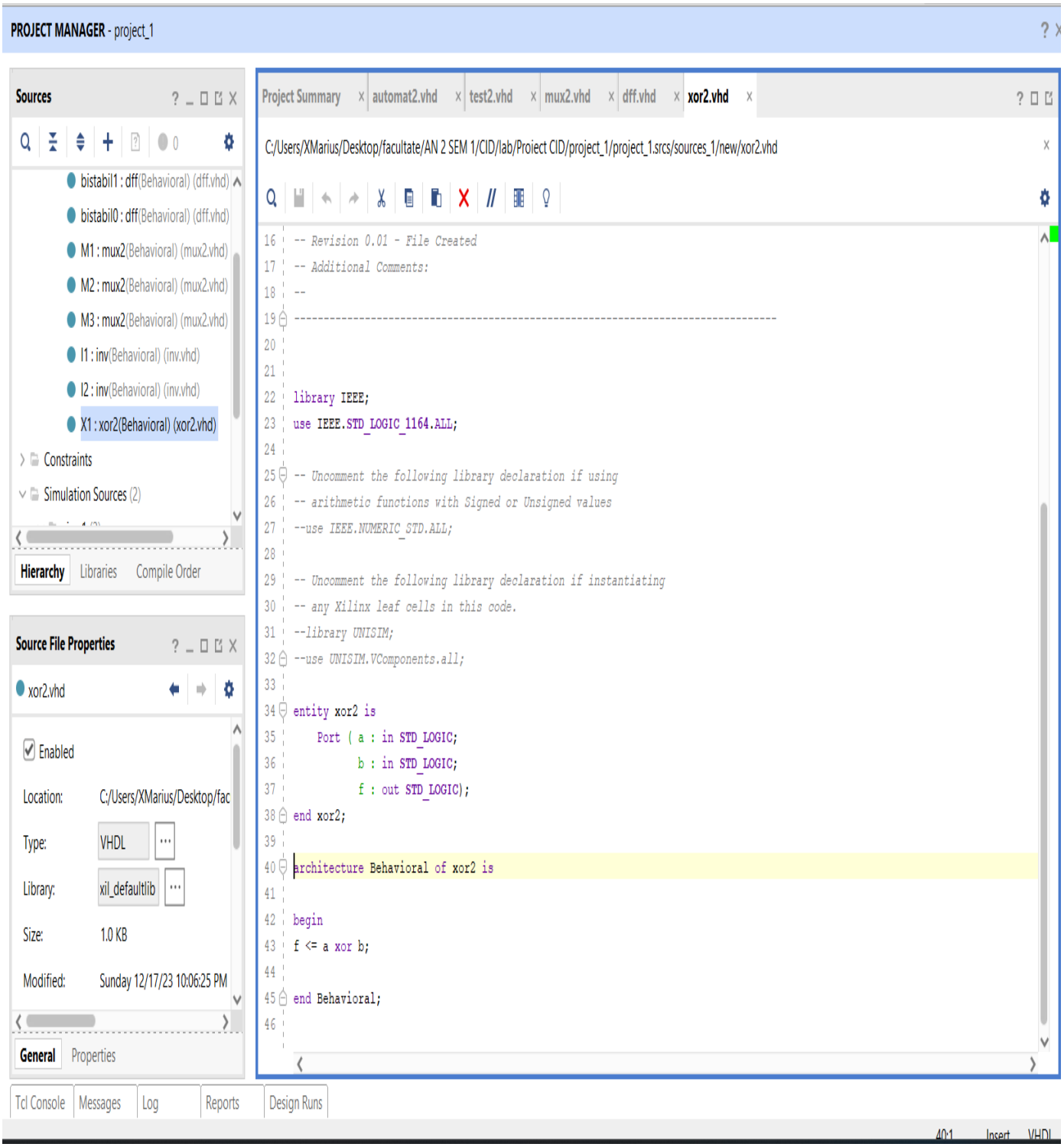
3.Implementarea sursei de design MUX 2:1



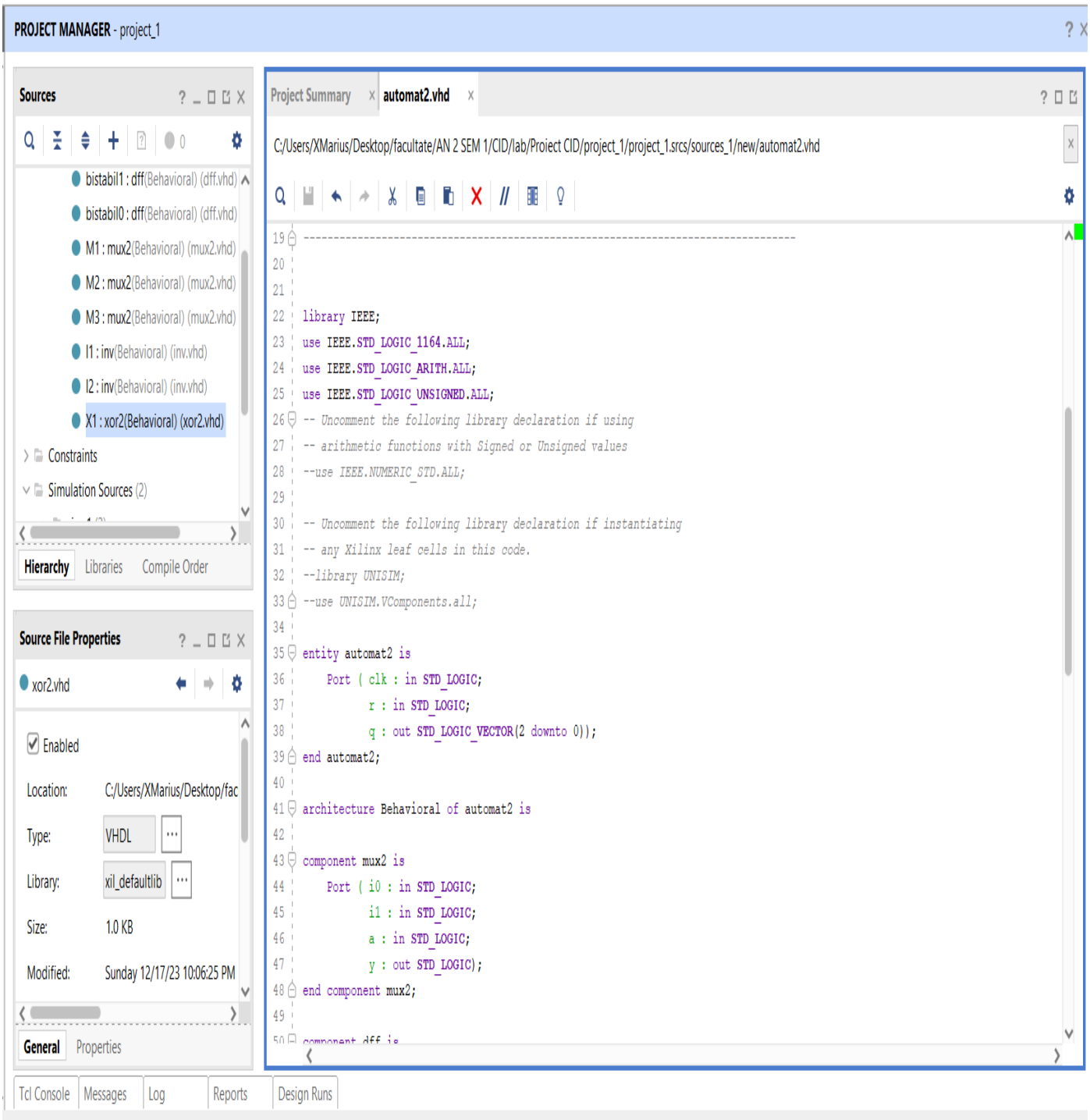
4.Implementarea sursei de design a inversorului

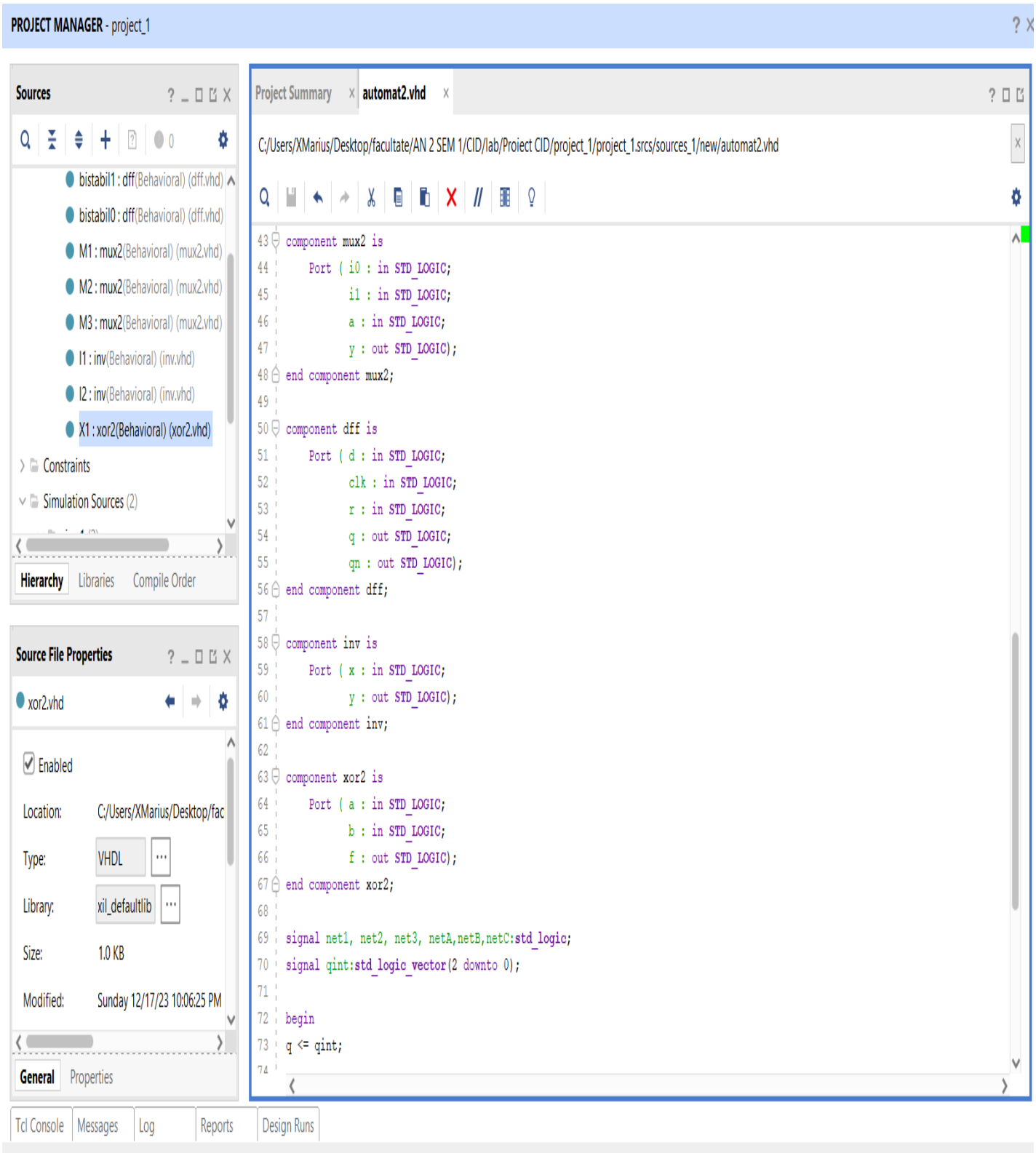


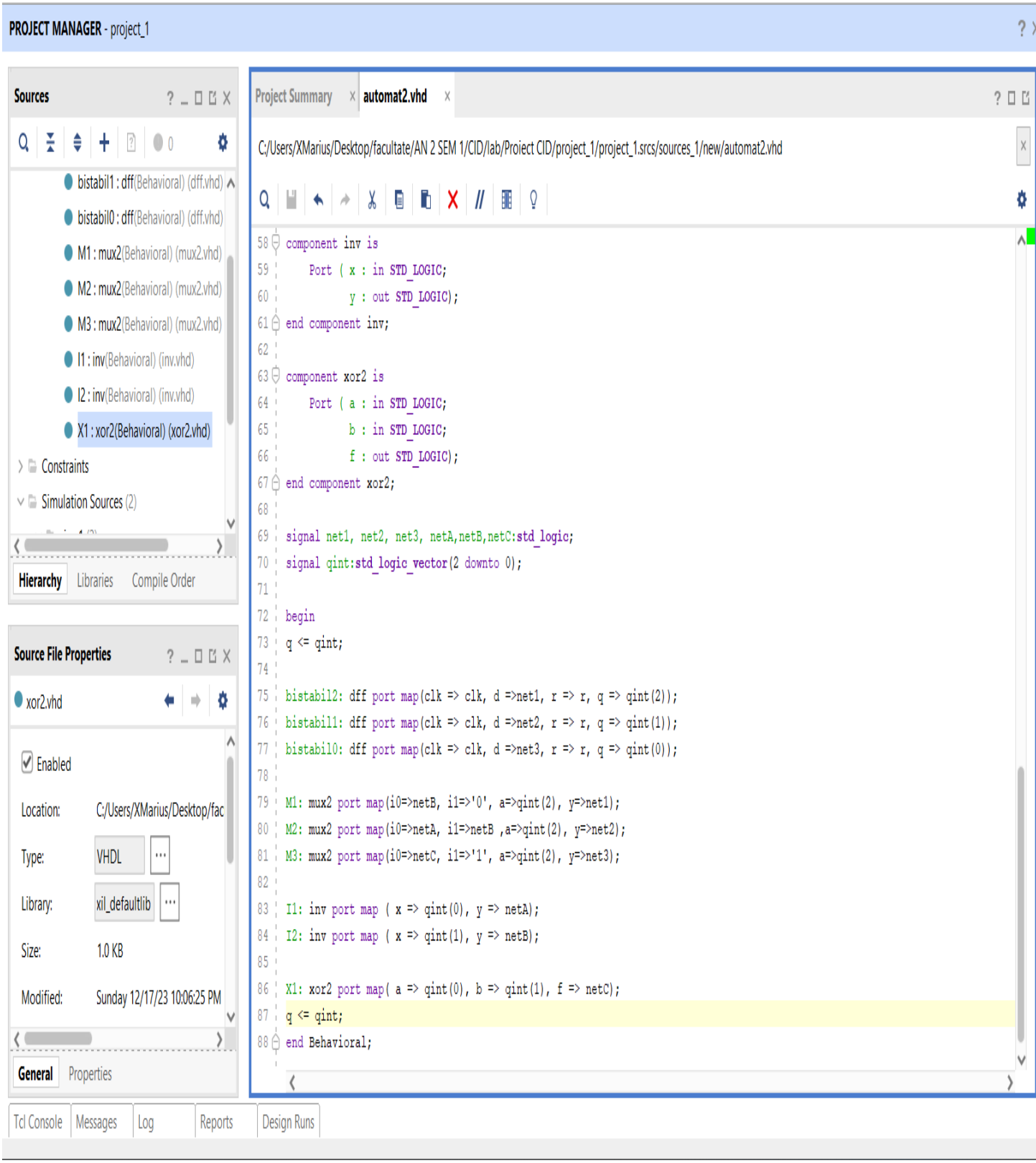
5.Implementarea sursei de design a portii logice xor.



6.Implementarea automatului




PROJECT MANAGER - project_1
Sources
bistabil1 : dff(Behavioral) (dff.vhd)
bistabil0 : dff(Behavioral) (dff.vhd)
M1 : mux2(Behavioral) (mux2.vhd)
M2 : mux2(Behavioral) (mux2.vhd)
M3 : mux2(Behavioral) (mux2.vhd)
I1 : inv(Behavioral) (inv.vhd)
I2 : inv(Behavioral) (inv.vhd)
X1 : xor2(Behavioral) (xor2.vhd)
Constraints
Simulation Sources (2)
Hierarchy
Libraries
Compile Order
Source File Properties
xor2.vhd
Enabled
Location: C:/Users/XMarius/Desktop/fac
Type: VHDL
Library: xil_defaultlib
Size: 1.0 KB
Modified: Sunday 12/17/23 10:06:25 PM
General
Properties
Project Summary
automat2.vhd
C:/Users/XMarius/Desktop/facultate/AN 2 SEM 1/CID/lab/Proiect CID/project_1/project_1.srcs/sources_1/new/automat2.vhd
43 component mux2 is
44 Port (i0 : in STD_LOGIC;
45 i1 : in STD_LOGIC;
46 a : in STD_LOGIC;
47 y : out STD_LOGIC);
48 end component mux2;
49
50 component dff is
51 Port (d : in STD_LOGIC;
52 clk : in STD_LOGIC;
53 r : in STD_LOGIC;
54 q : out STD_LOGIC;
55 qn : out STD_LOGIC);
56 end component dff;
57
58 component inv is
59 Port (x : in STD_LOGIC;
60 y : out STD_LOGIC);
61 end component inv;
62
63 component xor2 is
64 Port (a : in STD_LOGIC;
65 b : in STD_LOGIC;
66 f : out STD_LOGIC);
67 end component xor2;
68
69 signal net1, net2, net3, netA,netB,netC:std_logic;
70 signal qint:std_logic_vector(2 downto 0);
71
72 begin
73 q <= qint;
74
Tcl Console
Messages
Log
Reports
Design Runs


PROJECT MANAGER - project_1
Sources
bistabil1 : dff(Behavioral) (dff.vhd)
bistabil0 : dff(Behavioral) (dff.vhd)
M1 : mux2(Behavioral) (mux2.vhd)
M2 : mux2(Behavioral) (mux2.vhd)
M3 : mux2(Behavioral) (mux2.vhd)
I1 : inv(Behavioral) (inv.vhd)
I2 : inv(Behavioral) (inv.vhd)
X1 : xor2(Behavioral) (xor2.vhd)
Constraints
Simulation Sources (2)
Hierarchy
Libraries
Compile Order
Source File Properties
xor2.vhd
Enabled
Location: C:/Users/XMarius/Desktop/fac
Type: VHDL
Library: xil_defaultlib
Size: 1.0 KB
Modified: Sunday 12/17/23 10:06:25 PM
General
Properties
Project Summary
automat2.vhd
C:/Users/XMarius/Desktop/facultate/AN 2 SEM 1/CID/lab/Proiect CID/project_1/project_1.srcs/sources_1/new/automat2.vhd
58 component inv is
59 Port (x : in STD_LOGIC;
60 y : out STD_LOGIC);
61 end component inv;
62
63 component xor2 is
64 Port (a : in STD_LOGIC;
65 b : in STD_LOGIC;
66 f : out STD_LOGIC);
67 end component xor2;
68
69 signal net1, net2, net3, netA,netB,netC:std_logic;
70 signal qint:std_logic_vector(2 downto 0);
71
72 begin
73 q <= qint;
74
75 bistabil2: dff port map(clk => clk, d =>net1, r => r, q => qint(2));
76 bistabil1: dff port map(clk => clk, d =>net2, r => r, q => qint(1));
77 bistabil0: dff port map(clk => clk, d =>net3, r => r, q => qint(0));
78
79 M1: mux2 port map(i0=>netB, i1=>'0', a=>qint(2), y=>net1);
80 M2: mux2 port map(i0=>netA, i1=>netB ,a=>qint(2), y=>net2);
81 M3: mux2 port map(i0=>netC, i1=>'1', a=>qint(2), y=>net3);
82
83 I1: inv port map (x => qint(0), y => netA);
84 I2: inv port map (x => qint(1), y => netB);
85
86 X1: xor2 port map(a => qint(0), b => qint(1), f => netC);
87 q <= qint;
88 end Behavioral;
Tcl Console
Messages
Log
Reports
Design Runs

7.Sursa de test