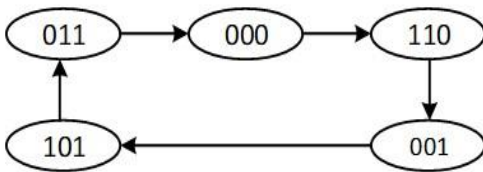



# Proiect

## Circuite integrate digitale

-Pop Catalin-Cornel-



r	clk	Action
0	x	Reset
1		$Q^+ = D$
otherwise		Wait

Implementare:

-MUX 2:1 cu Porti logice

Instructiuni implementare MUX:

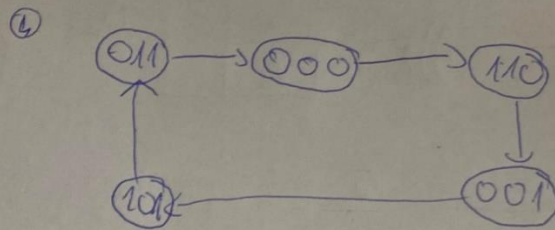
-IF...ELSE

<b>Q2</b>	<b>Q1</b>	<b>Q0</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	x	x	x
0	1	1	0	0	0
1	0	0	x	x	x
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	x	x	x

# 1. Rezolvarea circuitului pe foaie

Proiect  
Circuite integrate digitale

Papă Căvelim-Corad  
Gr: 2126

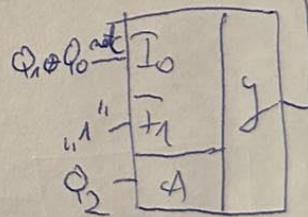
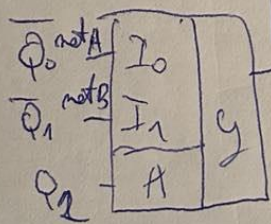
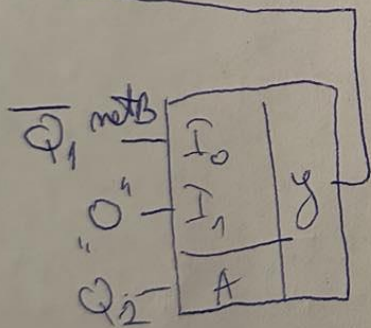
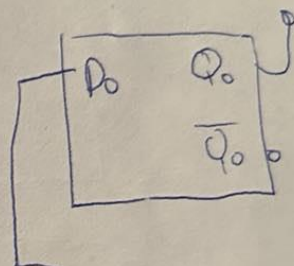
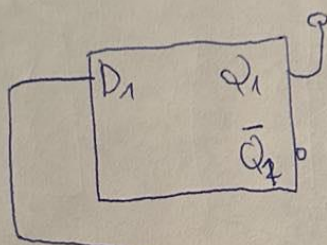
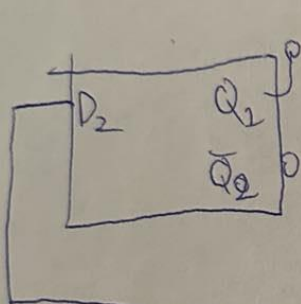


⑤

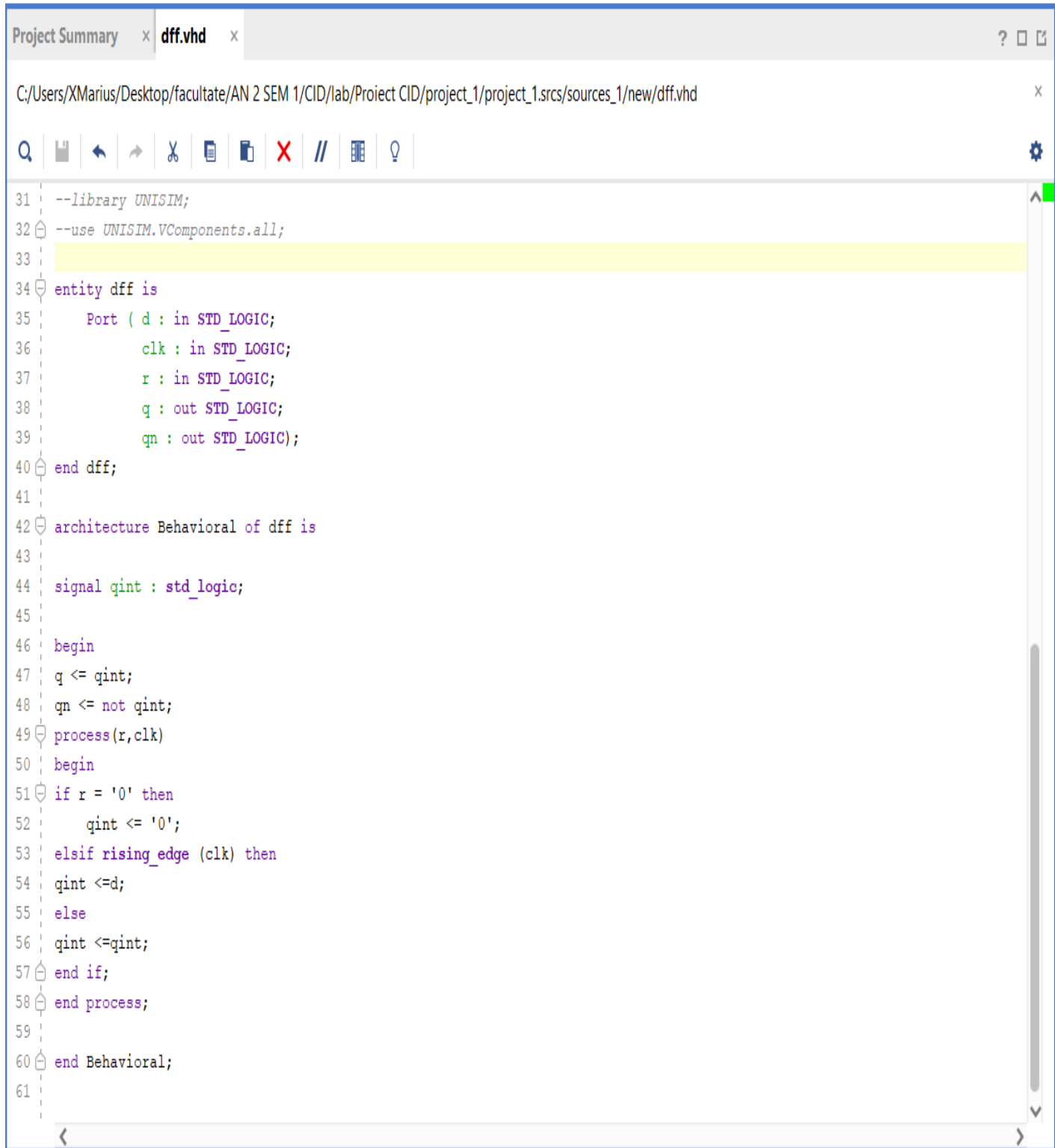
R	clk	Action
0	x	Reset
1		$Q^+ = D$
otherwise		Wait

MUX 2:1 in parti logice

$Q_2$	$Q_1$	$Q_0$	$D_2$ $Q_2^+$	$D_1$ $Q_1^+$	$D_0$ $Q_0^+$
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	x	x	x
0	1	1	0	0	0
1	0	0	x	x	x
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	x	x	x



## 2.Implementarea sursei de design a Bistabilului D



```
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity dff is
35     Port ( d : in STD_LOGIC;
36           clk : in STD_LOGIC;
37           r : in STD_LOGIC;
38           q : out STD_LOGIC;
39           qn : out STD_LOGIC);
40 end dff;
41
42 architecture Behavioral of dff is
43
44     signal qint : std_logic;
45
46     begin
47         q <= qint;
48         qn <= not qint;
49         process(r,clk)
50         begin
51             if r = '0' then
52                 qint <= '0';
53             elsif rising_edge (clk) then
54                 qint <=d;
55             else
56                 qint <=qint;
57             end if;
58         end process;
59
60     end Behavioral;
61
```

esign Runs

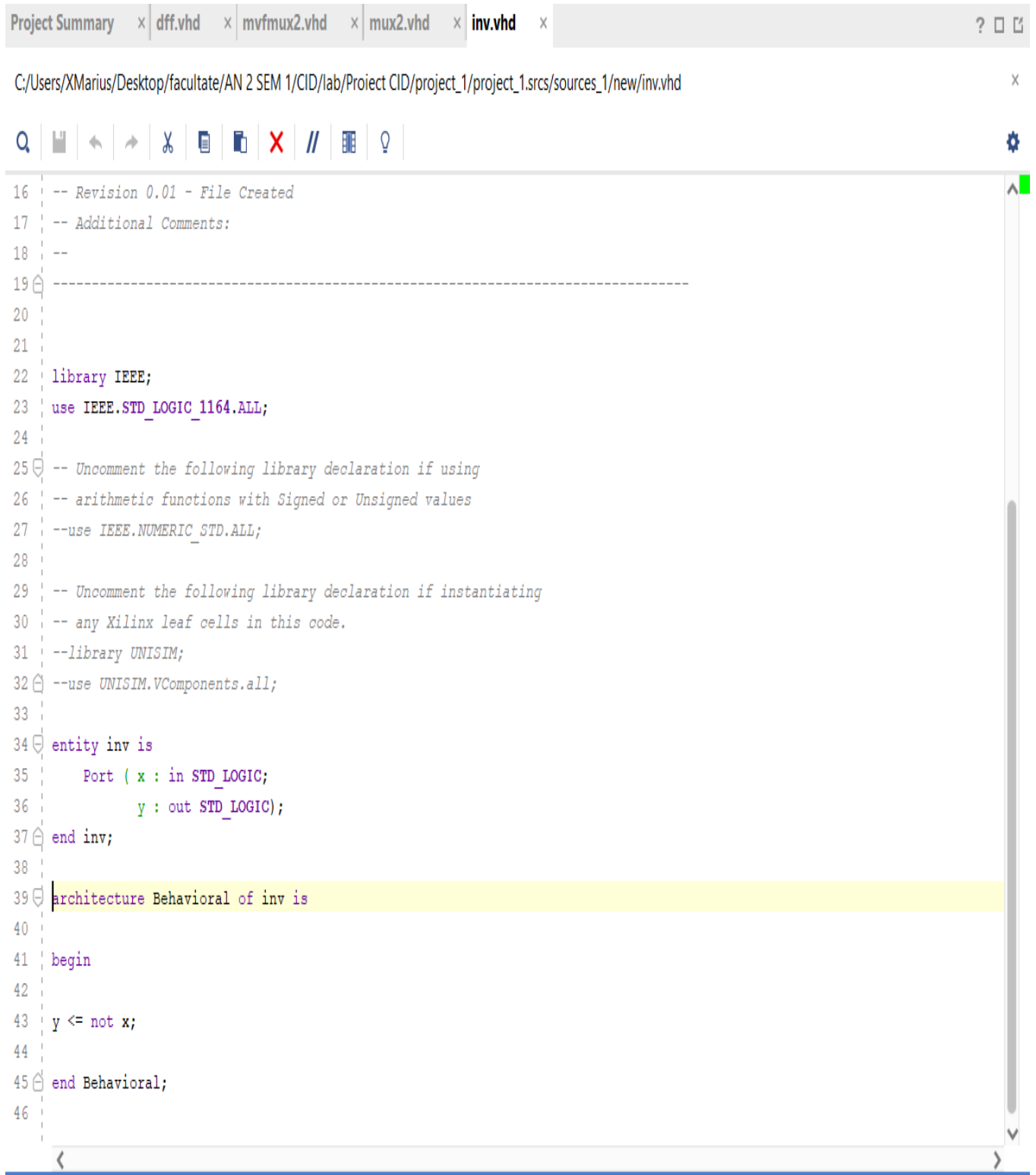
### 3.Implementarea sursei de design MUX 2:1

The screenshot displays the PROJECT MANAGER - project\_1 window. The main editor shows the mux2.vhd file, which defines a 2-to-1 multiplexer. The code is as follows:

```
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity mux2 is
35     Port (
36         i0 : in STD_LOGIC;
37         i1 : in STD_LOGIC;
38         a  : in STD_LOGIC;
39         y  : out STD_LOGIC
40     );
41 end entity mux2;
42
43 architecture Behavioral of mux2 is
44 begin
45     process(i0,i1,a)
46     begin
47
48         if a = '1' then y <= i1;
49         else y<= i0;
50         end if;
51     end process;
52 end process;
53
54
55
56
57 end architecture Behavioral;
```

The left sidebar shows the project hierarchy with folders for Design, Constraints, Simulation, and Utility Scripts. The bottom status bar includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs.

## 4.Implementarea sursei de design a inversorului



```
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  -----
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity inv is
35      Port ( x : in STD_LOGIC;
36            y : out STD_LOGIC);
37  end inv;
38
39  architecture Behavioral of inv is
40
41  begin
42
43      y <= not x;
44
45  end Behavioral;
46
```

## 5. Implementarea sursei de design a portii logice xor.

The screenshot displays the Xilinx ISE Project Manager interface for a project named 'project\_1'. The 'Sources' pane on the left lists various VHDL files, with 'X1:xor2(Behavioral) (xor2.vhd)' selected. The 'Source File Properties' pane below it shows details for 'xor2.vhd', including its location, type (VHDL), library (xil\_defaultlib), size (1.0 KB), and modification date (Sunday 12/17/23 10:06:25 PM). The main editor window shows the VHDL code for the 'xor2' entity. The code includes library declarations for IEEE and UNISIM, followed by the entity definition with two input ports 'a' and 'b', and one output port 'f'. The behavioral architecture is implemented using a simple XOR operation: `f <= a xor b;`.

PROJECT MANAGER - project\_1

Sources

- bistabil1: dff(Behavioral) (dff.vhd)
- bistabil0: dff(Behavioral) (dff.vhd)
- M1: mux2(Behavioral) (mux2.vhd)
- M2: mux2(Behavioral) (mux2.vhd)
- M3: mux2(Behavioral) (mux2.vhd)
- I1: inv(Behavioral) (inv.vhd)
- I2: inv(Behavioral) (inv.vhd)
- X1: xor2(Behavioral) (xor2.vhd)

Constraints

Simulation Sources (2)

Hierarchy Libraries Compile Order

Source File Properties

xor2.vhd

Enabled

Location: C:/Users/XMarius/Desktop/fac

Type: VHDL

Library: xil\_defaultlib

Size: 1.0 KB

Modified: Sunday 12/17/23 10:06:25 PM

General Properties

Project Summary x automat2.vhd x test2.vhd x mux2.vhd x dff.vhd x xor2.vhd x

C:/Users/XMarius/Desktop/facultate/AN 2 SEM 1/CID/lab/Project CID/project\_1/project\_1.srcs/sources\_1/new/xor2.vhd

```
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity xor2 is
35     Port ( a : in STD_LOGIC;
36           b : in STD_LOGIC;
37           f : out STD_LOGIC);
38 end xor2;
39
40 architecture Behavioral of xor2 is
41
42 begin
43     f <= a xor b;
44
45 end Behavioral;
```

Tcl Console Messages Log Reports Design Runs

40:1 Insert VHDL



## 6. Implementarea automatului

**PROJECT MANAGER - project\_1**

**Sources**

- bistabil1 : dff(Behavioral) (dff.vhd)
- bistabil0 : dff(Behavioral) (dff.vhd)
- M1 : mux2(Behavioral) (mux2.vhd)
- M2 : mux2(Behavioral) (mux2.vhd)
- M3 : mux2(Behavioral) (mux2.vhd)
- I1 : inv(Behavioral) (inv.vhd)
- I2 : inv(Behavioral) (inv.vhd)
- X1 : xor2(Behavioral) (xor2.vhd)**

Constraints  
Simulation Sources (2)

**Source File Properties**

xor2.vhd

☒ Enabled

Location: C:/Users/XMarius/Desktop/facultate/AN 2 SEM 1/CID/lab/Proiect CID/project\_1/project\_1.srcs/sources\_1/new/automat2.vhd

Type: VHDL

Library: xil\_defaultlib

Size: 1.0 KB

Modified: Sunday 12/17/23 10:06:25 PM

**Project Summary** x automat2.vhd x

C:/Users/XMarius/Desktop/facultate/AN 2 SEM 1/CID/lab/Proiect CID/project\_1/project\_1.srcs/sources\_1/new/automat2.vhd

```
19
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24 use IEEE.STD_LOGIC_ARITH.ALL;
25 use IEEE.STD_LOGIC_UNSIGNED.ALL;
26 -- Uncomment the following library declaration if using
27 -- arithmetic functions with Signed or Unsigned values
28 --use IEEE.NUMERIC_STD.ALL;
29
30 -- Uncomment the following library declaration if instantiating
31 -- any Xilinx leaf cells in this code.
32 --library UNISIM;
33 --use UNISIM.VComponents.all;
34
35 entity automat2 is
36     Port ( clk : in STD_LOGIC;
37           r : in STD_LOGIC;
38           q : out STD_LOGIC_VECTOR(2 downto 0));
39 end automat2;
40
41 architecture Behavioral of automat2 is
42
43     component mux2 is
44         Port ( i0 : in STD_LOGIC;
45               i1 : in STD_LOGIC;
46               a : in STD_LOGIC;
47               y : out STD_LOGIC);
48     end component mux2;
49
50     component dff is
```

**Sources** ? \_ □ ×

Q 0

- b1stabil1 : dff(Behavioral) (dff.vhd)
- b1stabil0 : dff(Behavioral) (dff.vhd)
- M1 : mux2(Behavioral) (mux2.vhd)
- M2 : mux2(Behavioral) (mux2.vhd)
- M3 : mux2(Behavioral) (mux2.vhd)
- I1 : inv(Behavioral) (inv.vhd)
- I2 : inv(Behavioral) (inv.vhd)
- X1 : xor2(Behavioral) (xor2.vhd)

> Constraints

▼ Simulation Sources (2)

< >

**Hierarchy** Libraries Compile Order

**Source File Properties** ? \_ □ ×

● xor2.vhd

☒ Enabled

Location: C:/Users/XMarius/Desktop/fac

Type: VHDL

Library: xil\_defaultlib

Size: 1.0 KB

Modified: Sunday 12/17/23 10:06:25 PM

< >

**General** Properties

**Project Summary** x automat2.vhd x ? \_ □ ×

C:/Users/XMarius/Desktop/facultate/AN 2 SEM 1/CID/lab/Proiect CID/project\_1/project\_1.srscs/sources\_1/new/automat2.vhd

Q

```
43 component mux2 is
44     Port ( i0 : in STD_LOGIC;
45           i1 : in STD_LOGIC;
46           a : in STD_LOGIC;
47           y : out STD_LOGIC);
48 end component mux2;
49
50 component dff is
51     Port ( d : in STD_LOGIC;
52           clk : in STD_LOGIC;
53           r : in STD_LOGIC;
54           q : out STD_LOGIC;
55           qn : out STD_LOGIC);
56 end component dff;
57
58 component inv is
59     Port ( x : in STD_LOGIC;
60           y : out STD_LOGIC);
61 end component inv;
62
63 component xor2 is
64     Port ( a : in STD_LOGIC;
65           b : in STD_LOGIC;
66           f : out STD_LOGIC);
67 end component xor2;
68
69 signal net1, net2, net3, netA, netB, netC : std_logic;
70 signal qint : std_logic_vector(2 downto 0);
71
72 begin
73     q <= qint;
74
```

Tcl Console	Messages	Log	Reports	Design Runs
-------------	----------	-----	---------	-------------

```
Project Summary x automat2.vhd x
C:/Users/XMarius/Desktop/facultate/AN 2 SEM 1/CID/lab/Proiect CID/project_1/project_1.srscs/sources_1/new/automat2.vhd

58 component inv is
59     Port ( x : in STD_LOGIC;
60           y : out STD_LOGIC);
61 end component inv;
62
63 component xor2 is
64     Port ( a : in STD_LOGIC;
65           b : in STD_LOGIC;
66           f : out STD_LOGIC);
67 end component xor2;
68
69 signal net1, net2, net3, netA,netB,netC:std_logic;
70 signal qint:std_logic_vector(2 downto 0);
71
72 begin
73     q <= qint;
74
75     bistabil2: dff port map(clk => clk, d =>net1, r => r, q => qint(2));
76     bistabil1: dff port map(clk => clk, d =>net2, r => r, q => qint(1));
77     bistabil0: dff port map(clk => clk, d =>net3, r => r, q => qint(0));
78
79     M1: mux2 port map(i0=>netB, i1=>'0', a=>qint(2), y=>net1);
80     M2: mux2 port map(i0=>netA, i1=>netB ,a=>qint(2), y=>net2);
81     M3: mux2 port map(i0=>netC, i1=>'1', a=>qint(2), y=>net3);
82
83     I1: inv port map ( x => qint(0), y => netA);
84     I2: inv port map ( x => qint(1), y => netB);
85
86     X1: xor2 port map( a => qint(0), b => qint(1), f => netC);
87     q <= qint;
88 end Behavioral;
```

## 7.Sursa de test

