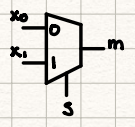
Review: **Multiplexer (MUX)** choose one of several inputs as the output, based on select signals.

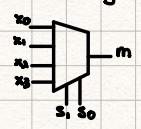
2-to-1 MUX



S	m
0	x_0
1	x_1

$m = Sx_1 + \bar{S}x_0$

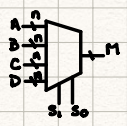
4-to-1 MUX



S_1	S_0	m
0	0	x_0
0	1	x_1
1	0	x_2
1	1	x_3

a n-bit 4 to 1 mux:

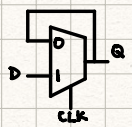
```
module nbit_4_to_1(A, B, C, D, S, M),
    parameter n=16;
    input [n-1:0] A, B, C, D;
    output reg [n-1:0] M;
    input [1:0] S;

    always @(*)
    begin
        if (S==0) M <= A;
        else if (S==1) M<= B;
        else if (S==2) M<= C;
        else M<=D;
    end
endmodule
```



Storage of Numbers

Latch

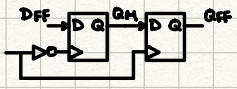
CLK	D	Q
0	0	0/1
0	1	0/1 (what it last was before CLK→0)
1	0	0
1	1	1

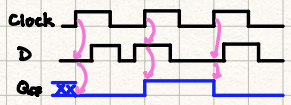


If CLK=1, Q=D, when clock becomes 0, Q stop changing

Flip-flop captures/stores the value of D on the edge (transition) of clock "edge-triggered"

Clock	Q
0	0/1
1	0/1
↓	0





Flip-flop with Enable

if E=0, Q doesn't change

E=1, flip operates as above