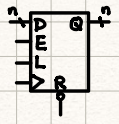
n-bit register

- store multi-bit number
- this n flip-flops . all with same clock & Enable signal
- Enable controls whether register activates on clock edges, copying D into Q

n-bit counter with reset & load



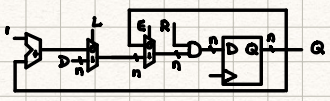
if R=0 . on ⌐ clock, Q=0

if E=1 ,

if L=1, on ⌐ clock, Q=D

else if L=0, on ⌐ clock, Q=Q+1 (increment)

else if E=0, Q doesn't change.



Verilog for the circuit:

```
module countn (R, L, E, Clock, D, Q);
    parameter n = 16;
    input R, L, E, Clock;
    input [n-1:0] D;
    output [n-1:0] Q;

    always @ (posedge Clock)
    begin
        if (R==0) Q<=0; // and gate
        else if (E==1)
            if (L==1) Q<=D; // mux
            else Q<=Q+1; // adder
    end
endmodule
```

Finite State Machine (FSM)

FSM controls **what** happens and **when** it happens

Enables, Loads, mux. on which clock cycle

select, add/sub.