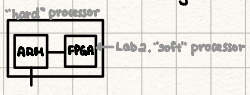
From now on, we'll be using a real processor that exists permanently on the big Cyclone SoC chip that also contains the FPGA

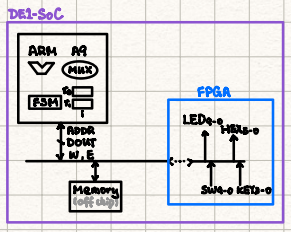


Brand Version

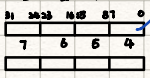
Hard processor: ARM Cortex A9

- More powerful than Lab 2 processor
- All registers are 32 bits wide (not 16)
- There are 16 processor registers (not 8)
- ADDR, DOUT, $\overline{W}$ wires also 32 bits wide (not 16)
- Memory is organized as so, each 8 bits (byte) gets its own address

  but we can access 32 bits (4 bytes) in a single memory access



Address: 3 2 1 0 — the 4 bytes @ address 0 make up 1 word.



0, 4, 8, ... similar

- 2^{32} memory locations = 4G bytes = 1G words (1 word = 4 bytes)
- The DE1-SoC has 1 Gbyte = 256 M words
- Exist at addresses: 0 to $3FFF\ FFFF_{16}$
- The other addresses are used for memory-mapped I/O

  e.g. LEDRs-0 @ address FF20 0000

  HEXs-0 ... ... FF20 0020 & FF20 0030

  SWs-0 ... ... FF20 0040

  KEYs-0 ... ... FF20 0050

Example program: Add 4 numbers in memory (put answer in R2)

```
        .text
        .global _start
_start: MOV  R0,#4      R0 ← 4
        MOV  R1,#LIST   R1 ← 32'h LIST
        LDR  R2,[R1]    R2 ← [32'h] = 10
        ADD  R1, R0     R1 ← R1 + R0 = R1 + 4 = 56
        LDR  R3,[R1]    R3 ← [56] = 20
        ADD  R2,R3      R2 ← R2 + R3 = 30
        ADD  R1, R0
        LDR  R3,[R1]
        ADD  R2,R3
        ADD  R1, R0
        LDR  R3,[R1]
        ADD  R2,R3
END:    B    END
LIST:   .word 10,20,30,40
        .end
```

	Address	
LIST:	52_{10}	10_{16}
	56	20
	60	30
	64	40

(Each instruction is 4 byte.

So LIST is @ 52 by counting)