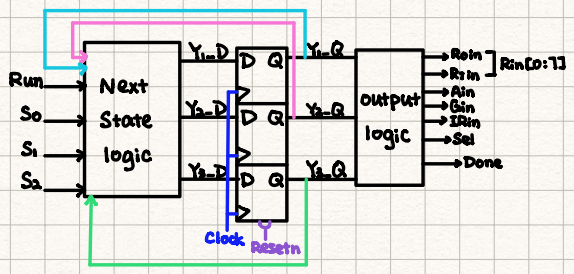
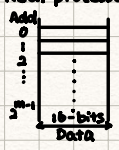
```
// state register
  reg [2:0] Tstep_Q, Tstep_D;
  always @ (posedge clock)
     If (!Resetn)
        Tstep_Q <= T0; //reset state
     else Tstep_Q = Tstep_D
See Lab 1 for the next state logic
```




```
// output logic based on current state & current instruction type
  always @ (*) begin
     //Default values for all the outputs
     Done = 1'b0; Ain = 1'b0; Gin = 1'b0; AddSub = 1'b0; IRin = 1'b0; Rin = 8'b0;
     case (Tstep_Q)
        T0: IRin = 1'b1; //copies DIN into IR
        T1: //do different things depends on instruction
           case (III)                                   IMM = IR[2]
              mv: begin                                 rY = IR[2:0]
                 if (!IMM) Sel = rY;                    III = IR[15:13]
                 else  Sel = Sel_D;
                 Rin = Xreg;
                 Done = 1'b1;
              end
              ... ...
```

Part 2

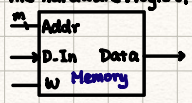
Real processors don't stop at DIN. instructions are "fetched" from memory.



width is 16

depth = 2^{m-1}

The hardware / logic of memory



In part 2, make a read-only memory & attach it to DIN