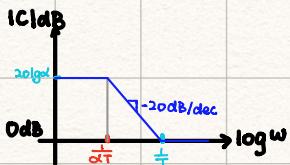
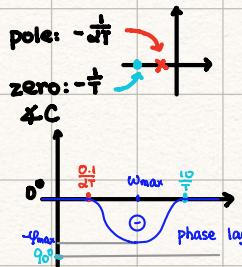


LAG COMPENSATOR DESIGN

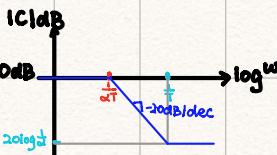
$$\textcircled{1} \quad C(s) = \alpha \cdot \frac{Ts+1}{\omega Ts+1} \quad \alpha > 1$$



$$C(0) = \alpha > 1 \quad |C(0)|_{dB} = 20 \log \alpha$$



$$\textcircled{2} \quad C(s) = \frac{Ts+1}{\alpha Ts+1} \quad \alpha > 1$$



$$C(0) = 1 \quad |C(0)|_{dB} = 0 \text{ dB}$$

Either introduces phase lag @ medium freq. \Rightarrow determine for the PM (reduce it)

Form ① has a DC gain of $20 \log \alpha > 0 \text{ dB}$ ("amplification")

\Rightarrow will help for increasing the DC gain of the overall loop

hence decrease the ess (steady-state spec error)

Form ② has 0 dB DC gain and $-20 \log \alpha$ gain @ high freq.

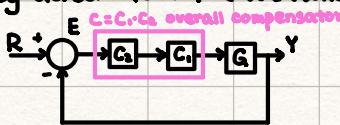
\Rightarrow will be potentially good to use if we reduce the ω_c and indirectly increase the PM

Form 1: to increase DC gain (for ess), without degrading the PM (assume PM is OK)

Step 1: decide α depending on DC gain. increase that is needed for ess spec. $C(0) = \alpha$

Step 2: choose T s.t. PM is not degraded. i.e. $\frac{10}{T} \leq \omega_c$ (where PM is read)

Example: LEAD ex 1:



$$C_1(s) = \frac{1 + 0.92s}{1 + 0.92 + 0.03s} ; G(s) = \frac{100}{s(s+1)(s+10)}$$

we designed $C_1(s)$ and achieved that $\omega_c^{\text{NEW}} \approx 6.3$; asy. tracking of step ref. signal and PM $^{\text{NEW}} \approx 45^\circ$

Consider that we want to keep the DM $^{\text{NEW}}$, but achieve a steady-state $\text{ess} = \text{e}(0) \leq 1\%$ for ramp ref. signal ($r(t) = t$)

$$R(s) (r=\text{ramp})$$

$$\text{Step 1: Use FVT: } \text{ess} = \text{e}(0) = \lim_{s \rightarrow 0} s \cdot \frac{1}{1 + C_1(s) \cdot G(s)} \cdot \frac{1}{s^2} = \frac{1}{10 C_1(0)} = 0.1 = 10\%$$

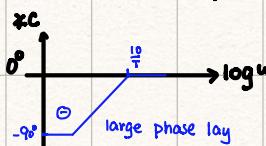
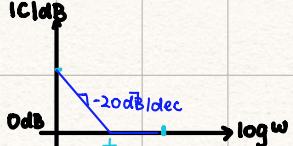
\Rightarrow to achieve $\text{ess} \leq 0.01 \Rightarrow$ DC gain \uparrow by 10 \Rightarrow we will use a LAG compensator to do this.

$$\Rightarrow C_2(s) = \frac{\alpha Ts+1}{\alpha T s+1} ; C_2(0) = \alpha \Rightarrow \text{ess} = \frac{1}{10 \cdot C_1(0) \cdot C_2(0)} \leq 0.01 \Rightarrow \alpha \geq 10$$

$$\text{Step 2: Select } T \text{ s.t. } \frac{10}{T} \leq 6.3 = \omega_c^{\text{NEW}} \Rightarrow \frac{1}{T} \leq 0.5 \Rightarrow T = 2$$

$$\text{LAG: } C_2(s) = 10 \cdot \frac{2s+1}{20s+1} ; \text{ overall is } C = C_1 C_2 \text{ LEAD/LAG compensator}$$

Limiting case of $\alpha \rightarrow \infty$: $C(s) = Ts + \frac{1}{\alpha} \Rightarrow C(s) = 1 + \frac{1}{Ts} \Rightarrow \text{"PI" (compensator)}$



due to pole in $s=0 \rightarrow \infty$ DC gain, slope = -20 dB/dec.

\Rightarrow This will be used to increase the order of system s.t. we have more poles in $s=0$. hence can track ref. signal with more poles in $s=0$

Due to phase lag \Rightarrow s.t. PM is not impacted select $\frac{10}{T} \leq w_c$

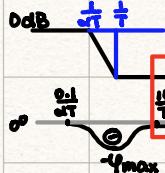
In example: as extra spec for $C \cdot G \rightarrow$ 1 pole in $s=0$ $\xrightarrow{\text{LEAD}}$

$e_{ss} = e(\infty) \approx 1\%$ for $r(t) = t$ (ramp) \rightarrow used a LAG compensator \uparrow DC gain by 10

But if want $e_{ss} = 0$ for $r(t) = t \cdot u(t) \rightarrow$ by IMP. we need 2 poles in $s=0$ in $C \cdot G \rightarrow$ need an extra pole in $s=0$

\Rightarrow use a PI controller instead of a LAG

Form 2: $C(s) = \frac{T_s + 1}{\alpha T_s + 1}$; $\alpha > 1$ Used to reduce gain at med. freq. s.t. w_c and indirectly PM



Design is simple \Rightarrow "slide" of the Bode plots to where we have the desired PM and set $\frac{10}{T} \leq w_c$ ^{NEW}

decrease gain with no phase lag in this freq. region

Example: $G(s) = \frac{100}{s(s+1)(s+10)}$ \leftarrow Ex ① LEAD, wanted PM $\xrightarrow{\text{NEW}} 45^\circ$

Here use a LAG, form ② instead to achieve PM $\xrightarrow{\text{NEW}} 45^\circ$

For PM of $45^\circ \Rightarrow$ need $w_c \xrightarrow{\text{NEW}} 1$ i.e. gain should be 0dB at that freq.

But $|G(jw)| \text{dB} \approx 20 \text{dB}$ (From Bode plot) \rightarrow use LAG with $-20 \log \alpha = -20 \text{dB} \Rightarrow \alpha = 10$

$$\Rightarrow \frac{10}{T} \leq w_c \xrightarrow{\text{NEW}} 1 \Rightarrow T = 10$$

Draw back: the sys. will be slower

