Name: Cayce Beames
Date: November 24, 2019
Professor Steven Gillette

Abstract

Learning Objectives

- Test transistor forward and reverse bias values
- Test transistor gain using a DMM
- Calculate transistor gain by measuring base and collector currents
- Plot transistor performance on a scatter plot

Notes:

1. Took all voltage measurements relative to ground (unless otherwise stated)
2. Recorded relevant measurements and calculation results in data tables
3. Recorded all measured values on the circuit schematics
4. Used all available precision in calculations, rounded off answers to 3 significant figures
5. ***Calculated collector currents using Ohm's Law and the voltage drop across R1.***
6. ***Calculated base currents using Ohm's Law and the voltage drop across R2.***

Materials

Quantity	Description
1	150kΩ resistor
1	430Ω resistor
1	1 MΩ potentiometer
1	NPN TO-18 power transistor (BJT)[1]
1	NPN TO-92 general purpose transistors (BJT)[1]
1	PNP TO-92 general purpose transistor (BJT)[1]
1	DMM
1	GS Trainer
1	Can – freeze spray

Procedure – Setup

1. Used the DMM to determine if the transistor is an NPN or PNP. Verified transistor leads configuration using the following procedure. Used findings to build a data table like the example provided in this lab.
    a. Set the DMM to diode check mode
    b. Clipped one DMM lead to the ***base*** and the other to the ***emitter***.

[1] Do not use FET's, (e.g. 2N5951) or TIP106

c. If the reading was greater than 3V, swapped the meter leads.

d. When the meter reads 0.5 to 0.7 V the junction is forward biased.

e. Added a (+) sign to the transistor schematic diagram base lead if the red lead is attached to base, or a (-) sign if the black lead is attached to the base.

f. Added the opposite sign to the transistor schematic for both the emitter and collector.

g. Drew in forward biased diodes on both emitter and collector.

2. Used the DMM diode test feature to ***measure and record*** the forward biased barrier potentials for V_{BE}, and V_{BC}.
3. Used the voltage readings to determine if the transistor is functional. (e.g. V_{BE} and $V_{BC} \approx 0.6$ V and $V_{CE} > 3$ V.

Procedure – Beta Measurement

4. Used the DMM HFE test feature to ***measure and record*** the transistor gains.
5. Built Circuit 1 for NPN transistors.
6. Verified that the transistor will turn off completely by lifting the conductor attached to the base lead. Checked near zero collector current using Ohm's Law and the voltage drop across R1.
7. Reconnected the base lead and adjusted the potentiometer until I_B was approximately 10µA. ***Calculated and recorded*** the base current value.
8. ***Calculated and recorded*** the collector current value.
9. ***Calculated and recorded*** the transistor beta using the Transistor Gain formula.
10. Increased the base current to approximately 20µA, 30µA, 40µA, and 50µA. ***Measured & recorded*** base and collector currents and calculate beta for each base current.
11. ***Created a scatter plot*** of the transistor response with base current on the X-axis (horizontal) and collector current on the Y-axis.
12. Repeated steps 4 to 10 for each of 3 transistors. Noted that circuit 2 is identical except for the PNP transistor and the negative polarity of the voltage source.

Procedure – Temperature Effect on Beta Measurement

13. For the last transistor, monitored I_B & I_C as you spray the circuit with a ***short*** burst of freeze spray. ***Calculated and recorded*** the percent change in base current (I_B) and collector current (I_C) with the cold spray.

	Room temperature	Cold spray	
Collector current I_C (V_{R1}/R_1)	**14mA**	**9.1mA**	
Base current I_B (V_{R2}/R_2)	**50µA**	**50µA**	**Gain Percent Change**
Gain (I_C / I_B)	**282**	**182**	**-35.5%**

Formulas

Transistor Beta

$$\beta_{dc} = \frac{I_C}{I_B}$$

Where;
β_{dc} = transistor beta (gain)
I_C = collector current
I_B = base current

Data Results - See spreadsheet in Appendix A, Lab Notes

Critical Thinking

1. How is transistor gain effected by a decrease in transistor temperature?

When the transistor is cooled, the gain was observed to decrease.

2. For an NPN transistor to conduct, the collector voltage should be more positive / negative (select one) then the emitter (see lab schematic).

When the forward bias current is applied to the base at the appropriate amount, the NPN transistor is switched on and the collector is now able to conduct from the source through the emitter to ground in conventional flow. This means that while switched off, the collector must be maintained to be more positive than the emitter.

3. For a PNP transistor to conduct, the collector voltage should be more positive / negative (select one) then the emitter (see lab schematic).

When the negative bias current is applied to the base at the appropriate amount, the PNP transistor is switched on and the emitter is now able to conduct from the emitter through the collector to the negative source in conventional flow. This means that while switched off, the collector must be maintained to be more negative than the emitter.

4. What is transistor beta?

Transistor beta, β is the current amplification gain of a transistor. It is the ratio of the current at the collector divided by the current at the base, $\beta = \frac{I_C}{I_B}$.

5. Use Ohm's law to determine the maximum current the lab circuit can provide to the base and collector of the transistor? Show your work.

The source for lab circuit 1 is configured for +12V, measured at +12.05V and the lab circuit 2 is configured for -12V, measured at -12.08V. Both circuits have an R1 of 430Ω resistor that was measured at 422Ω and a series resistor R2 of 150KΩ, measured at 149.7kΩ and a potentiometer R3 set to its minimum resistance, 0Ω. Therefore, for circuit 1, the maximum current to the collector is $\frac{Vs}{R1} = \frac{12.05V}{422\Omega} = 0.029A, or\ 29mA$. The maximum current to the base is $\frac{Vs}{R3} = \frac{12.05V}{149.7k\Omega} = 0.00008049A, or\ 80.5\mu A$. For circuit 2, the maximum current to the collector is $\frac{Vs}{R1} = \frac{-12.08V}{422\Omega} = -0.029A, or\ -29mA$. The maximum current to the base is $\frac{Vs}{R3} = \frac{-12.08V}{149.7k\Omega} = 0.00008069A, or\ 80.7\mu A$.

Appendix A – Lab Notes

SIERRA COLLEGE	MECH 10 - Lab 20 Transistor Gain	Mechatronics Real Skills Real Jobs
Name Cayce Beamer		11/19/19

Learning Objectives

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4. Use all available precision in calculations, round off answers to 3 significant figures
5. ***Calculate collector currents using Ohm's Law and the voltage drop across R1.***
6. ***Calculate base currents using Ohm's Law and the voltage drop across R2.***

Materials

MJE2955T -TO-220

Quantity	Description
1	150kΩ resistor
1	430Ω resistor
1	1 MΩ potentiometer
1	NPN TO-18 power transistor (BJT)[1]
1	NPN TO-92 general purpose transistors (BJT)[1]
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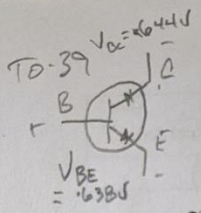
Procedure – Setup

1. Use the DMM to determine if the transistor is an NPN or PNP. Verify transistor leads configuration using the following procedure. Use your findings to build a data table like the example provided in this lab.
   a. Set the DMM to diode check mode
   b. Clip one DMM lead to the ***base*** and the other to the ***emitter***.
   c. If the reading is greater than 3V, swap the meter leads.
   d. When the meter reads 0.5 to 0.7 V the junction is forward biased.
   e. Add a (+) sign to the transistor schematic diagram base lead if the red lead is attached to base, or a (-) sign if the black lead is attached to the base.

[1] Do not use FET's, (e.g. 2N5951) or TIP106

SDG 04/14 MECH 10 - Lab 20 Page 1 of 3



f. Add the opposite sign to the transistor schematic for both the emitter and collector.

g. Draw in forward biased diodes on both emitter and collector.

2. Use the DMM diode test feature to ***measure and record*** the forward biased barrier potentials for V_{BE}, and V_{BC}.

3. Use the voltage readings to determine if the transistor is functional. (e.g. V_{BE} and $V_{BC} \approx 0.6$ V and $V_{CE} > 3$ V.

Procedure – Beta Measurement

4. Use the DMM HFE test feature to ***measure and record*** the transistor gains. 270

5. Build Circuit 1 for NPN transistors.

6. Verify that the transistor will turn off completely by lifting the conductor attached to the base lead. Check near zero collector current using Ohm's Law and the voltage drop across R1. ~15.6mA

7. Reconnect the base lead and adjust the potentiometer until I_B is approximately 10µA. ***Calculate and record*** the base current value.

8. ***Calculate and record*** the collector current value.

9. ***Calculate and record*** the transistor beta using the Transistor Gain formula.

10. Increase the base current to approximately 20µA, 30µA, 40µA, and 50µA. ***Measure & record*** base and collector currents and calculate beta for each base current.

11. ***Create a scatter plot*** of the transistor response with base current on the X-axis (horizontal) and collector current on the Y-axis. linear

12. Repeat steps 4 to 10 for each of 3 transistors. Note that circuit 2 is identical except for the PNP transistor and the negative polarity of the voltage source.

Procedure – Temperature Effect on Beta Measurement

13. For the last transistor, monitor I_B & I_C as you spray the circuit with a ***short*** burst of freeze spray. ***Calculate and record*** the percent change in base current (I_B) and collector current (I_C) with the cold spray.

	Room temperature	Cold spray	
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Formulas

Transistor Beta

$$\beta_{dc} = \frac{I_C}{I_B}$$

Where;
β_{dc} = transistor beta (gain)
I_C = collector current
I_B = base current

Data Results - attach spreadsheet

Critical Thinking

1. How is transistor gain effected by a decrease in transistor temperature? gain decreased
2. For an NPN transistor to conduct, the collector voltage should be more positive / negative (select one) then the emitter (see lab schematic).
3. For a PNP transistor to conduct, the collector voltage should be more positive / negative (select one) then the emitter (see lab schematic).
4. What is transistor beta? the gain
5. Use Ohm's law to determine the maximum current the lab circuit can provide to the base and collector of the transistor? Show your work.

$\frac{12}{422} = 28.4$, $\frac{12}{150k} = 80\mu A$

Grading Criteria

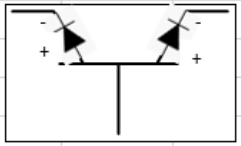
		Points Possible	Points Earned
Documentation	Abstract, introduction, experiment, data results, conclusions, attachments, clarity, spelling, grammar	**10**	
Setup	NPN / PNP configuration determined with diode test measurements; diode symbols and polarity drawn on transistor symbol, package sketch included, forward and reverse bias voltages recorded	**5**	
Beta Measurement	DMM HFE measured & recorded; I_B, I_C, beta calculated & recorded for three transistors	**20**	
Temperature Effect	Temperature impact on I_B and I_C observed and recorded	**5**	
Critical thinking	Questions answered completely & accurately. State conclusions drawn and lessons learned from the lab	**10**	
On-time submittal	Lab report is submitted in accordance with the assignment due date as posted on Canvas	**5**	
	Total	**55**	

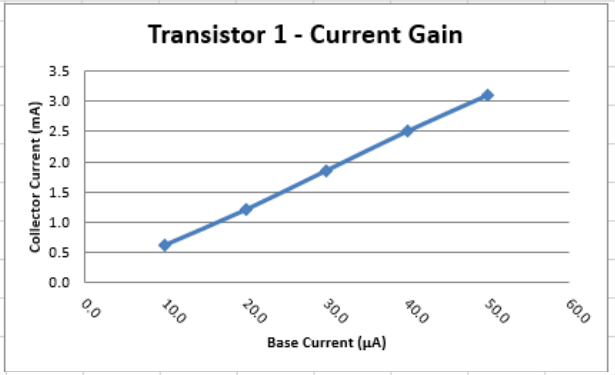
Lab Report Format

Abstract - a summary and high-level overview of the lab and its results
Introduction - State the objectives of the laboratory and list the equipment required
Experiment - Describe the procedure used to carry out the lab
Data Results - list data taken in table or graphical format where appropriate
Conclusion - State the conclusions drawn and lessons learned from the laboratory activities. Answer any questions found within the lab procedure.
Attachments – grading criteria, verification signatures, circuit diagrams, lab procedures & notes

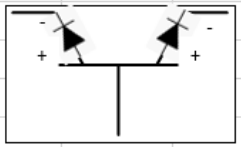
12.08V
-12V
R1
430Ω
Q1
R2
150KΩ
R3
1MΩ
CIRCUIT 2
PNP
12.05V
+12V
R1
430Ω
Q1
R2
150KΩ
R3
1MΩ
CIRCUIT 1
NPN
TO-18
2N3904
TO-92
MECH 10 – FUNDAMENTALS OF ELECTRONICS
LAB 20 – Transistor Gain
SIERRA COLLEGE
Mechatronics
Real Skills Real Jobs
DRAWN BY – S GILLETTE
AUGUST 2011
SIZE
FSCM NO
SCALE
NONE
DWG NO
MECH10-20
REV
0
SHEET
1 OF 1

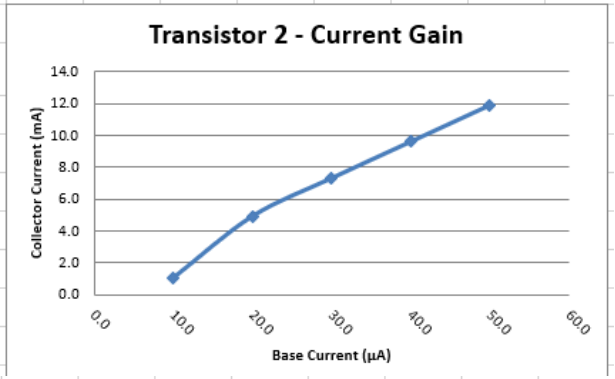
Transistor 1

Part #	Package Sketch	Package Designation	Diode Drawing	NPN or PNP?	Barrier V_{BE}	Barrier V_{BC}	Test Circuit I_B (µA)	Test Circuit I_C (mA)	HFE Calc	HFE Meas	Error %
2N1613		TO-39		NPN	0.638	0.644	10.0	0.6	61.6	70.0	12.00%
							20.0	1.2	60		14.29%
							30.0	1.85	61.6667		11.90%
							40.0	2.5	62.5		10.71%
							50.0	3.1	62		11.43%

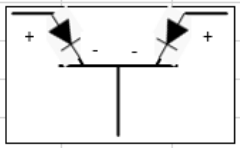


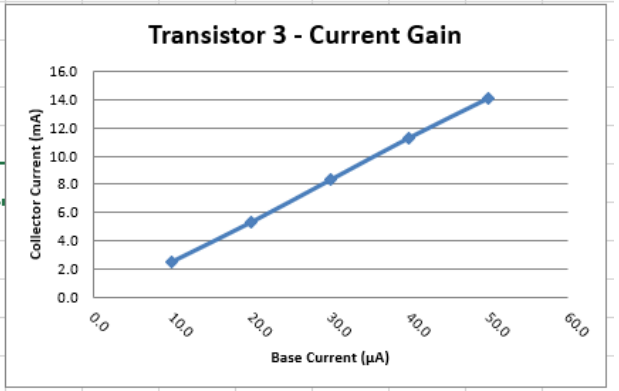
Transistor 2

Part #	Package Sketch	Package Designation	Diode Drawing	NPN or PNP?	Barrier Voltages V_{BE}	Barrier Voltages V_{BC}	Test Circuit I_B (µA)	Test Circuit I_C (mA)	HFE Calc	HFE Meas	Error %
2n3904		TO-92		NPN	0.681	0.663	10.0	1.0	101	248.0	59.27%
							20.0	4.9	245		1.21%
							30.0	7.3	243.333		1.88%
							40.0	9.6	240		3.23%
							50.0	11.9	238		4.03%



Transistor 3

Part #	Package Sketch	Package Designation	Diode Drawing	NPN or PNP?	Barrier Voltages V_{BE}	Barrier Voltages V_{BC}	Test Circuit I_B (µA)	Test Circuit I_C (mA)	HFE Calc	HFE Meas	Error %
MJE2955T		TO-220		PNP	0.611	0.610	10.0	2.5	250	265.0	5.66%
							20.0	5.3	265		0.00%
							30.0	8.3	276.667		-4.40%
							40.0	11.3	282.5		-6.60%
							50.0	14.1	282		-6.42%



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