Christopher Bannon

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Education

University of California, Berkeley — GPA: 3.72 **Aug 2020 – Present**
B.A. in Computer Science *Berkeley, California*

Coursework: UI/UX Design & Development, Data Structures, Algorithms, Computer Architecture, Operating Systems, Discrete Math & Probability, Data Science, AI, Machine Learning, Digital Design & Integrated Circuits

Experience

UC Berkeley EECS — Undergraduate HCI Researcher **Sep 2023 – Present**

- Experimented with functional bio-materials to create sustainable electronics and decomposable interactive systems
- Grew **conductive mycelium** and programmed microcontrollers for use in low power sensing/broadcasting applications

UC Berkeley EECS — Undergraduate Student Instructor (CS160) **Jun 2023 – Present**

- Organized scope, sequence, and delivery of instruction on **HCI**, **UI/UX**, **web dev**, and **product design**
- Developed a python script to automate staff Airtable-to-email logistical workflow saving **10**% of TA hours
- Critiqued **200**+ assignments/projects and received a **9.4/10.0** approval rating for **teaching effectiveness**

FavorX — Software Engineer Intern **May 2023 – Aug 2023**

- Collaborated closely with the design team to polish **user-centric** interfaces and deploy solutions in **React Native**
- Scaffolded a **scalable** service using Expo's API to upload profile pictures to a **secure url** in an **AWS S3** bucket
- Implemented and refined user's 'transfer tokens' flow; used **redux** to **integrate firebase** with the **backend API**, resulting in **improved** asynchronous efficiency and state management

Computer Science Mentors — Senior mentor (CS61B) **Jan 2022 – Jan 2024**

- Lead a weekly comprehensive review session for a group of 61B students; rated **9.2/10.0** for **teaching effectiveness**
- Hosted monthly conceptual workshops for up to **80** 61B students on **java**, **data structures**, and **algorithms**

Projects

RISCV CPU with Audio Synthesizer — *Verilog, C, Python*

- Designed and implemented a 3-stage pipelined RISC-V CPU with integrated UART for tethering, using Verilog
- Integrated audio and IO components to the CPU system, via memory mapping, to create a functional audio synthesizer
- **Doubled** clock speed to **100MHz** by adding pipeline stages, smart forwarding, and BTFNT branch prediction

NYT Connections API — *Python, SQL, Django*

- Engineered a **RESTful API** with **Django** and **SQLite** that provides data from The New York Times' Connections game
- Minimized downtime by integrating **Celery** for asynchronous task processing and **Selenium** and **BeautifulSoup** for web scraping

ASCII Sandbox — *React, Typescript, FastAPI* https://github.com/Cbannon35/ASCII-sandbox

- Built a **full-stack** web-app that **leverages Langchain** and **GPT** to query Figlet's API to generate ASCII messages from user's text input for Calhack's AI Hackathon
- Migrated development to **Svelte** and transitioned to client-side data fetching to improve performance

Skills

Computer Languages: Python, C, Java, Swift, HTML/CSS, JavaScript, Typescript, RISC-V Assembly, Verilog

Full-Stack Technologies: React, Redux, Svelte, Expo, Tailwind, Bootstrap, FastAPI, MongoDB, SQL, Firebase