Cortex M4-based LPC4300

The first asymmetric multi-core MCU for the industry

EMEA Regional Marketing MCUs

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Product Application Engineer MCUs

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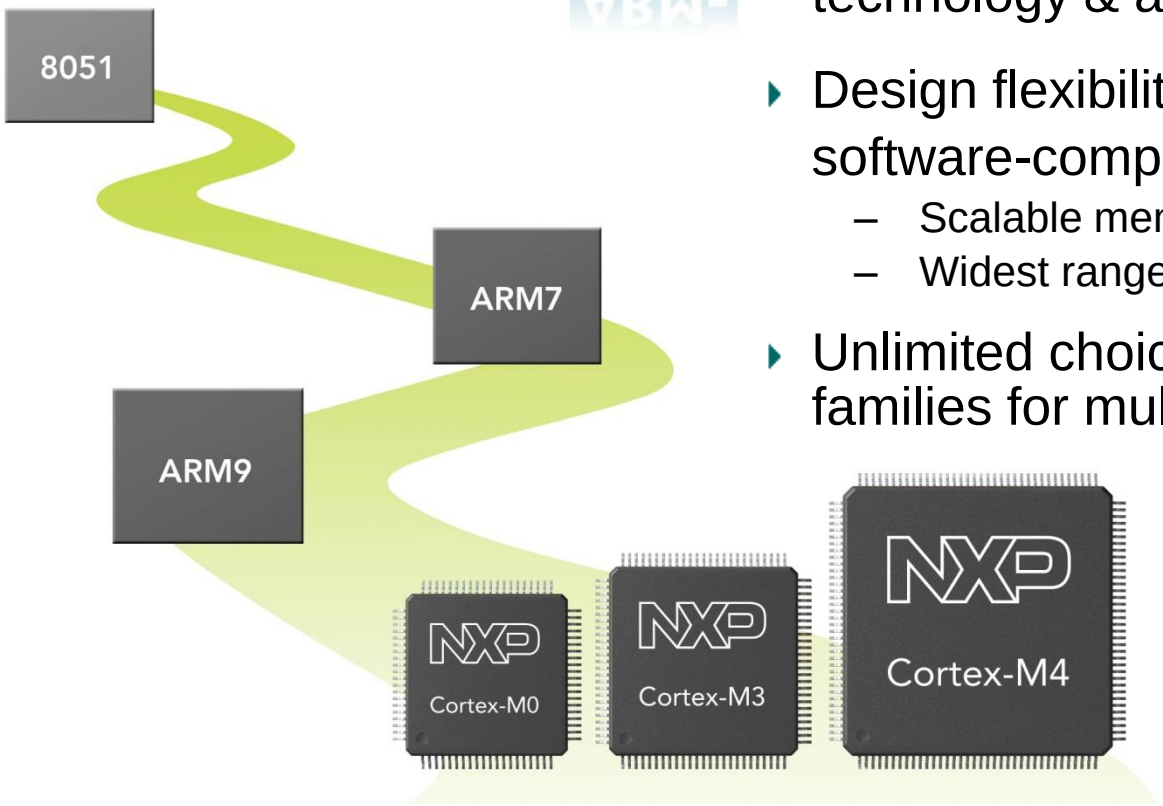
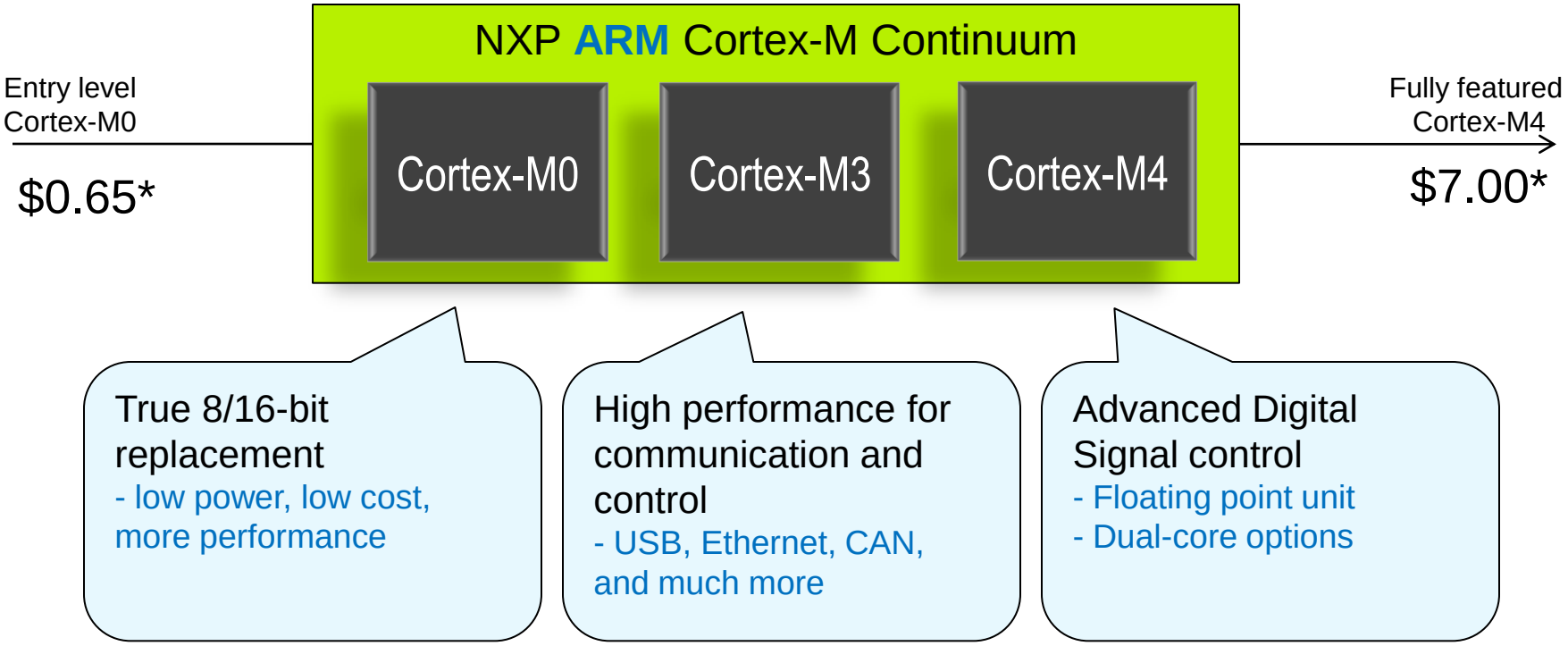
NXP is a leader in ARM Flash MCUs

- Clear strategy: 100% focus on ARM
- Top performance through leading technology & architecture
- Design flexibility through pin- and software-compatible solutions
  - Scalable memory sizes
  - Widest range of peripherals
- Unlimited choice through complete families for multiple cores



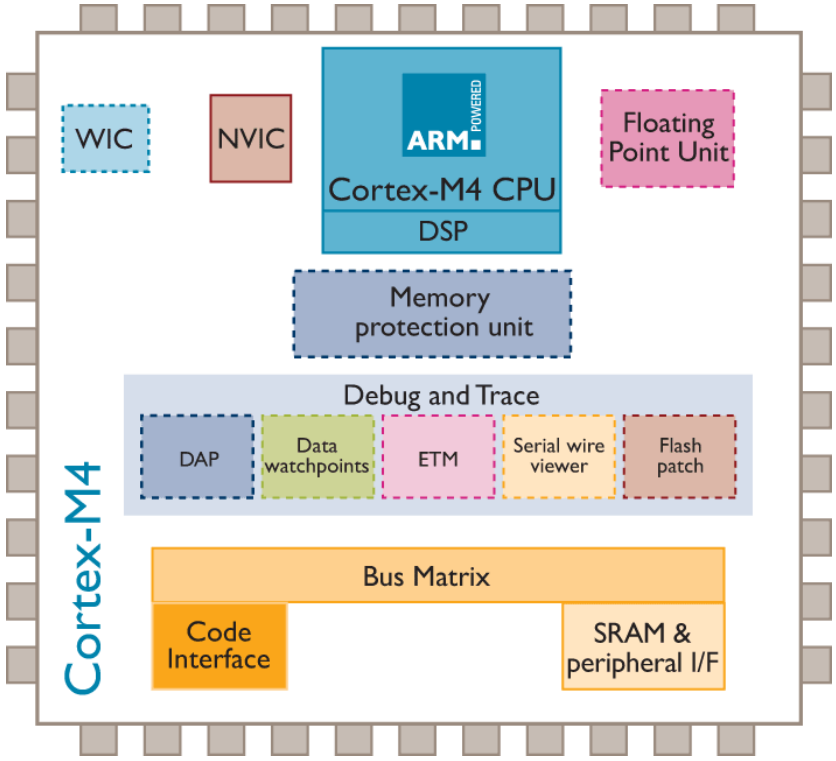
NXP MCU – the only complete ARM range of Cortex-M0, Cortex-M3 and Cortex-M4 processors



Over **250** different ARM based microcontrollers available!!

(Recommended price at 10kpcs)*

Cortex-M4: Digital Signal Controller

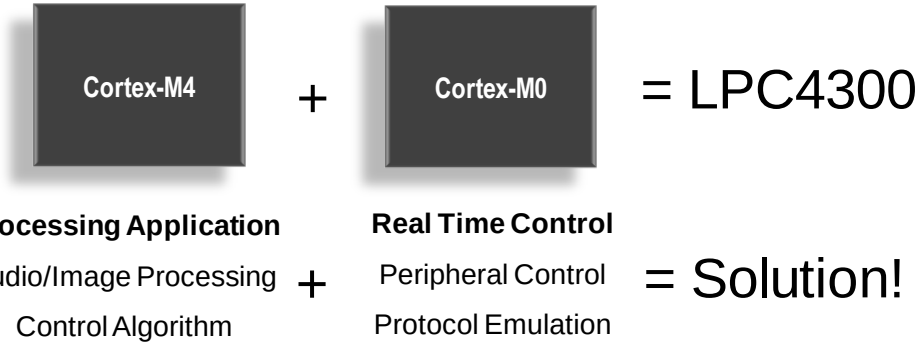


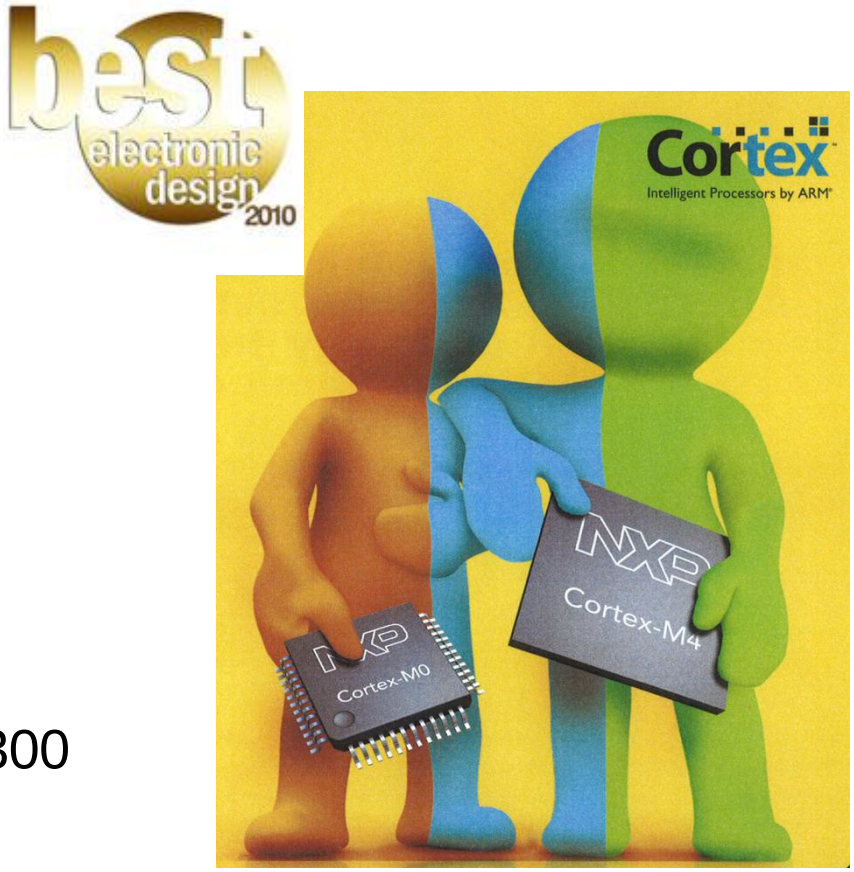
Dotted boxes denote optional blocks

- Memory optimized for Cortex-M4's DSC capabilities
- Adds DSP Extensions to M3
  - Single cycle 16,32-bit MAC
  - Single cycle dual 16-bit MAC
  - 8,16-bit SIMD arithmetic
  - Hardware Divide (2-12 Cycles)
- Adds a Floating Point Unit to M3
  - Single precision floating point unit
  - IEEE 754 compliant
- Can better tackle real-time signal processing algorithms
  - filtering (FIR, IIR)
  - spectrum processing (FFTs)
- Compatible with Cortex-M3
  - Will have an M3 pin-compatible version

Cortex-M4, LPC4300

- NXP Cortex-M4, introducing multi-core processing to microcontroller and DSP applications
  - Cortex-M4 based Digital Signal Controller featuring a highly flexible **Cortex-M0 subsystem**
  - Unique configurable peripherals especially suitable for **motor control**, **solar inverter**, **digital power** and **audio** applications



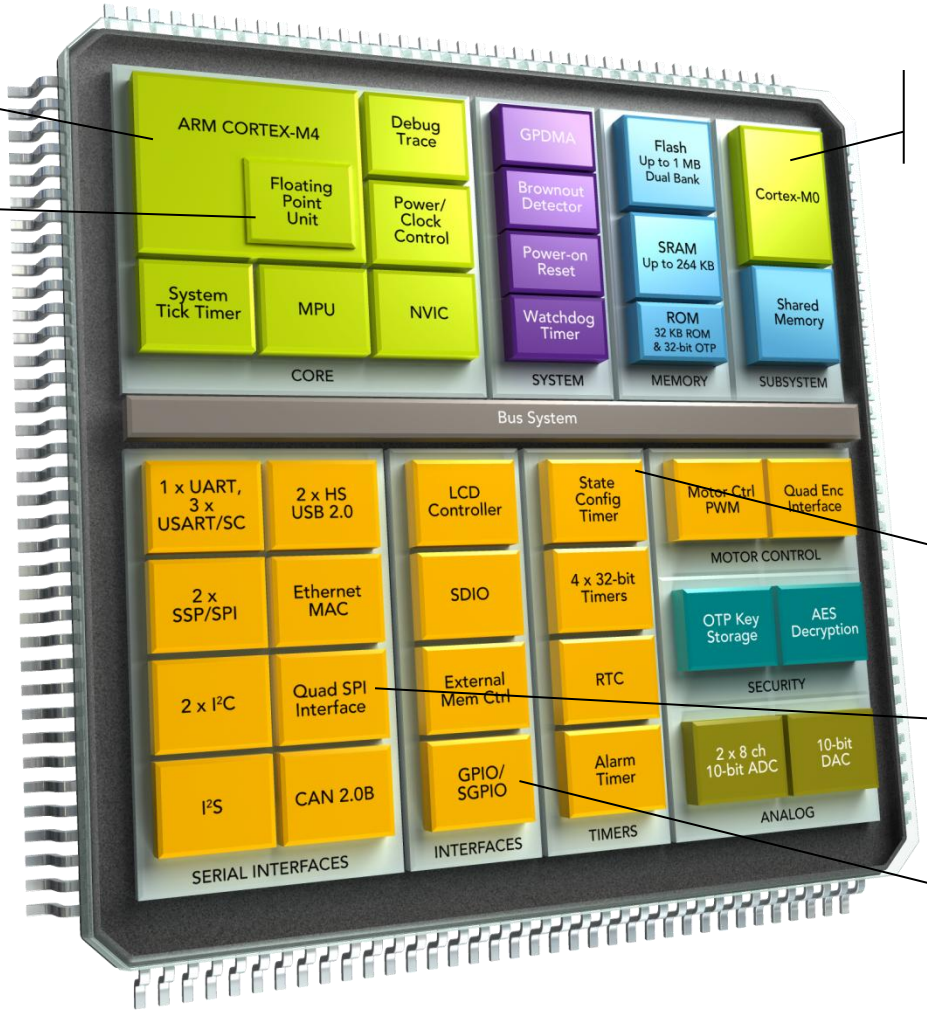


Digital *Multicore* award for NXP LPC4000 dual core microcontroller design

LPC4300

Best-in-class Cortex-M4 performance @ 180MHz

Floating point unit available on all LPC4300 derivatives



Cortex-M0 subsystem for real-time control tasks

NXP Unique

Unique State-Configurable timer system for flexible timer/PWM implementation

Unique Quad SPI flash interface for low-cost memory implementations

Unique SGPIO peripherals to support non-standard serial interfaces

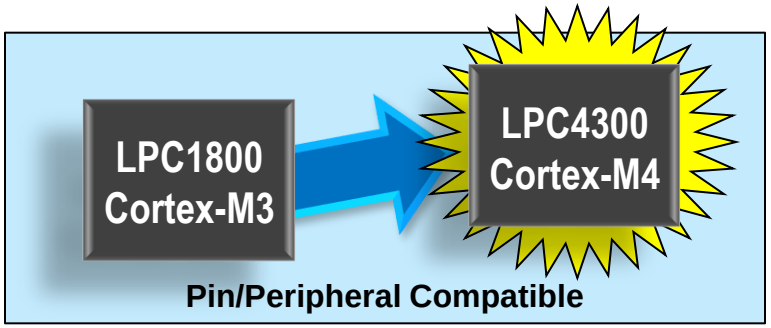
See web: http://ics.nxp.com/products/lpc4000/lpc43xx/

Introducing the LPC4300 Family

LPC4300

CMSIS COMPLIANT
ARM® Cortex™ Microcontroller Software Interface Standard

- Cortex-M4 based Digital Signal Controller
- **Cortex-M0 peripheral sub-system** with dedicated configurable 'smart' I/O and event handling
- Up to **1 MB Flash**
  - Dual-Bank Flash provides safe in-application programming (IAP)
- Large SRAM: up to **264 KB SRAM**
- **SPI Flash Interface** with four lanes and up to 40MB/s data transfer rate.
- State Configurable **Timer Subsystem**
- Serial GPIO (**SGPIO**)
- Two **High-speed USB 2.0** interfaces. An on-chip High-speed PHY
  - 10/100 Ethernet MAC
  - LCD panel controller (up to 1024H × 768V)
  - Two 10-bit ADCs and 10-bit DAC at 400ksps
  - Eight-channel General-Purpose DMA (GPDMA) controller
  - Motor Control PWM
  - Quadrature Encoder Interface
  - 4x UARTs, 2x I2C, 2x I2S, 2x CAN 2.0B, 3x SSP/SPI
  - Smart card interface
  - Up to 146 general purpose I/O pins

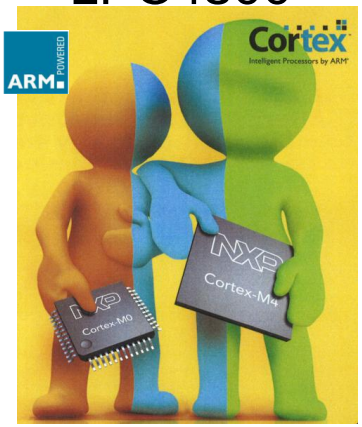


Target Applications: Examples

Industrial Automation

LPC4300

Motor Control

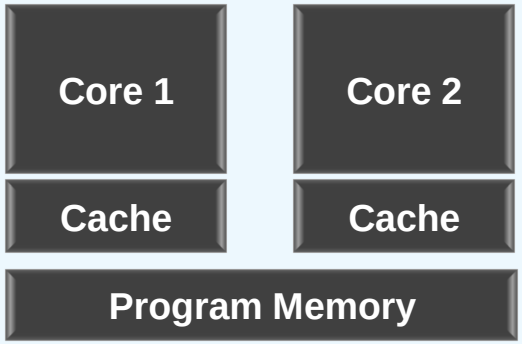
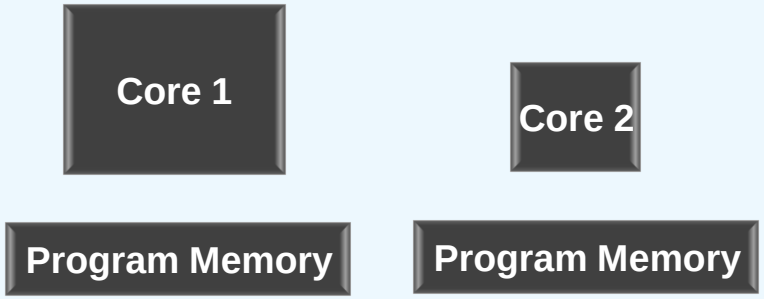


Solar Inverters

Power Management

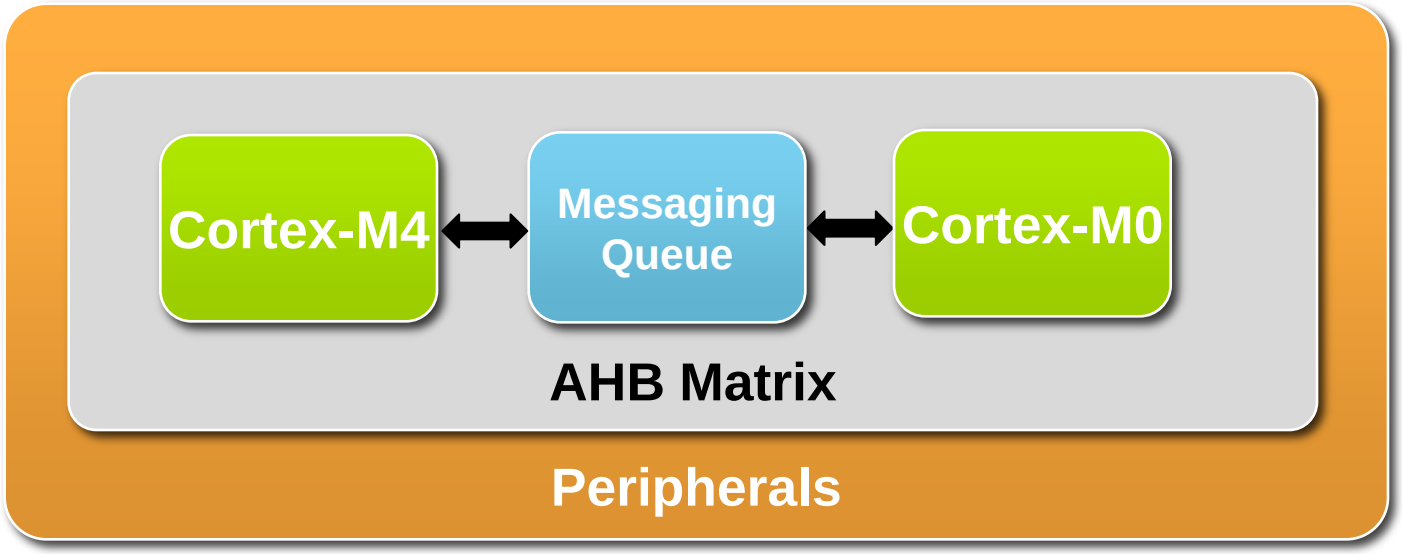
Human Machine Interface

Multi-core: Symmetric vs Asymmetric

Symmetric	Asymmetric
Single application distributed over N processors of the same type.	Each processor runs a different application.
Requires OS support	Specialized OS not required
Shared program memory	Separate program resource per core
	

Cortex-M0 Subsystem: Overview

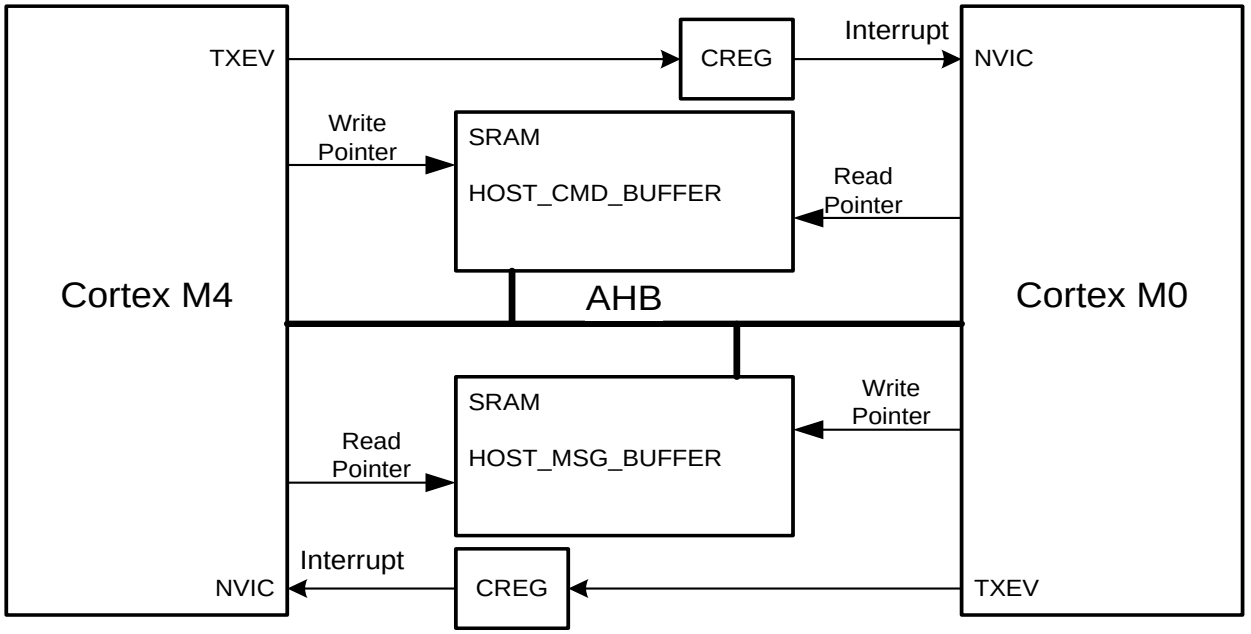
- Highly flexible Cortex-M0 subsystem features
  - Connected to the internal bus matrix giving access to all peripherals
  - NVIC for dedicated interrupt support
  - Separate clock and power control
  - Shared memory allows easy inter-processor communication



Cortex-M0: Inter Processor Communication (IPC)

Rev. A

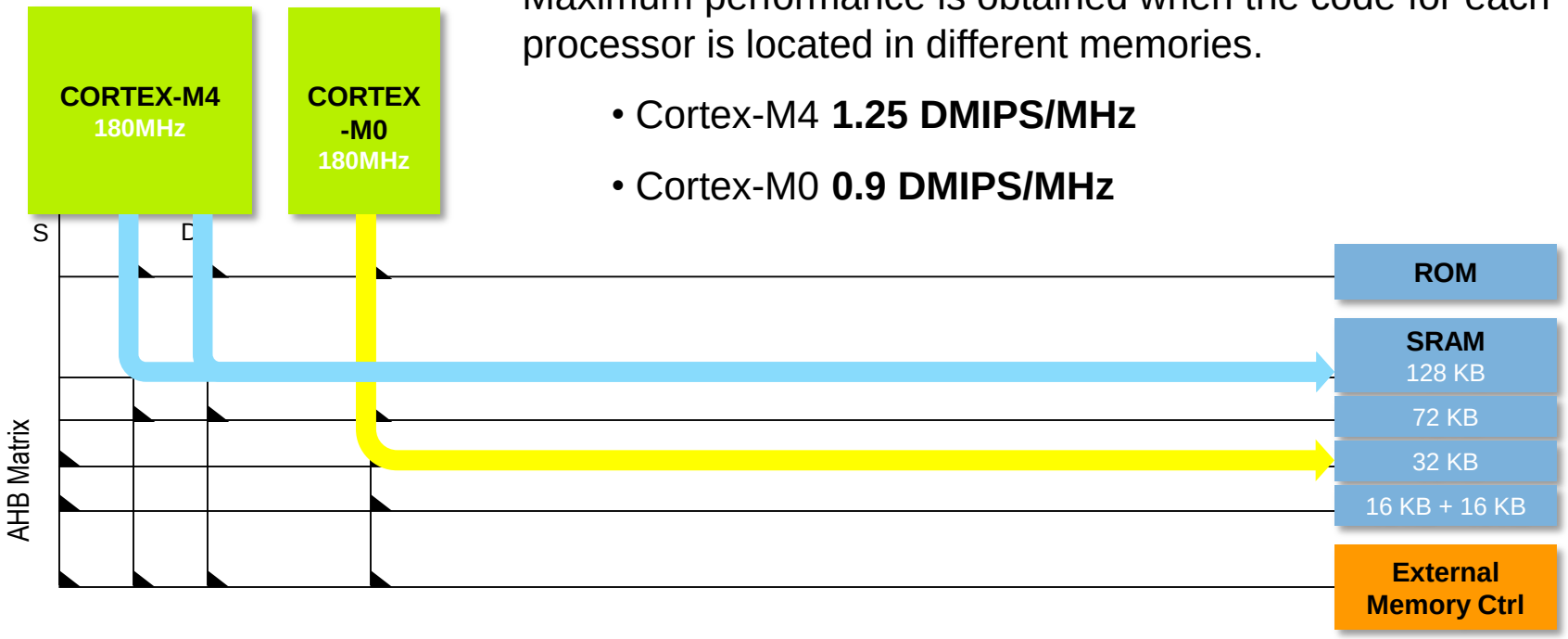
- IPC is implemented in software (ROM based API) using shared RAM
- Interrupt connections are the hardware link



Cortex-M0 Subsystem: Bus Matrix Connections

Maximum performance is obtained when the code for each processor is located in different memories.

- Cortex-M4 **1.25 DMIPS/MHz**
- Cortex-M0 **0.9 DMIPS/MHz**

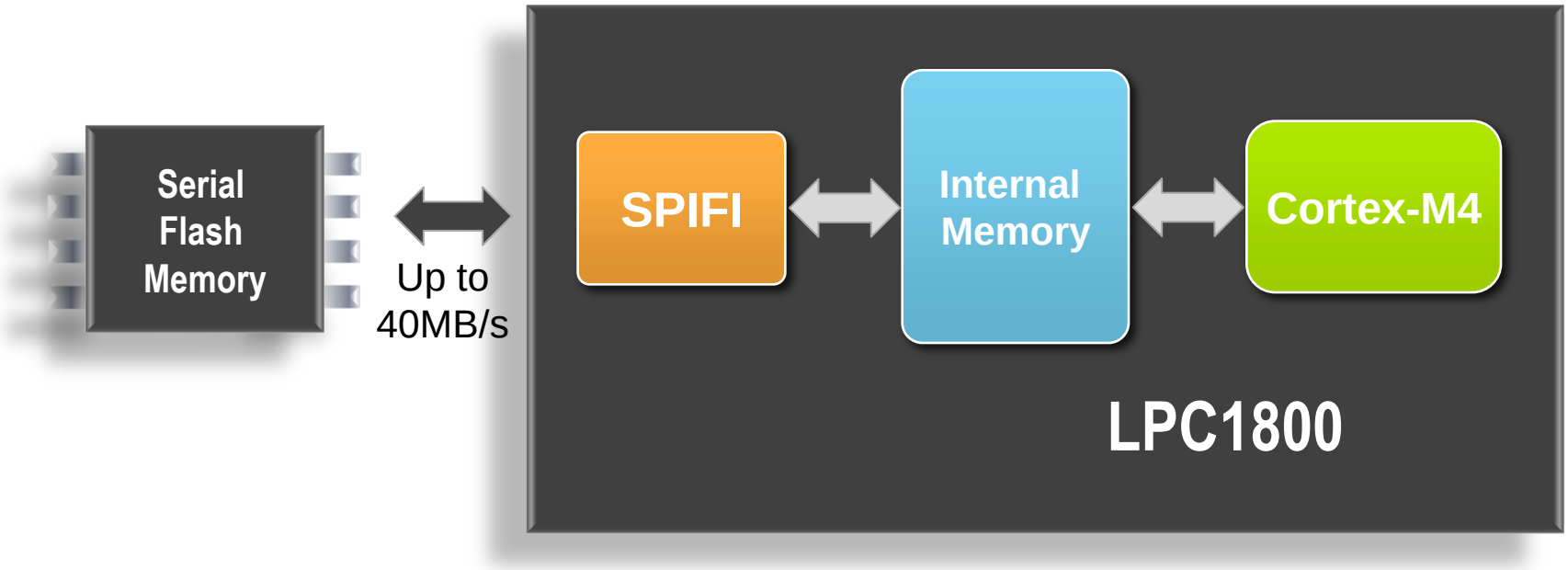


Both Cortex-M4 & Cortex-M0 can run at 180MHz

SPIFI - Overview

LPC1800
LPC4300

SPI Flash Interface



Unique NXP feature that maps low-cost serial flash memories into the internal memory system.

See web: *http://www.eetimes.com/electrical-engineers/education-training/tech-papers/4210512/Eliminating-parallel-serial-tradeoff-in-embedded-systems*

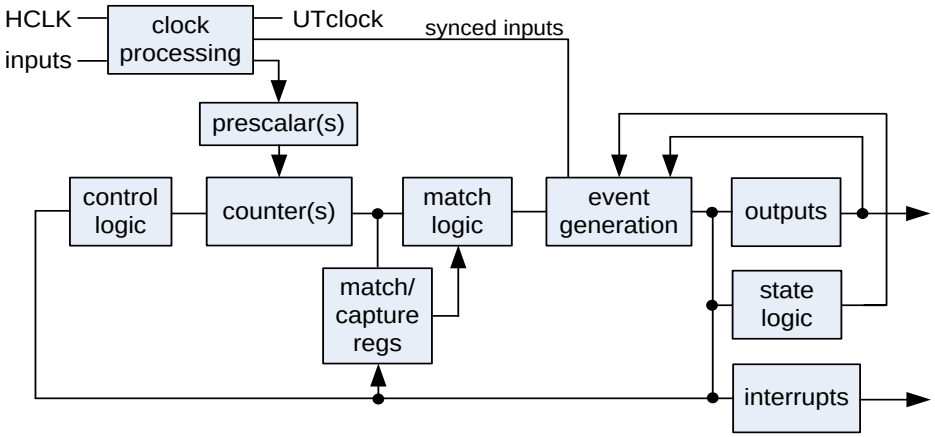
SPIFI: Supported Devices (Rev. A)

Mfg	Device(s)
AMIC	A25L512, A25L010, A25L020, A25L040, A25L080, A25L016, A25L032, A25LQ032
Atmel	AT25F512B, AT25DF021, AT25DF041A, AT25DF081A, AT25DF161, AT25DQ161, AT25DF321A, AT25DF641
Chingis	Pm25LD256C, Pm25LD512C, Pm25LD010C, Pm25LD020C, Pm25LD040, Pm25LQ032C
Gigadevice	25Q512, 25Q10, 25Q20, 25Q40, 25Q80, 25Q16
Macronix	MX25L8006E, MX25L8035E, MX25L8036E, MX25U8035E, MX25L1606E, MX25L1633E, MX25L1635E, MX25L1636E, MX25U1635E MX25L3206E, MX25L3235E, MX25L3236E, MX25U3235E, MX25L6436E, MX25L6445E, MX25L6465E, MX25L12836E, MX25L12845E, MX25L12865E, MX25L25635E, MX25L25735E
Numonyx	M25P10, M25P20, M25P40, M25PX80, M25P80, M25PX80, M25P16, M25PX16, M25P16, M25PX16, M25P32, M25PX32, M25P64, M25PX64, N25Q128
Spansion	25FL004K, 25FL008K, 25FL016K, 25FL032P, 25FL032K, 25FL064P, 25FL064K, 25FL129P
SST	26VF016, 26VF032
Winbond	25Q40, 25Q80, 25Q16, 25Q32, 25Q64

State Configurable Timer Subsystem

NXP Unique

- **Description:**
  - The State Configurable Timer (SCT) allows a wide variety of timing, counting, output modulation, and input capture operations.
- **Features:**
  - Supports up to 16 outputs for multi-phase complex wave form generation
  - Provides up to 8 inputs for capture



Generate complex waveforms without CPU intervention

SCT - Example Application

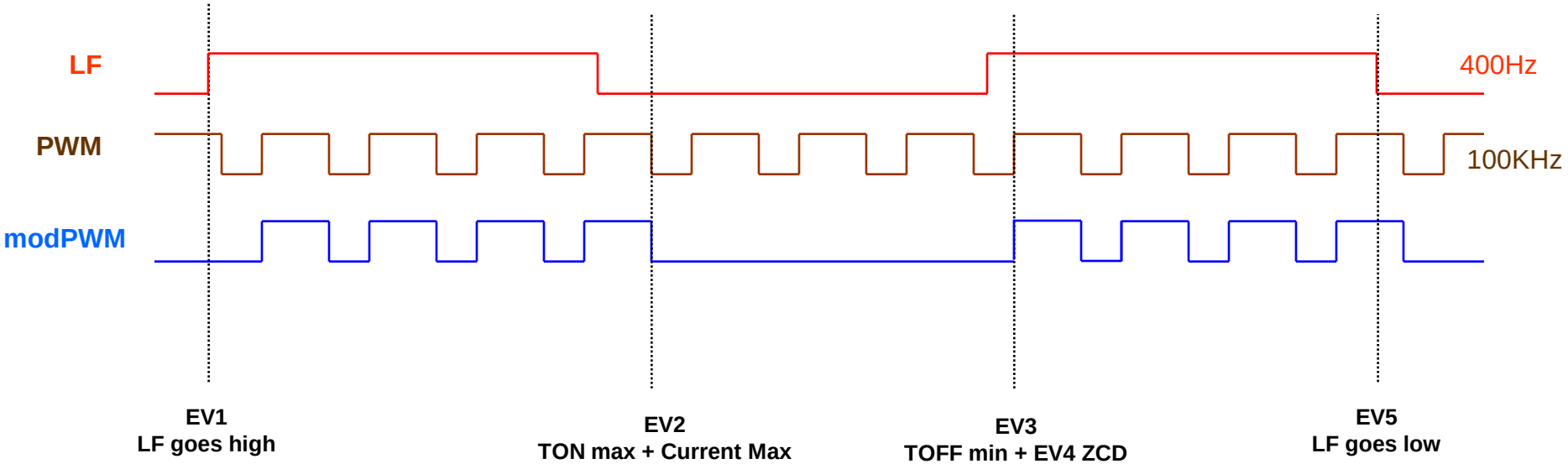
Simple traffic light:

- Five lights (outputs)
- One external button (input)
- Four different combinations (states)

#	Car lane lights	Pedestrian lane lights
1	Green	Red
2	Yellow	Red
3	Red	Red
4	Red	Green

SCT strengths: Low Latency

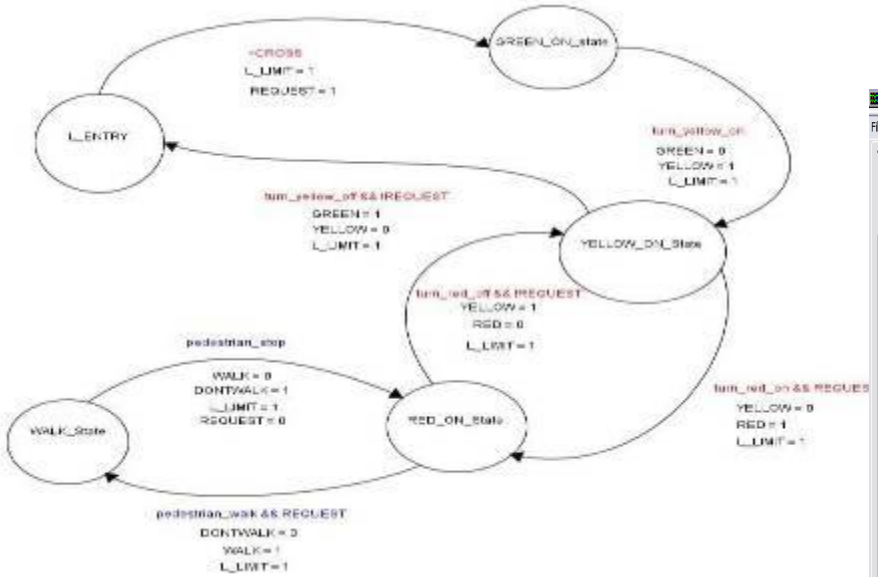
- Can run up to the CPU speed
  - High resolution of match points (20 ns @ 50MHz)
- Can react to input signals without CPU intervention
  - Jitter free quick reaction to input signals (40 ns @50 MHz)



SCT – Easy to use

SCT allows this application to be implemented in hardware!

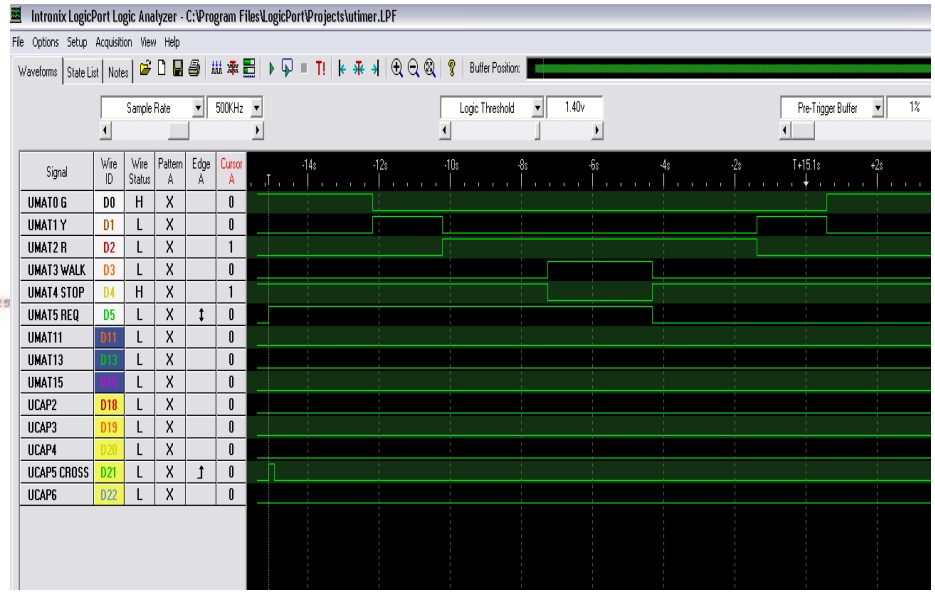
1. Design the state machine



2. Set the registers/timer

```
LPC_SCT->CTRL |= (1UL << 7);
LPC_SCT->TIM   = 0x4534;
LPC_SCT->ENB  &= 0x8001;
```

3. Let the SCT do the work!



Library of examples will be available!

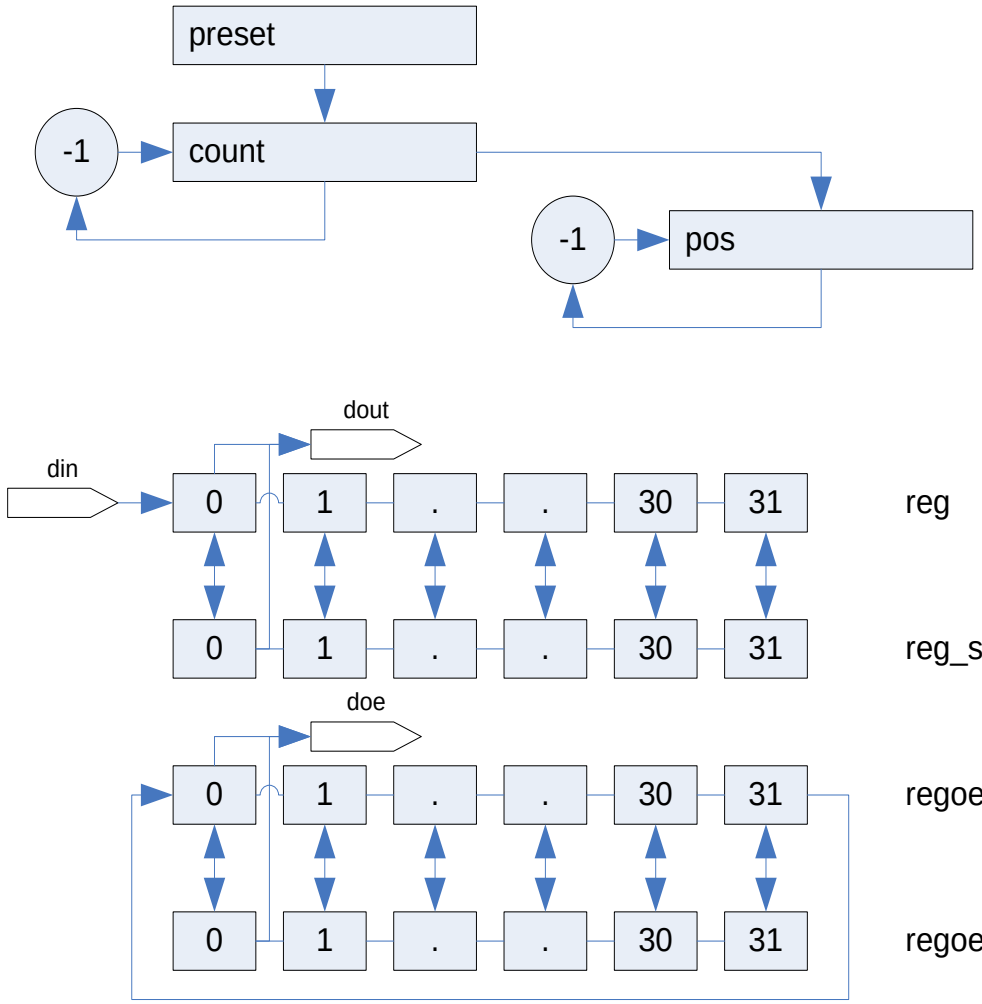
SGPIO - Overview

- Serial GPIO (SGPIO) = GPIO + Timer/Shift Register:
  - Used to create or captures multiple real time serial data streams.
  - No more having to write code loops to manipulate GPIO in real time.
  - **Easily replaces CPU intensive 'bit banging'**
- Key Features:
  - Up to **16 inputs/outputs** each with their own timer/shift register unit.
  - Counter to control the rate at which data is clocked in/out.
  - Counter to control the number of bits clocked out/in.
  - Output has three states high, low, or high impedance.

SGPIO - Operation

Each SGPIO unit features:

- Two 32-bit shift registers
- Counter to control bit rate
- Counter to control number of bits clocked out/in
- Register controls the state (enable/disable) of the output for each bit that is clocked out.

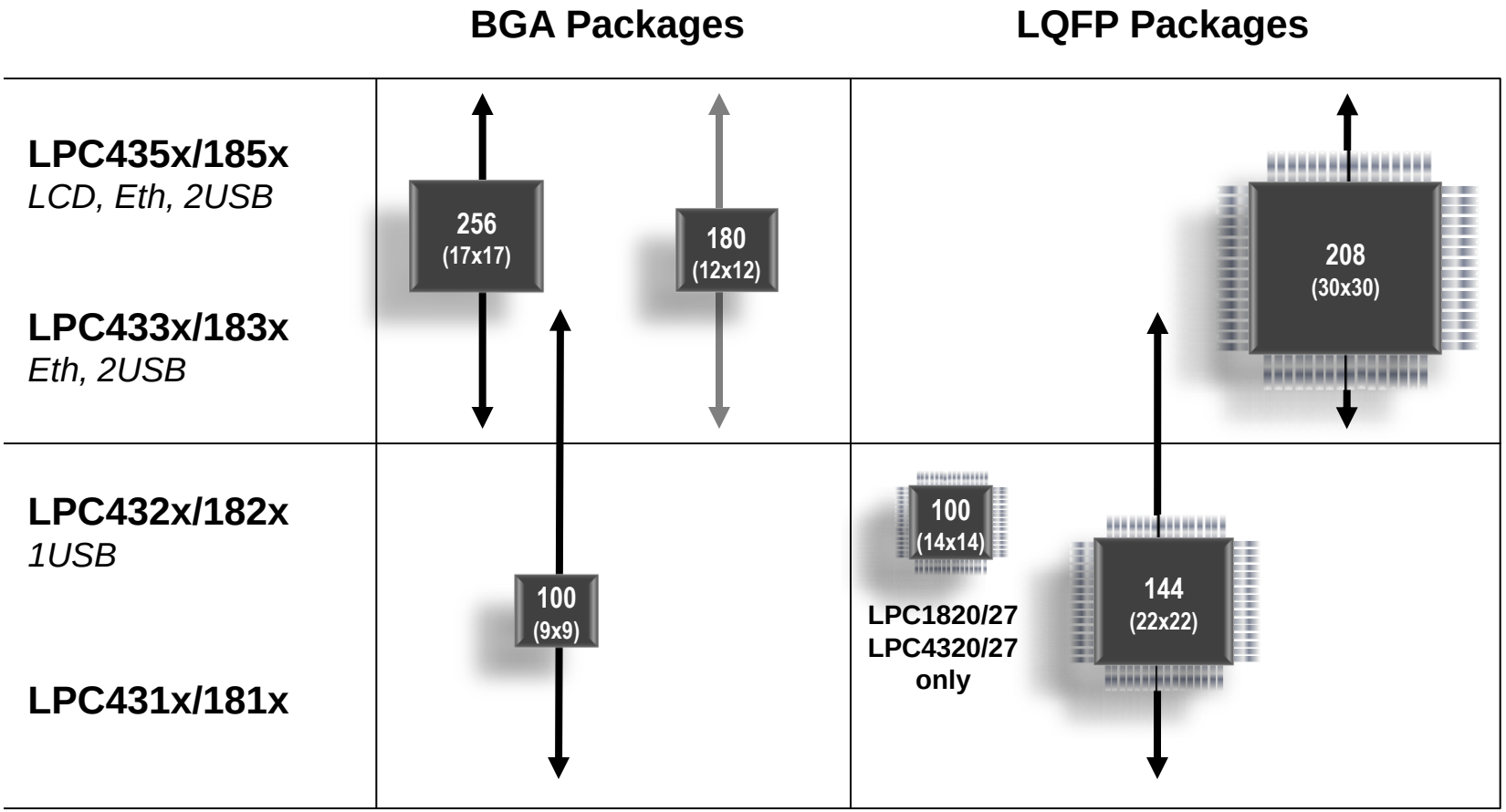


SGPIO = Proprietary Serial Interface

SGPIO can be used to emulate proprietary serial interfaces

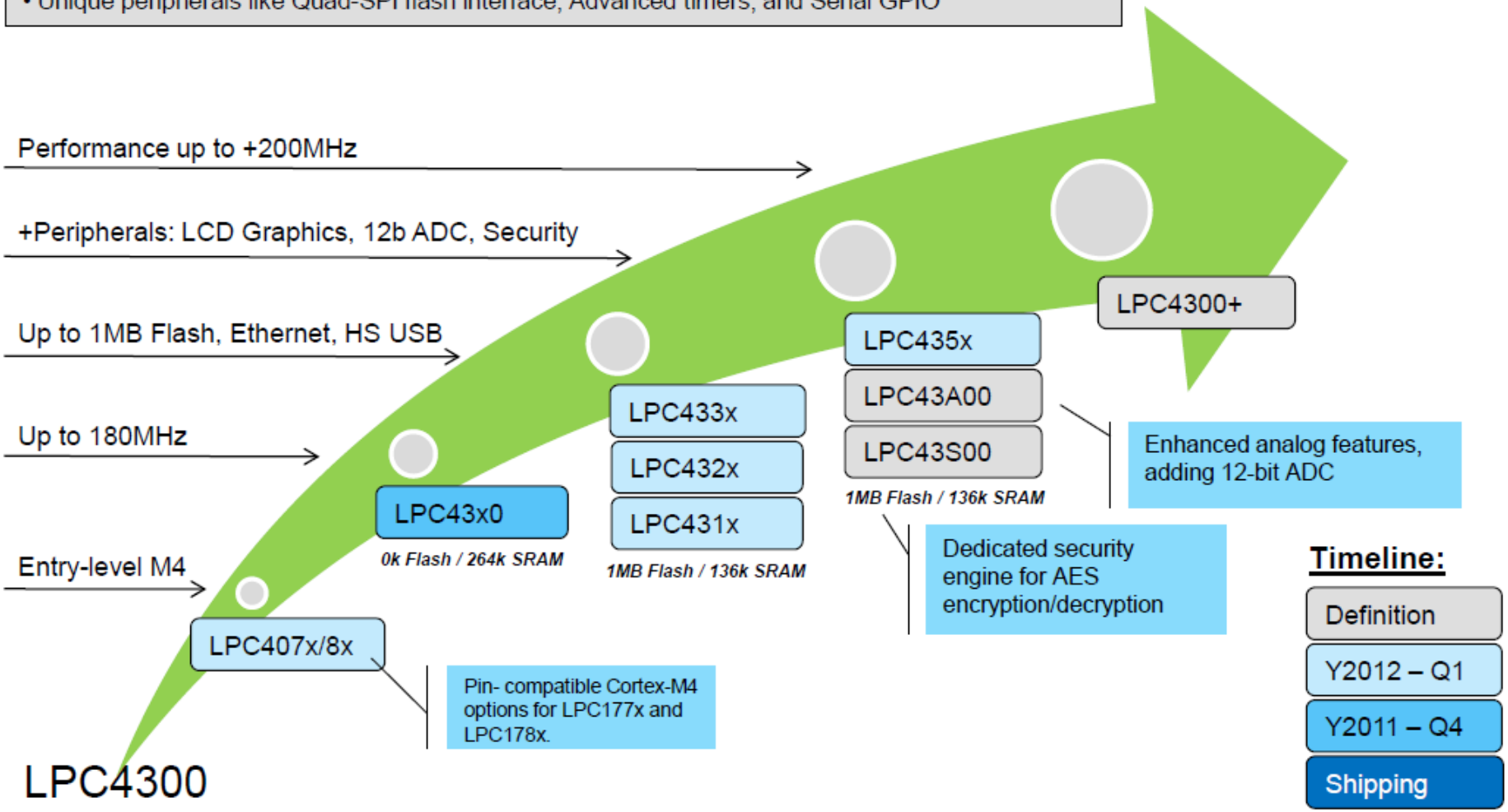
- **Problem:** Lots of peripherals on the market use **non-standard serial interfaces** (LCD drivers, audio codec etc).
- **Standard Microcontroller Solution (no SGPIO):**
  - Application designer has to write CPU intensive loops to create required bit streams – painful bit banging!
  - CPU is 100% occupied while waveform(s) are generated.
- **LPC4300 based Solution:**
  - Configure SGPIO to generate desired waveform(s) with just a few register writes.
  - Interrupt generated when data is clocked out – CPU is not blocked.

LPC1800 / LPC4300 packages



Digital Signal Controllers, first production parts in Q3

- Cortex-M4 including Floating Point Unit, and Cortex-M0 subsystem
- Package options: BGA100, LQFP144, LQFP208, BGA256
- Unique peripherals like Quad-SPI flash interface, Advanced timers, and Serial GPIO



Training, videos, books, and much more

LPCZONE

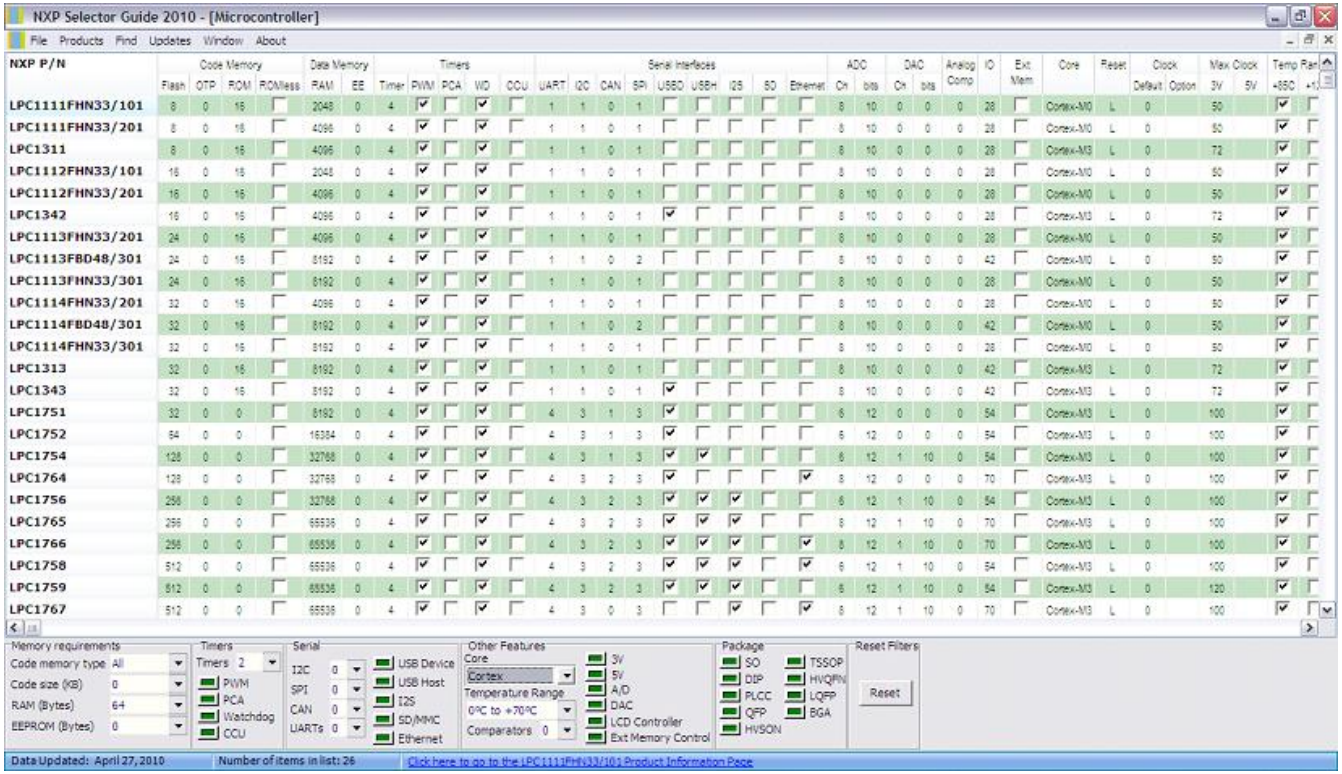
Brochure 2.0 (April 2011)

http://ics.nxp.com/literature/other/microcontrollers/pdf/line.card.cortex-m.pdf

Off-line NXP microcontroller selection guide

- Updated to version V5.6.8.2 on Dec 14, 2010

- http://ics.nxp.com/support/software/selector/



Where to get started?

- www.nxp.com/microcontrollers
  - MCU homepage

- www.nxp.com/lpczone
  - Product updates and training

- www.nxp.com/lpcxpresso
  - Low-cost development

- www.mbed.org
  - Rapid proto-typing

Social media for NXP microcontrollers

twitter LPCZone

http://twitter.com/LPCZone

- Online community for NXP LPC microcontrollers.
- Follow LPCZone and you will have the most up-to-date information on the LPC product families.

YouTube™

http://www.youtube.com/user/LPCZone

- Design videos, trainings, interviews, fun

YAHOO! GROUPS

http://tech.groups.yahoo.com/group/lpc2000/

- More than 9100 registered members (as of Jan, 2011)
- The #1 active Microcontroller user forum on Yahoo!

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