ARM MPU Presentation

Atmel Tech Live

October 2014
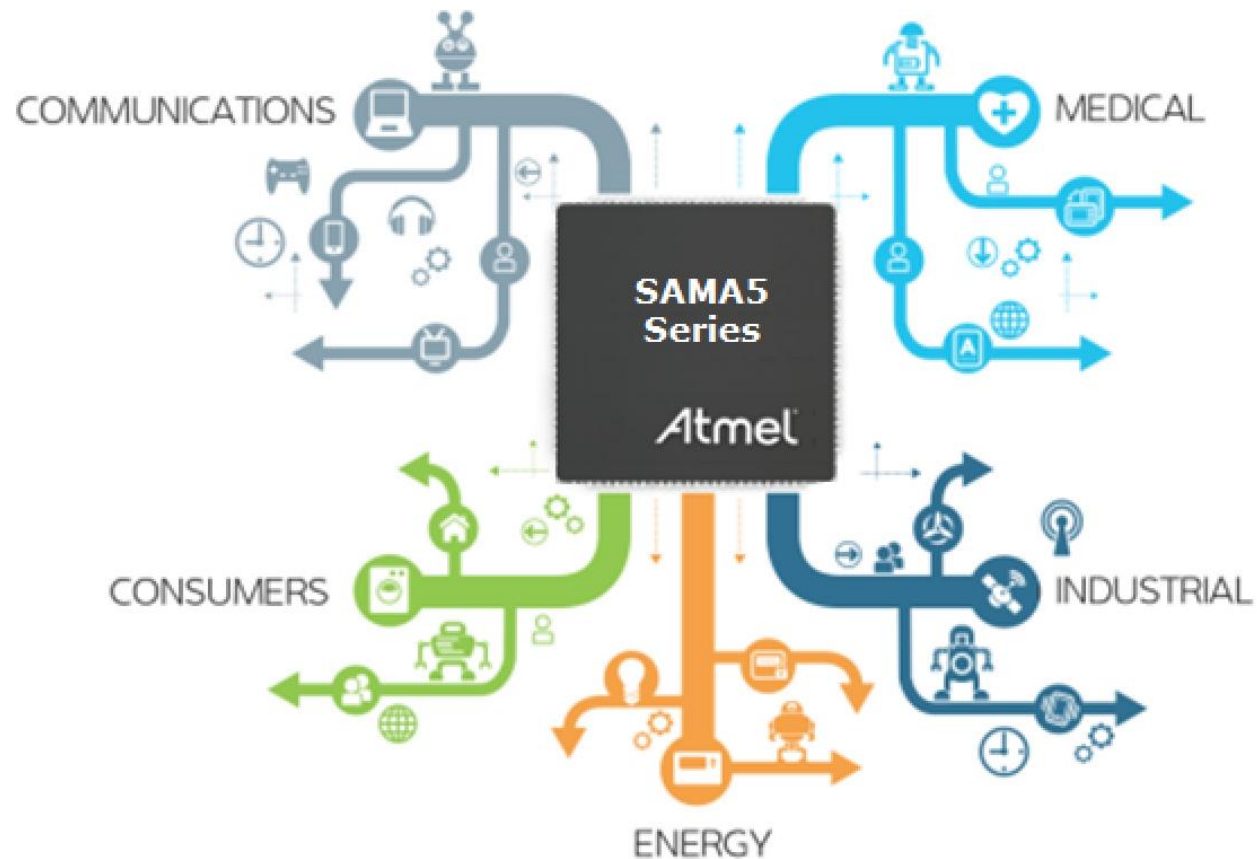
Atmel's ARM MPU history

Driving innovation since 1995

More than 400Mu ARM products shipped in the world…

Revenue

Time

Launch of the SAMA5D4

Launch of low cost MPU Xplained Boards

1st Cortex-A5 based embedded Microprocessor

SAM9N12 Series – ARM9 Entry Level MPU

1st Flash ARM7-based 32-bit Microcontroller

1st ARM9 32-bit Microprocessor

1st Flash Microcontroller

SAM9_5Series with DDR2

First 400 MHz ARM9 MPU

First ARM9 Flash MCU

1995

2002

2004

2007

2008

2010

2012

2013

2014

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Atmel MPU value proposition

- Low Power
  - Market leader with proven architectures

- Ease of Use
  - Low ball count, simple PMIC (power rails), maximum integration, long lifetime, available to the mass market

- Small footprint
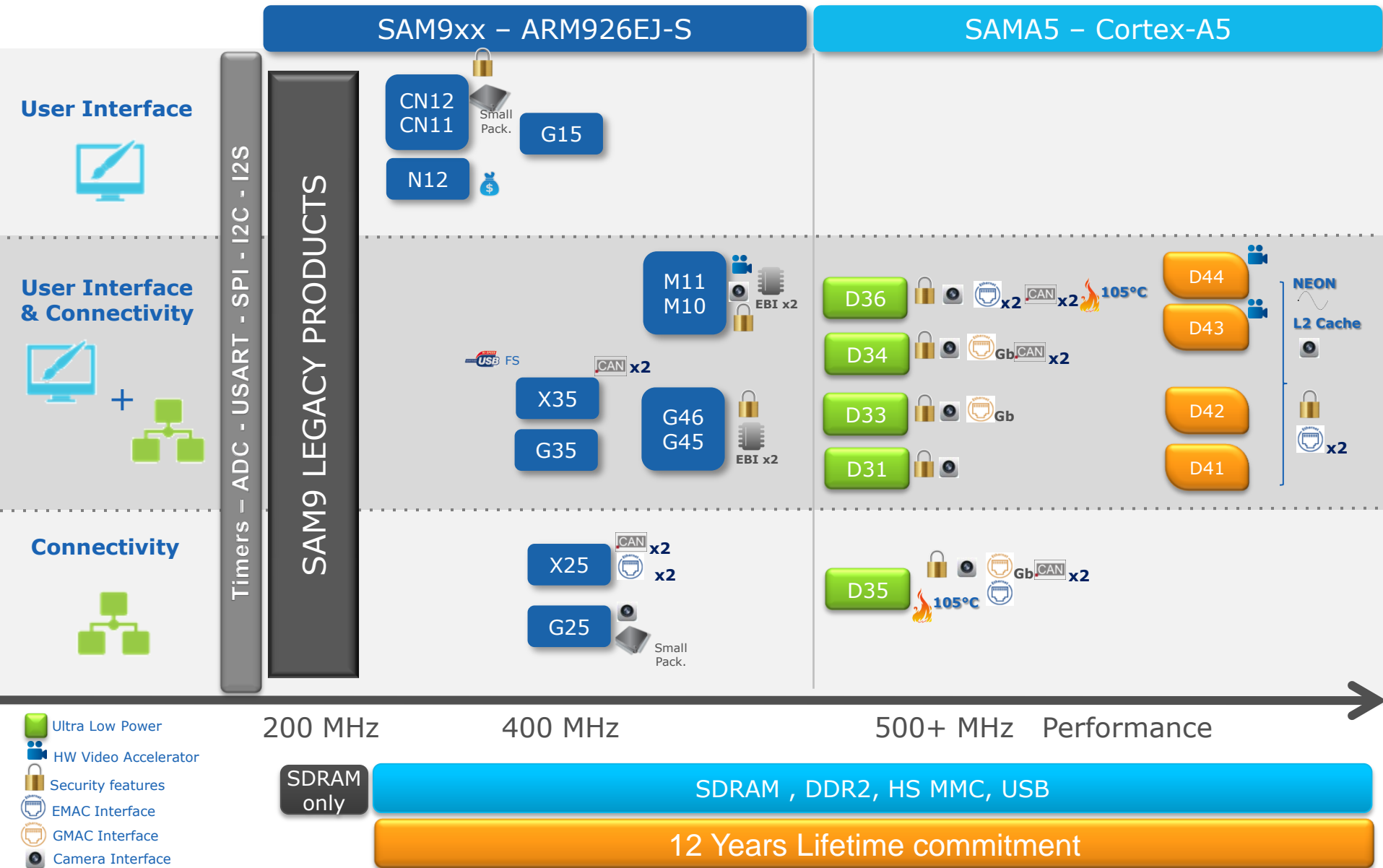 - Using 10X10 12x12 or 15x15 packages size

- Open source SW and HW
  - Schematics, Linux, Softpack, Android, Qt, RTOS

- Product Lifetime commitment from product launch
  - 12 years life time to meet Industrial application needs

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eMPU Product Portfolio

Some Key applications

Industrial/Building Automation

Home control / Thermostats panel

Entry level Industrial HMI

Intercom/ video surveillance

Barcode scanner

Wearables / Battery operated

Data concentrator/Smartgrid Gateways

Medical

Biometrics

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Wearable (Smartwatches, Portable Fitness)

- Market-leading low power
  - lowest active power consumption (<150mW at max speed)
  - ultra- low power with fast wake-up (<0.5mW)
- 0.5mm pitch 12x12 BGA package
- High integration, including
  - up to 3 USB HS hosts with PHYs
  - ADC for battery monitoring and resistive touchscreens
  - I2S audio support, and multiple SDIO interfaces
- LPDDR and LPDDR2 support

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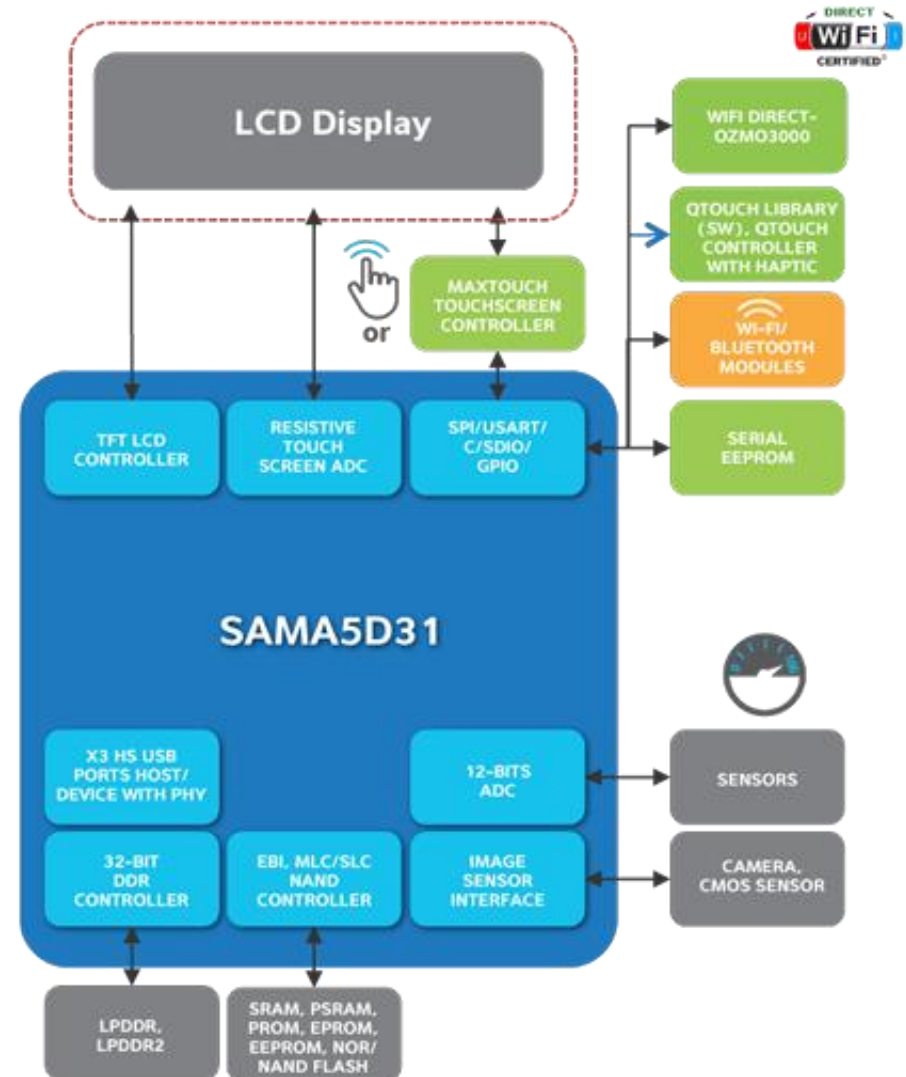
HMI/Control Panel
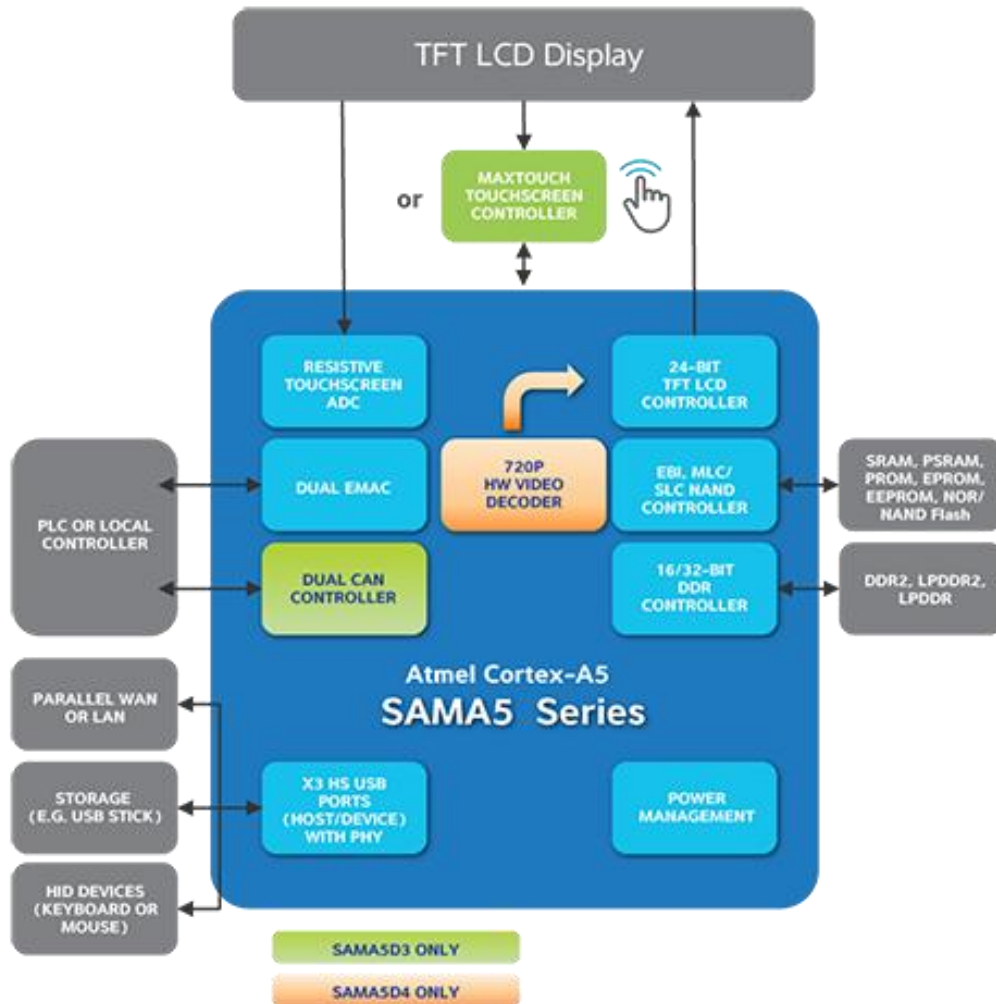
- Powerful ARM Cortex-A5 with Neon/vFPU and L2 cache for graphic accelerations

- 16/32-bit DDR memory interface delivering the data bandwidth to achieve high screen resolution and complex animation

- 720p Hardware Video Decoder to playback H264, VP8 videos

- 24-bit TFT LCD controller with overlays supporting up to XGA resolution

- Free Linux® distribution with OpenMax/Gstreamer, Qt SDK, free Android™ port, as well as other popular GUI

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IoT Secure Gateway

- Extensive communication peripherals include

    - Dual 10/100 Ethernet MAC with IEEE1588 real-time stamping

    - 3x HS USB ports, up to 7x UARTs, SPIs, I2Cs, SDIOs and more

- ARM Cortex-A5 core delivering up to 850 DMIPS with multiple DMAs

- Powerfull encryption engines supporing public key algorithms (RSA, ECC)

- Software protection with on the fly DDR encryption/decryption and secure boot, and tamper detection with secret key storage

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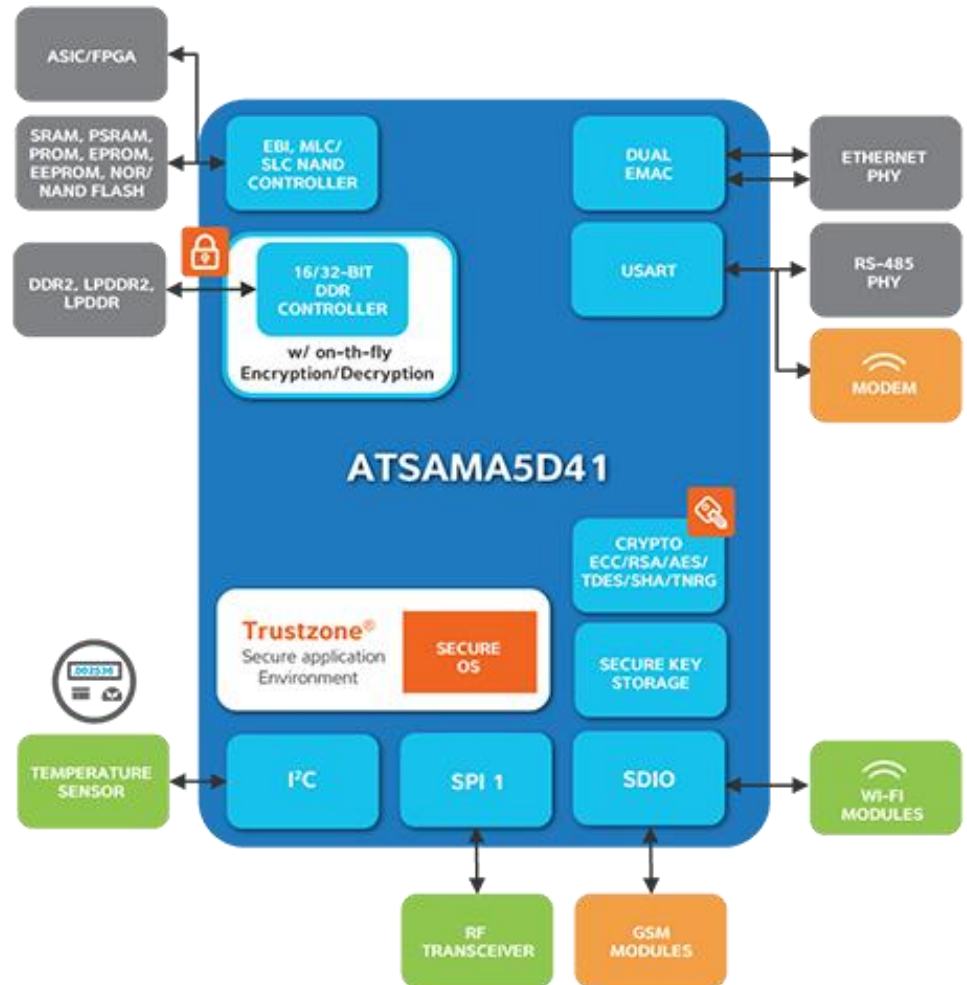
Barcode Scanner
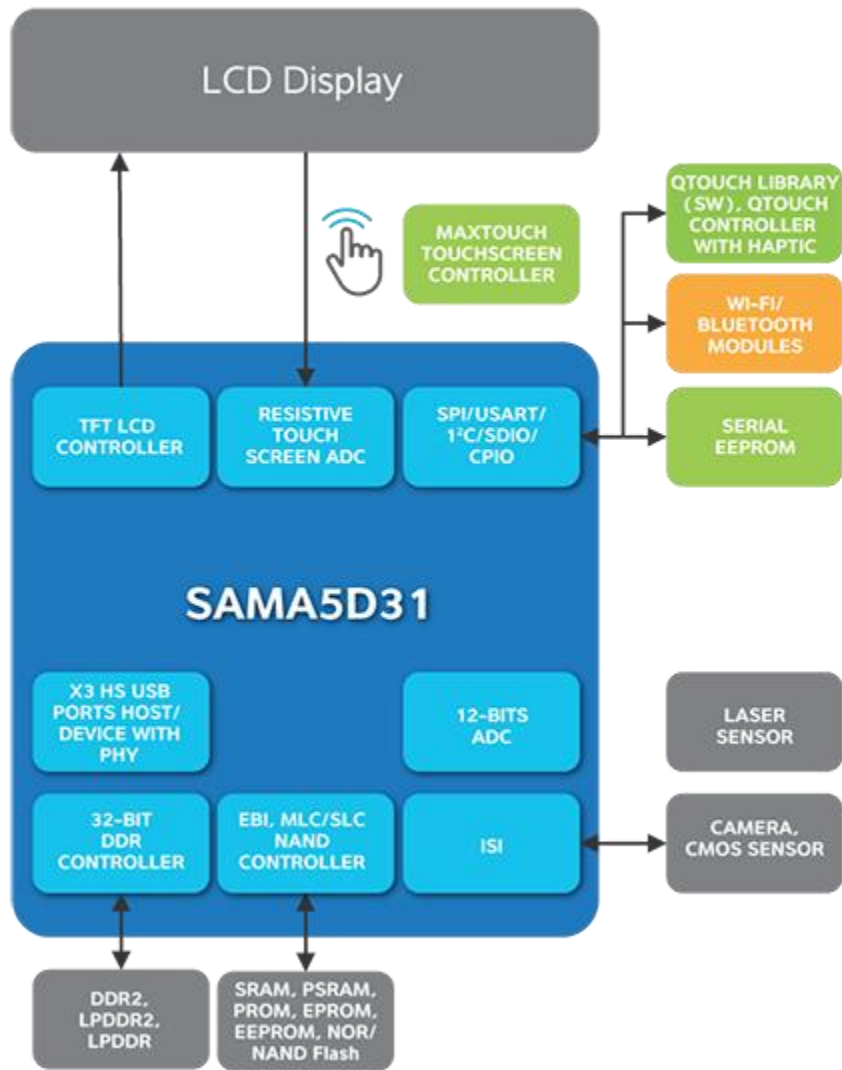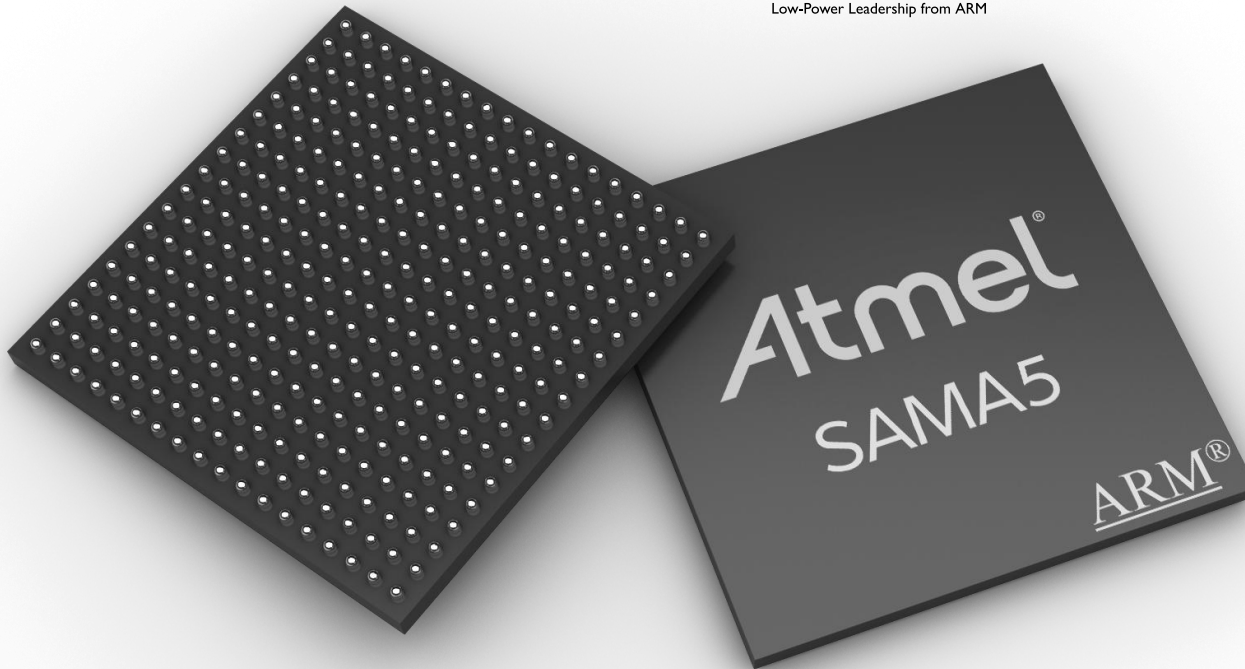

- ARM® Cortex®-A5 core and floating point unit for accelerated image processing

- Power consumption less than 150mW at 536MHz operation

- Compliant to USB suspend mode consumption target

- Seamless connection to CMOS sensors through the Image Sensor Interface (ISI)

- 12x12mm BGA324 package (0.5mm pitch) accomodates limited board space

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SAMA5 Series, ARM Cortex-A5 based

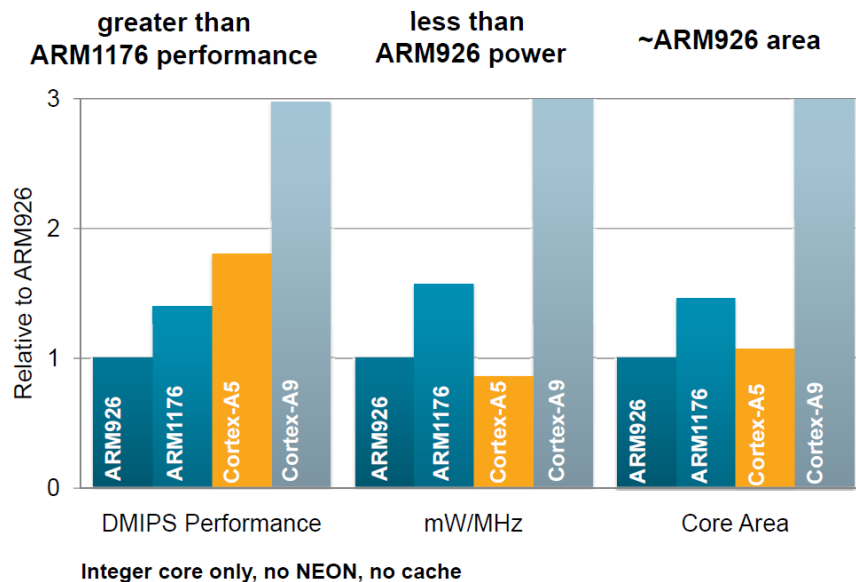Atmel Tech Live, Asia 2014   Oct 2014

ARM Processor comparison

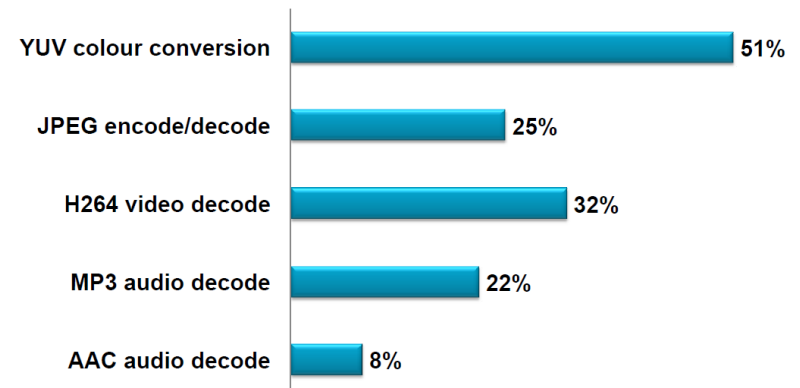## Cortex-A5 core is still best-in-class solution for Power efficiency

- SAMA5D3 the lowest power ARM MPU in the market
  - Best-in-class solution for Power efficiency
  - All competitors use high performance transistors penalizing power consumption (not the case on SAMA5)

- The SAMA5D4 performance boosted with NEON Coprocessor + L2 Cache

Cortex-A5 provides…

| greater than ARM1176 performance | less than ARM926 power | ~ARM926 area |

Relative to ARM926

- DMIPS Performance: ARM926, ARM1176, Cortex-A5, Cortex-A9
- mW/MHz: ARM926, ARM1176, Cortex-A5, Cortex-A9
- Core Area: ARM926, ARM1176, Cortex-A5, Cortex-A9

Integer core only, no NEON, no cache

Cortex-A5 NEON uplift over integer

Relative comparison of media algorithms based on OpenMAX DL libraries

Algorithm	Uplift
YUV colour conversion	51%
JPEG encode/decode	25%
H264 video decode	32%
MP3 audio decode	22%
AAC audio decode	8%

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SAMA5D3 vs D4 Comparison Table

	SAMA5D3	SAMA5D4
Max CPU speed	536Mhz	528Mhz
vFPU Neon/L2 cache	Yes No/No	Yes Yes/Yes
DDR support (DDR2/LPDDR/LPDDR2)	32-bit	16-bit/ 32-bit
Active power Static power Back-up power	< 150mW < 0.5mW <2µA	<350mW <10mW <10µA [1]
Video decoder	No	Yes
10/100 EMAC	Gbit w IEEE1588 + 10/100	Dual 10/100 w/ IEEE1588
CAN	yes	No
Cryptography DDR bus encrypted Tamper pin Secure storage ARM Trust Zone	AES/3DES, TRNG, SHA No No No No	AES/3DES, TRNG, SHA, RSA/ECC Yes Yes Yes yes
Temperature	-40/+85°C -40/+105°C	-40/+85°C
Packages	BGA324 (15x15) & (12x12)	BGA361 (16x16) BGA289 (14x14)

(1) Includes 8KBytes SRAM

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Introducing SAMA5 Series

SAMA5D3: Offers rich peripheral set, low power and ease of use

- Cortex™A5 Core
  - Up to 536MHz
  - ARM® VFPU v4

- Low Power
  - Run Mode < 150mW
  - Low-Power Mode < 0.5mW
  - Backup Mode < 2uW

- Industrial Solution
  - Dual CAN
  - Dual EMAC (GMAC w/ IEEE1588)
  - 7 UART, 6 SPI, 3 USB, …..
  - 105°C derivative

- Safety features
  - POR, MMU, SHA, RWP
  - Independent Watchdog, Xtal error detection

- Small Footprint
  - 15x15 or 12x12 packages
  - Available for die business
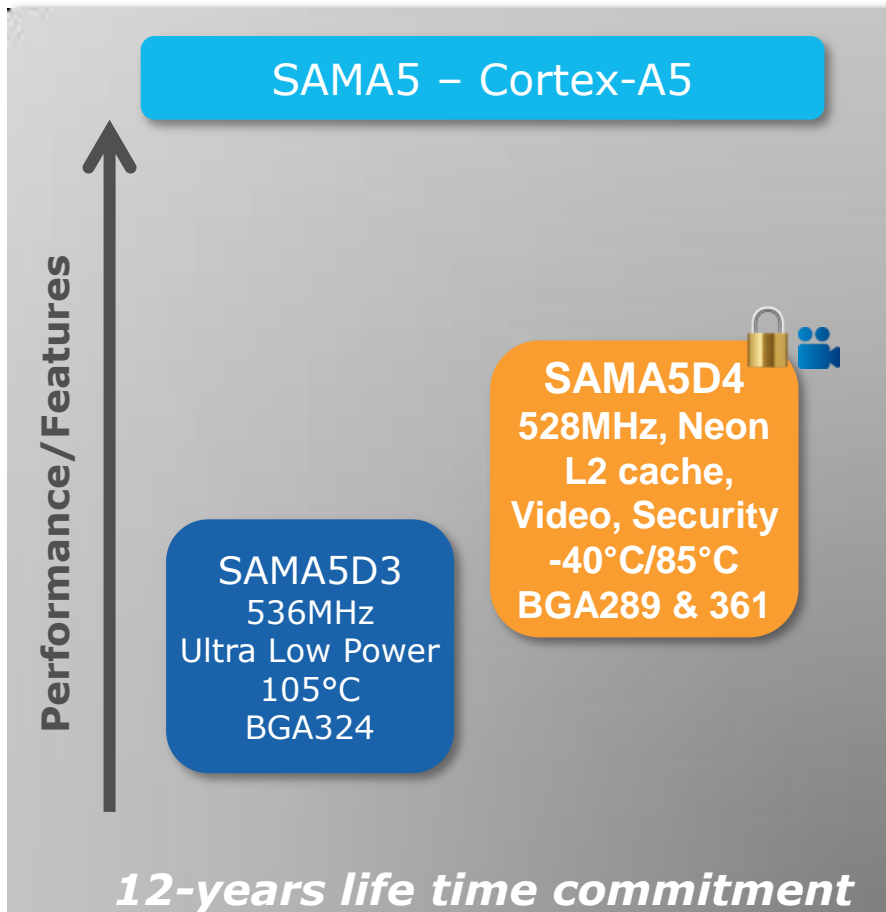
- 12-year Lifetime Commitment

Connectivity
- 3 HS/FS/LS USB port 3 Host or 2 Host+1Dev
- Gigabit EMAC w/ IEEE1588 + 10/100 EMAC
- 2 CAN
- 3 SDIO/SD/MMC
- 7 UART, 6 SPI 3 TWI, Soft modem

Cortex-A5 536 MHz
- MMU
- vFPU
- 2x32KB L1 Cache

System
- 2 RC OSC, 2 xtal OSC, 2 PLL
- Watchdog, POR , RTC
- Backup unit

- 39-ch DMA

Security
- Secure Boot
- HW Crypto AES, TDES, SHA, TRNG

64-bit AXI/AHB

Memory
- DDR2, LPDDR, LPDDR2 controller
- SLC/MLC NAND contr. w/ 24-bit ECC
- External Bus Interface
- 128KB SRAM
- BootROM
- 256 Fuse Bits

Control
- 12-ch 10-bit ADC
- 4 x 16-bit PWM 6 x 32-bit Timers
- 160 IOs

User interface
- TFT LCD Controller w/overlays
- Resistive Touchscreen controller
- Camera Interface, 2 I2S

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Lower Active and Standby Power Consumption

Extended Battery Life and Optimize Power Sensitive Designs

- SAMA5D3 devices are designed to minimize power consumption and leakage currents

PCK = 32KHz Tool Chain: IAR 6.50	Amb. Temp. = 25°C / 85°C SAMA5D3 series
Typical Active Power (Processor Clock/Master Clock) – Coremark Bench	**145 mW / 175 mW** (528Mhz/132Mhz)
Ultra Low Power Mode (SRAM and registers retention)	**0.5mW/ 5mW**
Typical RTC backup current (uW)	**1.4 uW / 1.7 uW**

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What brings SAMA5D4 versus SAMA5D3 ?

Performance/Features

SAMA5 – Cortex-A5

SAMA5D4
528MHz, Neon
L2 cache,
Video, Security
-40°C/85°C
BGA289 & 361

SAMA5D3
536MHz
Ultra Low Power
105°C
BGA324

12-years life time commitment

✓ **Performance uplift**

✓ **720p 30fps Hardware Video Decoder**

✓ **Higher Grade Security**

✓ **16 or 32-bit DDR interface**

- **What is different ?**
  - Not pin compatible with D3
  - Not as low power as D3
  - No CAN, no Gigabit EMAC
  - No 105°C support, no fine pitch
  - Different power scheme

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SAMA5D4 Key Features Overview

SAMA5D4 Block Diagram

Connectivity
- 3 HS/FS/LS USB port 3 Host or 2 Host +1 Device
- 2 EMAC 10/100 w/ IEEE1588
- 2 HS SDIO/SD/MMC
- 8 UART, 8 SPI, 4 TWI, Soft modem

Cortex®-A5 528 MHz
- Trust Zone /MMU
- vFPU/NEON™
- 2x32 kb L1 Cache
- 128 kb L2 Cache

Cortex Intelligent Processors by ARM®

- 42-ch DMA
- 64-bit AXI/AHB

System
- 2 RC OSC, 2 xtal OSC, 2 PLL, Voltage Regulator
- Watchdog, POR, RTC
- Backup unit with 8 kb SRAM

Memory
- DDR2, LPDDR, LPDDR2 Controller
- SLC/MLC NAND Controller with 24-bit ECC
- External Bus Interface
- 128 kb SRAM
- BootROM
- 512 Fuse Bits

Security
- 5-ch 10-bit ADC
- 4 x 16-bit PWM 9 x 32-bit Timers
- 152 IOs

Security
- RSA, ECC co-processor 3DES, AES, SHA, TRNG
- On the fly DDR Encryption/Decryption
- 8x Tamper Pins, Secure Boot

User Interface
- 720p Video Decoder
- TFT LCD Controller with Overlays
- Resistive Touchscreen Controller
- Camera Interface, 2 I2S

	Video Decoder	DDR bus	Packages
SAMA5D41A-CU	—	16-bit	BGA 289
SAMA5D42A-CU	—	16/32-bit	BGA 361
SAMA5D43A-CU	✓	16-bit	BGA 289
SAMA5D44A-CU	✓	16/32-bit	BGA 361

BGA 289 (14x14, pitch 0.8)
BGA 361 (16x16, pitch 0.8)

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720p/30fps Hardware Video Decoder

- Following CODECs are supported:
  - H.264 Baseline, Main and High Profiles (levels 1-4.1) (Youtube…)
  - H263 profile 0 (level 10 to 60)
  - VP8 (versions 0-3) (Google standard)
  - MPEG-4 ASP

- It also decodes JPEG images
  - JPEG Profile Baseline DCT

- Post-Processing engine for image composition :
  - Alpha blending, Color conversion, Scaling, Rotating

- Can decode videos up to 720p (1280 x 720) @ 30fps

SAMA5D4 LCD controller

Background
picture
(Base layer)
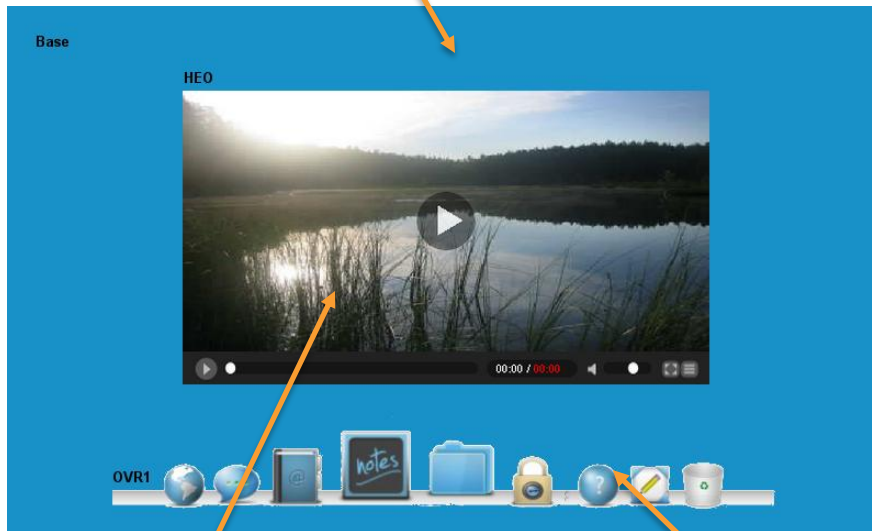
Window with video
(High-end HEO layer)

Dock
(OVR1 layer)

- 720p video format support
  - 1024x768 supported with rotation and resize only
  - Up to 2048x2048 for static image

- High bandwidth dual H64MX master interface

- 4-layer overlay
  - One base layer, two overlay layer windows, one high-end overlay

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Data Processing Increase with ARM® NEON™

- NEON™ is a general-purpose SIMD [1] engine providing powerful acceleration for signal computing including multimedia and graphics

Relative comparison of NEON media algorithms based on OpenMax DL libraries

Algorithm	Value
YUV colour conversion	51%
JPEG encode/decode	25%
H264 video decode	32%
MP3 audio decode	22%
AAC audio decode	8%

Source: ARM
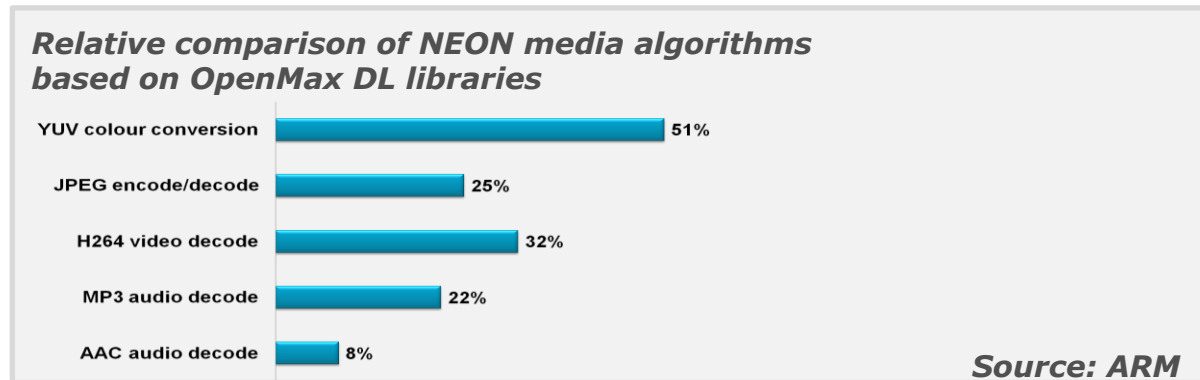
- 75% performance increase compare to SAMA5D3 on FFT [3] algorithms

- Benefits example for image encoding application:
  - H264 codec from ITTIAM[2]
  - SAMA5D4 double the performance compare to SAMA5D3

(1) Single Instruction Multiple Data
(2) see « What's available » for contact details
(3) Fast Fourrier Transform

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SAMA5D4 Advanced Security Features

Anti-cloning, Secure Communication, Software Protection

Advanced security

ARM Trust Zone
Tamper detection
Secret storage
DDR encryption

Secure boot

Medium security

Secure boot

Hardware Crypto engines

RSA, ECC, DSA

Entry level security

Hardware Crypto engines

SHA, TRNG
AES, 3DES

Hardware Crypto engines

SHA, TRNG
AES, 3DES

Hardware Crypto engines

SHA, TRNG
AES, 3DES

SAM9-5 series | SAMA5D3 SAM9CN12 | **SAMA5D4**
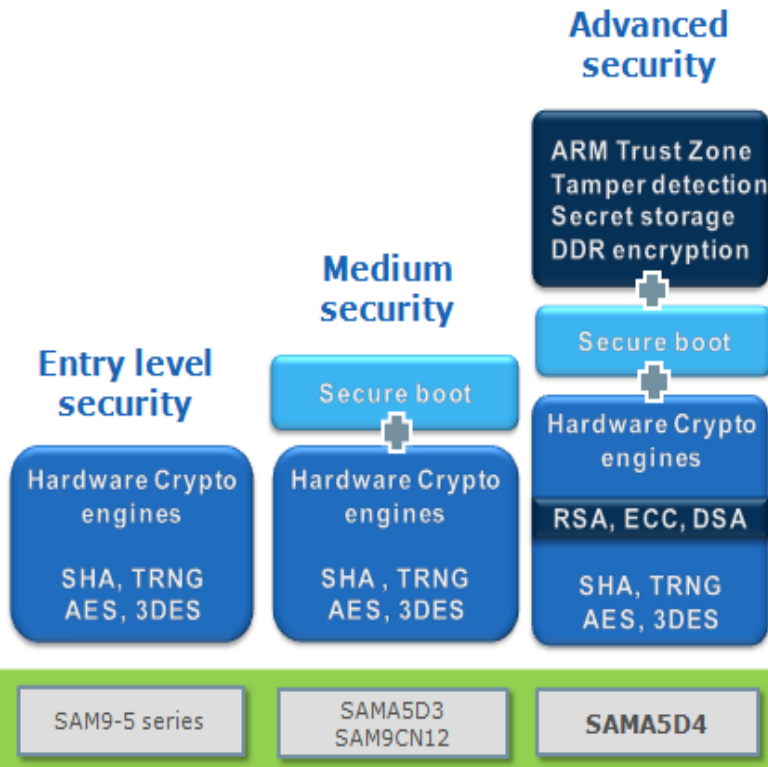
- ARM Trust Zone
- Secure Jtag/Debug
- On-the-fly encryption of external DRAM
- Scrambling on memories
- Secure boot
- Secure key storage
- Tamper pins

- Public Key encryption engines
  - RSA/ECC [1] + Atmel Library
- Private key Encryption engines
  - AES/TDES and TRNG/SHA256

(1) Elliptic Curve Cryptography

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ARM TrustZone® : Application Benefits

Misbehaving applications cannot disrupt or corrupt the system

Rich OS application environment

Normal Rich OS

Secure application environment

Secure OS

Trust Zone monitor

Normal HW ressouces and peripherals

Secure HW ressouces and peripherals

memories
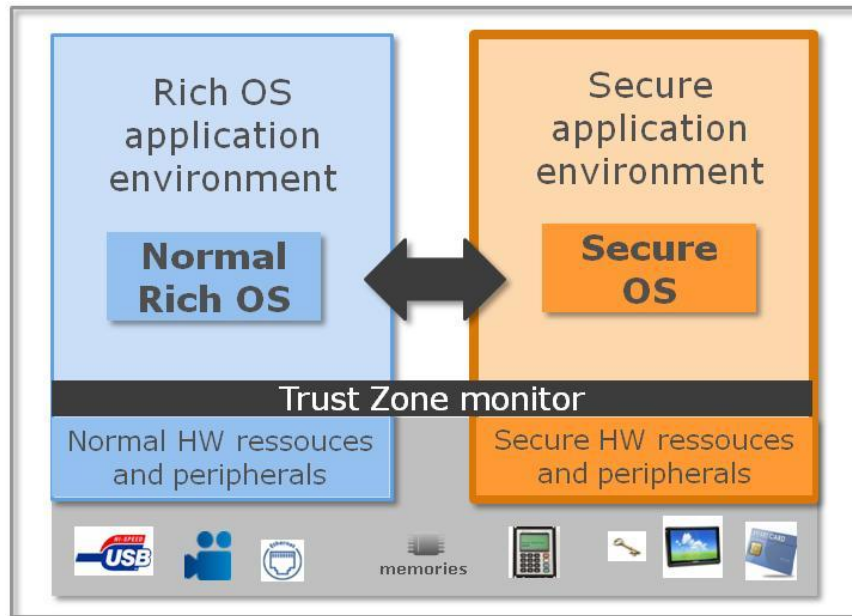
- TrustZone® is a security extension from ARM that allows to isolate safety /security critical software from an OS on the same processor.

- Splits the core in two operating domains
  - Normal domain / Secure domain
  - A monitor manages the switch between the 2 modes

- Enable secure debugging : Different Jtag mode

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Introduction to ARM TrustZone

Why is TrustZone needed?

- Non-TrustZone enabled SoCs are open to hacking in a number of ways:
  - Code and Memory dumping using a JTAG device
  - Privileged modes execution by hacking the ARM Exception Table
  - Entire SoC application can be accessed during development phase allowing passwords stealing and security features hacking

- TrustZone provides the following foundational elements that are essential for hardware-based security:
  - Secure environment separation
  - Secure Interrupts
  - Security aware bus, memories and peripherals
  - Security aware debug

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Introduction to ARM TrustZone

Secure Environment Separation
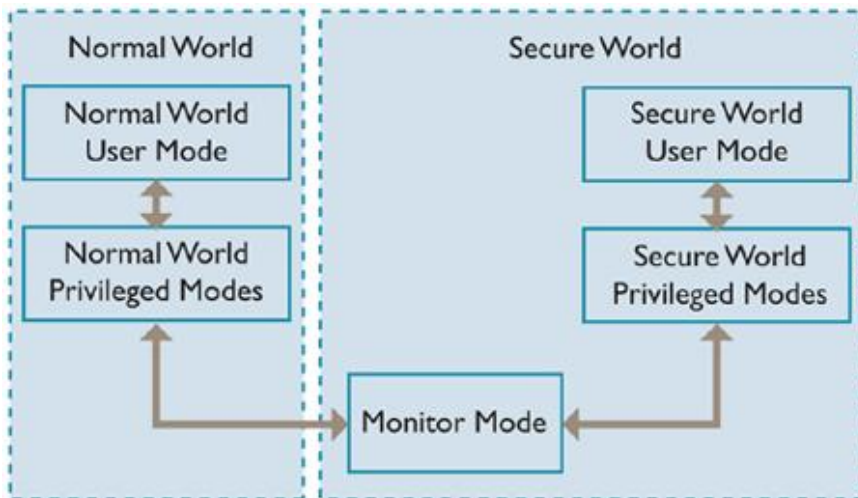
- TrustZone splits processor core into two virtual cores
  - One operating in a Normal World / One in a Secure World

- This mechanism creates another level of execution privilege in addition to the traditional user/privileged modes

- A Secure Monitor Mode is integrated to support moving between worlds
  - SMC (Secure Monitor Call) instruction can be used to enter Secure Monitor Mode

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Introduction to ARM TrustZone

Secure Environment Separation (cont.)

- Each virtual processor has access to its own virtual MMU
  - Secure translation tables are separated in memory with secure access

- Cache memories also have tag bits to distinguish between content cached by either secure or normal world virtual cores

- Security information is propagated on AXI/AHB bus
  - Access to different bus masters in the system can be authorized or not

- Some Memories & Peripherals are secured
  - Only secure masters might be allowed to access certain memories/peripherals
  - A non-secure access to a secure memory/peripheral will abort

- TrustZone provides secure interrupts for interfacing with secure peripherals
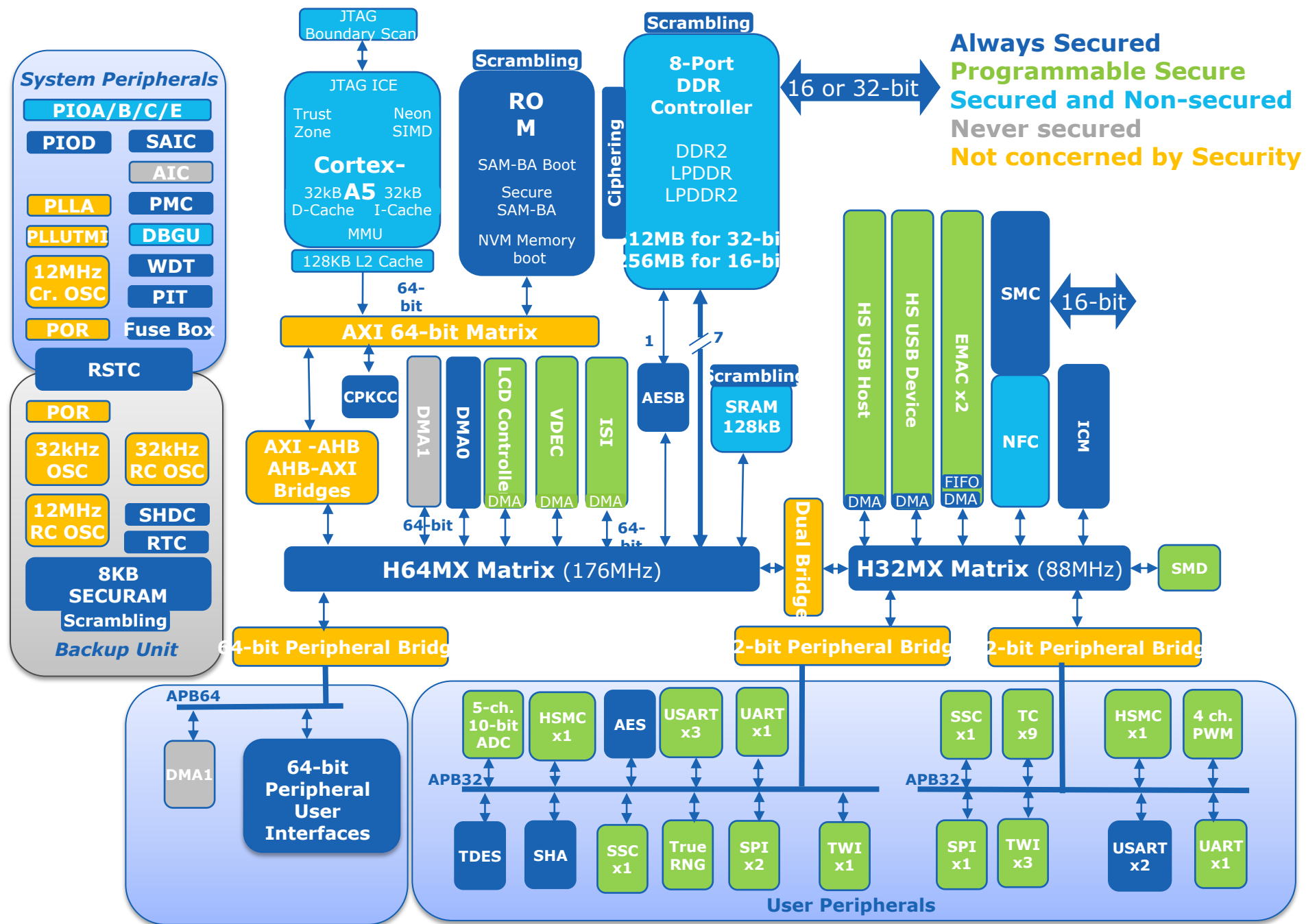
Secure JTAG/Debug

- Trustzone architecture provides separate signals to control secure and normal world software debugging
    - Secure world debugging can be enabled when the device is in a physically trusted development location
    - Secure world debugging must be disabled in production devices

- Hardware as Software configuration options are used to allow debug to be restricted to certain areas

SPIDEN	SUIDEN	Debug Security
1	X	Debug allowed everywhere
0	1	Debug everywhere EXCEPT in Secure Privileged mode
0	0	Debug Non-secure only

Protecting code with Unique on-the-fly encryption/decryption from DDR

Secure perimeter

Extended secure perimeter
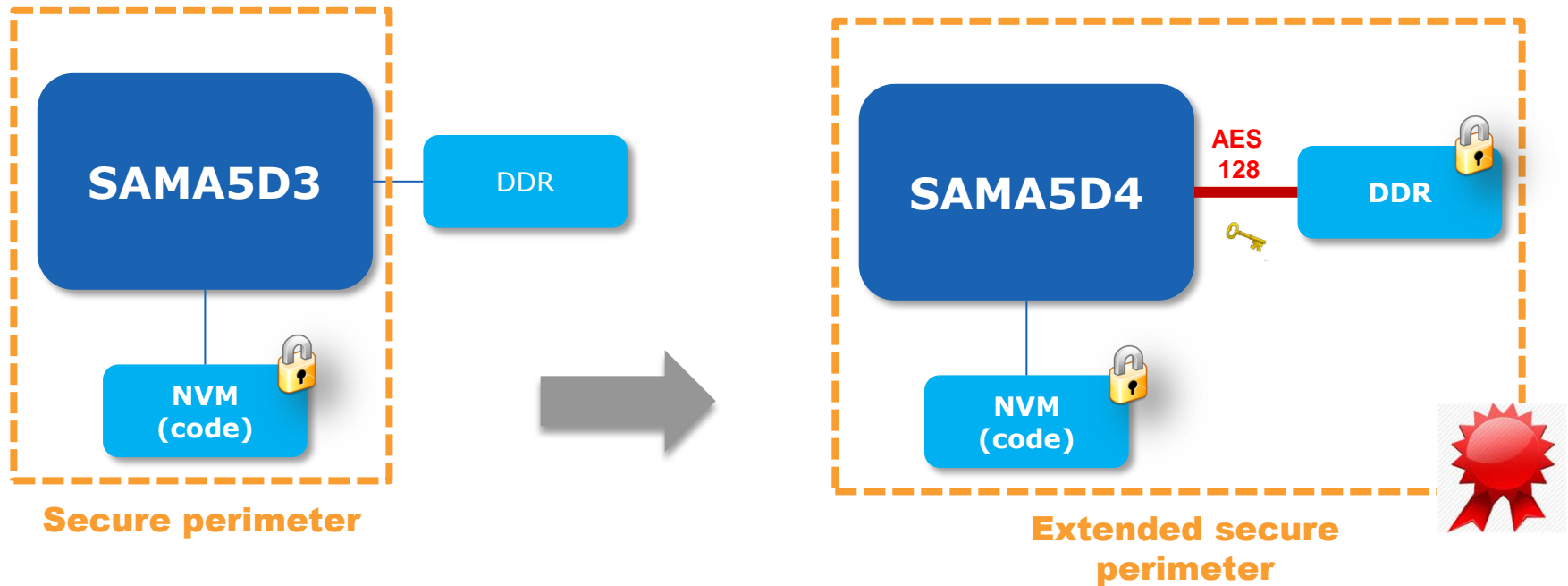
- Processor executes AES128 encrypted code from the external DDR, decrypted on the fly

- **No performance impact** with L2 cache enabled and data block under 128kB

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Where to store secrets on the chip?

- In the battery backed-up area

  - 8kBytes of SRAM

  - 512 bits of secure registers

  - ➤ Erasable upon tamper detection

  - ➤ Requires back-up area to be always powered

- SAMA5D4 also features 512 bits of fuse dedicated to customer to permanently store data.

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Detecting Physical System Intrusion and Protect Secrets

- 8 tamper pins in the back-up domain monitor the system and ensure fast key erasure upon intrusion

Protect the system enclosure

Switch Detector

SAMA5D4

System PCB

GND
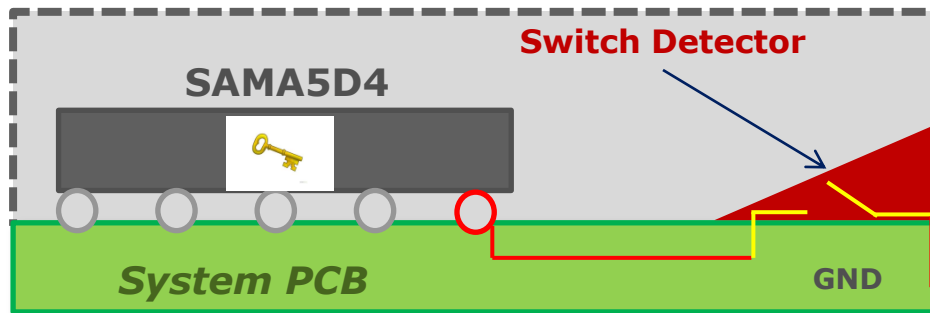
Opening of the system = Switch open

SAMA5D4

Sec.SRAM Fuse bits

Protect critical PCB area

011001….

External PCB active shield

SAMA5D4

System PCB

011001….
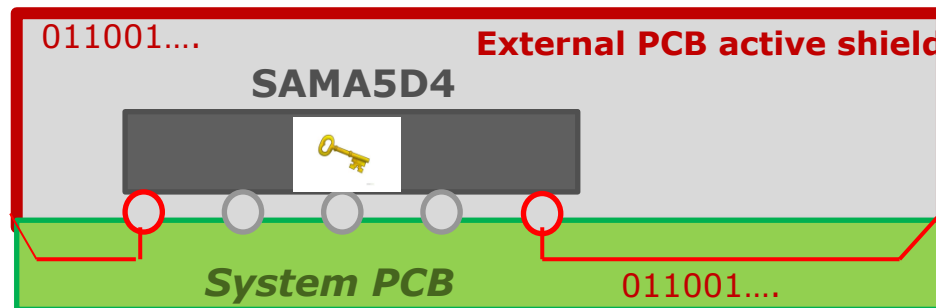
Removal, drilling, probing = perturbation to signal

Public key cryptography: Good to Know!

- Secure network communication uses **public key**
  - Mutual authentication and handshaking protocol to establish

- Public key usage is **mandatory for SSL (**TLS1.1 or TLS1.2) from from Janvier 2015

- SAMA5D4 has a dedicated hardware engine to compute RSA and ECC (Elliptic Curves) cryptography.

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Atmel and Partner Ecosystem

FREE OPEN SOURCE SW

SYSTEM ON MODULE

CONNECTIVITY SOLUTION

GRAPHICS /UI SOLUTION

POWER MANAGEMENT SOLUTION

DEBUGGER / IDE / COMPILLER

PROTOTYPE

PRE-PRODUCTION

EVALUATION

MASS PRODUCTION
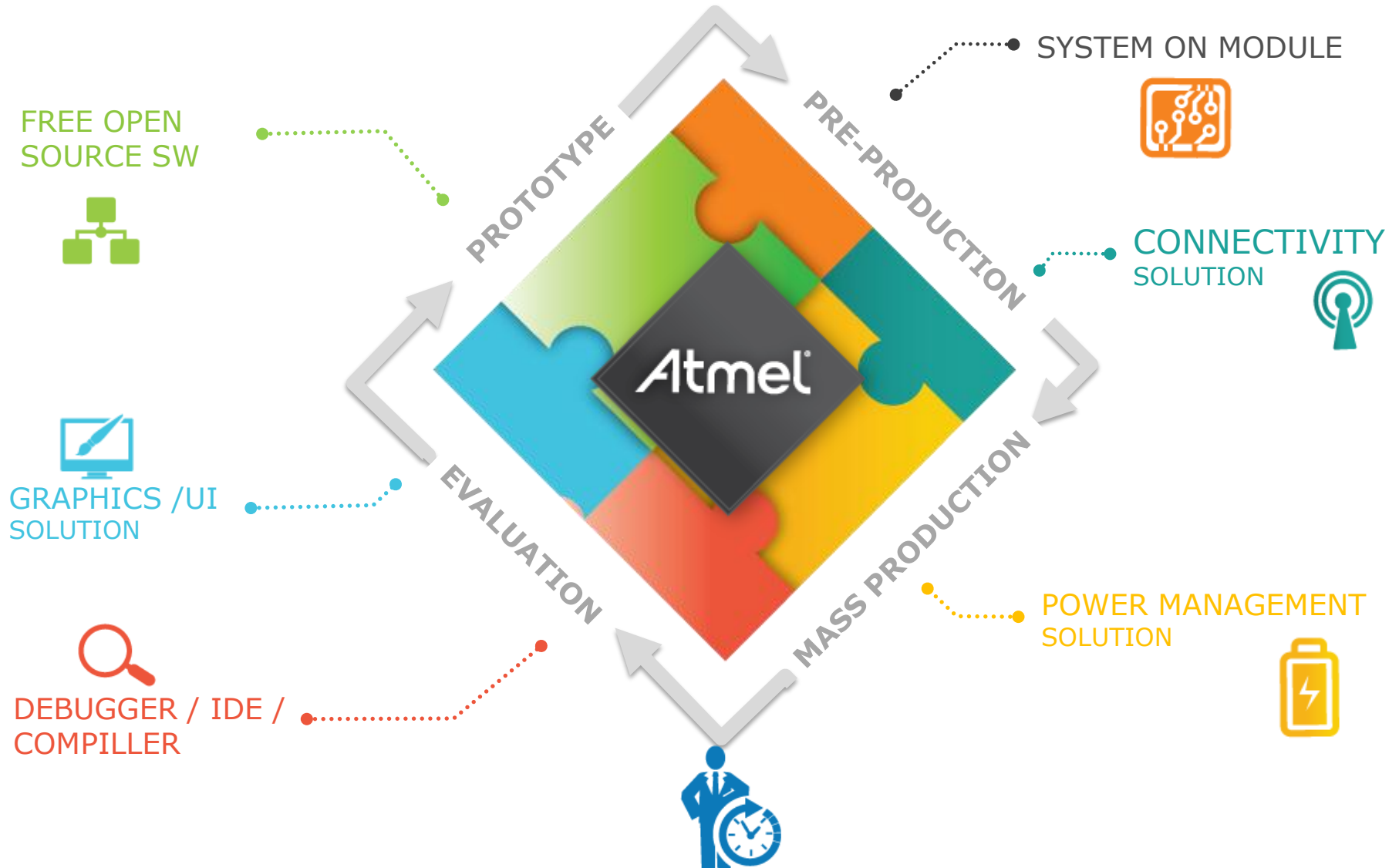
Faster Application Development

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Atmel Software offer

- Free Linux kernel 3.10 (go to www.linux4SAM.com)
  - Mainline Publication
  - Comprehensive Linux-Based system incl. Bootloaders, kernel, root files system
  - Yocto project OpenEmbedded- based distribution
  - Video support with Gstreamer

- Free QT5 SDK and Demo (go to www.linux4SAM.com)
  - Home automation & Smartfridge and demos loaded on the EK
  - Free Qt widgets and SDK provided by Atmel

- Softpack version v1.1 (Go to www.atmel/SAMA5D4 tab tools)
  - Support of tools: IAR EWARM, gcc
  - 40+ examples (USB, EMAC, L2 cache, AESB, TZ, ICM, AHB matrix, etc…)

- Secure boot loader and secure SAM-BA tools
  - Available under NDA via Atmel Sales

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SAMA5 Operating System support

Offering from Atmel and Partners

	OS supported for SAMA5D3x	OS supported for SAMA5D4x	OS that could be ported smoothly to SAMA5D3 or D4
Linux LTS Kernel 3.10	✅	✅	N/A
Windows compact 2014	✅	🟧	🟧
Android 4.2.2	✅	✅ * (4.4)	N/A
Windows Compact 7	✅	🟧	🟧
NuttX	✅	✅	N/A
QNX	✅	🟧	✅
uC-OS III	✅	🟧	✅
EmbOS	✅	✅	N/A
ThreadX®	✅	🟧	✅
uITRON4.0	✅	🟧	✅
eT-Kernel	✅	🟧	✅
FreeRTOS	🟧	✅	N/A
QuadrOS	🟧	🟧	✅
eCOS	🟧	🟧	✅

(*) planned e/o 2014

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Atmel WiFi solution

WILC1000 single-chip WiFi Link Controller
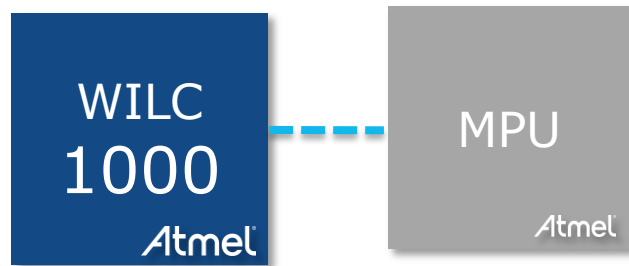
- Targeting high data rate and extended range

- Interfaced with MPU using SDIO interface.

- Linux and Android drivers and SDCard carrier board with WILC1000 module in development (end 2014)

Link Controller	WILC1000
Standards	802.11 b/g/n 1x1
Max PHY rate	72Mbps
Frequency	2.4GHz
Stacks	WPA Supplicant only
Applications	IoT, Audio/Video
Interfaces	SPI, SDIO
Tx peak (mA)	260mA @3.3V (18dBm)
Rx peak (mA)	60mA @3.3V (-90dBm)
Rx Sleep	280uA
Package	5x5mm QFN
Temp Range	-20 to +85°c

Active-Semi Power Management ICs

Alternative for discrete implementation

- **ACT8865QI305-T** :
  - 7-ch PMIC (3x DCDC, 4x LDOs)

- **ACT8945AQJ305-T** :
  - 7-ch PMIC (3x DCDC, 4x LDOs)
  - Battery charger
  - Power Path Management (ActivePath™)

- Tiny 4×4mm TQFN44-32 Package

- Capacity to support other on board components like memories.
  - LP-DDR (1.8V)
  - DDR2 (1.8V)
  - LP-DDR2 (1.2V + 1.8V) (SAMA5 only)

active-semi™
Solutions for Sustainability

Support Atmel SAMA5 and SAM9 ARM926-based MPUs

Visit: http://www.active-semi.com/AtmelPMU

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Memory suppliers – Life time commitment

Working with key leaders to support long lifetime

Minimum of 10 years lifetime

Premium **Lifecycle** Products
Micron° Parts List

ISSI® INTEGRATED SILICON SOLUTION, INC.

August 2014
Milpitas, CA

Subject: ISSI DRAM Production Duration

Dear Customer,

Thank You very much for your interest in ISSI's DRAM products   We would like to address your requirement for Long Term Availability of these parts.

ISSI has a strategic long-term business strategy for the DRAM product line.

Minimum of 12 years lifetime

- ISSI will sell a form, fit and function compatible device for all of its DRAMs for at least 12 years from the above date (the "supply period")

- In the event that any circumstances that are beyond our control or legislation obliges us to obsolete a particular device or that no orders have been received for a particular device for an 18-month Period, ISSI reserves the right to obsolete the device prior to expiration of the supply period, and will work with the customer in order to try to find a suitable solution. Additionally, ISSI will respect ISSI's EOL policy

If you have any concerns about anything in this letter, please feel free to contact us for further information.

Sincerely,

Ron Kalakuntla
SVP Marketing

Atmel

Lowest cost DRAM configuration from Micron™

	64Mb 8MB	128Mb 16MB	256Mb 32MB	512Mb 64MB	1Gb 128MB	2Gb 256MB	4Gb 512MB
SAMA5D4					LPDDR2 1Gb (x32) MT42L32M32D2AC-25 AIT:A / DDR2 1Gb (x16) MT47H64M16NF-187E:M	LPDDR2 2Gb (x32) MT42L64M32D1TK-18 IT:C / DDR2 1Gb (x16) / DDR2 1Gb (x16 or x8) MT47H128M8SH-187E:M	LPDDR2 4Gb (x32) MT42L128M32D1GU-18 WT:A / DDR2 / DDR2 / DDR2 / DDR2 1Gb (x8)
SAMA5D3					LPDDR2 1Gb (x32) MT42L32M32D2AC-25 AIT:A / DDR2 / DDR2 512Mb (x16) MT47H32M16NF-25E:H	LPDDR2 2Gb (x32) MT42L64M32D1TK-18 IT:C / DDR2 / DDR2 1Gb (x16) MT47H64M16NF-187E:M	LPDDR2 4Gb (x32) MT42L128M32D1GU-18 WT:A / DDR2 / DDR2 2Gb (x16) MT47H128M16RT-25E:C
SAM9-5s SAM9N12	SDRAM 64Mb (x16) MT48LC4M16 A2P-6A:J	SDRAM 128Mb (x16) MT48LC8M16 A2P-6A:L	SDRAM 256Mb (x16) MT48LC16M1 6A2P-6A:G	DDR2 512Mb (x16) MT47H32M16 NF-25E:H	DDR2 1Gb (x16) MT47H64M16 NF-187E:M		

Memory footprint needed for….	RTOS			LINUX	LINUX + Qt		ANDROID	

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Lowest cost DRAM configuration from ISSI

		64Mb 8MB	128Mb 16MB	256Mb 32MB	512Mb 64MB	1Gb 128MB	2Gb 256MB	4Gb 512MB

SAMA5D4

DDR2 IS43DR16160B (x16) | DDR2 IS43DR16320D (x16) | DDR2 IS43DR16640B (x16) | DDR2 IS43DR16128B (x16) | DDR2 IS43DR16128B (x16)

LPDDR IS43LR16160G IS43LR32800G (x16/x32) | LPDDR IS43LR16320C IS43LR32160C (x16/x32) | LPDDR IS43LR16640A (x16) | LPDDR IS43LR32640A (x32)

LPDDR2 IS43LD32800A (x32) | LPDDR2 IS43LD32160A (x32) | LPDDR2 IS43LD32320A (x32) | LPDDR2 IS43LD32640A* (x32) | LPDDR2 IS43LD32128A** (x32)

SAMA5D3

LPDDR IS43LR32800G (x32) | LPDDR IS43LR32160C (x32) | LPDDR IS43LR32320B (x32) | LPDDR IS43LR32640A (x32)

LPDDR2 IS43LD32320A (x32) | LPDDR2 IS43LD32640A* (x32)

DDR2 IS43DR32801B (x32) | DDR2 IS43DR32160C (x32) | DDR2 IS43DR16320D (x16) | DDR2/DDR3L IS43DR16640B IS43TR16640AL (x16) | DDR2 IS43DR16128B (x16)

LPDDR2 IS43LD32128A** (x32)

SAM9-5s SAM9N12

SDRAM IS42S16400J (x16) | SDRAM IS42S16800F (x16) | SDRAM /DDR2 IS42S16160J IS43DR16160B (x16) | DDR2/SDRAM IS43DR16320D IS42S16320F (x16) | DDR2 IS43DR16640B (x16)

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Atmel's MAC Address Devices

- Ideal for "Connected" Applications
  - Ethernet, WiFi, Bluetooth, SAS, FireWire, Zigbee, etc.
- Devices Contain a MAC Address (Extended Unique Identifier—EUI)
  - MAC/EUI value is guaranteed unique and pre-programmed into device by Atmel
  - MAC/EUI value is permanent read-only and cannot be tampered with, altered, or erased
- Devices Provide Full User EEPROM Array Access and Storage
  - MAC/EUI value is stored in extra, dedicated memory and accessed separately
    - The MAC/EUI value is stored at a different I^{2}C device address than the main EEPROM
- 48-bit and 64-bit MAC/EUI Devices Available

	AT24MAC4xx	AT24MAC6xx
MAC/EUI Type	48-bit value	True 64-bit value
Pre-programmed OUI Value*	FC-C2-3D	
Additional Pre-programmed 128-bit Serial Number	Yes (Atmel programmed)	
Multiple-MAC Address Capable	Yes (contact Atmel)	
EEPROM Density Ranges	1Kb – 32Kb (and growing)	

* - Atmel can program customer-specified OUIs and EUIs (setup charges and MOQs apply)

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System On Module (SOM)

Lower the design complexity and investment level

- ARM9 and Cortex-A5 based System on Modules
- Reduce product development cycle by providing embedded modules ready for use as complete control, HMI and processing units.

Where to find information and documentation?

Useful links

- SAMA5 Microsite:
    - http://www.atmel.com/microsite/sama5

- Information relative to SW
    - Linux: http://www.at91.com/linux4sam/bin/view/Linux4SAM/
    - Android: http://www.at91.com/android4sam/bin/view/Android4SAM/
    - Windows: http://www.at91.com/windows4sam/bin/view/Windows4SAM/
    - Atmel Community: http://www.at91.com/
    - GitHub: https://github.com/torvalds/linux/tree/master/arch/arm/mach-at91

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Atmel Embedded MPUs

High performance, low power, ease of use for industrial and consumer applications

- High-Performance Architecture

- Market-Leading Low Power Consumption

- High Integration Level and Low System Cost

- Extensive Ecosystem

"setting a new power/size/cost point in the embedded Linux box space"

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Thank you for listening

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