

1. Description

1.1. Project

Project Name	progetto
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 6.14.0
Date	03/16/2025

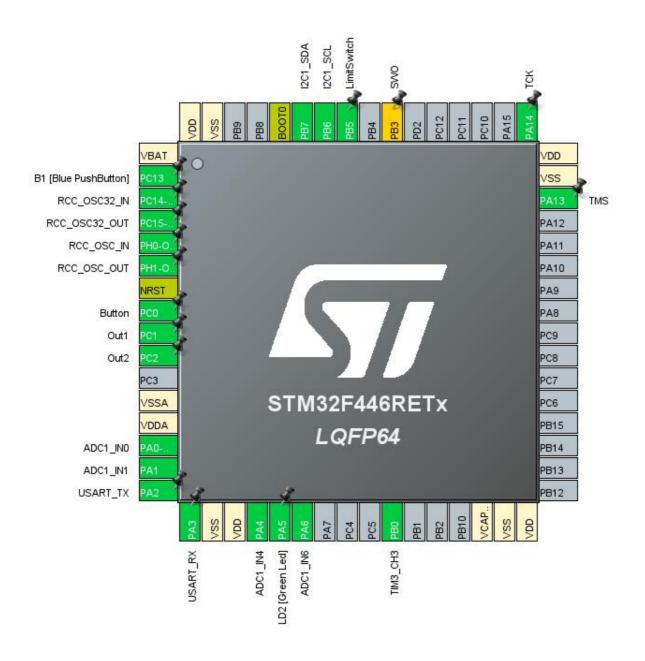
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



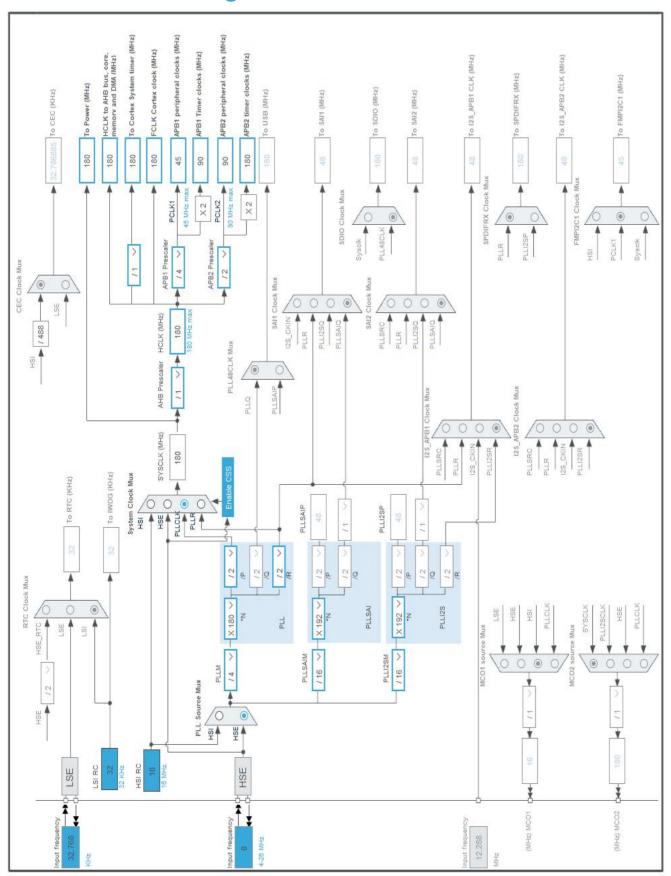
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after reset)		Function(s)	
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	GPIO_EXTI0	Button
9	PC1 *	I/O	GPIO_Output	Out1
10	PC2 *	I/O	GPIO_Output	Out2
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	
15	PA1	I/O	ADC1_IN1	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	ADC1_IN6	
26	PB0	I/O	TIM3_CH3	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
57	PB5 *	I/O	GPIO_Input	LimitSwitch
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	I2C1_SDA	
60	воото	Boot		
63	VSS	Power		
64	VDD	Power		

*	The	pin	is	affected	with	an	I/O	function
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^{**} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



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1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

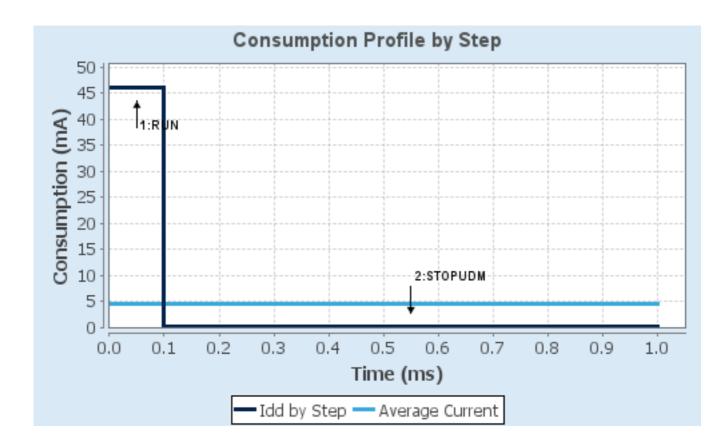
1.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/P REFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 μA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	progetto
Project Folder	C:\Users\39333\STM32CubelDE\workspace_1.17.0\progetto
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name Peripheral Instance National Peripheral Peripheral Instance National Peripheral Perip	
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART2_UART_Init	USART2
5	MX_I2C1_Init	I2C1
6	MX_ADC1_Init	ADC1
7	MX TIM3 Init	TIM3

3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: IN0 mode: IN1 mode: IN4 mode: IN6

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment
Scan Conversion Mode Enabled

Continuous Conversion Mode Enabled *

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Enabled *

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 4

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 0
Sampling Time 3 Cycles
Rank 2 *

Channel 1 *

Sampling Time 3 Cycles
Rank 3 *

Channel 4 *

Sampling Time 3 Cycles
Rank 4 *

Channel 6 *

Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode

false

3.2. I2C1 I2C: I2C

3.2.1. Parameter Settings:

Master Features:

I2C Speed Mode Fast Mode *

I2C Clock Speed (Hz) 400000

Fast Mode Duty Cycle Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

General Call address detection Disabled

3.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

3.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

Power Over Drive Enabled

3.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

3.5. TIM3

Channel3: PWM Generation CH3

3.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

No Division

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

3.6. USART2

Mode: Asynchronous

3.6.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

progetto Project
Configuration Report

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
7,501	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USART_RX
Single Mapped Signals	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	swo
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_EXTI0	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	Button
	PC1	GPIO_Output	Output Push Pull	Pull-up *	Low	Out1
	PC2	GPIO_Output	Output Push Pull	i un up	Low	Out2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
				Pull-up *		
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LimitSwitch

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Circular *

Use fifo: Enable *

FIFO Threshold:
Peripheral Increment:
Disable
Memory Increment:
Peripheral Data Width:
Half Word
Memory Data Width:
Half Word
Peripheral Burst Size:
Single
Memory Burst Size:
Single

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
EXTI line 0 interrupt	true	3	0	
DMA2 stream0 global interrupt	true	3	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1, ADC2 and ADC3 interrupts	unused			
TIM3 global interrupt	unused			
I2C1 event interrupt	unused			
I2C1 error interrupt	unused			
USART2 global interrupt	unused			
EXTI line[15:10] interrupts	unused			
FPU global interrupt		unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
	sequence ordening	Hariulei	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line 0 interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

progetto Project
Configuration Report

* User modified value

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f446_bsdl.zip lBIS models https://www.st.com/resource/en/ibis_model/stm32f446_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

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microcontroller-system-memory-boot-mode-stmicroelectronics.pdf

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stm32-mcus-a-consistent-832bit-product-line-for-painless-migration-

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- stm32s-usart-stmicroelectronics.pdf
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