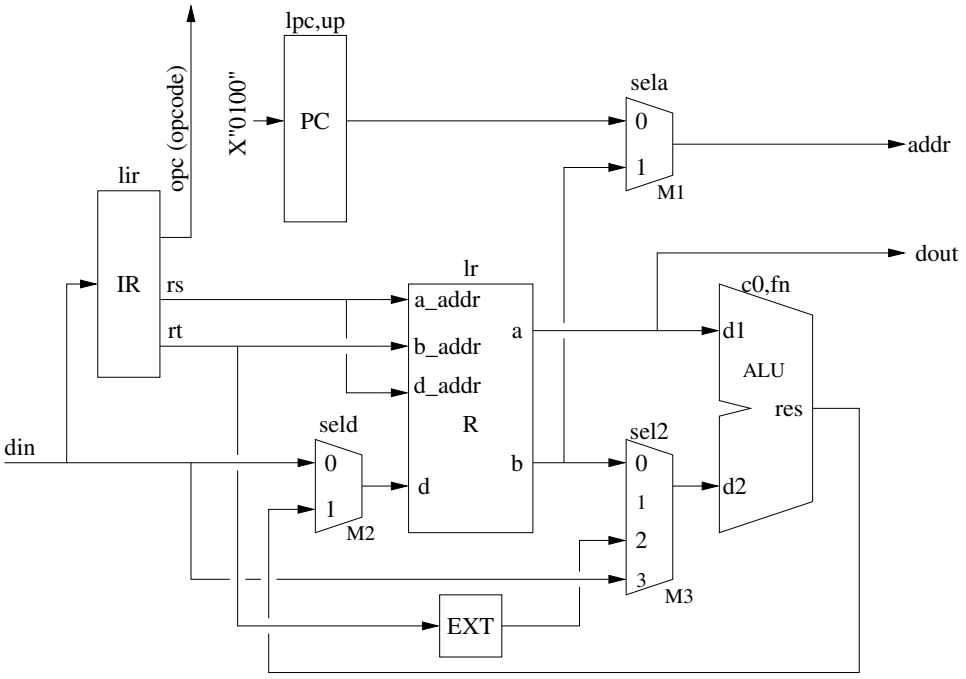
Sample Computer Design Questions SOLUTIONS

1. A proposed datapath of a CPU to implement an instruction set architecture is:



The functional specification of the ALU is:

fn	function	fn	function
000	res = 0	100	res = 1
001	res = d1	101	res = d2
010	res = a + b + c0	110	res = a + $\overline{\text{b}}$ + c0
011	res = a $\wedge$ b	111	res = a $\downarrow$ b

Among the instructions in the instruction set are:

	Syntax	Semantics
add	rs, rt	R[s] $\leftarrow$ R[s] + M[R[t]]
sw	rs, displ(rt)	M[displ + R[t]] $\leftarrow$ R[s]

(a) Define a suitable control word format for the CPU defined by the diagrams.

ANSWER:

lpc	up	sela	lir	seld	lr	sel2	c0	fn
11	10	9	8	7	6	5:4	3	2:0

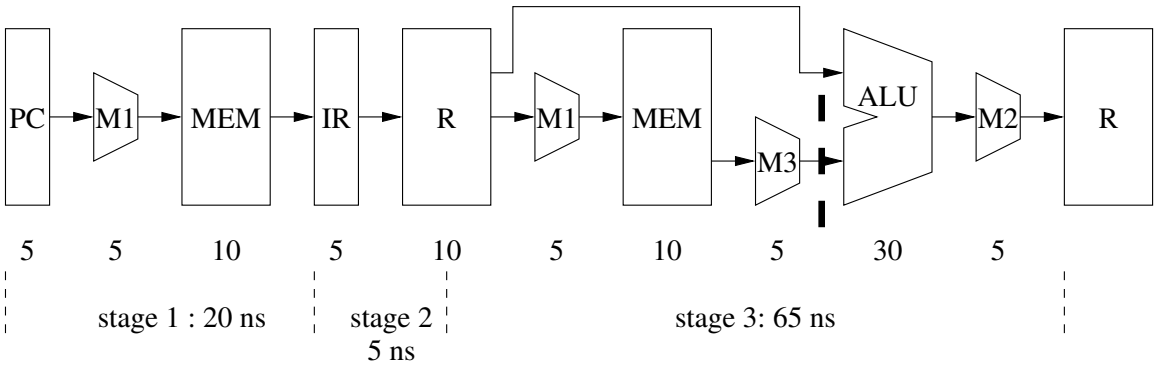
(b) Provide the binary sequence for the appropriate control for the μ-instruction "R[s] $\leftarrow$ R[s] + din".

ANSWER:

STATE	lpc	up	sela	lir	seld	lr	sel2	c0	fn
	11	10	9	8	7	6	5:4	3	2:0
ADD	0	0	1	0	1	1	11	0	010

(c) In the CPU datapath, all registers and multiplexers have a 5 ns propagation delay, register files and memories have a 10 ns delay, and the ALU has a 30 ns delay. Construct the unfolded data flow (UDF) diagram for the "`add`" instruction and determine the lower bound on clock period from the diagram. Label each component as it is labelled in the datapath and indicate each stage. Label the memory component by "MEM.

ANSWER:



(d) Determine the best place to place a single register in the CPU datapath so as to reduce the lower bound on the clock period. Indicate that location on both your UDF diagram (in 2.c) and on the CPU datapath (last page) and compute the lower bound on the clock period for the revised UDF diagram.

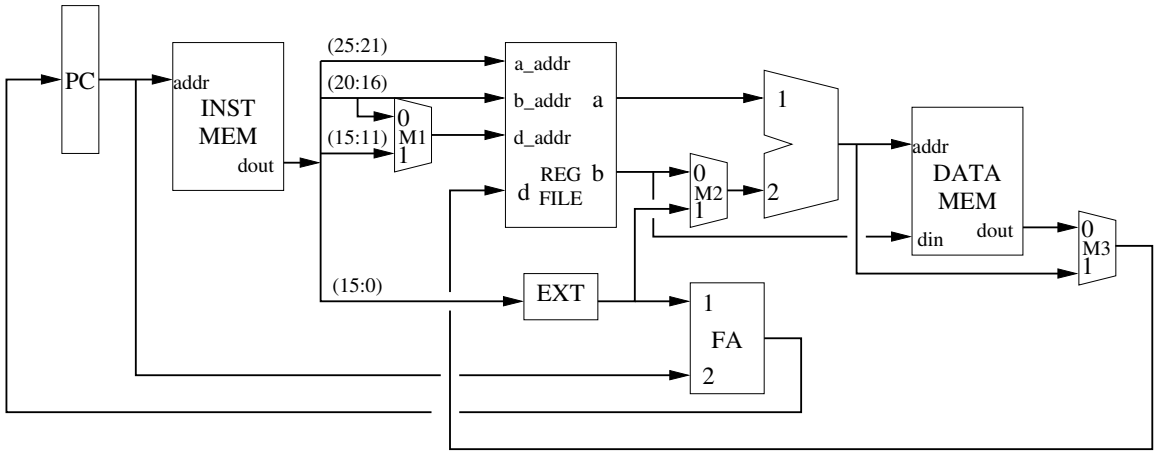
ANSWER: Place the register between M3 and ALU in stage 3: dashed line in UDF diagram.

Place the register between M3 and ALU in CPU datapath

New clock period > max (20, 5, 25, 30, 40) = 40 ns.

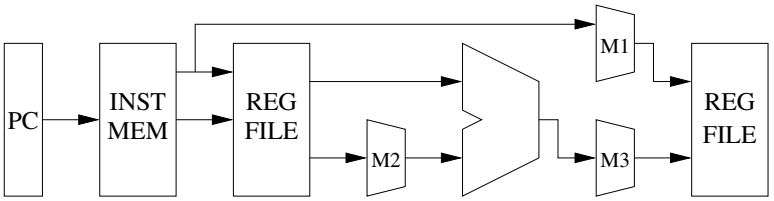
2. A designer proposes an alternate "non von Neumann" datapath for the implementation of a set of instructions that include:

	Syntax	Semantics
add	rs, rt	R[s] ← R[s] + R[t]
sw	rt, displ(rs)	M[displ + R[s]] ← R[t]



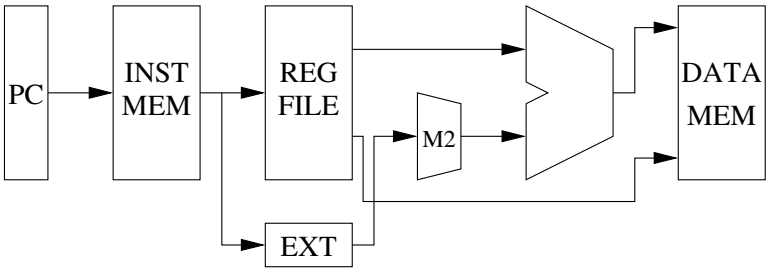
(a) Draw an unfolded dataflow (UDF) diagram for the "`add`" instruction. Label the components.

ANSWER:

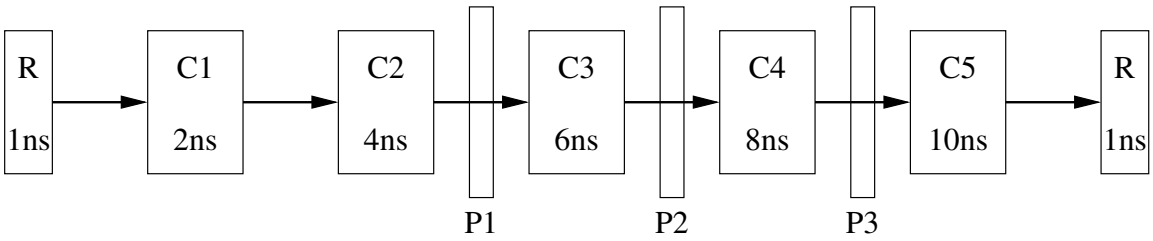


(b) Draw an unfolded dataflow (UDF) diagram for the "`sw`" instruction. Label the components.

ANSWER:



3. Consider the following unfolded data flow (UDF) diagram:



(a) What is the lower bound on the clock period necessary for the corresponding datapath to execute correctly?

ANSWER: 31 ns.

(b) You have a supply of registers (1 ns propagation delay) with which you can pipeline this UDF.

i. Determine the fewest number required to obtain the shortest possible clock period and indicate on the diagram where they would be placed.

ii. Determine the propagation delay of each stage.

ANSWER: Let P1, P2, P3 denote the pipeline registers:

Stage 1: (R to C2) - 7 ns;

Stage 2: (P1 to C3) - 7 ns;

Stage 3: (P2 to C4) - 9 ns;

Stage 4: (P3 to C5) - 11 ns.

iii. What is the minimum clock period?

ANSWER: Minimum clock period is 11 ns + t_{setup}