BSIM-IMG 102.9.2

Independent Multi-Gate MOSFET Compact Model

Technical Manual

Authors:
Pragya Kushwaha, Yen-Kai Lin, Harshit Agarwal
Chetan Kumar Dabhi, Avirup Dasgupta

Project Director:
Prof. Ali Niknejad, Prof. Sayeef Salahuddin and Prof. Chenming Hu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

Past Developers :

Juan Pablo Duarte, UC Berkeley
Sourabh Khandelwal, UC Berkeley
Srivatsava Jandhyala, UC Berkeley
Navid Paydavosi, UC Berkeley
Yogesh S. Chauhan, UC Berkeley
Sriramkumar V., UC Berkeley
Chung-Hsun Lin, UC Berkeley
Mohan Dunga, UC Berkeley
Darsen Lu, UC Berkeley
Shijing Yao, UC Berkeley

Contents

1 Introduction

The continuous evolution and enhancement of bulk CMOS technology has fueled the growth of the microelectronics industry over the past several decades. When we reach the end of the technology roadmap for the classical CMOS, multiple gate CMOS structures will likely take up the baton. We have developed a multiple gate MOSFET compact model for technology/circuits development in the short term and for product design in the longer term.

Several different multi-gate (MG) structures and two different modes of operation are being pursued in the industry today. In the case of planar double gate (Figure 1), the two gates will likely be asymmetric– having different work functions and dielectric thicknesses, complicating the compact model. Also, the two gates are likely to be biased at two different voltages, and these gates are called independent gates. In the other double, triple, or all-around gate cases, the gates are biased at the same voltage, and these cases are called common gate. One example of a common gate device is the FinFET transistor.

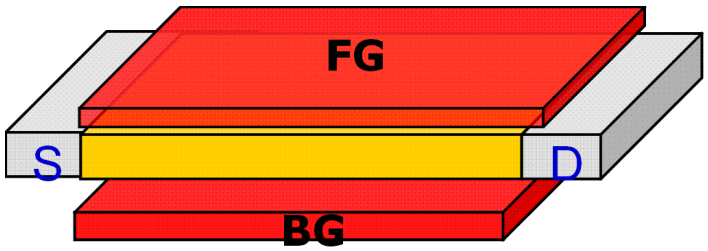


Figure 1: Planar double-gate SOI MOSFET.

The Independent Multi-Gate model BSIM-IMG described in this document has been developed to model the electrical characteristics of the independent double-gate structures. It allows different front- and back- gate work functions, dielectric thicknesses and dielectric constants.

A separate model, BSIM-CMG, has been developed to model the common-gate MG structure. Code and documentation for BSIM-CMG are also available upon request.

2 Model Description

The BSIM-IMG 102.9.2models the independent double-gate structure as a four terminal device, containing the source(s), drain(d), front gate(fg), and back gate(bg) terminals. The two gates (e.g., 1=fg, 2=bg) are allowed to have different workfunctions ($\Delta\psi_1$, $\Delta\psi_2$) and dielectric thicknesses (T_{ox1}, T_{ox2}). They can also be biased separately at different voltages.

Physical surface-potential-based formulations are derived in both intrinsic and extrinsic models of BSIM-IMG. Surface potentials and integrated charge densities at the source and drain ends are obtained by solving the Poisson's equation in a fully-depleted, lightly-doped body and calculating with efficient analytical approximations. Since the surface potential equation is derived based on Poisson's equation,

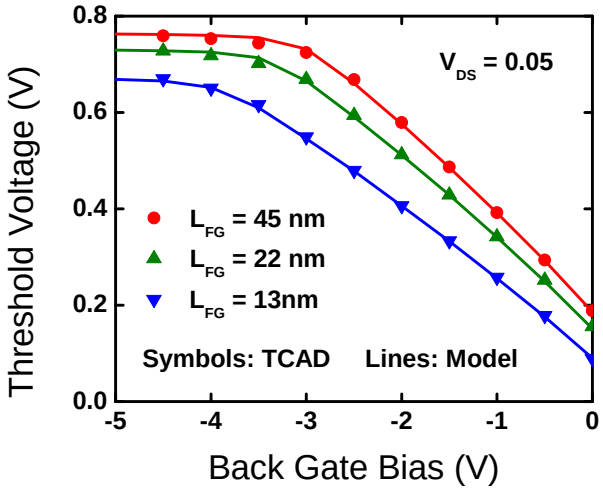


Figure 2: Threshold Voltage (V_{th}) versus back-gate bias (V_{bg}) for different gate lengths in NMOS transistor with p-type substrate (p-well). Symbols: TCAD; Lines: Model

the model captures volume inversion effects very well and shows excellent scalability compared with 2D device simulation.

To meet the requirements of future devices, new parameters has been included to model devices consisting of novel materials. This includes parameters for non-silicon channel devices and High-K gate insulators.

The back gate of a planar double-gate SOI FET is often used for tuning device threshold voltage (V_{th}). Therefore, the effect of back-gate on V_{th} must also be addressed by the model. The threshold voltage of FDSOI transistor is extracted from constant current method as shown in Figure 2. When the back gate bias (V_{bg}) is low, the threshold voltage follow a linear relationship. For higher back-gate bias, however, the back-gate effect slows down as a result of back surface accumulation.

The strength of back-gate control is often quantified as γ, defined as:

$$\gamma = \frac{dV_{th}}{dV_{bg}} \tag{1}$$

When the gate length is long, γ can be approximated using

$$\gamma = \frac{dV_{th}}{dV_{bg}} \approx -\frac{C_{ox2} \parallel C_{si}}{C_{ox1}} \tag{2}$$

where $C_{ox1} = \epsilon_{ox1}/T_{ox1}$, $C_{ox2} = \epsilon_{ox2}/T_{ox2}$, $C_{si} = \epsilon_{si}/T_{si}$. This long channel γ is inherently captured by the core model of BSIM-IMG. There are two inversion charge density models for the body charge available in the core of the model, which can be selected using the parameter CHARGEMOD. CHARGEMOD=0 is a simplified and computationally efficient charge density model which is the default model used in the core. A more accurate but computationally intensive charge density model, appropriate for body thickness less than 2 nm, can be selected using CHARGEMOD=1. As we shrink the gate length,

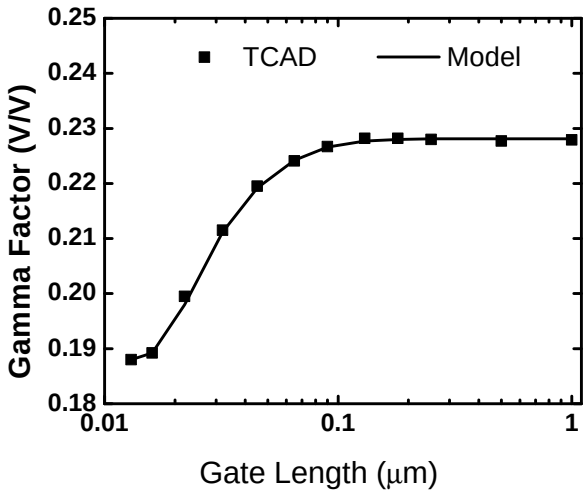


Figure 3: γ versus gate length. Symbols: TCAD; Lines: Model

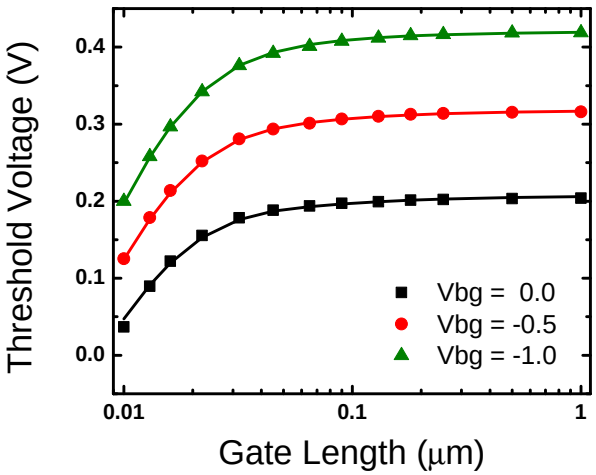


Figure 4: V_{th} roll-off for different back-gate biases. Symbols: TCAD; Lines: Model

γ is reduced due to the capacitive coupling from the source/drain (Figure 3). In BSIM-IMG, the length dependence of γ is model by equation (3.109), (3.111). Using a length-dependent γ, the model successfully captures V_{th} roll-off for different back-gate biases, as shown in Figure 4.

Other important effects, such as short channel effects, mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance, are also incorporated in the model.

The model continuous and is symmetric at Vds=0. This physics-based model is scalable and predictive over a wide range of device parameters.

3 BSIM-IMG 102.9.2 Model Equations

3.1 Bias Independent Calculations

3.1.1 Physical Constants

Physical quantities in BSIM-IMG are in M.K.S units unless specified otherwise.

$$q = 1.6 \times 10^{-19} \tag{3.3}$$
$$\epsilon_0 = 8.8542 \times 10^{-12} \tag{3.4}$$
$$k = 1.3787 \times 10^{-23} \tag{3.5}$$
$$\epsilon_{si} = EPSRSUB \cdot \epsilon_0 \tag{3.6}$$
$$\epsilon_{sub} = EPSRSUB \cdot \epsilon_0 \tag{3.7}$$
$$\epsilon_{ox1} = EPSROX1 \cdot \epsilon_0 \tag{3.8}$$
$$\epsilon_{ox2} = EPSROX2 \cdot \epsilon_0 \tag{3.9}$$
$$\epsilon_{ratio} = \frac{EPSRSUB}{3.9} \tag{3.10}$$
$$C_{ox1} = \frac{3.9 \cdot \epsilon_0}{EOT1} \tag{3.11}$$
$$C_{ox2} = \frac{3.9 \cdot \epsilon_0}{EOT2} \tag{3.12}$$
$$C_{ox1P} = \frac{3.9 \cdot \epsilon_0}{EOT1P} \tag{3.13}$$
$$C_{ox2P} = \frac{3.9 \cdot \epsilon_0}{EOT2P} \tag{3.14}$$
$$C_{si} = \frac{\epsilon_{si}}{TSI} \tag{3.15}$$
$$v_{tm} = \frac{kT}{q} \tag{3.16}$$
$$\delta_2 = 10^{-3} \tag{3.17}$$

3.1.2 Effective Channel Length and Channel Width

$$Lnew = L + XL \tag{3.18}$$
$$L_{\text{LLN}} = Lnew^{-LLN} \tag{3.19}$$
$$L_{\text{WLN}} = Lnew^{-WLN} \tag{3.20}$$
$$LW_{\text{LLN-LWN}} = L_{\text{LLN}} \cdot W_{\text{LWN}} \tag{3.21}$$
$$dLIV = LINT + LL \cdot L_{\text{LLN}} + LW \cdot W_{\text{LWN}} + LWL \cdot LW_{\text{LLN-LWN}} \tag{3.22}$$
$$Leff = Lnew - 2.0 \cdot dLIV \tag{3.23}$$

Here, dLIV is the overlap/underlap between the gate and the source/drain diffusions; LINT is dLIV for large devices; L is the designed (drawn) length; XL is the length variation due to process effects; LL, LW, LWL and L_{LLN}, W_{LWN}, $LW_{\text{LLN-LWN}}$ are fitting parameters.

$$dLCV = DLC + LLC \cdot L_{\text{LLN}} + LWC \cdot W_{\text{LWN}} + LWLC \cdot LW_{\text{LLN-LWN}} \tag{3.24}$$
$$LeffCV = Lnew - 2.0 \cdot dLCV \tag{3.25}$$

Here, dLCV is the overlap/underlap between the gate and the source/drain diffusions for C-V calculations; DLC is dLCV for large devices; LLC, LWC, LWLC and L_{LLN}, W_{LWN}, $LW_{\text{LLN-LWN}}$ are fitting parameters. **NFMOD** switch is used for W_{new} calculation, when NFMOD is 0: W is taken as total width like BSIM4 and when NFMOD is 1: W is taken as single finger width.

$$W_{new} = \begin{cases} \frac{W}{NF} & \text{NFMOD=0} \\ W & \text{NFMOD=1} \end{cases}$$
$$W_{new} = W + XW \tag{3.26}$$
$$W_{\text{LWN}} = W_{new}^{-LWN} \tag{3.27}$$
$$W_{\text{WWN}} = W_{new}^{-WWN} \tag{3.28}$$
$$LW_{\text{WLN-WWN}} = L_{\text{WLN}} \cdot W_{\text{WWN}} \tag{3.29}$$
$$dWIV = WINT + WL \cdot L_{\text{WLN}} + WW \cdot W_{\text{WWN}} + WWL \cdot LW_{\text{WLN-WWN}} \tag{3.30}$$
$$Weff = W_{new} - 2.0 \cdot dWIV \tag{3.31}$$

Here, dWIV is gate edge adjacent to STI for I-V calculations; WINT is dWIV for large devices; W is the designed (drawn) length; XW is the length variation due to process effects; WL, WW, WWL and L_{WLN}, W_{WWN}, $LW_{\text{WLN-WWN}}$ are fitting parameters.

$$dWCV = DWC + WLC \cdot L_{\text{WLN}} + WWC \cdot W_{\text{WWN}} + WWLC \cdot LW_{\text{WLN-WWN}} \tag{3.32}$$
$$WeffCV = W_{new} - 2.0 \cdot dWCV \tag{3.33}$$

Here, dWCV is gate edge adjacent to STI for C-V calculations; DWC is dWCV for large devices; WLC, WWC, WWLC and L_{WLN}, W_{WWN}, $LW_{\text{WLN-WWN}}$ are fitting parameters.

3.1.3 Binning Calculations

The optional binning methodology [1] is adopted in BSIM-IMG. In the binning methodology, the device W, L is divided into many bins according to the required model accuracy. For a given geometry, each model parameter

$PARAM_i$ is calculate as a function of a zero-order term, PARAM, a length dependent term, LPARAM, a width dependent term, WPARAM, and a WL product dependent term, PPARAM:

$$PARAM_i = PARAM + \frac{1}{L_{eff}} \cdot LPARAM + \frac{1}{W_{eff}} \cdot WPARAM + \frac{1}{W_{eff}L_{eff}} \cdot PPARAM \tag{3.34}$$

For the list of binnable parameters, please refer to the complete parameter list in the end of this technical note.

3.1.4 Length scaling equations

$$U0[L] = \begin{cases} U0_i \cdot \left[1 - UP_i \cdot {L_{eff}}^{-LPA}\right] & LPA > 0 \\ U0_i \cdot [1 - UP_i] & \text{Otherwise} \end{cases} \tag{3.35}$$

$$MEXP[L] = MEXP_i + AMEXP \cdot L_{eff}^{-BMEXP} \tag{3.36}$$

$$PCLM[L] = PCLM_i + APCLM \cdot \exp\left(-\frac{L_{eff}}{BPCLM}\right) \tag{3.37}$$

$$UA[L] = UA_i + AUA \cdot \exp\left(-\frac{L_{eff}}{BUA}\right) \tag{3.38}$$

$$EU[L] = EU_i + AEU \cdot \exp\left(-\frac{L_{eff}}{BEU}\right) \tag{3.39}$$

$$UD[L] = UD_i + AUD \cdot \exp\left(-\frac{L_{eff}}{BUD}\right) \tag{3.40}$$

$$UDB[L] = UDB_i + AUDB \cdot \exp\left(-\frac{L_{eff}}{BUDB}\right) \tag{3.41}$$

$$UC[L] = UC_i + AUC \cdot \exp\left(-\frac{L_{eff}}{BUC}\right) \tag{3.42}$$

$$DVTP0[L] = DVTP0_i + ADVTP0 \cdot \exp\left(-\frac{L_{eff}}{BDVTP0}\right) \tag{3.43}$$

$$DVTP1[L] = DVTP1_i + ADVTP1 \cdot \exp\left(-\frac{L_{eff}}{BDVTP1}\right) \tag{3.44}$$

$$PTWG[L] = PTWG_i + APTWG \cdot \exp\left(-\frac{L_{eff}}{BPTWG}\right) \tag{3.45}$$

$$PTWGB[L] = PTWGB_i + APTWGB \cdot \exp\left(-\frac{L_{eff}}{BPTWGB}\right) \tag{3.46}$$

$$PTWGR[L] = PTWGR_i + APTWG \cdot \exp\left(-\frac{L_{eff}}{BPTWG}\right) \tag{3.47}$$

$$VSAT[L] = VSAT_i + AVSAT \cdot \exp\left(-\frac{L_{eff}}{BVSAT}\right) \tag{3.48}$$

$$VSATB[L] = VSATB_i + AVSATB \cdot \exp\left(-\frac{L_{eff}}{BVSATB}\right) \tag{3.49}$$

$$VSAT1[L] = VSAT1_i + AVSAT1 \cdot \exp\left(-\frac{L_{eff}}{BVSAT1}\right) \tag{3.50}$$

$$VSATCV[L] = VSAT_i + AVSATCV \cdot \exp\left(-\frac{L_{eff}}{BVSATCV}\right) \tag{3.51}$$

$$\tag{3.52}$$

If $RDSMOD = 0$ then

$$RDSW[L] = RDSW_i + ARDSW \cdot \exp\left(-\frac{L_{eff}}{BRDSW}\right) \tag{3.53}$$

If $RDSMOD = 1$ then

$$RSW[L] = RSW_i + ARSW \cdot \exp\left(-\frac{L_{eff}}{BRSW}\right) \tag{3.54}$$

$$RDW[L] = RDW_i + ARDW \cdot \exp\left(-\frac{L_{eff}}{BRDW}\right) \tag{3.55}$$

3.1.5 Temperature Effects

$$E_g = BG0SUB - \frac{TBGASUB \cdot T^2}{T + TBGBSUB} \tag{3.56}$$

$$n_i = NI0SUB \cdot \left(\frac{T}{300.15}\right)^{\frac{3}{2}} \cdot \exp\left(\frac{BG0SUB \cdot q}{2k \cdot 300.15} - \frac{E_g \cdot q}{2k \cdot T}\right) \tag{3.57}$$

$$N_c = NC0SUB \cdot \left(\frac{T}{300.15}\right)^{\frac{3}{2}} \tag{3.58}$$

$$V_{bi} = \frac{kT}{q} \cdot \ln\left(\frac{NSD \cdot NBODY}{n_i^2}\right) \tag{3.59}$$

$$\Phi_B = \frac{kT}{q} \cdot \ln\left(\frac{NBODY}{n_i}\right) \tag{3.60}$$

$$\Phi_{SUB} = \frac{kT}{q} \cdot \ln\left(\frac{NBG}{n_i}\right) \tag{3.61}$$

$$\Delta V_{th,temp} = \left(KT1 + \frac{KT1L}{L_{eff}}\right) \cdot \left(\frac{T}{TNOM} - 1\right) + \left(KT2 + \frac{KT2L}{L_{eff}}\right) \cdot \left(\frac{T}{TNOM} - 1\right) \cdot V_{bgx} \tag{3.62}$$

$$\mu_0(T) = U0[L] \cdot \left(\frac{T}{TNOM}\right)^{UTE_i} + UTL_i \cdot (T - TNOM) \tag{3.63}$$

$$MEXP(T) = MEXP[L] \cdot (1.0 + TMEXP \cdot (T - TNOM)) \tag{3.64}$$

$$ETAMOB(T) = ETAMOB_i \cdot [1 + EMOBT_i \cdot (T - TNOM)] \tag{3.65}$$

$$UA(T) = UA[L] + UA1_i \cdot (T - TNOM) \tag{3.66}$$

$$UC(T) = UC[L] + UC1 \cdot (T - TNOM) \tag{3.67}$$

$$UD(T) = UD[L] \cdot \left(\frac{T}{TNOM}\right)^{UD1_i} \tag{3.68}$$

$$UCS(T) = UCS_i \cdot \left(\frac{T}{TNOM}\right)^{UCSTE_i} \tag{3.69}$$

$$ETA0(T) = ETA0[L] \cdot (1.0 + TETA0 \cdot (T - TNOM)) \tag{3.70}$$

$$AT = AT \cdot (1.0 + \frac{10^{-6}}{Leff} \cdot ATL) \tag{3.71}$$

$$ATB = ATB \cdot (1.0 + \frac{10^{-6}}{Leff} \cdot ATBL) \tag{3.72}$$

$$VSAT(T) = VSAT[L] \cdot (1 - AT \cdot (T - TNOM)) \tag{3.73}$$

$$VSAT1(T) = VSAT1[L] \cdot (1 - AT \cdot (T - TNOM)) \tag{3.74}$$

$$VSATB(T) = VSATB[L] \cdot (1 - ATB \cdot (T - TNOM)) \tag{3.75}$$

$$VSATCV(T) = VSATCV[L] \cdot (1 - AT \cdot (T - TNOM)) \tag{3.76}$$

$$PTWG(T) = PTWG[L] \cdot (1 - PTWGT \cdot (T - TNOM)) \tag{3.77}$$

$$BETA0(T) = BETA0_i \cdot \left(\frac{T}{TNOM}\right)^{IIT} \tag{3.78}$$

$$K0(T) = K0_i + K01_i \cdot (T - TNOM) \tag{3.79}$$

$$K0SI(T) = K0SI_i + K0SI1_i \cdot (T - TNOM) \tag{3.80}$$

$$BGIDL(T) = BGIDL_i \cdot (1 + TGIDL \cdot (T - TNOM)) \tag{3.81}$$

$$BGISL(T) = BGISL_i \cdot (1 + TGISL \cdot (T - TNOM)) \tag{3.82}$$

$$RDSWMIN(T) = RDSWMIN \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.83}$$

$$RDSW(T) = RDSW[L] \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.84}$$

$$RSWMIN(T) = RSWMIN \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.85}$$

$$RDWMIN(T) = RDWMIN \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.86}$$

$$RSW(T) = RSW[L] \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.87}$$

$$RDW(T) = RDW[L] \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.88}$$

$$R_{s,geo}(T) = R_{s,geo} \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.89}$$

$$R_{d,geo}(T) = R_{d,geo} \cdot (1 + PRT \cdot (T - TNOM)) \tag{3.90}$$

$$Igtemp = \left(\frac{T}{TNOM}\right)^{IGT_i} \tag{3.91}$$

3.1.6 Front and Back Gate Workfunction Calculation

$$PHIG2_i = \begin{cases} PHIG2 + 0.5 \cdot BG0SUB - \Phi_{SUB} & \text{for N-WELL} \\ PHIG2 - 0.5 \cdot BG0SUB + \Phi_{SUB} & \text{for P-WELL} \end{cases} \tag{3.92}$$

$$\Phi_{ref} = \begin{cases} EASUB & \text{for NMOS} \\ EASUB + E_g & \text{for PMOS} \end{cases} \tag{3.93}$$

$$devsign = \begin{cases} 1 & \text{for NMOS} \\ -1 & \text{for PMOS} \end{cases} \tag{3.94}$$

$$\Delta\Phi_1 = devsign \cdot (PHIG1_i - \Phi_{ref}) \tag{3.95}$$

$$\Delta\Phi_2 = devsign \cdot (PHIG2_i - \Phi_{ref}) \tag{3.96}$$

$$\Phi_{sd} = EASUB + \frac{E_g}{2} - devsign \cdot min\left[\frac{E_g}{2}, \frac{kT}{q} \cdot \ln\left(\frac{NSD}{ni}\right)\right] \tag{3.97}$$

$$V_{fbsd} = devsign \cdot (PHIG1_i - \Phi_{sd}) \tag{3.98}$$

3.2 Terminal Voltages and Pre-conditioning

3.2.1 Terminal Voltages and V_{dsx} Calculation

$$V_{fgs} = V_{fg} - V_s \tag{3.99}$$

$$V_{fgd} = V_{fg} - V_d \tag{3.100}$$

$$V_{bgs} = V_{bg} - V_s \tag{3.101}$$

$$V_{bgd} = V_{bg} - V_d \tag{3.102}$$

$$V_{ds} = V_d - V_s \tag{3.103}$$

$$V_{gfb1} = V_{fgs} - \Delta\Phi_1 \tag{3.104}$$

$$V_{gfb2} = V_{bgs} - \Delta\Phi_2 \tag{3.105}$$

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.0004} - 0.02 \tag{3.106}$$

$$symmetry\ factor = \frac{1}{2}\left(V_{dsx} - V_{ds}\right) \tag{3.107}$$

$$V_{bgx} = V_{bgs} + symmetry\ factor \tag{3.108}$$

3.2.2 Back Gate Biasing Effect

If **p-well**

$$K_{vbg} = KBG0PW - \frac{0.5 \cdot KBG1PW}{cosh(DBGPW \cdot \frac{L_{eff}}{\lambda})} \tag{3.109}$$

$$K^*_{vbg} = KBG2PW + \frac{1}{2}\left[K_{vbg} - KBG2PW + \sqrt{(K_{vbg} - KBG2PW)^2 + 0.0001}\right] \tag{3.110}$$

If **n-well**

$$K_{vbg} = KBG0NW - \frac{0.5 \cdot KBG1NW}{cosh(DBGNW \cdot \frac{L_{eff}}{\lambda})} \tag{3.111}$$

$$K^*_{vbg} = KBG2NW + \frac{1}{2}\left[K_{vbg} - KBG2NW + \sqrt{(K_{vbg} - KBG2NW)^2 + 0.0001}\right] \tag{3.112}$$

$$\gamma_0 = -\frac{C_{ox2} \cdot C_{si}}{(C_{ox2} + C_{si}) \cdot C_{ox1}} \tag{3.113}$$

$$V_{gfb2eff} = V_{gfb2n} - symmetry\ factor \tag{3.114}$$

where, V_{gfb2n} is the clamp limit for the back-gate bias ($V_{gfb2n} = -1.2$). λ is characteristic length and defined in equation 3.133.

3.2.3 Back-gate Depletion

Parameter BPFACTORPW (BPFACTORNW for N-type back gate) is used to invoke the effect of back-plane doping in the model (i.e., BPFACTORPW (BPFACTORNW) $\neq 0$ to invoke the substrate depletion effect) and VKNEE1PW (VKNEE1NW) is used to set the back-gate voltage at which measured data starts deviating from straight line behavior.

***If* P-type back gate**

$$welsign = -1 \tag{3.115}$$

$$Vknee1 = VKNEE1PW \tag{3.116}$$

$$Vknee2 = VKNEE2PW \tag{3.117}$$

$$bpfactor = BPFACTORPW \tag{3.118}$$

***If* N-type back gate**

$$welsign = 1 \tag{3.119}$$

$$Vknee1 = VKNEE1NW \tag{3.120}$$

$$Vknee2 = VKNEE2NW \tag{3.121}$$

$$bpfactor = BPFACTORNW \tag{3.122}$$

$$\tag{3.123}$$

3.2.4 Calculation of Threshold Voltage Shift due to Substrate Depletion Effect

$$T_0 = \begin{cases} \sqrt{1 + \frac{max\left[welsign(V_{bgx} - Vknee1), 0\right]}{V_{subdep0}}} - 1 & \text{NMOS} \\ \sqrt{1 + \frac{max\left[-welsign(V_{bgx} + Vknee1), 0\right]}{V_{subdep0}}} - 1 & \text{PMOS} \end{cases} \tag{3.124}$$

$$V_{subdep0} = \frac{1}{2} \frac{q \cdot NBG\epsilon_{sub}}{C_{ox2}^2} \tag{3.125}$$

$$V_{subdep} = V_{subdep0} \cdot T_0^2 \tag{3.126}$$

$$T_1 = -V_{subdep0} + Vknee2 - 10^{-2} \tag{3.127}$$

$$V_{subdep} = -Vknee2 + \frac{1}{2}\left[T_1 + \sqrt{T_1^2 + 0.04 \cdot V_{subdep0}}\right] \tag{3.128}$$

$$\Delta V_{th,vbg} = \begin{cases} \gamma_0 \cdot K_{vbg}^* \cdot [V_{gfb2} - (welsign \cdot bpfactor \cdot V_{subdep}) - V_{gfb2eff}] & \text{NMOS} \\ \gamma_0 \cdot K_{vbg}^* \cdot [V_{gfb2} + (welsign \cdot bpfactor \cdot V_{subdep}) - V_{gfb2eff}] & \text{PMOS} \end{cases} \tag{3.129}$$

3.3 Short Channel Effects

3.3.1 Scale Length λ

$$\lambda_f = \sqrt{TSI \cdot \epsilon_{ratio} \cdot EOT1} \tag{3.130}$$

$$\lambda_s = \sqrt{TSI \cdot \left(\epsilon_{ratio} \cdot EOT1 + \frac{3}{8} \cdot TSI\right)} \tag{3.131}$$

$$T_0 = \frac{V_{gfb1} \cdot EOT2 \cdot \epsilon_{ratio} + V_{gfb2} \cdot (EOT1 \cdot \epsilon_{ratio} + TSI)}{t_{eff}} + symmetry\ factor \tag{3.132}$$

$$x_\lambda = \frac{1}{2} + \frac{1}{\pi} \tan^{-1}\left[ASCL + BSCL \cdot T_0\right]$$

$$\lambda = \lambda_s + x_\lambda(\lambda_f - \lambda_s) \tag{3.133}$$

3.3.2 Vt Roll-off

$$\phi_{st} = 0.4 + \Phi_B + PHIN_i \tag{3.134}$$

$$\Delta V_{th,SCE} = -\frac{0.5 \cdot DVT0}{cosh\left(DVT1 \cdot \frac{L_{eff}}{\lambda}\right) - 1} \cdot (V_{bi} - \phi_{st}) \tag{3.135}$$

3.3.3 Drain Induced Barrier Lowering (DIBL) and Drain Induced Threshold Voltage Shift (DITS)

$$\Delta V_{th,DIBL} = -\frac{0.5 \cdot (ETA0(T) + ETAB[L] \cdot V_{bgx})}{cosh\left(DSUB \cdot \frac{L_{eff}}{\lambda}\right) - 1} \cdot \left(V_{dsx} + ETA1[L] \cdot \sqrt{(V_{dsx} + 0.01)}\right) \tag{3.136}$$

$$+ DVTP0 \cdot \frac{1}{1 + DVTP2 \cdot \left(cosh\left(DSUB \cdot \frac{L_{eff}}{\lambda}\right) - 2\right)} \cdot (V_{dsx} + 0.01)^{DVTP1} \tag{3.137}$$

3.3.4 Vt Roll on/off at moderate channel lengths

$$\Delta V_{th,RSCE} = K1RSCE \cdot \left[\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1\right] \cdot \sqrt{\phi_{st}} \tag{3.138}$$

3.3.5 Vt Roll on/off at moderate channel lengths and high V_{ds}

$$\Delta V_{th,DSC} = -\frac{DSC0}{DSC1 + L_{eff}} \cdot V_{dsx} \tag{3.139}$$

3.3.6 Sub-threshold Slope Degradation

$$V_{bgxpos} = 0.5 \cdot \left(V_{bgx} + \sqrt{(V_{bgx}^2 + 4 \cdot \delta_2^2)}\right) \tag{3.140}$$

$$\delta_1 = (CDSCD + CBGCBGD \cdot V_{bgxpos}) \cdot V_{dsx} \tag{3.141}$$

$$\theta_{SCE} = \frac{0.5}{cosh\left(DVT1 \cdot \frac{L_{eff}}{\lambda}\right) - 1} \tag{3.142}$$

$$C_{dsc} = CBGCBG0 \cdot V_{bgx} + CBGCBG0P \cdot V_{bgx}^2 \tag{3.143}$$
$$+ \theta_{SCE} \cdot \left(CDSC + CBGCBG \cdot V_{bgx} + CBGCBGP \cdot V_{bgx}^2 + \delta_1\right)$$

$$n = 1 + \frac{CIT + C_{dsc}}{C_{ox1} + C_{si} \parallel C_{ox2}} \tag{3.144}$$

where δ_2 is defined in equation 3.17.

3.3.7 Body Doping Effects

$$\Delta V_{th,nbody} = \frac{q \cdot NBODY \cdot TSI}{C_{ox1}} \left[1 - \frac{0.5 \cdot TSI}{TSI + \epsilon_{ratio} \cdot EOT2}\right] \tag{3.145}$$

3.3.8 Cumulative Threshold Voltage Adder

$$\Delta V_{th,all} = \Delta V_{th,vtroll} + \Delta V_{th,dibl} + \Delta V_{th,rsce} + \Delta V_{th,dsc} + \Delta V_{th,nbody} + \Delta V_{th,temp} + \Delta V_{th,vbg} \tag{3.146}$$

3.4 Surface Potential Calculation

Surface Potential is computed solving the Poisson's equation in silicon body [2]

$$E_{S1}^2 - E_{S2}^2 = \frac{2N_{DOS}kT}{\epsilon_{Si}} \left(e^{\frac{\psi_{s1} - V_{ch}}{v_{tm}}} - e^{\frac{\psi_{s2} - V_{ch}}{v_{tm}}}\right) \tag{3.147}$$

where N_{DOS} is the conduction band/valence band density of states for NMOS/PMOS transistor and V_{ch} is the channel potential. E_{S1}, the front side electric field and E_{S2}, the back side electric field are given by

$$E_{S1} = \frac{C_{ox1}(V_{gfb1eff} - \psi_{s1})}{\epsilon_{si}} \tag{3.148}$$

$$E_{S2} = \frac{C_{ox2}(V_{gfb2eff} - \psi_{s2})}{\epsilon_{si}} \tag{3.149}$$

where

$$V_{gfb1eff} = V_{gfb1} - \Delta V_{th,all} \tag{3.150}$$
$$V_{gfb2eff} = V_{gfb2n} \tag{3.151}$$

Equation (3.147) is simplified, similar to [3], replacing v_{tm} by nv_{tm} and neglecting the second exponential term on right side. Further approximating ψ_{s2} to be

$$\psi_{s2} = \frac{C_{si}}{C_{si} + C_{ox2}}\psi_{s1} + \frac{C_{ox2}}{C_{si} + C_{ox2}}V_{gfb2eff} \tag{3.152}$$

The simplified Poisson's equation is obtained as

$$\left(C_{ox1}\frac{V_{gfb1eff} - \psi_{s1}}{\epsilon_{Si}}\right)^2 - \left(\frac{V_{gfb2eff} - \psi_{s1}}{TSI + \frac{\epsilon_{si}}{\epsilon_{ox}}EOT2}\right)^2 = \frac{2N_{DOS}kT}{\epsilon_{Si}}\left(e^{\frac{\psi_{s1}-V_{ch}}{nv_{tm}}}\right) \tag{3.153}$$

This is rewritten as

$$f(x) \equiv \left(\frac{\nu_{gfb1} - x}{G}\right)^2 - B_{sq}\left(\nu_{gfb2} - x\right)^2 - e^{(x-\nu_{ch})} = 0 \tag{3.154}$$

where

$$\nu_{gfb1} = \frac{V_{gfb1eff}}{nv_{tm}} \tag{3.155}$$
$$\nu_{gfb2} = \frac{V_{gfb2eff}}{nv_{tm}} \tag{3.156}$$
$$\nu_{ch} = \frac{V_{ch}}{nv_{tm}} \tag{3.157}$$
$$x = \frac{\psi_{s1}}{nv_{tm}} \tag{3.158}$$
$$G = \frac{EOT1}{\epsilon_{ox}}\sqrt{\frac{2qN_{DOS}\epsilon_{si}}{nv_{tm}}} \tag{3.159}$$
$$B_{sq} = \left(\frac{1}{TSI} + \frac{\epsilon_{si}}{\epsilon_{ox}}EOT2\sqrt{\frac{\epsilon_{si}nv_{tm}}{2qN_C}}\right)^2 \tag{3.160}$$

The implicit equation (3.154) is solved using an iterative Halley's algorithm for a maximum of four iterations stopping when the error in surface potential solution is below 1 nV. Halley's algorithm is a second order Householder's method and can be written as

$$x_{n+1} = x_n - \frac{2f(x)f'(x)}{2[f'(x)]^2 - f(x)f''(x)} \tag{3.161}$$

where the iterant solutions x_n, x_{n+1} are related using $f'(x)$ and $f''(x)$, the first and second derivatives of equation(3.154) with respect to x. The initial guess for x is taken to be ψ^0_{s1}/nv_{tm}, where ψ^0_{s1} is the solution of (3.162). Equation (3.162) is obtained simplifying (3.147), assuming back-gate to remain always in very weak inversion, reducing it to become a function of only the front-gate parameters.

$$\left(C_{ox1}\frac{V_{gfb1eff}-\psi^0_{s1}}{\epsilon_{Si}}\right)^2=\frac{2N_{DOS}kT}{\epsilon_{Si}}\left(e^{\frac{\psi^0_{s1}-V_{ch}}{nv_{tm}}}\right) \tag{3.162}$$

The implicit equation (3.162) is solved using two iterations of Halley's algorithm, the solution to (3.162) is always stable and $\tilde{\psi}^0_{s1}$ given by (3.163), as the intial guess [4].

$$\tilde{\psi}^0_{s1}=\begin{cases}V_{gfb1eff} & \text{if } V_{gfb1eff}\leq 0\\ min\Big[V_{gfb1eff},\Big(V_{ch}+2nv_{tm}\ln[\frac{V_{gfb1eff}C_{ox1}}{\sqrt{2qN_cnv_{tm}\epsilon_{si}}}]\Big)\Big] & \text{if } V_{gfb1eff}>0\end{cases} \tag{3.163}$$

Once x satisfying (3.154) is known, ψ_{s1} is obtained from x using (3.164) and ψ_{s2} is obtained from ψ_{s1} using (3.152).

$$\psi_{s1}=x\cdot nv_{tm} \tag{3.164}$$

Equation (3.154) is solved once at the source side, with $V_{ch}=0$, and once at drain side, with $V_{ch}=V_{ds}$, to obtain the surface potentials at the two ends of the channel. More details can be found in [2]. The electric field and total inversion charges are then obtained as follows.

3.5 Calculation of Integrated Inversion Charge Density

As shown below, for CHARGEMOD=0 (default), the inversion charge density at source and drain ends in the body is calculated using [2].

3.5.1 For CHARGEMOD=0

At source end: ($V_{ch} = 0$)

$$\psi_{fs} = \psi_{s1} \tag{3.165}$$

$$\psi_{bs} = \psi_{s2} \tag{3.166}$$

$$E_{S1} = \frac{V_{gfb1eff} - \psi_{fs}}{EOT1} \tag{3.167}$$

$$E_{S2} = \frac{\psi_{fs} - \psi_{bs}}{TSI} \tag{3.168}$$

$$T_1 = \frac{1}{2}(\psi_{fs} - \psi_{bs}) + \frac{1}{2}\sqrt{((\psi_{fs} - \psi_{bs})^2 + 0.000004 * (nv_{tm})^2)} \tag{3.169}$$

$$Q_{tots} = \frac{2qN_{DOS}nv_{tm}}{E_{S1} + E_{S2}} \exp\frac{(\psi_{bs} - V_{ch})}{nv_{tm}} \exp(\frac{T_1}{nv_{tm}} - 1) \tag{3.170}$$

At drain end: ($V_{ch} = V_{ds}$)

$$\psi_{fd} = \psi_{s1} \tag{3.171}$$

$$\psi_{bd} = \psi_{s2} \tag{3.172}$$

$$E_{S1} = \frac{V_{gfb1eff} - \psi_{fd}}{EOT1} \tag{3.173}$$

$$E_{S2} = \frac{\psi_{fd} - \psi_{bd}}{TSI} \tag{3.174}$$

$$T_1 = \frac{1}{2}(\psi_{fd} - \psi_{bd}) + \frac{1}{2}\sqrt{((\psi_{fd} - \psi_{bd})^2 + 0.000004 * (nv_{tm})^2)} \tag{3.175}$$

$$Q_{totd} = \frac{2qN_{DOS}nv_{tm}}{E_{S1} + E_{S2}} \exp\frac{(\psi_{bd} - V_{ch})}{nv_{tm}} \exp(\frac{T_1}{nv_{tm}} - 1) \tag{3.176}$$

For body thickness less than 2 nm, a more accurate formulation of inversion charge density is needed. [3] develops the inversion charge density model valid for any generic body thickness and CHARGEMOD=1 makes use of this model. The increase in accuracy comes at a cost of slight increase in computation time.

3.5.2 For CHARGEMOD=1

$$\mathcal{E}_1 = \frac{V_{gfb1eff} - \psi_{s1}}{\epsilon_{ratio} \cdot EOT1} \tag{3.177}$$

$$A = \frac{2qN_{DOS}nv_{tm}}{\epsilon_{si}} \tag{3.178}$$

$$D = \mathcal{E}_1^2 - A \cdot \exp\left(\frac{\psi_{s1} - V_{ch}}{nv_{tm}}\right) \tag{3.179}$$

If $D = 0$ then

$$T_1 = \exp\left(-\frac{\psi_{s1} - V_{ch}}{2nv_{tm}}\right) + \frac{\sqrt{A} \cdot TSI}{2nv_{tm}} \tag{3.180}$$

$$\mathcal{E}_2 = \frac{\sqrt{A}}{T_1} \tag{3.181}$$

$$\tag{3.182}$$

If $D < 0$ then

$$\theta_{20} = \frac{\sqrt{-D}}{nv_{tm}} \cdot \frac{TSI}{2} - \cos^{-1}\left[\sqrt{\frac{-D}{A}} e^{-\frac{\psi_{s1} - V_{ch}}{nv_{tm}}}\right] \tag{3.183}$$

$$\theta_{20}^* = \begin{cases} |\theta_{20}| & \mathcal{E}_1 > 0 \\ \theta_{20} & \mathcal{E}_1 \leq 0 \end{cases} \tag{3.184}$$

$$\mathcal{E}_2 = -\sqrt{-D} \cdot tan(\theta_{20}^*) \tag{3.185}$$

If $D > 0$ then

$$C = \frac{exp\left(\frac{-sgn(\mathcal{E}_1) \cdot \sqrt{D} \cdot TSI}{2nv_{tm}}\right)}{\sqrt{\frac{D}{A}\exp\left(-\frac{\psi_{s1} - V_{ch}}{nv_{tm}}\right) + 1} + \sqrt{\frac{D}{A}\exp\left(-\frac{\psi_{s1} - V_{ch}}{nv_{tm}}\right)}} \tag{3.186}$$

$$\mathcal{E}_2 = sgn(\mathcal{E}_1) \cdot \sqrt{D} \cdot \frac{1 + C^2}{1 - C^2} \tag{3.187}$$

At source end: ($V_{ch} = 0$)

$$\psi_{fs} = \psi_{s1} \tag{3.188}$$

$$\psi_{bs} = \psi_{s2} \tag{3.189}$$

$$E_{S1} = \mathcal{E}_1 \tag{3.190}$$

$$E_{S2} = \mathcal{E}_2 \tag{3.191}$$

$$Q_{tots} = \epsilon_{si}(\mathcal{E}_1 - \mathcal{E}_2) \tag{3.192}$$

At drain end: ($V_{ch} = V_{ds}$)

$$\psi_{fd} = \psi_{s1} \tag{3.193}$$

$$\psi_{bd} = \psi_{s2} \tag{3.194}$$

$$E_{S1} = \mathcal{E}_1 \tag{3.195}$$

$$E_{S2} = \mathcal{E}_2 \tag{3.196}$$

$$Q_{totd} = \epsilon_{si}(\mathcal{E}_1 - \mathcal{E}_2) \tag{3.197}$$

3.6 Drain Saturation Voltage

The drain saturation voltage model is calculated after the source-side surface potential (ψ_s) has been calculated. V_{dseff} is subsequently used to compute the drain-side surface potential (ψ_d).

3.6.1 Electric Field Calculations

$$\eta = \begin{cases} \frac{1}{2} \cdot ETAMOB & \text{for NMOS} \\ \frac{1}{3} \cdot ETAMOB & \text{for PMOS} \end{cases} \tag{3.198}$$

$$q_{is} = \frac{Q_{tots}}{C_{ox1}} \tag{3.199}$$

$$q_{bs} = \frac{q \cdot NBODY \cdot TSI}{C_{ox1}} \tag{3.200}$$

$$T_2 = \eta \cdot q_{is} + q_{bs} + E_{S2} \cdot \frac{\epsilon_{si}}{C_{ox1}} \tag{3.201}$$

$$T_3 = \frac{1}{2}(T_2 + \sqrt{T_2^2 + 0.001}) \tag{3.202}$$

$$E_{effs} = 10^{-8} \cdot \frac{C_{ox1}}{\epsilon_{si}} \cdot T_3 \tag{3.203}$$

3.6.2 Drain Saturation Voltage

$$D_{mobs} = 1 + (UA(T) + UC(T) \cdot V_{bgs}) \cdot (E_{effs})^{EU} + \frac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{is}}{10^{-2}/C_{ox1}}\right)\right)^{UCS(T)}} \tag{3.204}$$

$$E_{sat} = \frac{2 \cdot VSAT(T)}{\mu_0(T) D_{mobs}} \tag{3.205}$$

Note: RDSMOD is parasitic resistance mode selector switch. Details of RDSMOD is discussed in Section 3.15.

$$\underline{RDSMOD = 0, 2}$$

$$T_6 = KSATIV \cdot \left(\frac{Q_{tots}}{C_{ox1} + C_{ox2}} + 2V_t \cdot KSUBIV\right) \tag{3.206}$$

$$a = 2W \cdot VSAT \cdot C_{ox1} \cdot R_{ds}(V) \tag{3.207}$$

$$b = T_6 + E_{sat}L_{eff} + 3T_6W_{eff} \cdot VSAT \cdot C_{ox1} \cdot R_{ds}(V) \tag{3.208}$$

$$c = T_6 \cdot [E_{sat}L_{eff} + T_6 \cdot a] \tag{3.209}$$

$$V_{dsat} = \frac{b - \sqrt{b^2 - 2ac}}{a} \tag{3.210}$$

$\underline{RDSMOD = 1}$

$$V_{dsat} = \frac{E_{sat}L_{eff}\left(\frac{Q_{tots}}{C_{ox1}+C_{ox2}}\right)}{E_{sat}L_{eff} + \frac{Q_{tots}}{C_{ox1}+C_{ox2}}} \tag{3.211}$$

Then [5],

$$V_{dseff} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{dsat}}\right)^{\frac{1}{MEXP}}\right]^{MEXP}} \tag{3.212}$$

3.7 Average Field, Potential, and Charge Calculation

$$q_{ia} = \frac{Q_{tots} + Q_{totd}}{2C_{ox1}} \tag{3.213}$$

$$q_{ba} = \frac{qN_A \cdot TSI}{C_{ox1}} \tag{3.214}$$

$$E_{ba} = \frac{E_{bs} + E_{bd}}{2} \tag{3.215}$$

$$\Delta\psi = \psi_{fd} - \psi_{fs} \tag{3.216}$$

$$\Delta q_i = \frac{Q_{tots} - Q_{totd}}{C_{ox1}} \tag{3.217}$$

(3.218)

3.8 Quantum Mechanical Effects

Effects that arise due to electrical confinement in the ultra-thin body SOI are dealt in this section. Currently, only the C-V effect, the bias-dependence of effective oxide thickness due to the inversion charge centroid being away from the interface, is included in the model.

$$T5 = 1 + \left(\frac{q_{ia} + ETAQM_i \cdot q_{ba}}{QM0_i}\right)^{PQM_i} \tag{3.219}$$

$$C_{ox,eff} = \begin{cases} \frac{3.9\cdot\epsilon_0}{EOT1P\frac{3.9}{EPSROX1} + \frac{T_{cen0}}{T5}\cdot\frac{QMTCENCV_i}{\epsilon_{ratio}}} & \text{if } QMTCENCV_i = 1 \\ C_{ox1P} & \text{if } QMTCENCV_i = 0 \end{cases} \tag{3.220}$$

(3.221)

3.9 Mobility Degradation

Eeffective transverse field (E_{effm}) gets modified by introducing the parameter CHARGEWF. This parameter changes the average charge which goes into the effective transverse field calculation (+1:source-side, 0:middle, -1:drain-side).

$$q_{ia2} = \begin{cases} 0.5 \cdot (q_{is} + q_{id}) & \text{for } CHARGEWF = 0 \\ 0.5 \cdot (q_{is} + q_{id}) + CHARGEWF \cdot \left(1 - exp(-\frac{a}{2}) \cdot 0.5 \cdot \Delta q_i\right) & \text{for } CHARGEWF \neq 0 \end{cases} \tag{3.222}$$

where a is define in equation 3.207. The mobility model is based on the BSIM4 model [6].

$$T_2 = \eta \cdot q_{ia2} + q_{ba} + E_{ba} \cdot \frac{\epsilon_{si}}{C_{ox1}} \tag{3.223}$$

$$T_3 = \frac{1}{2}(T_2 + \sqrt{T_2^2 + 0.001}) \tag{3.224}$$

$$E_{effm} = 10^{-8} \cdot \frac{C_{ox1}}{\epsilon_{si}} \cdot T_3 \tag{3.225}$$

$$D_{mob0} = 1 + (UA(T) + UC(T) \cdot V_{bgx}) \cdot (E_{effm})^{EU} + \frac{UD(T) + UDB \cdot V_{bgx}}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{ia}}{10^{-2}/C_{ox1}}\right)\right)^{UCS(T)}} \tag{3.226}$$

$$D_{mob} = \frac{D_{mob0}}{U0MULT} \tag{3.227}$$

3.10 Lateral Non-uniform Doping Model

Lateral non-uniform doping along the length of the channel leads to I-V and C-V display different threshold voltages. However the self-consistent surface potential based I-V and C-V model doesn't allow for the usage of different Vth values. A straightforward method would be to re-compute the surface potentials at the source and drain end twice for I-V and C-V separately breaking the consistency but at the expense of computation time. The below model has been introduced as a multiplicative factor to the drain current (I-V) to allow for that Vth shift. This model should be exercised after the C-V extraction step to match the Vth for the subthreshold region Id,lin-Vg curve. Parameter K0 is used to fit the subthresold region, while parameter K0SI helps reclaim the fit in the inversion region.

$$M_{nud} = \exp\left(-\frac{K0(T)}{K0SI(T) \cdot q_{ia} + 2.0 \cdot \frac{nkT}{q}}\right) \tag{3.228}$$

A word of CAUTION: The above lateral non-uniform doping model is empirical and has its limits as to how much Vth shift can be achieved without distorting the I-V curve. Over usage could lead to

negative g_m or negative g_{ds}. The lateral non-uniform doping model could be used in combination with the mobility model to achieve high Vth shift between C-V and I-V curved to avoid any distortion of higher order derivatives.

3.11 Output Conductance

Channel length modulation and DIBL effects are considered to model the output conductance.

3.11.1 Channel Length Modulation

$$\frac{1}{C_{clm}} = \begin{cases} PCLM + PCLMG \cdot q_{ia} & \text{for } PCLMG \geq 0 \\ \frac{1}{\frac{1}{PCLM} - PCLMG \cdot q_{ia}} & \text{for } PCLMG < 0 \end{cases} \tag{3.229}$$

$$M_{clm} = \begin{cases} 1 + \frac{1}{C_{clm}} \ln\left[1 + \frac{V_{ds} - V_{dseff}}{V_{dsat} + E_{satL}} \cdot C_{clm}\right] & \text{for } PCLM > 0 \\ 1 & \text{for } PCLM \leq 0 \end{cases} \tag{3.230}$$

3.11.2 Output Conductance due to DIBL

$$PVAGfactor = \begin{cases} 1 + PVAG \cdot \frac{q_{ia}}{E_{sat} L_{eff}} & \text{for } PVAG > 0 \\ \frac{1}{1 - PVAG \cdot \frac{q_{ia}}{E_{sat} L_{eff}}} & \text{for } PVAG \leq 0 \end{cases} \tag{3.231}$$

$$\theta_{rout} = \frac{0.5 \cdot PDIBL1}{cosh\left(DROUT \cdot \frac{L_{eff}}{\lambda}\right) - 1} + PDIBL2 \tag{3.232}$$

$$V_{ADIBL} = \frac{q_{ia} + 2kT/q}{\theta_{rout}} \cdot \left(1 - \frac{V_{dsat}}{V_{dsat} + q_{ia} + 2kT/q}\right) \cdot PVAGfactor \tag{3.233}$$

$$M_{oc} = \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \cdot M_{clm} \tag{3.234}$$

M_{oc} is multiplied to I_{ds} in the final drain current expression.

3.12 Velocity Saturation

The following formulation models the current degradation factor due to velocity saturation in the linear region. It is adopted from the BSIM5 model [7, 8].

$$E_{sat1} = \frac{2 \cdot VSAT1(T)}{\mu_0(T) D_{mobs}} \tag{3.235}$$

$$\delta_{vsat} = DELTAVSAT \tag{3.236}$$

$$T_0 = 0.8 + VSATB(T) \cdot V_{bgx} \tag{3.237}$$

$$X_{sat} = 0.2 + \frac{\left[T_0 + \sqrt{{T_0}^2 + 0.01}\right]}{2} \tag{3.238}$$

$$D_{vsat} = \frac{1 + \sqrt{\delta_{vsat} + \left(\frac{\Delta q_i}{E_{sat1} L_{eff}} \cdot X_{sat}\right)^2}}{1 + \sqrt{\delta_{vsat}}} \tag{3.239}$$

$$+ \frac{1}{2} \cdot (PTWG(T) - PTWGB \cdot V_{bgxpos} - PTWGB2 \cdot V_{bgx}) \cdot q_{ia} \cdot \Delta q_i^2$$

3.13 Drain Current Model

$$i_{ds0} = q_{ia} \cdot \Delta\psi + V_t \cdot \Delta q_i \tag{3.240}$$

$$I_{ds0} = \mu_0 \cdot C_{ox1} \cdot \frac{W_{eff}}{L_{eff}} \cdot i_{ds0} \cdot \frac{M_{oc}}{D_{mob} \cdot D_r \cdot D_{vsat}} \tag{3.241}$$

$$I_{ds} = I_{ds0} \cdot NF \tag{3.242}$$

See section 3.15 for the definition of series resistance term Dr.

3.14 C-V Model

3.14.1 C-V Model (Front Surface)

$$T_0 = \frac{C_{ox2}}{C_{ox1}} \cdot \frac{C_{si}}{C_{ox2} + C_{si}} \tag{3.243}$$

$$T_1 = \frac{1 + T_0}{2} \tag{3.244}$$

$$T_2 = V_{gfb1eff} + T_0 \cdot V_{gfb2eff} + v_t \cdot \left(1 + \frac{C_{ox2}}{C_{ox1}}\right) \tag{3.245}$$

$$T_3 = \psi_{fs} + \psi_{fd} \tag{3.246}$$

$$T_4 = \psi_{fd} - \psi_{fs} \tag{3.247}$$

$$T_5 = V_{gfb1eff} - \frac{T_3}{2} \tag{3.248}$$

$$T_6 = \frac{T_1 \cdot T_4}{6(T_2 - T_1 T_3)} \tag{3.249}$$

$$q_{fg} = T_5 + T_6 T_4 + \Delta V_{th,vbg} \tag{3.250}$$

$$q_{d1} = \frac{T_5}{2} + \frac{T_6 T_4}{10} - \frac{T_6/T_1}{10(T_2 - T_1 T_3)} (5T_2 - 4T_1\psi_{fd} - 6T_1\psi_{fs}) \cdot (T_2 - 2T_1\psi_{fd}) \tag{3.251}$$

3.14.2 C-V Model (Back Surface)

$$T_0 = \frac{C_{ox1}}{C_{ox2}} \cdot \frac{C_{si}}{C_{ox1} + C_{si}} \tag{3.252}$$

$$T_1 = \frac{1 + T_0}{2} \tag{3.253}$$

$$T_2 = V_{gfb2eff} + T_0 \cdot V_{gfb1eff} + V_t \cdot \left(1 + \frac{C_{ox1}}{C_{ox2}}\right) \tag{3.254}$$

$$T_3 = \psi_{bs} + \psi_{bd} \tag{3.255}$$

$$T_4 = \psi_{bd} - \psi_{bs} \tag{3.256}$$

$$T_5 = V_{gfb2eff} - \frac{T_3}{2} \tag{3.257}$$

$$T_6 = \frac{T_1 \cdot T_4}{6(T_2 - T_1 T_3)} \tag{3.258}$$

$$q_{bg} = \frac{C_{ox2}}{C_{ox1}}(T_5 + T_6 T_4 - \Delta V_{th,vbg}) \tag{3.259}$$

$$q_{d2} = \frac{C_{ox2}}{C_{ox1}}\left[\frac{T_5}{2} + \frac{T_6 T_4}{10} - \frac{T_6/T_1}{10(T_2 - T_1 T_3)}\left(5T_2 - 4T_1\psi_{bd} - 6T_1\psi_{bs}\right) \cdot \left(T_2 - 2T_1\psi_{bd}\right)\right] \tag{3.260}$$

3.14.3 Mobility Degradation for C-V Calculation

$$\eta_{cv} = \begin{cases} \frac{1}{2} & \text{for NMOS} \\ \frac{1}{3} & \text{for PMOS} \end{cases} \tag{3.261}$$

Note: η is used in mobility degradation calculation hence user can tune parameter ETAMOB in I-V fitting while η_{cv} is used in mobility degradation calculation for C-V fitting.

$$E_{effa,cv} = 10^{-8} \cdot \left(\frac{q_{ba} + \eta_{cv} \cdot q_{ia}}{\epsilon_{ratio} \cdot EOT}\right) \tag{3.262}$$

$$D_{mob,cv} = 1 + UA(T) \cdot (E_{effa,cv})^{EU} + \frac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{ia}}{q_{ba}}\right)\right)^{UCS(T)}} \tag{3.263}$$

$$D_{mob,CV} = \frac{D_{mob,cv}}{U0MULT} \tag{3.264}$$

3.14.4 Velocity Saturation for C-V Calculation

$$E_{satCV} = \frac{2 \cdot VSATCV(T) \cdot D_{mob,CV}}{\mu_0(T)} \tag{3.265}$$

$$E_{satCVL} = E_{satCV} L_{effCV} \tag{3.266}$$

3.14.5 Channel Length Modulation for C-V Calculation

Channel length modulation causes an effective reduction of the intrinsic capacitance at high drain bias. This reduction factor is modeled by $M_{clm,CV}$:

$$M_{clm,CV} = 1 + \frac{1}{PCLMCV} \ln \left[1 + \frac{V_{ds} - V_{dseff}}{Vdsat + E_{satCVL}} \cdot PCLMCV \right] \tag{3.267}$$

3.14.6 Assign Variables

$$Q_{fg} = \frac{NF}{M_{clm,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot q_{fg} \tag{3.268}$$

$$Q_{bg} = \frac{NF}{M_{clm,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot q_{bg} \tag{3.269}$$

$$Q_{d,intrinsic} = \frac{NF}{M_{clm,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot (-q_{d1} - q_{d2}) \tag{3.270}$$

$$Q_{s,intrinsic} = -Q_{d,intrinsic} - Q_{fg} - Q_{bg} \tag{3.271}$$

3.15 Parasitic Resistances and Capacitance Models

In this section we will describe the models for parasitic resistances and capacitances in BSIM-IMG.

BSIM-IMG models the parasitic source/drain resistance in two components: a bias-dependent extension resistance and a bias-independent diffusion resistance.

The parasitic capacitance model in BSIM-IMG (adopted from BSIM-CMG) includes a bias-indepedent outer fringe capacitance, a bias-dependent inner fringe capacitance, a bias-dependent overlap capacitance, and substrate capacitances.

3.15.1 Bias-independent Diffusion Resistance

$R_{s,geo}$ and $R_{d,geo}$ are the source and drain diffusion resistances. The diffusion resistances are simply calculated as the sheet resistance ($RSHS$,$RSHD$) times the number of squares (NRS,NRD):

$$R_{s,geo} = NRS \cdot RSHS \tag{3.272}$$

$$R_{d,geo} = NRD \cdot RSHD \tag{3.273}$$

3.15.2 Bias-dependent extension resistance

The bias-dependent extension resistance model is adopted from BSIM4 [6]. There are two options for this bias dependent component. In BSIM3 models $R_{ds}(V)$ is modeled internally through the I-V

equation and symmetry is assumed for the source and drain sides. BSIM4 and BSIM-CMG keep this option for the sake of simulation efficiency. In addition, BSIM4 and BSIM-CMG allow the source extension resistance $R_s(V)$ and the drain extension resistance $R_d(V)$ to be external and asymmetric (i.e. $R_s(V)$ and $R_d(V)$ can be connected between the external and internal source and drain nodes, respectively; furthermore, $R_s(V)$ does not have to be equal to $R_d(V)$). This feature makes accurate RF CMOS simulation possible.

The internal $R_{ds}(V)$ option can be invoked by setting the model selector $RDSMOD = 0$ (internal) and $RDSMOD = 2$ (internal and geometry dependent), the external one for $R_s(V)$ and $R_d(V)$ by setting $RDSMOD = 1$ (external). The expressions for source/drain series resistances are as follows:

$\underline{RDSMOD = 0}$ **(Internal)**

$$R_{ds}(V) = \frac{1}{NF \times Weff^{WR}} \cdot \left(RDSWMIN(T) + \frac{RDSW(T)}{1 + PRWG \cdot q_{ia}} \right) \tag{3.274}$$

$$D_r = 1.0 + NF \times \mu_0(T) \cdot C_{ox1} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{i_{ds0}}{\Delta q_i} \cdot \frac{1}{D_{mob} \cdot D_{vsat}} \cdot (R_{ds}(V)) \tag{3.275}$$

D_r goes into the denominator of the final I_{ds} expression.

$\underline{RDSMOD = 1}$ **(External)**

$$R_{ds}(V) = 0.0 \tag{3.276}$$

$$V_{gs,eff} = \frac{1}{2} \left[V_{gs} - V_{fbsd} + \sqrt{(V_{gs} - V_{fbsd})^2 + 10^{-4}} \right] \tag{3.277}$$

$$V_{gd,eff} = \frac{1}{2} \left[V_{gd} - V_{fbsd} + \sqrt{(V_{gd} - V_{fbsd})^2 + 10^{-4}} \right] \tag{3.278}$$

$$R_{source} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left(RSWMIN(T) + \frac{RSW(T)}{1 + PRWG \cdot V_{gs,eff}} \right) + R_{s,geo} \tag{3.279}$$

$$R_{drain} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left(RDWMIN(T) + \frac{RDW(T)}{1 + PRWG \cdot V_{gd,eff}} \right) + R_{d,geo} \tag{3.280}$$

$$D_r = 1.0 \tag{3.281}$$

$\underline{RDSMOD = 2}$ **(Internal and Geometry dependent)**

$$R_{ds}(V) = \frac{1}{NF \times Weff^{WR}} \cdot \left(R_{s,geo} + R_{d,geo} + RDSWMIN(T) + \frac{RDSW(T)}{1 + PRWG \cdot q_{ia}} \right) \tag{3.282}$$

$$D_r = 1.0 + NF \times \mu_0(T) \cdot C_{ox1} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{i_{ds0}}{\Delta q_i} \cdot \frac{1}{D_{mob} \cdot D_{vsat}} \cdot (R_{ds}(V)) \tag{3.283}$$

D_r goes into the denominator of the final I_{ds} expression.

3.15.3 Overlap Capacitances

$$T0 = V_{fgs} - V_{fbsd} + \delta_1 + PCOVBS1 \cdot (V_{bgs} - V_{fbsdbg} - PCOVBS0) \tag{3.284}$$

$$V_{fgs,ov} = \frac{1}{2}\left(T0 - \sqrt{T0^2 + 4\delta_1}\right) \tag{3.285}$$

$$T1 = NF \cdot W_{eff,CV} \cdot LOVS \cdot C_{ox1} \cdot V_{g,es} \tag{3.286}$$

$$T2 = \frac{1}{2} \cdot CKAPPAS \cdot \left[\sqrt{1 - \frac{4 \cdot V_{fgs,ov}}{CKAPPAS}} - 1\right] \tag{3.287}$$

$$Q_{fgs,ov} = T1 + NF \cdot W_{eff,CV} \cdot CGSL \cdot \left\{V_{fgs} - V_{fbsd} - V_{fgs,ov} - T2\right\} \cdot devsign \tag{3.288}$$

$$T0 = V_{fgs} - V_{fbsd} + \delta_1 + PCOVBD1 \cdot (V_{bgs} - V_{fbsdbg} - PCOVBD0) \tag{3.289}$$

$$V_{fgd,ov} = \frac{1}{2}\left(T0 - \sqrt{T0^2 + 4\delta_1}\right) \tag{3.290}$$

$$T1 = NF \cdot W_{eff,CV} \cdot LOVD \cdot C_{ox1} \cdot V_{g,ed} \tag{3.291}$$

$$T2 = \frac{1}{2} \cdot CKAPPAD \cdot \left[\sqrt{1 - \frac{4 \cdot V_{fgd,ov}}{CKAPPAD}} - 1\right] \tag{3.292}$$

$$Q_{fgd,ov} = T1 + NF \cdot W_{eff,CV} \cdot CGDL \cdot \left\{V_{fgd} - V_{fbsd} - V_{fgd,ov} - T2\right\} \cdot devsign \tag{3.293}$$

3.15.4 Outer Fringe Capacitances

$$Q_{fgs,of} = NF \cdot W_{eff,CV} \cdot CFS \cdot V_{g,es} \tag{3.294}$$
$$Q_{fgd,of} = NF \cdot W_{eff,CV} \cdot CFD \cdot V_{g,ed} \tag{3.295}$$

3.15.5 Source/drain to Substrate Capacitances

$$C_{sdbgsw0} = CSDBGSW \cdot \ln\left(1 + \frac{TSI}{EOT2}\right) \tag{3.296}$$
$$Q_{sbg} = NF \cdot [C_{ox2} \cdot AS + (PS - W) \cdot C_{sdbgsw0}] \cdot V_{s,bg} \tag{3.297}$$
$$Q_{dbg} = NF \cdot [C_{ox2} \cdot AD + (PD - W) \cdot C_{sdbgsw0}] \cdot V_{d,bg} \tag{3.298}$$

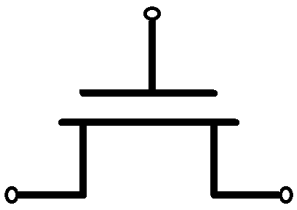


Figure 5: Gate resistance network for $RGATEMOD = 0$

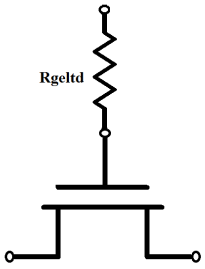


Figure 6: Gate resistance network for $RGATEMOD = 1$

3.16 Gate Electrode Resistance Model

BSIM-IMG provides two options for modeling gate electrode resistance. The model selector RGATEMOD is used to choose different options.

There are two model selectors for gate resistance network.

RGATEMOD = 0 (zero-resistance): In this case, no gate resistance is generated (see Figure 5).

RGATEMOD = 1 (constant-resistance): In this case, only the electrode gate resistance (bias-independent) is generated by adding an internal gate node (see Figure 6). *Rgeltd* is given by

$$Rgeltd = \frac{RSHG \cdot (XGW + \frac{W_{eff}}{3 \cdot NGCON})}{NGCON \cdot (L_{eff} - XGL) \cdot NF} \tag{3.299}$$

3.17 Impact Ionization Current

In a fully-depleted independent double-gate FET, the impact ionization current flows from drain to source.

$$I_{ii} = \frac{ALPHA0 + ALPHA1 \cdot L_{eff}}{L_{eff}} (V_{ds} - V_{dseff}) \cdot e^{\frac{-BETA0}{V_{ds} - V_{dseff}}} \cdot I_{ds} \tag{3.300}$$

3.18 Gate Induced Source/Drain Leakage

$$V_{fbsdbg} = devsign \cdot (PHIG2_i - \Phi_{sd}) \tag{3.301}$$

3.18.1 Gate Induced Drain Leakage (GIDL)

$$\begin{aligned} I_{gidl} &= AGIDL \cdot W_{eff} \cdot NF \\ &\times \left(\frac{V_{ds} - V_{fgs} - EGIDL + V_{fbsd} + VBGIDL \cdot \gamma_0 \cdot (V_{bgs} - V_{fbsdbg} - VBEGIDL)}{\epsilon_{ratio} \cdot EOT1} \right)^{PGIDL} \\ &\times \exp\left(- \frac{\epsilon_{ratio} \cdot EOT1 \cdot BGIDL}{V_{ds} - V_{fgs} - EGIDL + V_{fbsd} + VBGIDL \cdot \gamma_0 \cdot (V_{bgs} - V_{fbsdbg} - VBEGIDL)} \right) \end{aligned} \tag{3.302}$$

3.18.2 Gate Induced Source Leakage (GISL) Current

$$\begin{aligned} I_{gisl} &= AGISL \cdot W_{eff} \cdot NF \\ &\times \left(\frac{V_{ds} - V_{fgs} - EGISL + V_{fbsd} + VBGISL \cdot \gamma_0 \cdot (V_{bgs} - V_{fbsdbg} - VBEGISL)}{\epsilon_{ratio} \cdot EOT1} \right)^{PGISL} \\ &\times \exp\left(- \frac{\epsilon_{ratio} \cdot EOT1 \cdot BGISL}{V_{ds} - V_{fgs} - EGISL + V_{fbsd} + VBGISL \cdot \gamma_0 \cdot (V_{bgs} - V_{fbsdbg} - VBEGISL)} \right) \end{aligned} \tag{3.303}$$

3.19 Front Gate Tunneling Current

Tunneling through the back-gate dielectric is assumed to be negligible.

$$T_{ox,ratio} = \frac{1}{TOXP^2} \cdot \left(\frac{TOXREF}{TOXP} \right)^{NTOX} \tag{3.304}$$

3.19.1 Gate-to-Body current

I_{gb} is partitioned into a source component, I_{gbs} and a drain component, I_{gbd} in this section.

I_{gbinv} and I_{gbacc} calculated only if $IGBMOD = 1$

$$A = 3.75956 \times 10^{-7} \tag{3.305}$$

$$B = 9.82222 \times 10^{11} \tag{3.306}$$

$$V_{aux,igbinv} = NIGBINV \cdot \frac{kT}{q} \cdot \ln\left(1 + \exp\left(\frac{q_{ia} - EIGBINV}{NIGBINV \cdot kT/q}\right)\right) \tag{3.307}$$

$$\begin{aligned} I_{gbinv} &= W_{new} \cdot L_{eff} \cdot NF \cdot A \cdot T_{ox,ratio} \cdot V_{gbg} \cdot V_{aux,igbinv} \cdot Igtemp \\ &\times \exp\left(-B \cdot TOXP \cdot (AIGBINV - BIGBINV \cdot q_{ia}) \cdot (1 + CIGBINV \cdot q_{ia})\right) \end{aligned} \tag{3.308}$$

$$A = 4.97232 \times 10^{-7} \tag{3.309}$$

$$B = 7.45669 \times 10^{11} \tag{3.310}$$

$$V_{fbzb} = \Delta\Phi_1 - E_g/2 - \phi_B \tag{3.311}$$

$$T0 = V_{fbzb} - V_{gbg} \tag{3.312}$$

$$T1 = T0 - 0.02; \tag{3.313}$$

$$V_{aux,igbacc} = NIGBACC \cdot \frac{kT}{q} \cdot \ln\left(1 + \exp\left(\frac{T0}{NIGBACC \cdot kT/q}\right)\right) \tag{3.314}$$

$$V_{oxacc} = \begin{cases} 0.5 \cdot [T1 + \sqrt{(T1)^2 - 0.08 \cdot V_{fbzb}}] & V_{fbzb} \leq 0 \\ 0.5 \cdot [T1 + \sqrt{(T1)^2 + 0.08 \cdot V_{fbzb}}] & V_{fbzb} > 0 \end{cases} \tag{3.315}$$

$$I_{gbacc} = W_{new} \cdot L_{eff} \cdot NF \cdot A \cdot T_{ox,ratio} \cdot V_{gbg} \cdot V_{aux,igbacc} \cdot Igtemp$$
$$\times \exp\left(-B \cdot TOXP \cdot (AIGBACC - BIGBACC \cdot V_{oxacc}) \cdot (1 + CIGBACC \cdot V_{oxacc})\right) \tag{3.316}$$

I_{gb} mostly flows into the source because the potential barrier for holes is lower at the source, which has a lower potential. To ensure continuity when V_{ds} switches sign, I_{gb} is partitioned into a source component, I_{gbs} and a drain component, I_{gbd} using a partition function:

$$T0 = tanh\left(\frac{0.6 \cdot q \cdot V_{ds}}{kT}\right) \tag{3.317}$$

$$W_f = 0.5 + 0.5 \cdot T0 \tag{3.318}$$

$$W_r = 0.5 - 0.5 \cdot T0 \tag{3.319}$$

$$I_{gbs} = (I_{gbinv} + I_{gbacc}) \cdot W_f \tag{3.320}$$

$$I_{gbd} = (I_{gbinv} + I_{gbacc}) \cdot W_r \tag{3.321}$$

3.19.2 Gate-to-Channel current

I_{gc} is calculated only for $IGCMOD = 1$

$$A = \begin{cases} 4.97232 \times 10^{-7} & \text{for NMOS} \\ 3.42536 \times 10^{-7} & \text{for PMOS} \end{cases} \tag{3.322}$$

$$B = \begin{cases} 7.45669 \times 10^{11} & \text{for NMOS} \\ 1.16645 \times 10^{12} & \text{for PMOS} \end{cases} \tag{3.323}$$

$$T0 = q_{ia} \cdot (V_{gbg} - 0.5 \cdot V_{dsx} + 0.5 \cdot V_{bgs} + 0.5 \cdot V_{bgd}) \tag{3.324}$$

$$I_{gc0} = W_{new} \cdot L_{eff} \cdot NF \cdot A \cdot T_{ox,ratio} \cdot Igtemp \cdot T0 \\ \times \exp\left(-B \cdot TOXP \cdot (AIGC - BIGC \cdot (V_{gfb1} - DIGC \cdot \psi_{fs})) \cdot (1 + CIGC \cdot (V_{gfb1} - DIGC \cdot \psi_{fs}))\right) \tag{3.325}$$

$$V_{dseffx} = \sqrt{V_{dseff}^2 + 0.01} - 0.1 \tag{3.326}$$

$$I_{gcs} = I_{gc0} \cdot \frac{PIGCD \cdot V_{dseffx} + \exp(PIGCD \cdot V_{dseffx}) - 1.0 + 10^{-4}}{PIGCD^2 \cdot V_{dseffx}^2 + 2 \cdot 10^{-4}} \tag{3.327}$$

$$I_{gcd} = I_{gc0} \cdot \frac{1.0 - (PIGCD \cdot V_{dseffx} + 1.0)\exp(-PIGCD \cdot V_{dseffx}) + 10^{-4}}{PIGCD^2 \cdot V_{dseffx}^2 + 2 \cdot 10^{-4}} \tag{3.328}$$

3.19.3 Gate-to-Source/Drain current

I_{gs}, I_{gd} are calculated only for $IGCMOD = 1$

$$A = \begin{cases} 4.97232 \times 10^{-7} & \text{for NMOS} \\ 3.42536 \times 10^{-7} & \text{for PMOS} \end{cases} \tag{3.329}$$

$$B = \begin{cases} 7.45669 \times 10^{11} & \text{for NMOS} \\ 1.16645 \times 10^{12} & \text{for PMOS} \end{cases} \tag{3.330}$$

$$V'_{gs} = \sqrt{(V_{gs} - V_{fbsd} + DIGS \cdot \gamma_0 \cdot (V_{bgs} - V_{fbsdbg}))^2 + 10^{-4}} \tag{3.331}$$

$$V'_{gd} = \sqrt{(V_{gd} - V_{fbsd} + DIGD \cdot \gamma_0 \cdot (V_{bgs} - V_{fbsdbg}))^2 + 10^{-4}} \tag{3.332}$$

$$i_{gsd,mult} = Igtemp \cdot \frac{W_{new} \cdot A}{(TOXP \cdot POXEDGE)^2} \cdot \left(\frac{TOXREF}{TOXP \cdot POXEDGE} \right)^{NTOX} \tag{3.333}$$

$$I_{gs} = NF \cdot i_{gsd,mult} \cdot DLCIGS \cdot V_{gs} \cdot V'_{gs} \times \exp\left(-B \cdot TOXP \cdot POXEDGE \cdot \left(AIGS - BIGS \cdot V'_{gs}\right) \cdot \left(1 + CIGS \cdot V'_{gs}\right)\right) \tag{3.334}$$

$$I_{gd} = NF \cdot i_{gsd,mult} \cdot DLCIGD \cdot V_{gd} \cdot V'_{gd} \times \exp\left(-B \cdot TOXP \cdot POXEDGE \cdot \left(AIGD - BIGD \cdot V'_{gd}\right) \cdot \left(1 + CIGD \cdot V'_{gd}\right)\right) \tag{3.335}$$

3.20 Non Quasi-static Models

This version offers one Non quasi-static (NQS) model. This can be turned on/off using the NQSMOD switch. Setting $NQSMOD = 0$ turns off NQS models and switches to plain quasi-static calculations.

3.20.1 Gate Resistance Model ($NQSMOD = 1$)

NQS effects for $NQSMOD = 1$ is modeled through an effective intrinsic input resistance, R_{ii} [9] as shown in Figure 7. This would introduce a gate node in between the intrinsic gate and the physical gate electrode resistance (RGATEMOD). This node collapses to the intrinsic gate if the user turns off this model.

$$\beta = \mu_0 \cdot C_{ox1} \cdot \frac{W_{eff}}{L_{eff}} \tag{3.336}$$

$$I_{dsovVds} = \frac{\beta \cdot M_{oc} \cdot q_{ia}}{D_{mob} \cdot D_r \cdot D_{vsat}} \tag{3.337}$$

$$\frac{1}{R_{ii}} = NF \cdot XRCRG1 \cdot \left(I_{dsovVds} + XRCRG2 \cdot \frac{\mu_{eff} \cdot C_{ox1} \cdot W_{eff} \cdot kT}{q \cdot L_{eff}} \right) \tag{3.338}$$

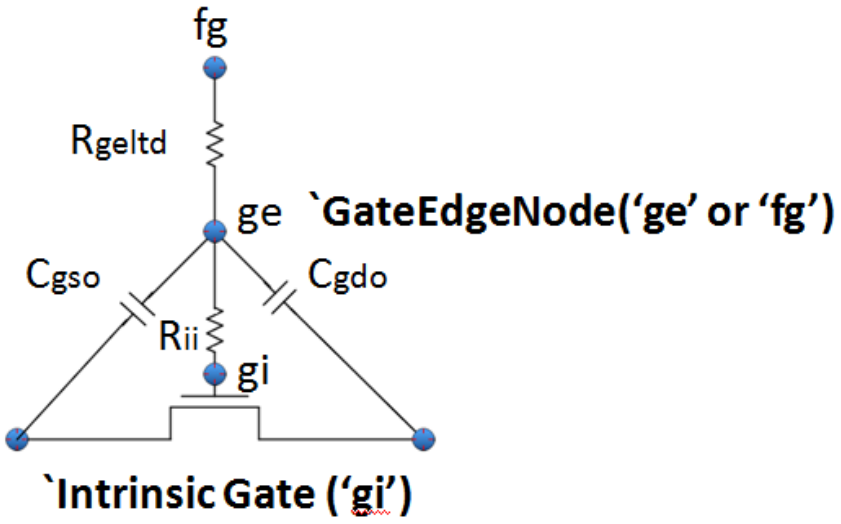


Figure 7: Illustration of case when $RGATEMOD = 1$ and $NQSMOD = 1$

3.21 Self-Heating Model

The self-heating effect is modeled using an R-C network approach (based on BSIMSOI [10]), as illustrated in figure 8. The voltage at the temperature node (T) is used for all temperature-dependence calculations in the

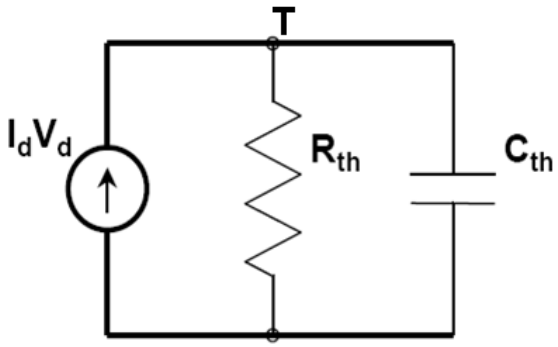


Figure 8: R-C network for self-heating calculation [10]

model. The total temperature (T) used in the model is ambient temperature (T) plus the ΔT_{SHE} computed on the temperature node (T).

Thermal resistance and capacitance calculations

The thermal resistance (R_{th}) and capacitance (C_{th}) are modified from BSIMSOI to capture the width dependence.

$$\frac{1}{R_{th}} = G_{th} = \frac{WTH0 + W_{eff}}{RTH0} \cdot NF \tag{3.339}$$

$$C_{th} = CTH0 \cdot (WTH0 + W_{eff}) \cdot NF \tag{3.340}$$

Use of External thermal node t

In circuits, there are instances where the particular device does not dissipate enough power to get affected by self-heating. However, the other transistors in its vicinity undergoing self-heating may raise the temperature of this particular device. To model such effect, external thermal node is added in the BSIM-IMG model. The thermal node of the two transistors can be coupled by connecting a resistor between the external thermal nodes. This enables the model to accurately capture thermal effects in the device. The external thermal node may also be used to measure the device temperature by simply probing the voltage at the 5th node. The equivalent circuit of self-heating effect is shown in Fig. 9.

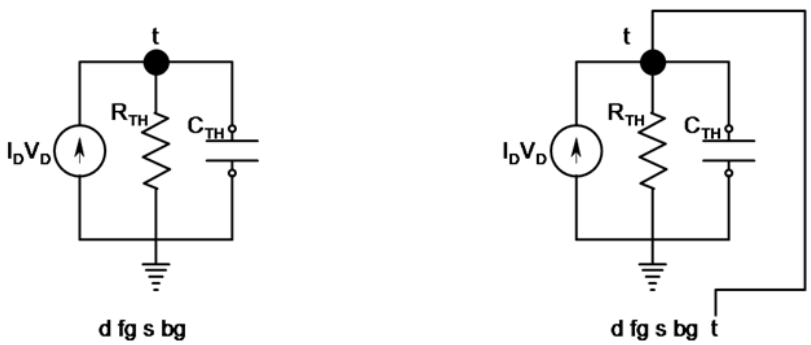


Figure 9: Equivalent self-heating circuit in BSIM-IMG model. Left sub-circuit is without external thermal node while right sub-circuit is illustrated with an external thermal node.

In this update, following configurations are possible:

- If only 4 terminals are specified in the netlist:
  a. SHMOD≠0 and RTH>0, internal self-heating network activates. The simulation temperature is governed by the ambient temperature and SHE network.
  b. SHMOD=0 or RTH<=0, SHE network is not activated and V(t)=0.

- If 5 terminals are specified in the netlist:
  a. SHMOD≠0 and RTH>0, internal self-heating network activates. The 5th node can be connected to the thermal node of the other transistor(s). However, if a voltage source is connected at this node, the V(t) will be decided by that voltage, irrespective of the RTH value i.e. V(t)=Vext.
  b. SHMOD=0 or RTH<=0, SHE network is not activated and V(t)=0. For this case, voltage source must not be connected at the 5th node as it will create conflict by forcing voltage at the t node to be Vext.

3.22 Noise Modeling

The following noise sources in MOSFETs are modeled in BSIM4 [6] for SPICE noise ananlysis: flicker noise (also known as 1/f noise), channel thermal noise and induced gate noise.

Table 3.22 lists the origin of each noise model:

Noise models in BSIM-IMG 102.9.2	**Origin**
Flicker noise model	BSIM4 Unified Model (FNOIMOD=1)
Thermal noise	BSIM4 (TNOIMOD=0)
Gate current shot noise	BSIM4 gate current noise

3.22.1 Flicker Noise Model

BSIM-IMG 102.9.2flicker noise model is same as FNOIMOD=1 in BSIM4. The unified physical flicker noise model is smooth over all bias regions. The physical mechanism for the flicker noise is trapping/detrapping-related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobilities in the channel. The unified flicker noise model captures this physical process. In the inversion region, the noise density is expressed as [11]

$$E_{sat,noi} = \frac{2 \cdot VSAT(T)}{\mu_0(T) D_{mobs}} \tag{3.341}$$

$$L_{eff,noi} = L_{eff} - 2 \cdot LINTNOI \tag{3.342}$$

ΔL_{clm} is the channel length reduction due to channel length modulation and given by

$$\Delta L_{clm} = l \cdot \ln \left[\frac{1}{E_{sat,noi}} \cdot \left(\frac{V_{ds} - V_{dseff}}{l} + EM \right) \right] \tag{3.343}$$

where $L_{eff,noi} = L_{eff} - 2 \cdot LINTNOI$, $\mu_0(T)$ is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source side given by

$$N_0 = \frac{C_{ox1} \cdot q_{is}}{q} \tag{3.344}$$

The parameter N_l is the charge density at the drain end given by

$$N_l = \frac{C_{ox1} \cdot q_{id}}{q} \tag{3.345}$$

and N* is given by

$$N^* = \frac{kT}{q^2} \left(C_{ox1} + CIT \right) \tag{3.346}$$

where CIT is a model parameter from DC IV.

$$FN1 = NOIA \cdot \ln\left(\frac{N_0 + N^*}{N_l + N^*}\right) + NOIB \cdot (N_0 - N_l) + \frac{NOIC}{2}(N_0^2 - N_l^2) \tag{3.347}$$

$$FN2 = \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + N^*)^2} \tag{3.348}$$

In the strong inversion region, the noise density is written as

$$S_{si} = \frac{kTq^2\mu_0(T)I_{ds}}{C_{ox1}L_{eff,noi}^2 \cdot 10^{10}} \cdot FN1 + \frac{kTI_{ds}^2\Delta L_{clm}}{W_{eff} \cdot NF \cdot L_{eff,noi}^2 \cdot 10^{10}} \cdot FN2 \tag{3.349}$$

In the subthreshold region, the noise density is written as

$$S_{wi} = \frac{NOIA \cdot kT \cdot I_{ds}^2}{W_{eff} \cdot NF \cdot L_{eff,noi} \cdot 10^{10} \cdot N^{*2}} \tag{3.350}$$

The total flicker noise density is

$$S_{id,flicker} = \frac{S_{wi}S_{si}}{S_{wi} + S_{si}} \tag{3.351}$$

3.22.2 Thermal Noise Model

Charge-based model (default model) similar to that used in BSIM3v3.2 and BSIM4.7.0 (TNOIMOD=0) is modeled.

TNOIMOD = 0 (Charge based Model): The noise current is given by

$$Q_{inv} = |Q_{s,intrinsic} + Q_{d,intrinsic}| \tag{3.352}$$

$$\overline{i_d^2} = \begin{cases} NTNOI \cdot \frac{4kT\Delta f}{R_{ds}(V) + \frac{L_{eff}^2}{\mu_0(T)Q_{inv}}} & \text{if RDSMOD} = 0 \\ NTNOI \cdot \frac{4kT\Delta f}{L_{eff}^2} \cdot \mu_0(T)Q_{inv} & \text{if RDSMOD} = 1 \end{cases} \tag{3.353}$$

where $R_{ds}(V)$ is the bias-dependent LDD source/drain resistance, and the parameter NTNOI is introduced for more accurate fitting of short-channel devices. Q_{inv} is the total inversion charge in the channel. $Q_{s,intrinsic}, Q_{d,intrinsic}$ are intrinsic charges at source/drain ends.

Gate current shot noise

$$\overline{i_{gs}^2} = 2q(I_{gcs} + I_{gs} + I_{gbs}) \tag{3.354}$$

$$\overline{i_{gd}^2} = 2q(I_{gcd} + I_{gd} + I_{gbd}) \tag{3.355}$$

3.22.3 Resistor Noise Model

The noise associated with each parasitic resistors in BSIM-IMG are calculated

If $RDSMOD = 1$ then

$$\frac{\overline{i_{RS}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{source}} \tag{3.356}$$

$$\frac{\overline{i_{RD}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{drain}} \tag{3.357}$$

If $RGATEMOD = 1$ then

$$\frac{\overline{i_{RG}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{geltd}} \tag{3.358}$$

4 Model Calibration Introduction

The objective of this section is to provide guidelines for the extraction of the main model parameters. The procedure is structured in such a way that parameters linked to specific psychical phenomena are extracted from analyses where these effects are prominent. Although parameter extraction is not always a straight-forward procedure, the aim is to minimize the effort invested and the number of the essential loops performed. If all the steps of the described procedure are followed then a global model card is obtained which means that the model can be used across the entire width/length plane of the technology.

Before proceeding to the extraction of any parameter, it is very important that **TNOM** is set to the value of the temperature at which the nominal measurements were carried out. Biases in extraction steps using N-type bias convention. P-type can be performed using reverse sign conventions.

5 Global Parameter Extraction

The objective of this procedure is to find one global set of parameters for BSIM-IMG to fit experimental data for devices with channel length ranging from short to long dimensions. Some parameters are measured or specified by user, and need not be extracted, such as those given in Table 1.

Table 1: Examples of parameters that are measured or specified by the user

Parameter Name	**Description**
EPSROX	Relative Gate Dielectric Constant
EPSRSUB	Relative Dielectric Constant of the Channel
EOT1	Electrical Gate Equivalent Oxide Thickness of Front Gate
EOT2	Electrical Gate Equivalent Oxide Thickness of Back Gate
NBODY	Channel Doping Concentration
NSD	S/D Doping Concentration
XW/XL	Channel W/L Offset due to Mask/Etch Effect
L	Designed Gate Length
W	Designed Gate Width
NF	Number of Fingers in parallel
GIDLMOD	0: off 1:on
RDSMOD	0: fixed bias dependence, 1: external bias dependence,
	2: Both bias dependent and geometry dependent part of source/drain resistance
TYPE	-1: PMOS 1:NMOS

Now we start extracting all the global parameters. The extraction procedure can be divided into 6 stages:

- Gate Capacitance Fitting (C_{GG} vs V_{GS})
- Gate Current Fitting (I_{GS} vs V_{GS})
- Drain Current Fitting (I_{DS} vs V_{GS}) in Linear region
- Drain Current Fitting (I_{DS} vs V_{GS}) in Saturation region
- Drain Current Fitting (I_{DS} vs V_{DS})
- Drain Current Fitting (I_{DS} vs V_{DS}) for threshold voltage substrate sensitivity

5.1 Extraction of Long Channel and Long Width Device Parameters

5.1.1 Long Channel Gate Capacitance Fitting: (C_{GG} vs V_{GS}) @ $V_{DS} = 0\ V$ & $V_{BG} = 0\ V$

Step 1: At this step, process parameters and parameters related to quantum mechanical effect are extracted. Even if values have been already assigned to process parameters, a fine tuning should be made in order to fit accurately the electrical behavior of the device. From C_{GG} vs V_{GS} curve, the following process parameters can be extracted: **NBODY**, **EOT1**, **EOT2** and **NGATE**, **PHIG1**, **PHIG2**. Each of these parameters affects a different region or in a different way the C_{GG} capacitance, so they should be extracted accordingly. More specifically:

- **NBODY** is affecting C_{GG} in the depletion region/weak inversion region.
- **EOT1** and **EOT2** are defined as physical gate equivalent oxide thickness for front/back gates.

Furthermore, the value of front gate capacitance C_{OX} is affected by the Quantum Mechanical effect. So, the parameters: **PQM**,**QM0** and **ETAQM** are also extracted from C_{GG} vs V_{GS} analysis, when focusing at the slope of C_{GG} at the onset of the strong-inversion region.

5.1.2 Long Channel Drain Current Fitting: I_{DS} vs V_{GS} Analysis in Linear Region

Step 2: In this step, the V_G dependence of the drain current I_{DS}, is extracted. Carrier mobility and interface charge related parameters are extracted.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
CIT, CDSC	Long device I_{DS} vs V_{GS} @ $V_{DS} = 0.05V$ @$V_{BG} = 0.0V$	Observe sub-threshold region offset and slope.
CBGCBG0, CBGCBG, KBG0P(N)W, KBG1P(N)W, KBG2P(N)W, BPFACTORP(N)W, DBGP(N)W, VKNEE1P(N)W, VKNEE2P(N)W	Long device I_{DS} vs V_{GS} @ $V_{DS} = 0.05V$ @$V_{BG} \neq 0.0V$	Observe sub-threshold region offset and slope as well as threshold voltage.
UD_0, UCS_0	Long device I_{DS} vs V_{DS} @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$	Observe intermediate inversion region I_{Dlin} and g_{mlin} in linear scale.
$U0_0$, UA_0, EU_0, ETAMOB, PRWG, RSW, RDW	Long device I_{DS} vs V_{DS} @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$	Observe strong inversion region I_{Dlin} and g_{mlin} in linear scale.
UC_0, UDB, PRWB	Long device I_{DS} vs V_{DS} @ $V_{DS} = 0.05V$ @ $V_{BG} \neq 0.0V$	Observe strong inversion region I_{Dlin} and g_{mlin} in linear scale.

Note: 0 subscript denotes nominal T (300K). **Note:** The Coulombic scattering parameters (UD, UCS) may change the threshold voltage. Meanwhile, observing and fine tuning threshold voltage are needed.

5.1.3 Long Channel Drain Current Fitting: I_{DS} vs V_{GS} Analysis in Saturation Region

Step 3: Tune DIBL parameters.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
ETA0, DSUB, CDSCD	Long devices I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$ @ $V_{BG} = 0.0V$	Observe sub-threshold region of all devices in the same plot.
ETAB, CBGCBGD	Short and long devices I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$ @$V_{BG} \neq 0.0V$	Observe sub-threshold region offset and slope.

Note: Velocity saturation, smoothing function and output conductance parameters are tuned for better fitting.

Step 4: Extract velocity saturation parameters for long gate lengths, see short channel effects section.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
$VSAT$, $PTWG$, $KSATIV$, $MEXP$	long device and medium devices I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$ @ $V_{BG} = 0.0V$	Observe strong inversion region I_{Dsat}, g_{msat}.
$VSATB$, $PTWGB$, $PTWGB2$	long device and medium devices I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$ @$V_{BG} \neq 0.0V$	Observe strong inversion region I_{Dsat}, g_{msat}.

Note: long channel alone is not enough to accurately extract velocity saturation parameters.
Step 5: Extract output conductance parameters.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
MEXP, PCLM, PDIBL1, PDIBL2, DROUT, PVAG	Long and short devices I_{DS} vs V_{DS} @ differentV_{GS} @ $V_{BG} = 0.0V$	Observe strong inversion region I_{DS} vs V_{DS} & g_{DS} vs V_{DS} @ different V_{GS} @ $V_{BG} = 0.0V$.

5.1.4 Drain Current Fitting (I_{DS} vs V_{DS}) for Threshold Voltage Substrate Sensitivity

Threshold voltage of the FDSOI transistor is extracted from constant current method. To calibrate V_{th} vs back gate voltage V_{bgs}, start with BPFACTORPW (or BPFACTORNW FOR N-type back gate) equal to zero which means no substrate depletion effect is considered. Calibrate V_{th} data for positive V_{bgs} for p-type substrate (or equivalently, V_{th} data for negative Vbgs for n-type substrate). See Figure 10.

If the measured data show a deviation from an straight line due to depletion in the substrate, 1) set VKNEE1PW (or VKNEE1NW) equal to the back gate voltage at which the lines depart and 2) start increasing BPFACTORPW (or BPFACTORNW) and adjusting VKNEE2PW (or VKNEE2NW) for a good fit. See Figure 11.

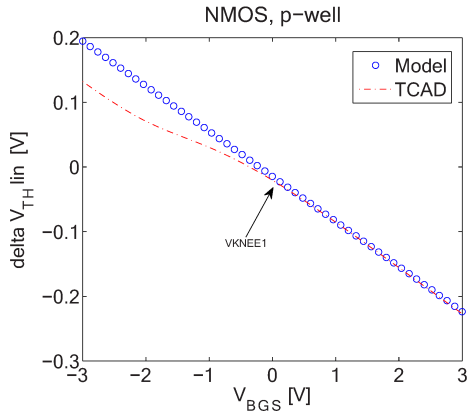


Figure 10: V_{th} vs back gate voltage V_{bgs}, NMOS with p-type substrate (p-well). The substrate depletion effect is turned off in the model.

5.2 Extraction of Short Channel Effects & Length Scaling Parameters

5.2.1 Short Channel Gate Capacitance Fitting: (C_{GG} vs V_{GS}) @ $V_{DS} = 0\ V$ & $V_{BG} = 0\ V$

Step 6: In this step, parameters related to overlap and fringing capacitances are extracted. More specifically:

- Extraction of parameters related to overlap and fringing capacitances is carried out by studying the entire range of V_{GS} bias of C_{GG} vs V_{GS} characteristic. These parameters are: **CGSL**, **CGDL**, **CKAPPAS**, **CKAPPAD**. **CGSL**, **CGDL**, **CKAPPAS** and **CKAPPAD** are extracted from C_{GD} vs V_{GS} at high V_{BG} (when S, D and B terminals are connected together).
- **DLC**, which is the channel-length offset parameter for the CV model, is extracted in the strong-inversion region of C_{GG}.

A sample global fitting for C-V characteristics of NMOS and PMOS device is shown in Figure 12.

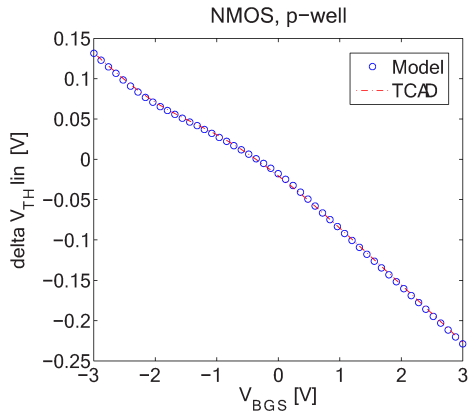


Figure 11: V_{th} vs back gate voltage V_{bgs}, NMOS with p-substrate (well), including substrate depletion effect.

5.2.2 Short Channel Drain Current Fitting: I_{DS} vs V_{GS} Analysis in Linear Region

Step 7: Tune Vth roll-off, DIBL and SS degradation parameters.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
DVT0, DVT1, CDSC, DSUB, ETA0, ETAB	Both short and medium devices I_{DS} vs V_{GS} @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$	Observe sub-threshold region of all devices in the same plot. Optimize DVT0, DVT1, CDSC, DSUB, ETA0, ETAB.

Step 8: Extract low field mobility U0[L] for long and medium gate lengths. So far, we have good fit with data in sub-threshold regions from long to short channel devices, and strong inversion for long channel devices. We need good fit for strong inversion in medium and short channel devices. In linear region, current is to the first order, governed by low field mobility. So we start by tuning low field mobility values. In short channel devices series resistance and enhanced mobility degradation effects are pronounced. To avoid the influence of these effects, long and medium channel length devices are selected to especially extract low field mobility parameters.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
UP, LPA	Long and medium devices I_{DS} vs V_{GS} @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$	Observe strong inversion region I_{Dlin} and g_{mlin}, extract U0[L] to get UP, LP.

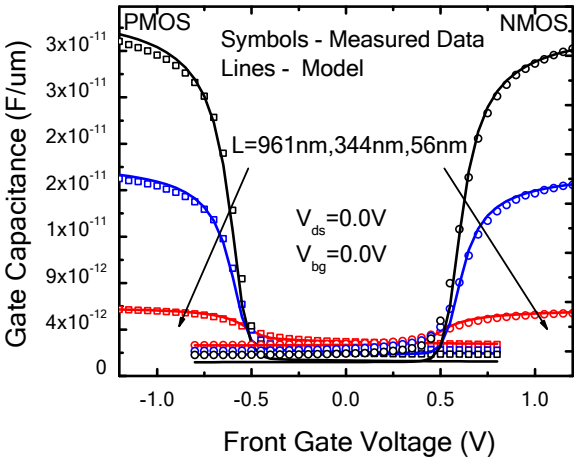


Figure 12: C_{GG} vs V_{GS} @ $V_{DS} = 0.05V$ and $V_{BG} = 0.0V$, Symbols: Data [12], Lines: the BSIM-IMG model.

Step 9: Extract mobility and series resistance parameters for short gate lengths.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
AParam (i.e., AUA, AEU, AUC, AUD, AUDB, ARDSW, ARSW, ARDW), BParam (i.e., BUA, BEU, BUC, BUD, BUDB, BRDSW, BRSW, BRDW), LINT, LL, LLN	Short and medium devices I_{DS} vs V_{GS} @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$	a. Observe strong inversion region I_{dlin} and g_{mlin}. Similar to Step 8, find values of UA, UD, RDSW that gives good fit to experimental data, varying them simultaneously. UA_0, UD_0 are provided from Step 2 and LINT is provided from parameter Initialization. b. Variation of each parameter with respect to L should be kept minimal with smooth continuous trend. c. From the length dependence of UA, UD, RDSW and L, find AUA, BUA; AUD, BUD; ARDSW, BRDSW; LL, LLN .

Note: Step 8 parameters are extracted from long and medium channel lengths, whereas, Step 9 involves short and medium channel lengths. Thus, the extracted parameters remain valid for all channel lengths to bring forth the intended length dependence in effect.

Step 10: Tune geometry scaling parameters for mobility degradation parameters.

Refined Parameters	**Device & Experimental Data**	**Extraction Methodology**
AUA, AUD, ARDSW, LL	Short and medium devices I_{DS} vs V_{GS} @ $V_{DS} = 0.05V$, @ $V_{BG} = 0.0V$	Observe strong inversion region of all devices in the same plot; optimize AUA, AUD, ARDSW, LL.

Step 11: Further optimize the parameters by repeating step 10 and 7. If not getting good fitting, tune LLN, BUA, BUD, BRDSW. Iteration ends in step 10 and then proceeds to step 12.

5.2.3 Short Channel Drain Current Fitting: I_{DS} vs V_{GS} Analysis in Saturation Region

Step 12: Extract velocity saturation parameters for short and medium gate lengths

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
AVSAT, AVSAT1, APTWG, BVSAT, BVSAT1, BPTWG	short and medium devices I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$, @ $V_{BG} = 0.0V$	a. Observe strong inversion region of I_{Dsat} and g_{msat}. Find VSAT1, VSAT, PTWG, AVSAT1, BVSAT1, AVSAT, BVSAT, APTWG, BPTWG to fit data.

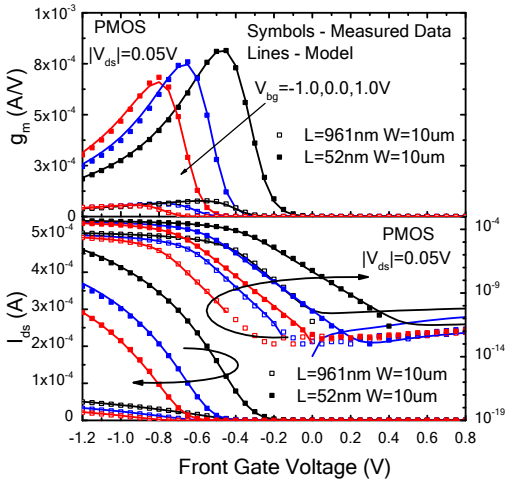
Step 13: Tune geometry scaling parameters for velocity saturation, over the range from short to long channel devices.

Refined Parameters	**Device & Experimental Data**	**Extraction Methodology**
AVSAT, AVSAT1, APTWG	medium and short devices I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$, @ $V_{BG} = 0.0V$	Observe strong inversion region of all devices in the same plot. Optimize AVSAT, AVSAT1, APTWG.

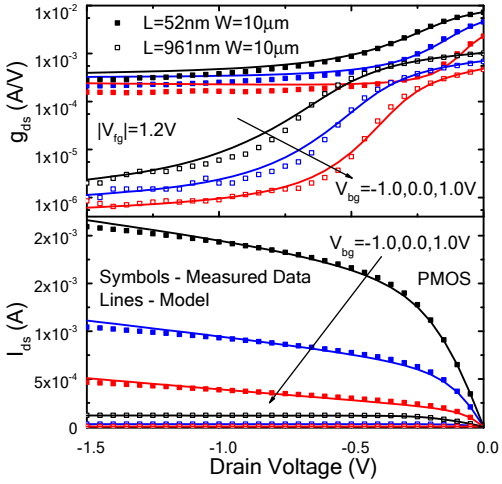
5.2.4 Other Parameters Representing Important Physical Effects

Step 14: Extract GIDL current model parameters.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
AGIDL, BGIDL, EGIDL	long and short devices I_{DS} vs V_{DS} @ different V_{GS} @ $V_{BG} = 0.0V$	Observe sub-threshold region I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$ & R_{out} vs V_{DS} @ $V_{GS} < 0V$ and $V_{GS} = 0V$.



(a) I_{DS} vs V_{GS} @ $V_{DS} = 0.05V$



(b) I_{DS} vs V_{DS} @ $V_{GS} = 1.2V$

Figure 13: I_{DS} vs V_{GS} characteristics and I_{DS} vs V_{DS} characteristics for PMOS device with L_g=961nm and L_g=52nm , Symbols: Data [12], Lines: the BSIM-IMG model.

5.2.5 Smoothing between Linear and Saturation Regions

Step 15: Extract geometry scaling parameters for smoothing function parameter.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
MEXP, AMEXP, BMEXP	long and short devices I_{DS} vs V_{DS} @ different V_{GS}	Observe data trend; extract AMEXP and BMEXP.

Note: MEXP may not be sufficient for transition (from linear to saturation) region in short devices. VSAT, DIBL parameters, and mobility should be fine tuned if needed.

A sample global fitting for long channel and short channel PMOS device is shown in Figure 13.

See the length scaling extraction overview flow chart for details in Figure 14.

5.3 Extraction of Narrow Channel Effects & Width Scaling Parameters

The next step in the parameter extraction procedure is the extraction of the parameters that are either related to narrow channel effects or express the different width dependencies. So at this part, devices across the entire width range of the technology, from the narrowest to the widest one, are studied simultaneously. A full range of W-binning model parameters is listed in section 6.1 (see terms with small b superscript). In order to avoid the impact of short channel effects or the length dependencies these devices should have the same **long** channel. The extraction that is carried out follows the same flow as in Figure 14, but now a set of devices with constant **long** channel but different channel widths is used.

5.3.1 Gate Capacitance C_{GG} vs V_{GS} Analysis @ $V_S = 0\ V$, $V_D = 0\ V$ & $V_{BG} = 0\ V$

In this step, parameters related to the width dependencies of the CV behavior of the device are extracted. More specifically:

- **DWC**, which is the channel-width offset parameter for the CV model, is extracted in the strong-inversion region of C_{GG}.
- **LWLC** and **WWLC**, which are coefficients of length/width dependencies for CV model, are extracted in the strong-inversion region of C_{GG}.

5.3.2 Drain Current I_D vs V_{GS} Analysis @ $V_{DS} = [V_{D,lin}, V_{D,sat}]$, $V_S = 0\ V$ & $V_{BG} = 0\ V$

In this step, geometry dependent parameters for modeling I_{DS} of the narrow/short channel devices, are extracted. Similar to the procedure described in Figure 14, the parameters are divided in two groups, those which are extracted in *linear mode* (i.e. $V_D \ll V_G - V_{th}$) and those which are extracted in *saturation* (i.e. $V_D \gg V_G - V_{th}$). It is very important that during the extraction both I_D and g_m of all the devices are studied at once. Parameter **WINT** is the channel width offset parameter and is used to fit both the sub-threshold slope and the V_{th} across W.

5.4 Other Effects

Step 16: Temperature and Self-Heating Effects.

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
Thermal resistance (RTH0) and capacitances (CTH0) for the self-heating model and etc.	I_{DS} vs V_{GS} @ $V_{DS} = V_{dd}$ under different temperatures.	Observe data trend and tune RTH0, CTH0.

Step 17: Gate leakage current

Extracted Parameters	**Device & Experimental Data**	**Extraction Methodology**
Gate tunneling current parameters.	I_{GC} vs V_{GS} @ $V_{DS} = 0V$.	Observe data trend and tune NIGCINV, AIGCINV, BIGCINV, CIGCINV, EIGCINV etc.

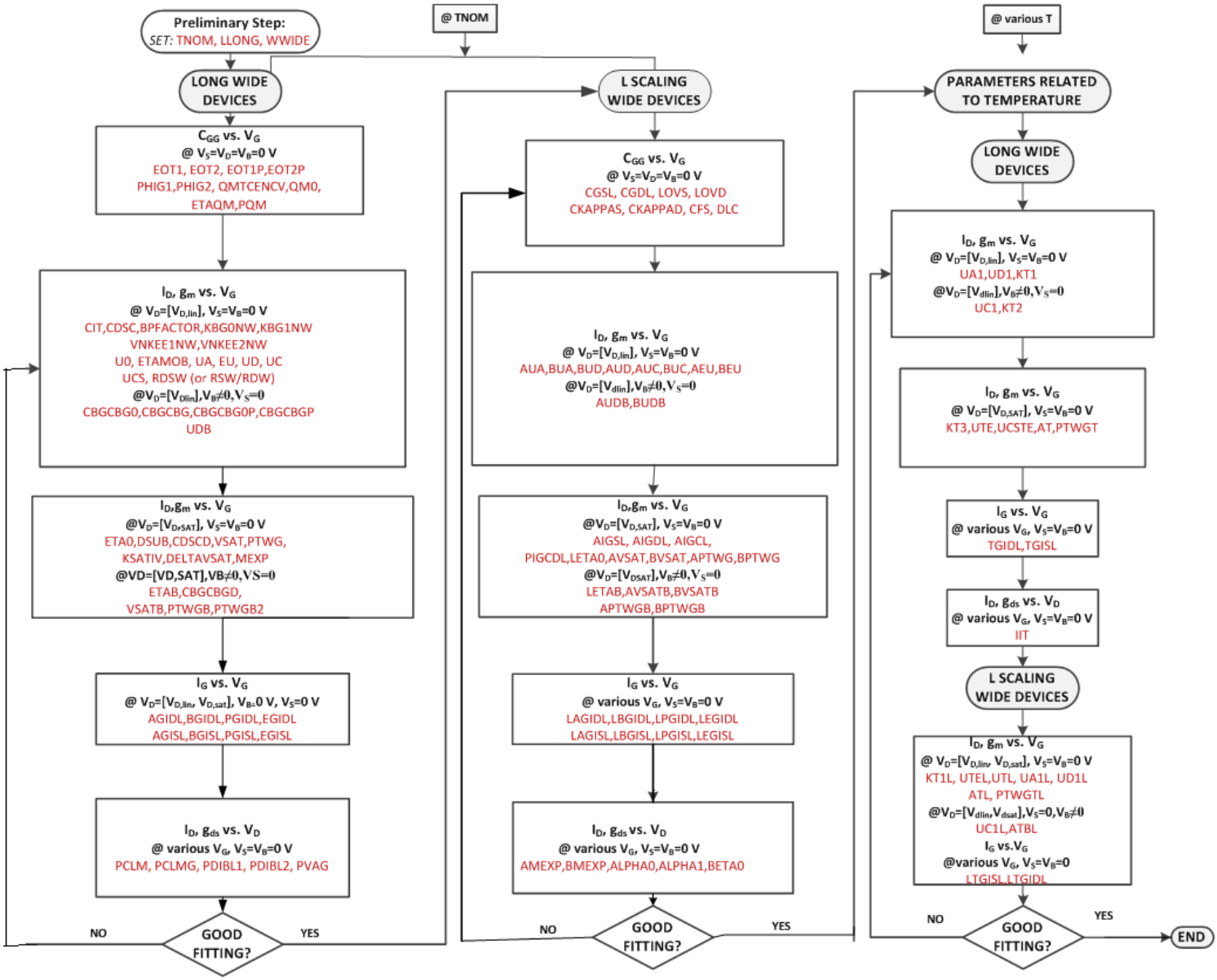


Figure 14: Parameters Extraction Procedure in BSIM-IMG Model.

6 Complete Parameter List

6.1 Instance Parameters

Note: Instance parameters with superscript $^{(m)}$ are also model parameters

Name	Unit	Default	Min	Max	Description
$L^{(m)}$	m	30n	1n	-	Designed Gate Length
W	m	1e-6	1n	-	Designed Gate Width
NF	-	1	1	-	Number of fingers
$AS^{(m)}$	m^2	0	0	-	Source to substrate overlap area through oxide (all fingers)
$AD^{(m)}$	m^2	0	0	-	Drain to substrate overlap area through oxide (all fingers)
$PS^{(m)}$	m	0	0	-	Perimeter of source to substrate overlap region through oxide (all fingers)
$PD^{(m)}$	m	0	0	-	Perimeter of drain to substrate overlap region through oxide (all fingers)
$NRS^{(m)}$	-	0	0	-	Number of source diffusion squares (for $RGEOMOD = 0$)
$NRD^{(m)}$	-	0	0	-	Number of drain diffusion squares (for $RGEOMOD = 0$)

Note: Parameters for global variability modeling

Name	Unit	Default	Min	Max	Description
XL	m	0	-	-	L offset for channel length due to mask/etch effect
DTEMP	^{0}C	0	-	-	Variability handle for temperature
DELVTRAND	V	0	-	-	Variability in Vth
U0MULT	-	1	-	-	Variability in carrier mobility

6.2 Model Controllers and Process Parameters

Note: binnable parameters are marked as: $^{(b)}$

Name	Unit	Default	Min	Max	Description
TYPE	-	NMOS	PMOS	NMOS	NMOS=1, PMOS=-1
WELLTYPE	-	p-well	p-well	n-well	n-well=1, p-well=-1
CHARGEMOD	-	0	0	1	Selects the inversion charge density model for the body; 0= simplified, 1= more accurate
RDSMOD	-	0	0	2	bias-dependent source/drain resistance model selector (controls *si* and *di* nodes); 0 = internal, 1 = external, 2 = bias and geometry dependent
IGCMOD	-	0	0	1	model selector for Igc, Igs and Igd; 1=turn on, 0=turn off
IGBMOD	-	0	0	1	model selector for Igb; 1=turn on, 0=turn off
GIDLMOD	-	0	0	1	GIDL/GISL current switcher; 1=turn on, 0=turn off
SHMOD	-	0	-	-	Self-heating mode switch; 1=turn on, 0=turn off
RGATEMOD	-	0	-	-	Gate resistance model selector; 1=turn on, 0=turn off
NFMOD	-	0	-	-	Number of Finger selector; 1=W taken as single finger width, 0=W taken as total width like BSIM4
CHARGEWF	-	-	-	-	Average Channel Charge Weighting Factor, +1:source-side, 0:middle, -1:drain-side
XW	m	0	-	-	W offset for channel length due to mask/etch effect
LINT	m	0	-	-	Length reduction parameter (dopant diffusion effect)
LL	$m^{(LLN+1)}$	0	-	-	Length reduction parameter (dopant diffusion effect)
LW	m	0	-	-	Length scaling parameter
LWL	m	0	-	-	Length scaling parameter
LLN	-	1	-	-	Length reduction parameter (dopant diffusion effect)
LWN	m	1	-	-	Length scaling parameter
WINT$^{(b)}$	m	0	-	-	Width reduction parameter (dopant diffusion effect)
WL$^{(b)}$	$m^{(WLN+1)}$	0	-	-	Width reduction parameter (dopant diffusion effect)

Name	Unit	Default	Min	Max	Description
WW$^{(b)}$	m	0	-	-	Width scaling parameter
WWL$^{(b)}$	m	0	-	-	Width scaling parameter
WLN$^{(b)}$	-	1	-	-	Width reduction parameter (dopant diffusion effect)
WWN$^{(b)}$	m	1	-	-	Width scaling parameter
DLC	m	0	-	-	Length reduction parameter for CV (dopant diffusion effect)
LLC	m	0	-	-	Length scaling parameter
LWC	m	0	-	-	Length scaling parameter
LWLC	m	0	-	-	Length scaling parameter
DWC	m	0	-	-	Width reduction parameter for CV (dopant diffusion effect)
WLC	m	0	-	-	Width scaling parameter
WWC	m	0	-	-	Width scaling parameter
WWLC	m	0	-	-	Width scaling parameter
EOT1	m	1.0n	0.1n	-	SiO_2 equivalent front gate dielectric thickness (including inversion layer thickness)
EOT2	m	140n	0.1n	-	SiO_2 equivalent back gate dielectric thickness (including substrate depletion layer thickness)
EOT1P	m	EOT1	0.1n	-	physical front gate dielectric thickness for CV
DTOX1	m	0.0	-	-	Difference between effective dielectric thickness and physical thickness
TSI	m	8n	1n	-	body thickness
NBODY $^{(b)}$	m^{-3}	1e22	1e18	5e24	Channel doping concentration
NBG	m^{-3}	5e23	-	-	Substrate (well) or back gate doping level, zero for metal back gate
EASUB	eV	4.05	0	-	electron affinity of the substrate material
NI0SUB	m^{-3}	1.1e16	-	-	intrinsic carrier concentration of channel at 300.15K
BG0SUB	eV	1.12	-	-	band gap of the channel material at 300.15K
NC0SUB	m^{-3}	2.86e25	-	-	conduction band density of states at 300.15K

Name	Unit	Default	Min	Max	Description
PHIG1 $^{(b)}$	V	4.61	-	-	Workfunction of the front gate
PHIG2 $^{(b)}$	V	$EASUB+BG0SUB$ for n-well; $EASUB$ for p-well	-	-	Substrate (well) or back gate workfunction, eV, it will be modified according to NBG later in the code if 1) the back gate is NOT metallic and 2) its value is not provided by user
EPSRSUB		11.9	-	-	Relative dielectric constant of the substrate material
EPSROX1		3.9	-	-	Relative dielectric constant of the front gate insulator material
NSD$^{(b)}$	m^{-3}	2e26	2e25	1e27	S/D doping concentration

6.3 Basic Model Parameters

Note: binnable parameters are marked as: $^{(b)}$

Name	Unit	Default	Min	Max	Description
CIT$^{(b)}$	F/m^2	0.0	-	-	Parameter for interface trap
CDSC$^{(b)}$	F/m^2	0.14	0.0	-	Coupling capacitance between S/D and channel
CDSCD$^{(b)}$	F/m^2V	0.14	0.0	-	Drain-bias sensitivity of CDSC
CBGCBG$^{(b)}$	F/m^2V	0.1	0.0	-	Back-gate bias sensitivity of coupling capacitance to channel
CBGCBG0$^{(b)}$	F/m^2V	0.0	0.0	-	Backgate-Bias sensitivity of SS for long channel
CBGCBG0P$^{(b)}$	F/m^2V^2	0.0	0.0	-	Sublinear Backgate-Bias sensitivity of SS for long channel
CBGCBGP$^{(b)}$	F/m^2V^2	0.0	0.0	-	Nonlinear backgate-bias sensitivity of SS
CBGCBGD$^{(b)}$	F/m^2V^2	0.0	0.0	-	Backgate-Bias sensitivity of CDSCD
DVT0$^{(b)}$	-	19.20	0.0	-	SCE coefficient
DVT1$^{(b)}$	-	0.45	0.0	-	SCE exponent coefficient
PHIN$^{(b)}$	V	0.045	-	-	Nonuniform vertical doping effect on surface potential
ETA0$^{(b)}$	-	2.00	0.0	-	DIBL coefficient
ETA1$^{(b)}$	-	0.00	0.0	-	DIBL coefficient for low gate overdrive
ETAB$^{(b)}$	$1/V$	0.00	0.0	-	DIBL coefficient-Back Gate Bais Dependence
DSUB$^{(b)}$	-	0.375	0.0	-	DIBL exponent coefficient
DVTP0	-	0	-	-	Coefficient for Drain-Induced Vth Shift (DITS)
DVTP1	-	0	-	-	DITS exponent coefficient
DVTP2	-	0	-	-	DITS model parameter
K1RSCE$^{(b)}$	$V^{1/2}$	-0.32	-	-	Prefactor for reverse short channel effect
LPE0$^{(b)}$	m	8.2e-9	$-L_{eff}$	-	Equivalent length of pocket region at zero bias
DSC0	m	0.0	-	-	Parameter for short channel effect at moderate L and high drain bias
DSC1	m	1n	-	-	Parameter for short channel effect at moderate L and high drain bias
ASCL	-	0.0	-	-	Parameter for back-gate dependent scale length

BSCL	$1/V$	0.0	-	-	Parameter for back-gate dependent scale length
VSAT$^{(b)}$	m/s	85000	-	-	Saturation velocity in the saturation region

Name	Unit	Default	Min	Max	Description
AVSAT$^{(b)}$	-	0	-	-	Saturation velocity in the saturation region for short channel devices
BVSAT$^{(b)}$	-	100.0e-9	-	-	Saturation velocity coefficient in the saturation region for short channel devices
VSATB$^{(b)}$	$1/V$	0.00	0.0	-	Saturation velocity parameter for Back Gate Bais dependence on mobility at high Vds
AVSATB$^{(b)}$	-	0.00	0.0	-	Saturation velocity parameter for Back Gate Bais dependence on mobility at high Vds for short channel devices
BVSATB$^{(b)}$	-	100.0e-9	0.0	-	Saturation velocity parameter for Back Gate Bais dependence on mobility at high Vds for short channel devices
VSAT1$^{(b)}$	m/s	VSAT	-	-	Saturation velocity in the linear region
AVSAT1$^{(b)}$	-	AVSAT	-	-	Saturation velocity in the linear region for short channel devices
BVSAT1$^{(b)}$	-	BVSAT	-	-	Saturation velocity coefficient in the linear region for short channel devices
VSATCV$^{(b)}$	m/s	VSAT	-	-	Saturation velocity for the saturation region for C-V
AVSATCV$^{(b)}$	m/s	AVSAT	-	-	Saturation velocity in the saturation region for short channel C-V
BVSATCV$^{(b)}$	m/s	BVSAT	-	-	Saturation velocity coefficient in the saturation region for short channel C-V
DELTAVSAT	m/s	1	0.01	-	Velocity saturation parameter
KSATIV$^{(b)}$	-	1.0	-	-	Parameter for strong inversion regime for long channel Vdsat
KSUBIV$^{(b)}$	-	1.0	-	-	Parameter for weak inversion regime for long channel Vdsat
MEXP$^{(b)}$	-	4	2	-	Smoothing function factor for Vdsat
AMEXP$^{(b)}$	-	0	0	-	Smoothing function factor for Vdsat in short channel devices
BMEXP$^{(b)}$	-	1	-	-	Smoothing function coefficient for Vdsat in short channel devices
PTWG$^{(b)}$	$1/V^2$	0.0	-	-	Correction factor for velocity saturation
APTWG$^{(b)}$	-	0.0	-	-	Correction factor for velocity saturation in short channel devices

Name	Unit	Default	Min	Max	Description
BPTWG$^{(b)}$	-	100.0e-9	-	-	Coefficient for correction factor for velocity saturation in short channel devices
PTWGB$^{(b)}$	$1/V^3$	0.0	-	-	Parameter for Back Gate Bais sensitivity in PTWGB
APTWGB$^{(b)}$	-	0.0	-	-	Parameter for Back Gate Bais sensitivity in PTWGB for short channel devices
BPTWGB$^{(b)}$	-	100.0e-9	-	-	Parameter for Back Gate Bais sensitivity in PTWGB for short channel devices
PTWGB2$^{(b)}$	$1/V^3$	0.0	-	-	Parameter for Back Gate Bais sensitivity in PTWGB
APTWGB2$^{(b)}$	-	0.0	-	-	Parameter for Back Gate Bais sensitivity in PTWGB for short channel devices
BPTWGB2$^{(b)}$	-	100.0e-9	-	-	Parameter for Back Gate Bais sensitivity in PTWGB for short channel devices
U0$^{(b)}$	$m^2/V-s$	3e-2	-	-	Low field mobility
ETAMOB$^{(b)}$	-	2.0	-	-	Effective field parameter
UP$^{(b)}$	μm^{LPA}	0.0	-	-	Mobility L coefficient
LPA	-	1.0	-	-	Mobility L power coefficient
UA$^{(b)}$	$(cm/MV)^{EU}$	0.3	0.0	-	Phonon / surface roughness scattering
AUA$^{(b)}$	-	0	-	-	Phonon / surface roughness scattering for short channel devices
BUA$^{(b)}$	-	100.0e-9	-	-	Phonon / surface roughness scattering for short channel devices
EU$^{(b)}$	cm/MV	2.5	0.0	-	Phonon / surface roughness scattering
AEU$^{(b)}$	-	0	-	-	Phonon / surface roughness scattering for short channel devices
BEU$^{(b)}$	-	100.0e-9	-	-	Phonon / surface roughness scattering for short channel devices
UD$^{(b)}$	cm/MV	0.0	0.0	-	Columbic scattering (Experimental)
AUD$^{(b)}$	-	0.0	-	-	Columbic scattering (Experimental) for short channel devices
BUD$^{(b)}$	-	50.0e-9	-	-	Columbic scattering (Experimental) for short channel devices
UDB$^{(b)}$	cm/MV	0.0	0.0	-	Back bias sensitivity on columbic scattering (Experimental)
AUDB$^{(b)}$	-	0.0	-	-	Back bias sensitivity on columbic scattering (Experimental) for short channel devices

Name	Unit	Default	Min	Max	Description
BUDB$^{(b)}$	-	50.0e-9	-	-	Back bias sensitivity on columbic scattering (Experimental) for short channel devices
UC$^{(b)}$	$(cm/MV)^{EU} \cdot 1/V$	0.0	0.0	-	Parameter for Back Gate Bais dependence on mobility at low Vds
AUC$^{(b)}$	-	0.0	-	-	Parameter for Back Gate Bais dependence on mobility at low Vds for short channel devices
BUC$^{(b)}$	-	100.0e-9	-	-	Parameter for Back Gate Bais dependence on mobility at low Vds for short channel devices
UCS$^{(b)}$	-	1.0	0.0	-	columbic scattering (Experimental)
PCLM$^{(b)}$	-	0.013	0.0	-	Channel Length Modulation (CLM) parameter
APCLM$^{(b)}$	-	0	-	-	Channel Length Modulation (CLM) parameter for short channel devices
BPCLM$^{(b)}$	-	100.0e-9	-	-	Channel Length Modulation (CLM) parameter for short channel devices
PCLMG	-	0	-	-	Gate bias dependent parameter for channel Length Modulation (CLM)
PCLMCV$^{(b)}$	-	0.013	0.0	-	Channel Length Modulation (CLM) parameter for C-V
RDSWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	$RDSMOD = 0$ S/D extension resistance per unit width at high V_{gs}
RDSW$^{(b)}$	$\Omega - \mu_m^{WR}$	100	0.0	-	$RDSMOD = 0$ zero bias S/D extension resistance per unit width
ARDSW$^{(b)}$	-	0	-	-	$RDSMOD = 0$ zero bias S/D extension resistance per unit width for short channel devices
BRDSW$^{(b)}$	-	100.0e-9	-	-	$RDSMOD = 0$ zero bias S/D extension resistance per unit width for short channel devices
RSWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	$RDSMOD = 1$ source extension resistance per unit width at high V_{gs}
RSW$^{(b)}$	$\Omega - \mu_m^{WR}$	50	0.0	-	$RDSMOD = 1$ zero bias source extension resistance per unit width
ARSW$^{(b)}$	-	0	-	-	$RDSMOD = 1$ zero bias source extension resistance per unit width for short channel devices

Name	Unit	Default	Min	Max	Description
BRSW$^{(b)}$	-	100.0e-9	-	-	$RDSMOD = 1$ zero bias source extension resistance per unit width for short channel devices
RDWMIN	$\Omega - \mu_m^{WR}$	RSWMIN	0.0	-	$RDSMOD = 1$ drain extension resistance per unit width at high V_{gs}
RDW$^{(b)}$	$\Omega - \mu_m^{WR}$	RSW	0.0	-	$RDSMOD = 1$ zero bias drain extension resistance per unit width
ARDW$^{(b)}$	-	ARSW	-	-	$RDSMOD = 1$ zero bias drain extension resistance per unit width for short channel devices
BRDW$^{(b)}$	-	BRSW	-	-	$RDSMOD = 1$ zero bias drain extension resistance per unit width for short channel devices
PRWG$^{(b)}$	$1/V$	0.0	0.0	-	front gate bias dependence of S/D extension resistance
PRWB$^{(b)}$	$1/V$	0.0	-	-	back gate bias dependence of S/D extension resistance
WR$^{(b)}$	-	1.0	-	-	W dependence parameter of S/D extension resistance
RSHS	Ω	0.0	0.0	-	Source-side sheet resistance
RSHD	Ω	RSHS	0.0	-	Drain-side sheet resistance
XGW	m	0	-	-	Dist from gate contact center to dev edge
XGL	m	0	-	-	Variation in Ldrawn
NGCON	-	1	-	-	Number of gate contacts
RSHG	Ohm	0.1	-	-	Gate sheet resistance
PDIBL1$^{(b)}$	-	1.30	0.0	-	parameter for DIBL effect on Rout
PDIBL2$^{(b)}$	-	2e-4	0.0	-	parameter for DIBL effect on Rout
DROUT$^{(b)}$	-	1.06	0.0	-	L dependence of DIBL effect on Rout
PVAG$^{(b)}$	-	1.0	-	-	V_{gs} dependence on early voltage
AIGBINV$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}$	1.11e-2	-	-	parameter for Igb in inversion
BIGBINV$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1} \cdot 1/V$	9.49e-4	-	-	parameter for Igb in inversion
CIGBINV$^{(b)}$	$1/V$	6.00e-3	-	-	parameter for Igb in inversion
EIGBINV$^{(b)}$	V	1.1	-	-	parameter for Igb in inversion
NIGBINV$^{(b)}$	-	3.0	0.0	-	parameter for Igb in inversion
AIGBACC$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}$	1.36e-2	-	-	parameter for Igb in accumulation
BIGBACC$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}/V$	1.71e-3	-	-	parameter for Igb in accumulation
CIGBACC$^{(b)}$	$1/V$	7.5e-2	-	-	parameter for Igb in accumulation

Name	Unit	Default	Min	Max	Description
NIGBACC$^{(b)}$	-	1.0	0.0	-	parameter for Igb in accumulation
TOXP$^{(b)}$	m	-	-	-	physical oxide thickness
AIGC$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}$	1.36e-2	-	-	parameter for Igc in inversion
BIGC$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}/V$	1.71e-3	-	-	parameter for Igc in inversion
CIGC$^{(b)}$	$1/V$	0.075	-	-	parameter for Igc in inversion
DIGC$^{(b)}$	-	1.0	-	-	parameter for Igc in inversion
PIGCD$^{(b)}$	-	1.0	0.0	-	V_{ds} dependence of Igcs and Igcd
DLCIGS	m	0.0	-	-	Delta L for Igs model.
AIGS$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}$	1.36e-2	-	-	parameter for Igs in inversion
BIGS$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}/V$	1.71e-3	-	-	parameter for Igs in inversion
CIGS$^{(b)}$	$1/V$	0.075	-	-	parameter for Igs in inversion
DIGS$^{(b)}$	-	1.0	-	-	parameter for Igs in inversion
AIGD$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}$	AIGS	-	-	parameter for Igd in inversion
BIGD$^{(b)}$	$(Fs^2/g)^{0.5}m^{-1}/V$	BIGS	-	-	parameter for Igd in inversion
CIGD$^{(b)}$	$1/V$	CIGS	-	-	parameter for Igd in inversion
DIGD$^{(b)}$	-	DIGS	-	-	parameter for Igd in inversion
DLCIGD	m	DLCIGS	-	-	Delta L for Igd model.
POXEDGE $^{(b)}$	-	1	0.0	-	Factor for the gate edge Tox
TOXREF	m	1.2nm	0.0	-	Nominal gate oxide thickness for Gate tunneling current
NTOX$^{(b)}$	-	1.0	-	-	Exponent for gate oxide ratio
AGIDL$^{(b)}$	Ω^{-1}	6.055e-12	-	-	pre-exponetial coeff. for GIDL
BGIDL$^{(b)}$	V/m	0.3e9	-	-	exponential coeff. for GIDL
EGIDL$^{(b)}$	V	0.2	-	-	band bending parameter for GIDL
PGIDL$^{(b)}$	$-$	1.0	-	-	Exponent of electric field for GIDL
VBGIDL$^{(b)}$	-	1.0	-	-	Back gate correction factor for GIDL
VBEGIDL$^{(b)}$	V	0.5	-	-	Back band bending parameter for GIDL
AGISL$^{(b)}$	Ω^{-1}	AGIDL	-	-	pre-exponetial coeff for GISL.
BGISL$^{(b)}$	V/m	BGIDL	-	-	exponential coeff. for GISL
EGISL$^{(b)}$	V	EGIDL	-	-	band bending parameter for GISL
PGISL$^{(b)}$	$-$	PGIDL	-	-	Exponent of electric field for GISL
VBGISL$^{(b)}$	-	VBGIDL	-	-	Back gate correction factor for GISL
VBEGISL$^{(b)}$	V	VBEGIDL	-	-	Back band bending parameter for GISL
ALPHA0$^{(b)}$	m/V	0.0	-	-	first parameter of Iii
ALPHA1 $^{(b)}$	$1/V$	0.0	-	-	L scaling parameter of Iii
BETA0$^{(b)}$	$1/V$	0.0	-	-	Vds dependent paramter of Iii

Name	Unit	Default	Min	Max	Description
LOVS	m	0.0	-	-	overlap length for g/s overlap (for capacitance calculation)
LOVD	m	LOVS	-	-	overlap length for g/d overlap (for capacitance calculation)
CFS	F/m	0.0	-	-	outer fringe cap
CFD	F/m	CFS	-	-	outer fringe cap
CGSL$^{(b)}$	F/m	0	0.0	-	Overlap capacitance between gate and lightly-doped source region
CGDL$^{(b)}$	F/m	CGSL	0.0	-	Overlap capacitance between gate and lightly-doped drain region
CKAPPAS$^{(b)}$	V	0.6	0.02	-	Coefficient of bias-dependent overlap capacitance for the source side
CKAPPAD$^{(b)}$	V	CKAPPAS	0.02	-	Coefficient of bias-dependent overlap capacitance for the drain side
PCOVBS0	V	0.0	-	-	Back-gate dependent overlap capacitance clamping shift voltage for the source side
PCOVBD0	V	PCOVBS0	-	-	Back-gate dependent overlap capacitance clamping shift voltage for the drain side
PCOVBS1	-	0.0	-	-	Parameter of back-gate dependent overlap capacitance for the source side
PCOVBD1	-	PCOVBS1	-	-	Parameter of back-gate dependent overlap capacitance for the drain side
CSDBGSW	F/m	0.0	-	-	Prefactor for bias-dependent inner fringe capacitance model
KBG0PW$^{(b)}$	-	1.0	-	-	Parameter for p-type substrate factor
KBG1PW$^{(b)}$	-	0	-	-	Parameter for length dependence p-type substrate factor
KBG2PW$^{(b)}$	-	-1	-	-	Parameter for length dependence of p-type substrate factor
DBGPW$^{(b)}$	-	0.12	-	-	Parameter for length dependence of p-type substrate factor
BPFACTORPW$^{(b)}$	-	0.0	0.0	1.0	Back-plane (BP) effect for p-type substrate, 0 means no BP
VKNEE1PW$^{(b)}$	V	0.0	-	-	Back gate voltage at which the p-type substrate depletion below the BOX starts

Name	Unit	Default	Min	Max	Description
VKNEE2PW$^{(b)}$	V	1.0	0.0	-	Maximum potential drop below the BOX for p-type substrate
KBG0NW$^{(b)}$	-	1.0	-	-	Parameter for n-type substrate factor
KBG1NW$^{(b)}$	-	0	-	-	Parameter for length dependence n-type substrate factor
KBG2NW$^{(b)}$	-	-1	-	-	Parameter for length dependence of n-type substrate factor
DBGNW$^{(b)}$	-	0.12	-	-	Parameter for length dependence of n-type substrate factor
BPFACTORNW$^{(b)}$	-	0.0	0.0	1.0	Back-plane (BP) effect for n-type substrate, 0 means no BP
VKNEE1NW$^{(b)}$	V	0.0	-	-	Back gate voltage at which the n-type substrate depletion below the BOX starts
VKNEE2NW$^{(b)}$	V	1.0	0.0	-	Maximum potential drop below the BOX for n-type substrate
EF	-	1.0	0.0	2.0	Flicker noise frequency exponent
LINTNOI	m	0.0	-	$L_{eff}/2$	L_{int} offset for flicker noise calculation
EM	V/m	4.1e7	-	-	Flicker noise parameter
NOIA	$eV^{-1}s^{1-EF}m^{-3}$	6.250e39	-	-	Flicker noise parameter
NOIB	$eV^{-1}s^{1-EF}m^{-1}$	3.125e24	-	-	Flicker noise parameter
NOIC	$eV^{-1}s^{1-EF}m$	8.750e7	-	-	Flicker noise parameter
NTNOI	-	1.0	0.0	-	Thermal noise parameter
QMTCENCV$^{(b)}$	-	0.0	-	-	Prefactor/switch for QM effective width and oxide thickness correction for CV
ETAQM$^{(b)}$	-	0.54	-	-	Body-charge coefficient for QM charge centroid
QM0$^{(b)}$	V	1e-3	0.0	-	Normalization parameter for QM charge centroid (inversion)
PQM$^{(b)}$	-	0.66	-	-	Fitting parameter for QM charge centroid (inversion)

6.4 Parameters for Temperature Dependence and Self Heating

Note: binnable parameters are marked as: $^{(b)}$

Name	Unit	Default	Min	Max	Description
TNOM	C	27	-273.15	-	Temperature at which the model is extracted (in Celcius)
TMAXC	C	400	-	-	Maximum Device Temperature (in Celcius)
TBGASUB	eV/K	7.02e-4	-	-	Bandgap Temperature Coefficient
TBGBSUB	K	1108.0	-	-	Bandgap Temperature Coefficient
KT1$^{(b)}$	V	0.0	-	-	V_{th} Temperature Coefficient
KT1L	$V \cdot m$	0.0	-	-	V_{th} Temperature Coefficient
KT2$^{(b)}$	$-$	0.0	-	-	V_{th} Temperature Coefficient
KT2L	m	0.0	-	-	Length dependent parameter for Vth Temperature Vbg Coefficient
UTE$^{(b)}$	-	0.0	-	-	Mobility Temperature Coefficient
UTL$^{(b)}$	-	-1.5e-3	-	-	Mobility Temperature Coefficient
UA1$^{(b)}$	-	1.032e-3	-	-	Mobility Temperature Coefficient for UA
UC1$^{(b)}$	-	0.0	-	-	Mobility Temperature Coefficient for UC
UD1$^{(b)}$	-	0.0	-	-	Mobility Temperature Coefficient
UCSTE$^{(b)}$	-	-4.775e-3	-	-	Mobility Temperature Coefficient
AT$^{(b)}$	$1/K$	-0.00156	-	-	Saturation Velocity Temperature Coefficient
ATL$^{(b)}$	m	0.0	-	-	Length scaling parameter for AT
TMEXP$^{(b)}$	-	0	-	-	Temperature Coefficient for smoothing function factor for Vdsat
ATB$^{(b)}$	$1/K$	0.0	-	-	Back bias sensitivity parameter for saturation velocity temperature coefficient
ATBL$^{(b)}$	m	0.0	-	-	Length scaling parameter for ATB
K0$^{(b)}$	V	0.0	-	-	Lateral NUD voltage parameter
K01$^{(b)}$	V/K	0.0	-	-	Temperature dependence of K0
K0SI$^{(b)}$	-	1.0	-	-	Correction factor for strong inversion, used in Mnud
K0SI1$^{(b)}$	$1/K$	0.0	-	-	Temperature dependence of K0SI
PTWGT$^{(b)}$	$1/K$	0.004	-	-	PTWG Temperature Coefficient
PRT$^{(b)}$	$1/K$	0.001	-	-	Series Resistance Temperature Coefficient
TETA0$^{(b)}$	-	0.0	-	-	Temperature Depdence for DIBL effect

IIT$^{(b)}$	-	-0.5	-	-	Impact Ionization Temperature Coefficient

Name	**Unit**	**Default**	**Min**	**Max**	**Description**
TGIDL$^{(b)}$	$1/K$	-0.003	-	-	GIDL Temperature Coefficient
TGISL$^{(b)}$	$1/K$	TGIDL	-	-	GISL Temperature Coefficient
IGT$^{(b)}$	-	2.5	-	-	Gate Current Temperature Coefficient
RTH0	$\Omega \cdot m \cdot K/W$	0.01	0.0	-	Thermal resistance for self-heating calculation
CTH0	$W \cdot s/m/K$	1.0e-5	0.0	-	Thermal capacitance for self-heating calculation
WTH0	m	0.0	0.0	-	Width-dependence coefficient for self-heating calculation

References

[1] Y. Cheng and C. Hu, *MOSFET Modeling and BSIM3 User's Guide*. Kluwer Academic Publishers, 1999.

[2] S. Khandelwal, Y. Chauhan, D. Lu, S. Venugopalan, M. Karim, A. B.-Y. N. Sachid, O. Rozeau, O. Faynot, A. Niknejad, and C. Hu, "BSIM-IMG: a compact model for ultrathin-body SOI MOSFETs with back-gate control," *IEEE Transaction on Electron Devices*, vol. 59, no. 8, pp. 2019–2026, August 2012.

[3] D. Lu, M. V. Dunga, C.-H. Lin, A. M. Niknejad, and C. Hu, "A multi-gate MOSFET compact model featuring independent-gate operation," in *IEDM Technical Digest*, 2007, p. 565.

[4] S. jandhyala and S. Mahapatra, "An Efficient Robust Algorithm for the Surface-Potential Calculation of Independent DG MOSFET," june 2011.

[5] K. Jordar, K. K. Gullapalli, C. C. McAndrew, M. E. Burnham, and A. Wild, "An Improved MOSFET Model for Circuit Simulation," *IEEE Transaction on Electron Devices*, vol. 45, no. 1, pp. 134–148, 1998.

[6] *BSIM Models*. Department of Electrical Engineering and Computer Science, UC Berkeley. [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIM4

[7] J. He, J. Xi, M. Chan, H. Wan, M. Dunga, B. Heydari, A. M. Niknejad, and C. Hu, "Charge-Based Core and the Model Architecture of BSIM5," in *International Symposium on Quality Electronic Design*, 2005, pp. 96–101.

[8] *BSIM5.0.0 MOSFET Model*, BSIM Group, The Regents of the University of California, February 2005.

[9] X. Jin, J.-J. Ou, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, "An Effective Gate Resistance Model for CMOS RF and Noise Modeling," in *IEDM Technical Digest*, 1998, p. 961.

[10] *BSIM-SOI Model*. Department of Electrical Engineering and Computer Science, UC Berkeley. [Online]. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIMSOI

[11] K. Hung, P.-K. Ko, C. Hu, and Y. Cheng, "A physics-based mosfet noise model for circuit simulators," *Electron Devices, IEEE Transactions on*, vol. 37, no. 5, pp. 1323–1333, May 1990.

[12] Y. Morita *et al.*, "Smallest Vth Variability Achieved by Intrinsic Silicon on Thin BOX (SOTB) CMOS with Single Metal Gate," *VLSI Technology, IEEE Symposium on*, pp. 166 – 167, 2008.

Acknowledgments

We deeply appreciate the feedback we received from (in alphabetical order by last name):

Brian Chen (Accelicon)

Wei-Hung Chen (UC Berkeley)

Jung-Suk Goo (GlobalFoundries)

Keith Green (TI)

Ben Gu (Freescale)

Wilfried Haensch (IBM)

Min-Chie Jeng (TSMC)

Yeung Gil Kim (Proplus Solutions)

Wai-Kit Lee (TSMC)

Dayong Li (Cadence)

Hancheng Liang (Proplus Solutions)

Sally Liu (TSMC)

Weidong Liu (Synopsys)

James Ma (Proplus Solutions)

Colin C. McAndrew (Freescale)

Slobodan Mijalkovic (Silvaco)

Andrei Pashkovich (Silvaco)

S. C. Song (Qualcomm)

Ke-wei Su (TSMC)

Robert Tu (GlobalFoundries)

Charly Sun (Synopsys)

Lawrence Wagner (IBM)

Joddy Wang (Synopsys)

Qingxue Wang (Synopsys)

Josef Watts (IBM)

Richard Williams (IBM)

Dehuang Wu (Synopsys)

Jane Xi (Synopsys)

Jushan Xie (Cadence)

Wade Xiong (TI)

Wenwei Yang (Proplus Solutions)
Fulong Zhao (Cadence)

Manual updated: 10/30/2018