DEV Board learning project

Variant: [No Variations]

22/06/2020
V1I1

Cannot open file 28Pins3D.png

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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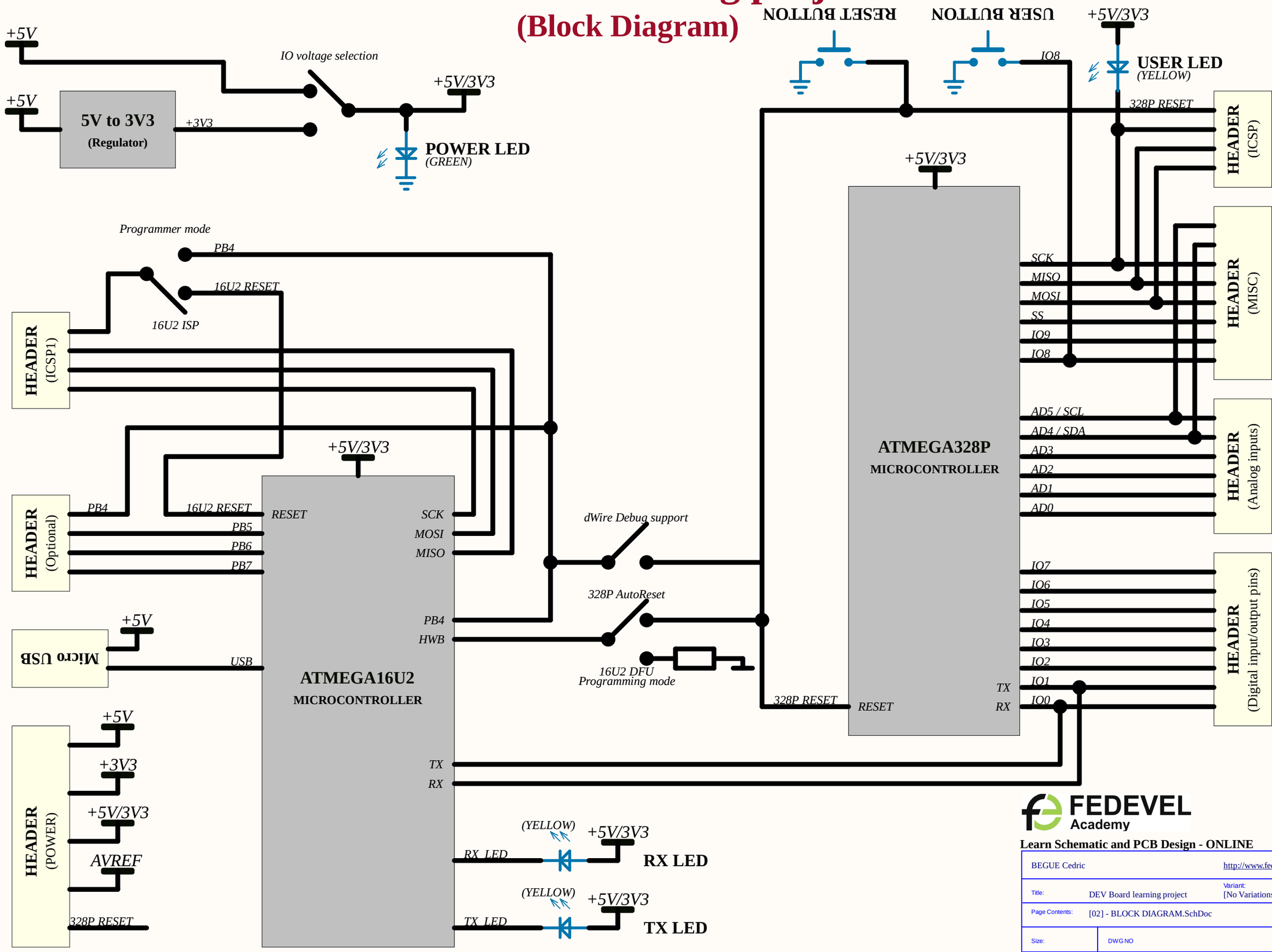
DEV Board learning project

(Block Diagram)



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28PINS - SCHEMATIC

based on : http://www.28pins.com

DESIGN NOTE:
This board supports 5V or 3V3 voltage level on the IO pins:
1) 5V IO - Fit everything as defined in this schematic. NF means, do not fit this component.

2) 3.3V IO - Remove R27, Fit R28, *Replace Y1 (change from 16MHz to 10MHz), *Replace Y2 (change from 16MHz to 8MHz).

3) Both 5V and 3V3, selected through JP4 - Remove R27, Remove R28, Fit JP4, *Replace Y1 (change from 16MHz to 10MHz), *Replace Y2 (change from 16MHz to 8MHz).

*Note: The 16MHz crystals are not recommended for 3.3V operation. We need to adjust their values, thats why the change.

IMPORTANT: Once you change the crystal value, you may need to re-compile your source code.

DESIGN NOTE:

About JP3:
1) DebugWire support - Short 1&2. This was added to support possible debugWire debugging (programming?) of 328P through 16U2. In this case, the 16U2 needs to have a correct firmware and has to behave as a debugWire tool.

2) ISP programmer mode - Short 2&3. In this case, take a cable and connect J5 & J6 together. Upload AVRISP MKII firmware into 16U2 and you can program 328P. Example of AVRISP MKII firmware can be found at LUFA projects: http://www.fourwalledcubicle.com/LUFA.php (Tip: remap LEDs of the default AVRISP MKII LUFA project to the RX and TX LEDs on the 28Pin board)

3) ISP header - Short 3 & 4. In this mode, the ICSP1 header is used as a standard ISP header to program 16U2 through ISP interaface by an ISP programmer.

DESIGN NOTE:

About JP1:
1) Autoreset Enabled - Short 1&2. In this case, 16U2 is used to reset 328P when firmware inside 328P is updated from Arduino IDE.

2) 16U2 DFU mode Enabled - Short 2&3. 16U2 HWB pin is sampled by 16U2 during RESET. If pulled low, then after Reset the 16U2 will go into DFU mode (it's the mode when you can flash 16U2 firmware through USB and Atmel Flip software: http://www.atmel.com/tools/flip.aspx).

Micro USB

USB board/pc - pc/board filter

+5V_USB
L1 2u2 / 2A
C1 100u / 10V
C2 100u / 10V
J7 10118193-0001LF
CON_USB_N
CON_USB_P
R8 0R
Z1 CG0603MLC-05E
Z2 CG0603MLC-05E

One 100n near VCC, one near AVCC

+5V3V3 FB1 MPZ2012S601AT000 +5V3V3_16U2
C3 10u / 16V
C4 100n
C5 100n
+5V3V3 +5V R4 10K C6 100n
16U2_RESETn
NF R26 0R
C7 1u / 25V +3V3_16U2_UCAP

16U2

U2 ATMEGA16U2-AU

VCC		
AVCC		
UVCC		
	(PCINT7 / OC.0A / OC.1C) PB7	16U2_PB7
	(PCINT6) PB6	16U2_PB6
	(PCINT5) PB5	16U2_PB5
	(T1 / PCINT4) PB4	16U2_PB4
Reset (PC1 / dW)	(PDO / MISO / PCINT3) PB3	16U2_MISO
	(PDI / MOSI / PCINT2) PB2	16U2_MOSI
	(SCLK / PCINT1) PB1	16U2_SCLK_R
UCAP	(SS / PCINT0) PB0	
	(INT4 / ICP1 / CLKO) PC7	
	(OC.1A / PCINT8) PC6	
D-	(PCINT9/ OC.1B) PC5	
D+	(PCINT10) PC4	
	(PCINT11 /AIN2) PC2	
	(CTS/ HWB / AIN6 / T0 / INT7) PD7	16U2PROG_328P_RESETn
XTAL2 (PC0)	(RTS / AIN5 / INT6) PD6	16U2TX_LED
XTAL1	(XCK AIN4 / PCINT12) PD5	16U2RX_LED
	(INT5/ AIN3) PD4	16U2_TXD
	(TXD1 / INT3) PD3	16U2_RXD
	(RXD1 / AIN1 / INT2) PD2	
UGND	(AIN0 / INT1) PD1	
GND	(OC.0B / INT0) PD0	

C9 18p
16U2_16MHZ_XTAL2
Y2
R9 1M
16U2_16MHZ_XTAL1
C10 18p
ABM7-16.000MHZ-D2Y-T

+5V3V3 R1 100K
+5V3V3 R2 560R
+5V3V3 R3 560R
D3 Orange
D4 Orange

R6 22R USB_N
R7 22R USB_P
R8 0R
R10 1K
R11 1K
R5 22R 16U2_SCLK

JP2

JP2 HDR 2x2 2.54
NF
J6 HDR 2x3 2.54
+5V3V3 C8 100n

ICSP1

JP3

JP3 HDR 1x4
328P_RESETn
16U2_PB4
16U2_HDR_RESETn
16U2_RESETn
LINK1 LINK

JP1

328P_AUTORESETn
C11 100n
JP1 HDR 1x3
16U2PROG_328P_RESETn
R12 1K
LINK2 LINK

Power

+5V +5V3V3 +3V3 +5V3V3
C14 100n
C15 100n
C16 100n
C34 10u / 16V
J1 HDR FEMALE 1x8 2.54
328P_RESETn

DESIGN NOTE:
Pin 8 (VIN) is not supported

Power pads

+5V JP8 4MMx1.5MM
JP9 4MMx1.5MM

To power the board when not using the usb port

3V3 LDO

+5V U3 TL1963A-33DCQR +3V3
C12 10u / 16V
C13 10u / 16V

Power selection

+5V R27 0R +5V3V3 R28 NF 0R +3V3
JP4 HDR 1x3
LINK3 NF LINK

DESIGN NOTE:
This board can be powered from micro USB connector (J7) or a single +3.3V power rail (through J1 pin 4). If +3.3V is used, fit R26 and R28. In this case, JP4 & R27 must NOT be fitted, otherwise the board may be damaged.

ICSP

J5 HDR 2x3 2.54
MISO
328P_RESETn
+5V3V3 C17 100n

DIP socket

SCKT FOR U1
20 DIP SOCKET
28-DIP Socket

Mounting Holes

plated mounting holes
non plated mounting hole
MH4
MH1 MH2 MH3
Mounting holes 7.4mm pad 3.2mm drill
BOARD MOUNTING HOLES
ONE IN EACH CORNER

Power led

+5V3V3 R17 560R D1 Green

User led

+5V3V3 R15 560R D2 Green
+5V3V3 C26 100n
SCK
U4 SN74AHC1G09DBVR
AND
DESIGN NOTE:
This LED is inverted:
- SCK High = LED OFF
- SCK Low = LED ON

328P

+5V3V3 FB2 MPZ2012S601AT000 +5V3V3_328P_VCC
C19 10u / 16V
C20 100n
+5V3V3 FB3 MPZ2012S601AT000 +5V3V3_328P_AVCC
C22 10u / 16V
C23 100n
+5V3V3 +AREF
C24 100n
R14 10K
328P_RESETn
C25 18p
328P_16MHZ_XTAL2
Y1
R16 1M
328P_16MHZ_XTAL1
C27 18p
ABM7-16.000MHZ-D2Y-T

U1 ATMEGA328P-PU

VCC		
AVCC		
AREF		
	SCK/PCINT5/PB5	SCK_R
	MISO/PCINT4/PB4	MISO
	MOSI/OC2A/PCINT3/PB3	MOSI
	SS/OC1B/PCINT2/PB2	SS
	OC1A/PCINT1/PB1	IO9
	CLKO/ICP1/PCINT0/PB0	IO8
	SLC/PCINT13/ADC5/PC5	AD5/SCL
	SDA/PCINT12/ADC4/PC4	AD4/SDA
	PCINT11/ADC3/PC3	AD3
	PCINT10/ADC2/PC2	AD2
	PCINT9/ADC1/PC1	AD1
	PCINT8/ADC0/PC0	AD0
PC6/PCINT14/RESET		
	AIN1/PCINT23/PD7	IO7
	OC0A/AIN0/PCINT22/PD6	IO6
PB7/PCINT7/TOSC2/XTAL2	OC0B/T1/PCINT21/PD5	IO5
	XCK/T0/PCINT20/PD4	IO4
PB6/PCINT6/TOSC1/XTAL1	OC2B/INT1/PCINT19/PD3	IO3
	INT0/PCINT18/PD2	IO2
GND_1	TXD/PCINT17/PD1	IO1
GND_2	RXD/PCINT16/PD0	IO0

22R are usually placed close to clk outputs

R13 22R SCK_R

IOH

J4 HDR Female 1x10 2.54
AD5/SCL
AD4/SDA
SCK

AD

J2 HDR Female 1x6 2.54

IOL

J3 HDR FEMALE 1x8 2.54

Fiducials

FID1 FID2 FID3 FID4

LAYOUT NOTE:
1) Route all the POWER tracks with minimum track width 0.4mm.
2) Route all the other tracks by 0.4mm and change them by the end of the design to 0.2mm. To change all of them at once, use this filter "(not InNet('+*') and not InNet('GND')) and IsTrack and (OnLayer('L1') or OnLayer ('L2'))" and then set 0.2mm width in PCB Inspector panel.

Reset (16U2)

+5V3V3 +5V3V3 D5 BAT54HT1G
R19 10K
22R R23 16U2_BUF_RESETn
+5V3V3 C30 100n
U5 SN74AHC1G09DBVR
AND
16U2_RESETn
C31 100n

Reset (328P)

+5V3V3 +5V3V3 D6 BAT54HT1G
R20 10K
SW1 1825910-6
BUTTON_RESETn
22R R24 328P_BUF_RESETn
+5V3V3 R18 10K
+5V3V3 C28 100n
328P_AUTORESETn
U6 SN74AHC1G09DBVR
AND
328P_RESETn
C32 100n

User Button

+5V3V3 R21 10K
SW2 1825910-6
USER_BUTTON
22R R25 USER_BUTTON_BUF
+5V3V3 C29 100n
U7 SN74AHC1G09DBVR
AND
R22 560R IO8
C33 100n

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Designator
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Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - 28PINS SCHEMATIC.SchDoc

Designator
[04] - REVISION HISTORY.SchDoc

NOTES

Mark Not Fitted Components as
NF

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

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