



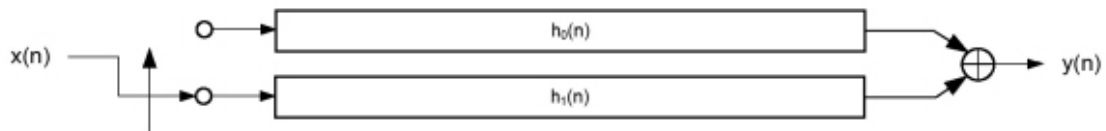
FIR Compiler (PG149)

Half-band Decimator

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The half-band decimator is a polyphase filter with an embedded 2-to-1 down-sampling of the input signal. [This Figure](#) shows the structure.

Figure: Half-band Decimation Filter



The filter is very similar to the polyphase decimator described in Polyphase Decimator with the decimation factor set to $M = 2$. However, there is a subtle difference in the implementation that makes the half-band decimator a more area-efficient 2-to-1 down-sampling filter when the frequency response reflects a true half-band characteristic.

The frequency and time response of a half-band filter are shown in [This Figure](#) and [This Figure](#), respectively. Observe the alternating zero-valued coefficients in the impulse response. [This Figure](#) details a 7-tap half-band polyphase filter when the coefficients are allocated to the two polyphase segments $h_0(n)$ and $h_1(n)$ shown in [This Figure](#). [This Figure](#) (a) is the filter impulse response ($a_1 = 0 = a_5$). [This Figure](#) (b) provides a detailed illustration of the polyphase subfilters and shows how the filter coefficients are allocated to the two polyphase arms.

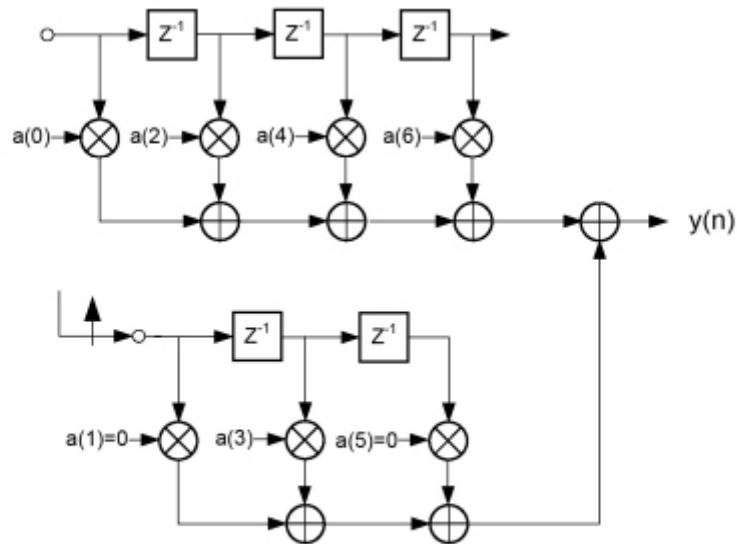
In the bottom arm, $h_1(n)$, the only non-zero coefficient, is the center value of the impulse response a_3 . [This Figure](#) (c) shows the optimized architecture when the redundant multipliers and adders are removed and coefficient symmetry is exploited. The final structure has a reduced computation workload in contrast to a more general 2:1 down-sampling filter.

The number of multiply-accumulate (MAC) operations required to compute an output sample has been lowered by a factor of approximately two. In this figure, the high density of zero-valued filter coefficients is exploited in the FPGA realization to produce a minimal area implementation.

Figure: 7-Tap Half-band Decimation Filter

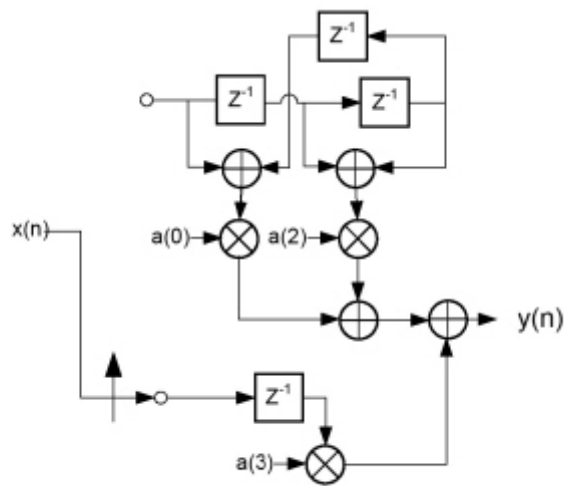


(a) Impulse Repsonse



$x(n)$ —

(b) Polyphase Partition



(c) Reduced Complexity (Hardware Optimized) Realization