AC300

Datasheet

Revision 1.0

September 2, 2022

Revision History

Revision	Date	Author	Description
1.0	September 2, 2022	KPA0569	Initial release version

Contents

Figures

Tables

About This Document

Purpose and Scope

This document describes the block diagram, power supply diagram, power-on and power-off sequence, clock and reset tree, and system registers of the TOP module of AC300.

Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Reset Value Conventions

In the register definition tables:

If other column value in the row of a bit or multiple bits is “/”, this bit of these multiple bits are unused.

If the default value of a bit or multiple bits is “UDF”, this default value is undefined.

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has no effect
R/W1C	Read/Write 1 to Clear, Writing 0 has no effect
R/W1S	Read/Write 1 to Set, Writing 0 has no effect
W	Write Only

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

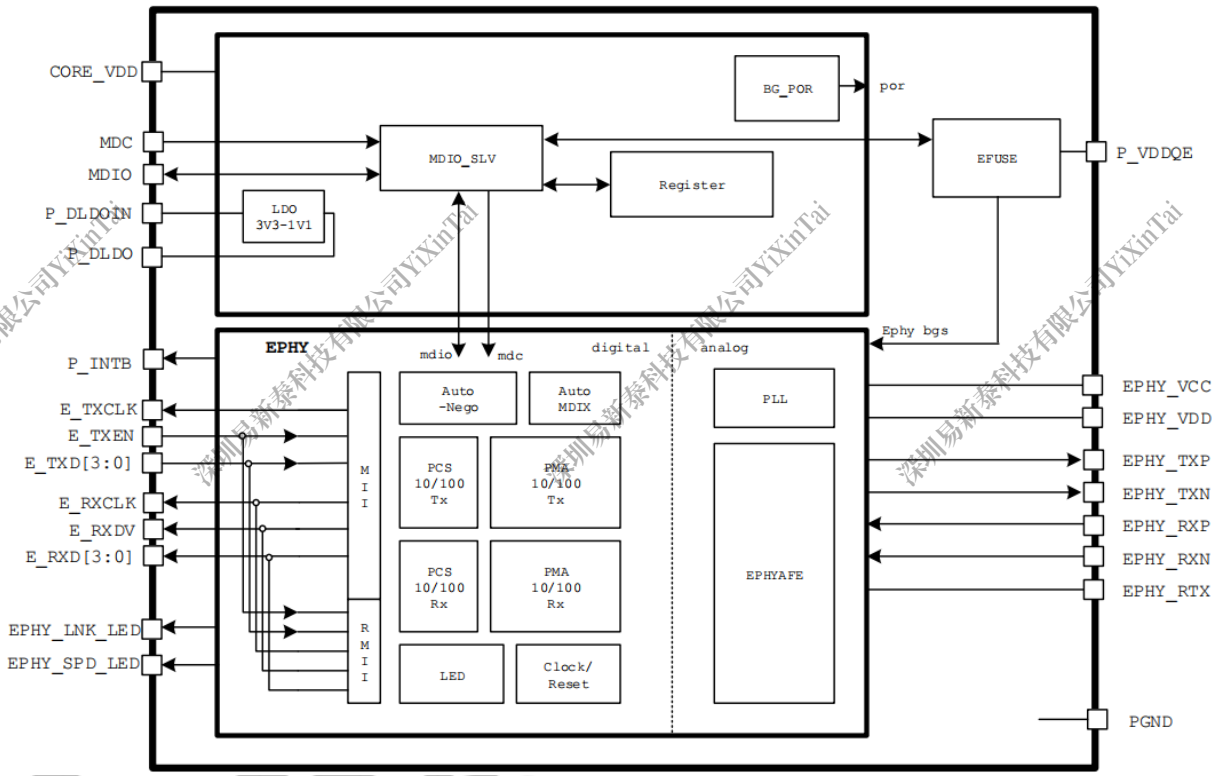
The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary (register description is excluded.)
X	00X,XX1	In data expression, X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

1 Block Diagram

Figure 1-1 shows the block diagram of the AC300.

Figure 1-1 AC300 Block Diagram

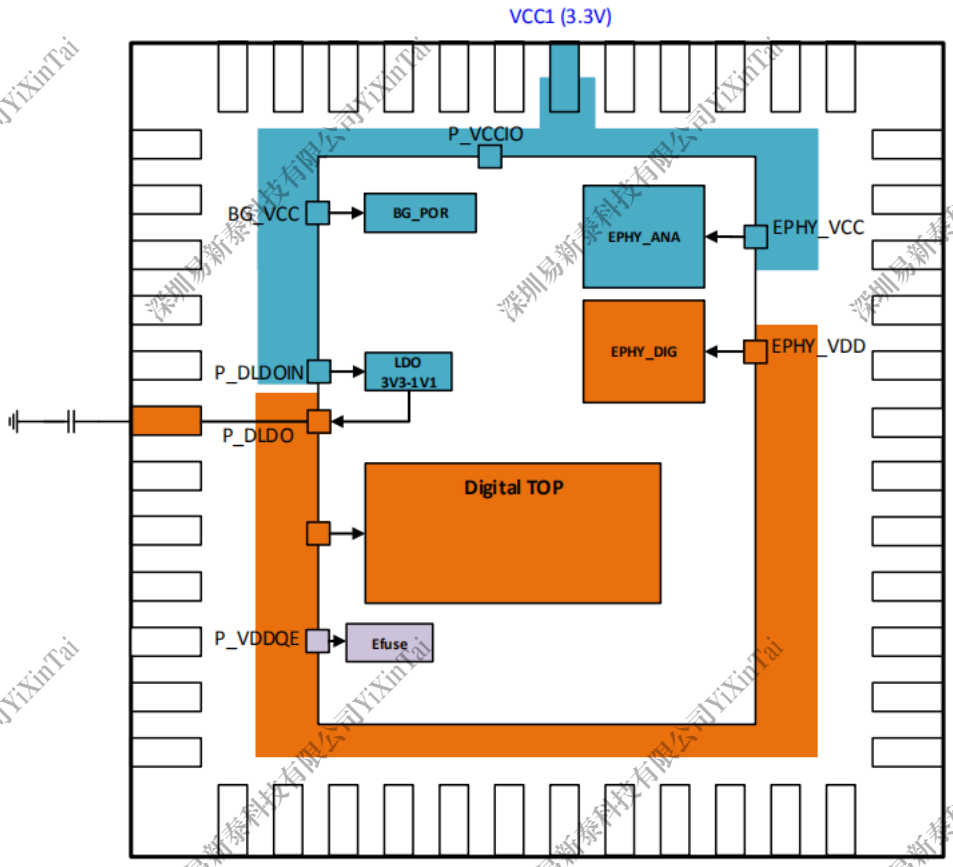


2 Power & Timing

2.1 Power Supply Diagram

Figure 2-1 shows the power supply diagram of the AC300.

Figure 2-1 AC300 Power Supply Diagram

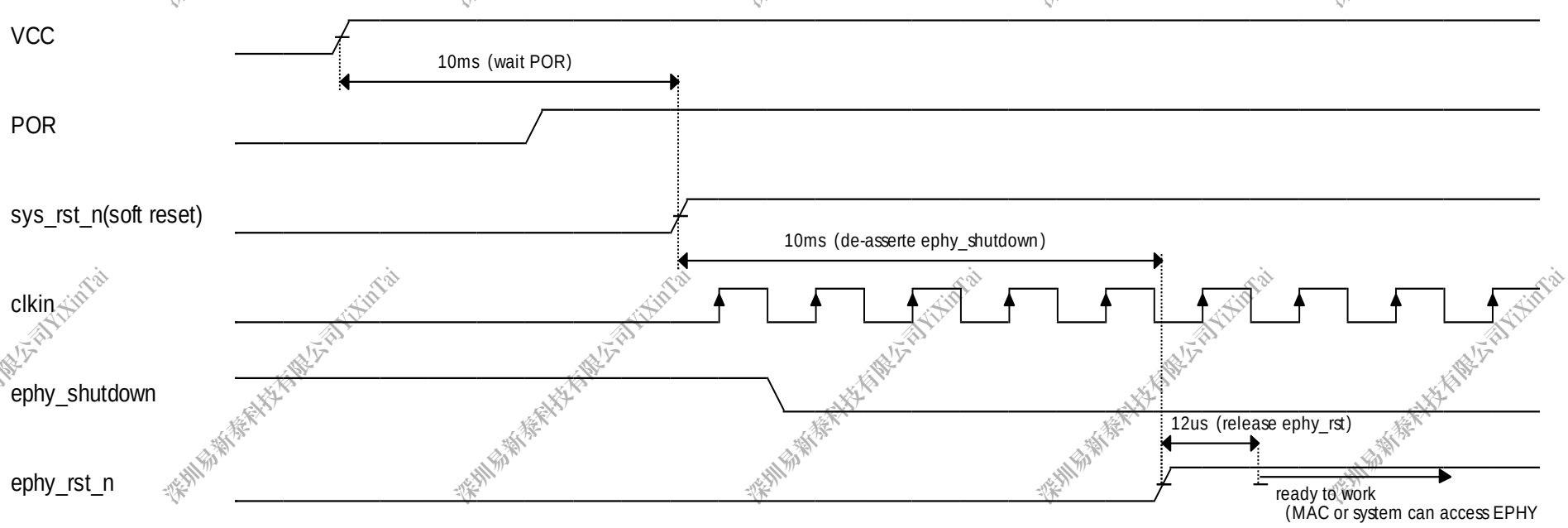


2.2 Power-On and Power-Off Sequence

2.2.1 Power-On Sequence

Figure 2-2 shows the power-on sequence for the AC300.

Figure 2-2 AC300 Power-On Sequence

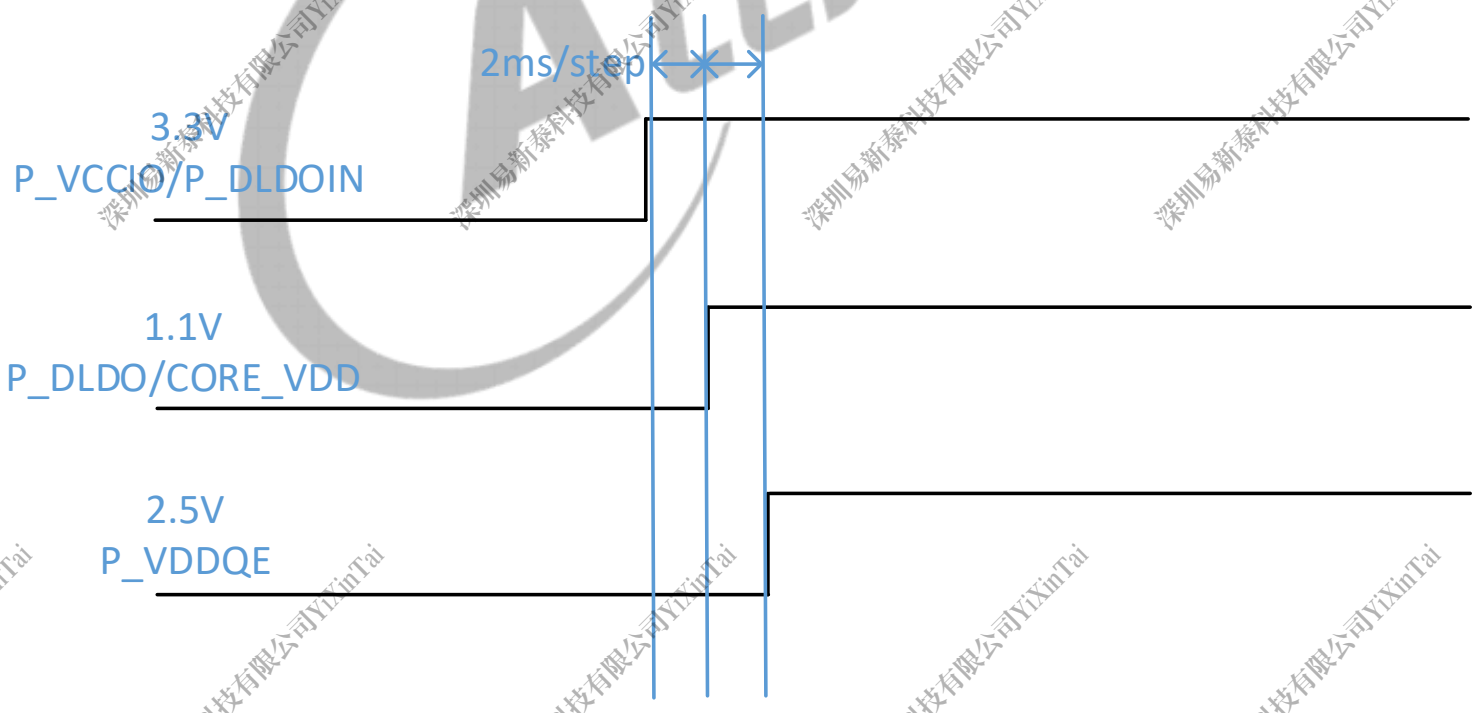


When performing eFuse programming, ensure that CORE_VDD is powered on earlier than VDDQE.

2.2.2 Power-Off Sequence

Figure 2-3 shows the power-off sequence for the AC300.

Figure 2-3 AC300 Power-Off Sequence



3 Clock & Reset Tree

Figure 3-1 shows the clock and reset tree for the AC300.

Figure 3-1 AC300 Clock and Reset Tree

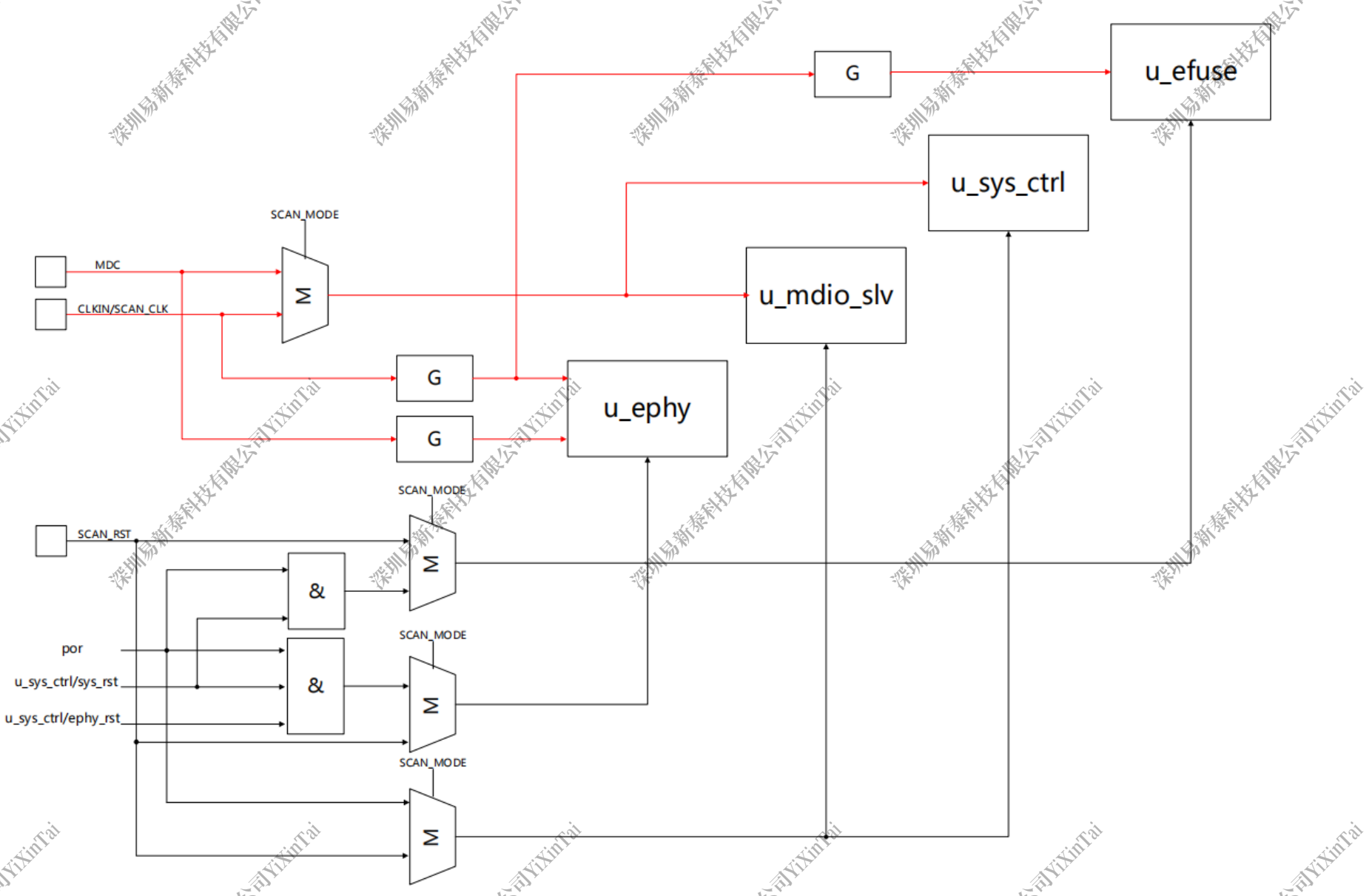


Table 3-1 lists the requirements for CLKIN.

Table 3-1 CLKIN Requirements

Symbol	Description	Value	Unit
F_{sys}	System clock frequency	24+/-50ppm 25+/-50ppm 27+/-50ppm	MHz
D_{sys}	System clock duty-cycle	45-55	%
T_{sys_jit}	System clock TIE peak-to-peak jitter	0.15(maximum)	ns

4 Register

4.1 System Register List

Register Name	Offset	Description
System control Register	0x00	00h System control Register
System BIAS Register0	0x01	01h System BIAS Register0
System BIAS Register1	0x02	02h System BIAS Register1
System IO Register	0x05	04h Mask version Register
EPHY Configurate Register	0x06	05h System IO Register
EPHY BIST Register	0x07	06h EPHY Configurate Register
SID Program/Read Register	0x08	07h EPHY BIST Register
SID Program/Read timing control Register0	0x09	08h SID Program/Read Register
SID Program/Read timing control Register1	0x0a	09h SID Program/Read timing control Register0
SID_EPHY Parameter Register	0x10	0ah SID Program/Read timing control Register1
SID_BG Parameter Register	0x11	10h SID_EPHY Parameter Register
SID_RESERVED Parameter Register	0x12~17	12~17h SID_RESERVED Parameter Register
SID_EPHY Program Parameter Register	0x18	18h SID_EPHY Program Parameter Register
SID_BG Program Parameter Register	0x19	19h SID_BG Program Parameter Register
SID_RESERVED Program Parameter Register	0x1a~1f	1a~1fh SID_RESERVED Program Parameter Register

4.2 System Register Description

PHY_ADR=~PKG[2:0], default: 0, CFG_ADR=16+PHY_ADR

RESET_SEL=PKG[3], default: 1 choose POR and internal DLDO, when tie0, choose RESET PIN and external VDD.

4.2.1 00h System control Register

Default: 0x1f80			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
15:12	/	0x1	Chip version
11:8	R	0xf	PKG_STATUS
7:6	R/W	0x2	EPHY_CLK_SEL 0: 25MHz 1: 27MHz 2: 24MHz
5	R/W	0	EFUSE_REG_CLK_GATING 0: Clock is OFF 1: Clock is ON Before program or read efuse, first release CHIP_RESET (bit0), then release EFUSE_REG_CLK_GATING.
4	R/W	0	EPHY_REG_CLK_GATING 0: Clock is OFF 1: Clock is ON
3	R/W1C	0	MDIO ERROR
2	R/W	0	CLKIN_GATING (for EPHY and Efuse) 0: 24/25/27M Clock is OFF 1: 24/25/27M Clock is ON
1	R/W	0	EPHY_RESET_INVALID 0: Reset 1: Reset Invalid First release CHIP_RESET and EPHY_RESET_INVALID, then release CLKIN_GATING and EPHY_REG_CLK_GATING.
0	R/W	0	CHIP_RESET 0: reset all register to their default state. 1: reset invalid

4.2.2 01h System BIAS Register0

Default: 0x1084			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
12:8	R/W	0x10	BGTC BANDGAP Temp Coefficient Tuning Coefficient should be statistic from test.

Default: 0x1084			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
7	R/W	0x1	BG_EN BANDGAP Enable 0: Disable 1: Enable
6	/	/	/
5:0	R/W	0x4	BGV BANDGAP Voltage Tuning 011111: 814.8mV 000004: 701.4mV 000000: 684.6mV 100000: 550.2mV Step is 4.2mV

4.2.3 02h System BIAS Register1

Default: 0xC000			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x1	DLDOEN Digital LDO enable 0: disable; 1: enable When PKG[3] is tied 0,digital top use external VDD_CORE, and this bit should set 0.
14:12	R/W	0x4	DLDOVOL DLDO Voltage select 000: 0.825V 001: 0.880V, 010: 0.943V 011: 1.015V 100: 1.1V 101: 1.2V 110: 1.32V 111: 1.467V
11:0	/	/	/

4.2.4 04h Mask version Register

Default: 0x0			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
15:3	/	/	/
2:0	R	0x0	MASK version These bits show the mask version of the chip

4.2.5 05h System IO Register

Default: 0xa800			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
15:14	R/W	0x2	MDIO DRV Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x2	LED DRV Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x2	MII DRV Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9	R	0	EPHY_IRQ_STATUS 0: IRQ is waiting 1: IRQ is pending
8	R/W	0	EPHY_IRQ_ENABLE 0: IRQ is disable 1: IRQ is enable
7:5	/	/	/
4	R/W	0	CLKIN_PAD_EN(24M/25M/27M) 0: CLKIN_PAD io is disable 1: CLKIN_PAD io is enable
3	R/W	0	E_DPX_LED_IO_EN 0: E_DPX_LED io is disable 1: E_DPX_LED io is enable
2	R/W	0	E_SPD_LED_IO_EN 0: E_SPD_LED io is disable 1: E_SPD_LED io is enable

Default: 0xa800			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
1	R/W	0	E_LNK_LED_IO_EN 0: E_LNK_LED io is disable 1: E_LNK_LED io is enable
0	R/W	0	EPHY_MII_IO_EN 0: all MII io is disable 1: MII

4.2.6 06h EPHY Configurate Register

Default: 0x01			Register Name: SYS_IRQ_ENABLE0
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	BGS_EFFUSE
11	R/W	0x0	XMII_SEL 0: MII 1: RMII
10:9	R/W	0x0	EPHY_MODE Operation Mode Selection 00: Normal Mode 01: Sim Mode 10: AFE Test Mode 11: /
8:4	/	/	/
3	R/W	0x0	BIST_CLK_EN 0: BIST clk disable 1: BIST clk enable
2	/	/	/
1	R/W	0x0	LED_POL 0: High active 1: Low active
0	R/W	0x1	SHUTDOWN 0: Power up 1: Shutdown

4.2.7 07h EPHY BIST Register

Default: 0x00			Register Name: SYS_IRQ_ENABLE1
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/

Default: 0x00			Register Name: SYS_IRQ_ENABLE1
Bit	Read/Write	Default	Description
13:8	R	0x0	BIST_STATUS bist_status[5]:BIST_FAIL_RMII2MII bist_status[4]:BIST_FAIL_MII2RMII bist_status[3]:BIST_FAIL_PLPIC bist_status[2]:BIST_FINISH_RMII2MII bist_status[1]:BIST_FINISH_MII2RMII bist_status[0]:BIST_FINISH_PLPIC
7:1	/	/	/
0	R/W	0x0	BIST_START 0: disable 1: Start

4.2.8 08h SID Program/Read Register

Default: 0x0			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:8	R/W	0x0	OP_LOCK, 0xAC
7:2	/	/	/
1	WAC	0x0	Efuse read start, write 1 to start, and self clear after finish (A efuse program start during reading will be ignored. If read and program start at same time, program will be ignored. This bit can't be cleared by writing 0.) (Efuse 128~256bit used for backup)
0	WAC	0x0	Efuse program start, write 1 to start, and self clear after finish efuse read start during programming will be ignored. If read and program start at same time, program will be ignored. This bit can't be cleared by writing 0. (Efuse 128~256bit used for backup)

4.2.9 09h SID Program/Read timing control Register0

Default: 0xBB05			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:8	R/W	0xBB	Taen_pgm cycles (actuall cycles = reg_val X2)
7:0	R/W	0x5	Taen_rd cycles

4.2.10 0ah SID Program/Read timing control Register1

Default: 0x7e03			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:8	R/W	0x7E	Tpgm cycles (actual cycles = reg_val X 2)

Default: 0x7e03			Register Name: GPIO Register
Bit	Read/Write	Default	Description
7:0	R/W	0x3	Trd cycles

4.2.11 10h SID_EPHY Parameter Register

Default: 0x			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:0	R	x	EPHY Parameter

4.2.12 11h SID_BG Parameter Register

Default: 0x			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:0	R	x	BG Parameter

4.2.13 12~17h SID_RESERVED Parameter Register

Default: 0x			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:0	R	x	Reserved

4.2.14 18h SID_EPHY Program Parameter Register

Default: 0x			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:0	R/W	0	EPHY Program Parameter

4.2.15 19h SID_BG Program Parameter Register

Default: 0x			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:0	R/W	0	BG Program Parameter

4.2.16 1a~1fh SID_RESERVED Program Parameter Register

Default: 0x			Register Name: GPIO Register
Bit	Read/Write	Default	Description
15:0	R/W	0	Reserved

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