REVISION HISTORY

Schematics Index:

Revision	Description	Date	Drawn	Checked
Ver 0.1	Initial Version	2020-01-10	YJY	
Ver 0.2	Change some ref name ADD DDR3 16X2 ADD BT	2020-03-09	YJY	
Ver 1.0	ADD DCDCE FOR WIFI	2020-03-09	YJY	
Ver 1.1	ADD resistor at GPIOI for PCB version.	2020-03-17	YJY	
Ver 1.2	CUT twi3,which is be used by internal	2020-03-23	YJY	
Ver 1.3	Modify CLOD1 and DCDCE defalut on。 Change WIFI crystal to 40Mhz. ADD DDR4 16X4	2020-04-14	YJY	
Ver 1.4	Modify DRAM para identification cicuit ADD Note	2020-05-11	HHY	
Ver 1.5	ADD Note	2020-05-13	HHY	
Ver 1.6	VCC-3V3 modify	2020-06-08	HHY	
Ver 2.0	ADD AXP313A	2020-11-10	HHY	
Ver 2.1	ADD REXT Decoupling capacitor	2020-12-15	HHY	
Ver 2.2	ADD LDO and DCDC	2021-02-03	HHY	
Ver 2.3	Delete 5gwifi-en	2021-03-03	HHY	
Ver 2.4	HDMI-5V add NC schottky diode	2021-09-16	HHY	
Ver 2.5	Updated U3 package on page 16	2021-12-28	HHY	

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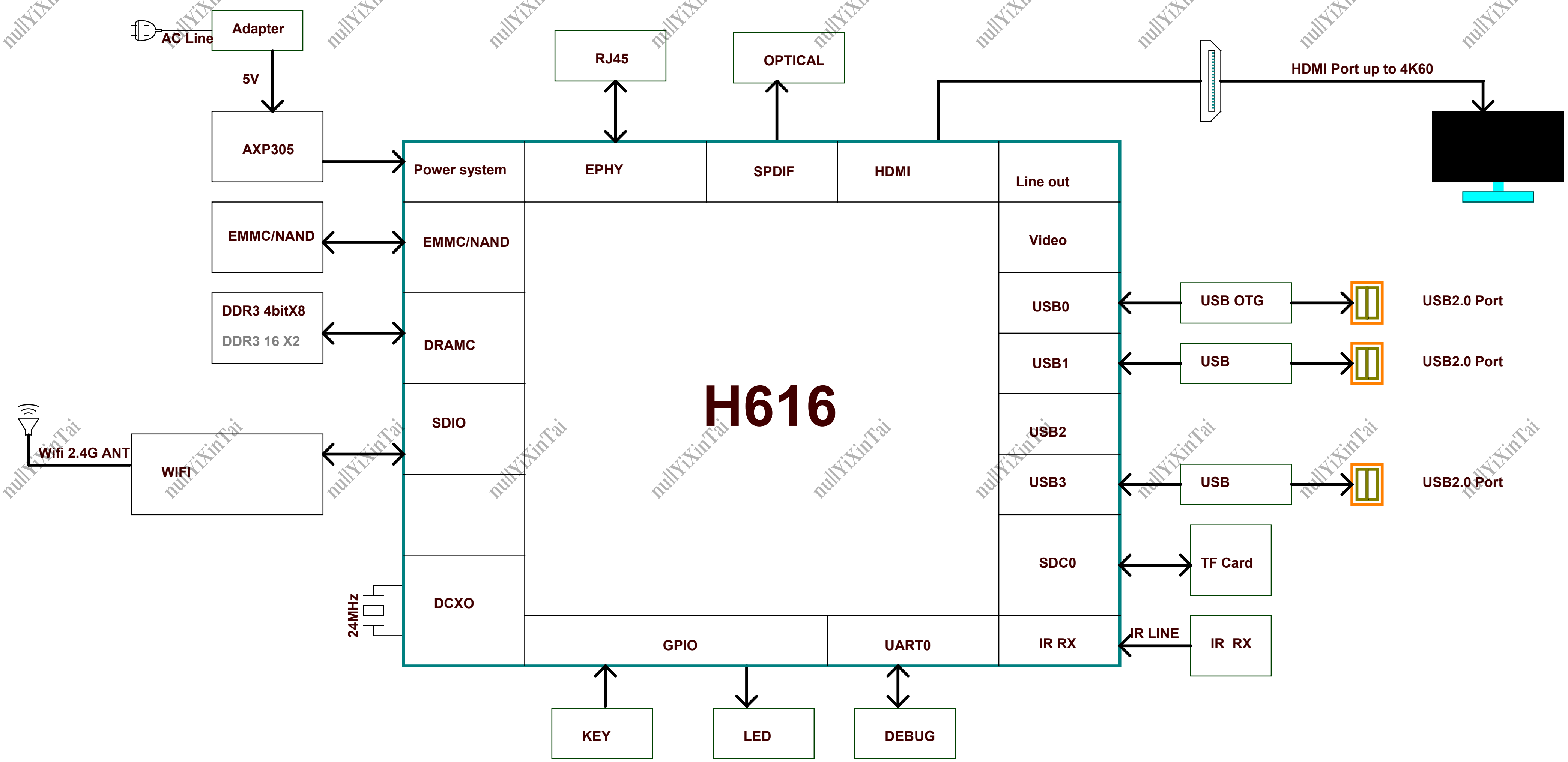
BLOCK



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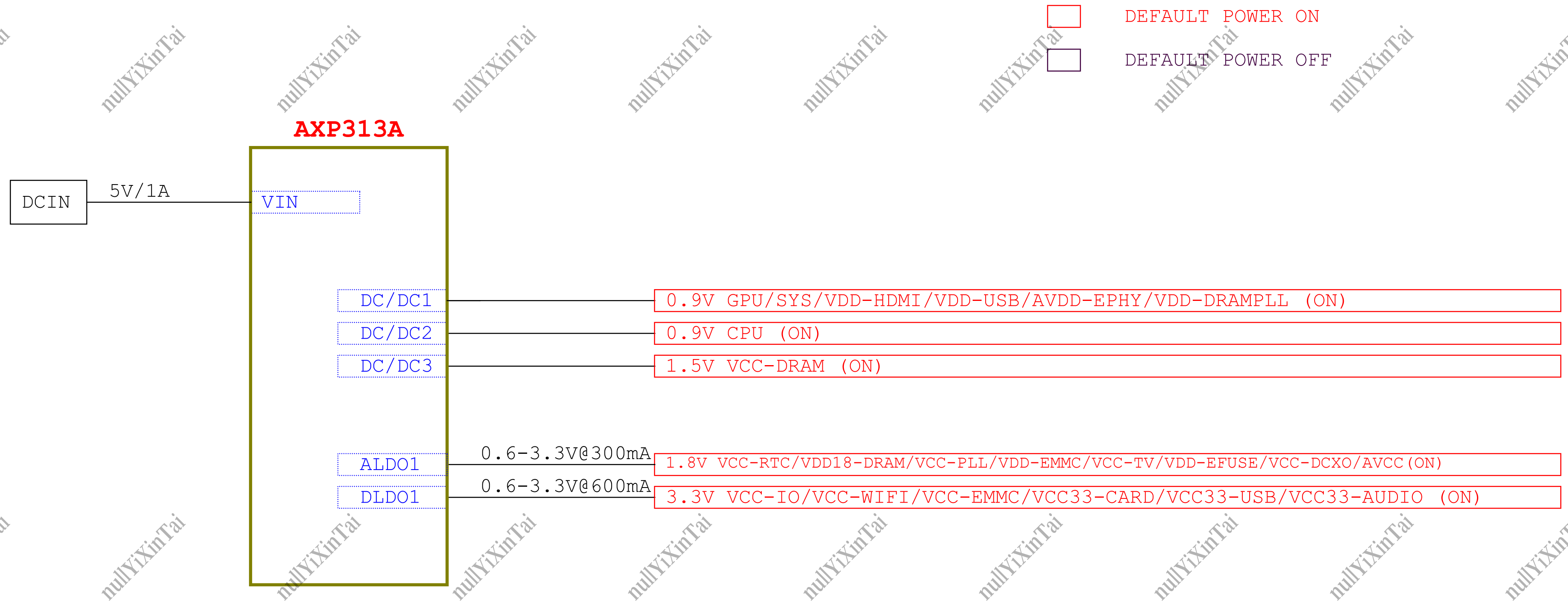
POWER TREE


DEFAULT POWER ON
DEFAULT POWER OFF
AXP313A
DCIN
5V/1A
VIN
DC/DC1
DC/DC2
DC/DC3
ALDO1
DLDO1
0.9V GPU/SYS/VDD-HDMI/VDD-USB/AVDD-EPHY/VDD-DRAMPLL (ON)
0.9V CPU (ON)
1.5V VCC-DRAM (ON)
0.6-3.3V@300mA
1.8V VCC-RTC/VDD18-DRAM/VCC-PLL/VDD-EMMC/VCC-TV/VDD-EFUSE/VCC-DCXO/AVCC(ON)
0.6-3.3V@600mA
3.3V VCC-IO/VCC-WIFI/VCC-EMMC/VCC33-CARD/VCC33-USB/VCC33-AUDIO (ON)

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GPIO ASSIGNMENT

PIN	Define	CFG	Function
PC0	NAND_WE/SDC2_DS	2/3	NAND/eMMC
PC1	NAND_ALE/SDC2_RST	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE1	2	
PC4	NAND_CE0	2	
PC5	NAND_RE/SDC2_CLK	2/3	
PC6	NAND_RB0/SDC2_CMD	2/3	
PC7	NAND_RB1	2	
PC8	NAND_DQ7/SDC2_D3	2/3	
PC9	NAND_DQ6/SDC2_D4	2/3	
PC10	NAND_DQ5/SDC2_D0	2/3	
PC11	NAND_DQ4/SDC2_D5	2/3	
PC12	NAND_DQS	2	
PC13	NAND_DQ3/SDC2_D1	2/3	
PC14	NAND_DQ2/SDC2_D6	2/3	
PC15	NAND_DQ1/SDC2_D2	2/3	
PC16	NAND_DQ0/SDC2_D7	2/3	

PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD0
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	WIFI+BT
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	
PG7	UART1_RX	2	
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	AP-CK32KO	3	
PG11	PCM2_SYNC	2	
PG12	PCM2_CLK	2	
PG13	PCM2_DOUT	2	
PG14	PCM2_DIN	2	
PG15	WL-WAKE-AP	0	
PG16	BT-WAKE-AP	0	
PG17	AP-WAKE-BT	1	
PG18	WL-REG-ON	1	
PG19	BT-REG-ON	1	

PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2	FD628-SCK	X	
PH3	FD628-SDA	X	
PH4	SPDIF-OUT	3	
PH5		1	
PH6	SYS-LED	1	
PH7		1	
PH8	USB0-DRVVBUS	1	
PH9	RECOVERY	0	
PH10	IR-RX	3	

X: Network port lights need to be configured

PIN	Define	CFG	Function
PI0			
PI1			
PI2			
PI3			
PI4			
PI5			
PI6			
PI7			
PI8			
PI9			
PI10			
PI11			
PI12			
PI13			
PI14			
PI15			
PI16			

PIN	Define	CFG	Function
PL0	PMU-SCK	2	
PL1	PMU-SDA	2	

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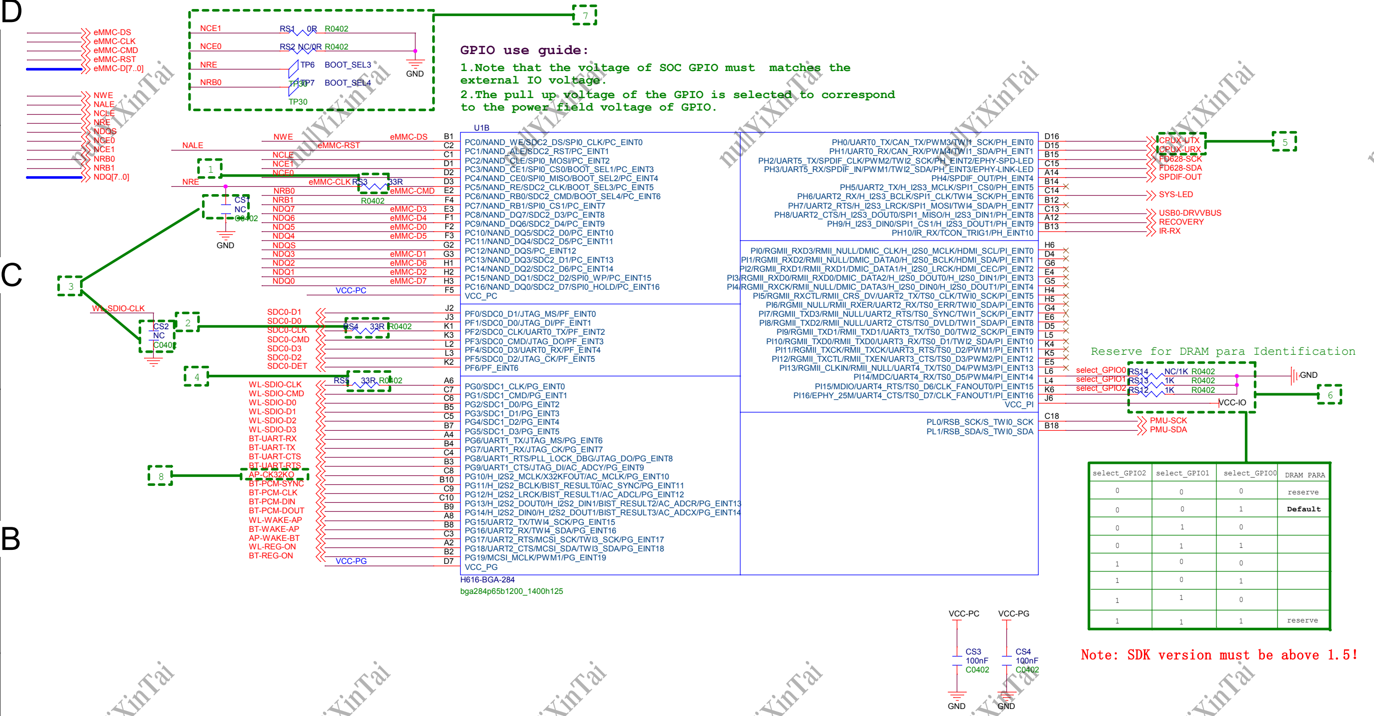
GPIO



eMMC-DS
eMMC-CLK
eMMC-CMD
eMMC-RST
eMMC-D[7..0]
NWE
NALE
NCLE
NRE
NDQS
NCE0
NCE1
NRB0
NRB1
NDQ[7..0]
NCE1
NCE0
NRE
NRB0
RS1 0R R0402
RS2 NC/0R R0402
TP6 BOOT_SEL3
TP7 BOOT_SEL4
TP30
GND
U1B
PC0/NAND_WE/SDC2_DS/SPI0_CLK/PC_EINT0
PC1/NAND_ALE/SDC2_RST/PC_EINT1
PC2/NAND_CLE/SPI0_MOSI/PC_EINT2
PC3/NAND_CE1/SPI0_CS0/BOOT_SEL1/PC_EINT3
PC4/NAND_CE0/SPI0_MISO/BOOT_SEL2/PC_EINT4
PC5/NAND_RE/SDC2_CLK/BOOT_SEL3/PC_EINT5
PC6/NAND_RB0/SDC2_CMD/BOOT_SEL4/PC_EINT6
PC7/NAND_RB1/SPI0_CS1/PC_EINT7
PC8/NAND_DQ7/SDC2_D3/PC_EINT8
PC9/NAND_DQ6/SDC2_D4/PC_EINT9
PC10/NAND_DQ5/SDC2_D0/PC_EINT10
PC11/NAND_DQ4/SDC2_D5/PC_EINT11
PC12/NAND_DQS/PC_EINT12
PC13/NAND_DQ3/SDC2_D1/PC_EINT13
PC14/NAND_DQ2/SDC2_D6/PC_EINT14
PC15/NAND_DQ1/SDC2_D2/SPI0_WP/PC_EINT15
PC16/NAND_DQ0/SDC2_D7/SPI0_HOLD/PC_EINT16
VCC_PC
PF0/SDC0_D1/JTAG_MS/PF_EINT0
PF1/SDC0_D0/JTAG_DI/PF_EINT1
PF2/SDC0_CLK/UART0_TX/PF_EINT2
PF3/SDC0_CMD/JTAG_DO/PF_EINT3
PF4/SDC0_D3/UART0_RX/PF_EINT4
PF5/SDC0_D2/JTAG_CK/PF_EINT5
PF6/PF_EINT6
PG0/SDC1_CLK/PG_EINT0
PG1/SDC1_CMD/PG_EINT1
PG2/SDC1_D0/PG_EINT2
PG3/SDC1_D1/PG_EINT3
PG4/SDC1_D2/PG_EINT4
PG5/SDC1_D3/PG_EINT5
PG6/UART1_TX/JTAG_MS/PG_EINT6
PG7/UART1_RX/JTAG_CK/PG_EINT7
PG8/UART1_RTS/PLL_LOCK_DBG/JTAG_DO/PG_EINT8
PG9/UART1_CTS/JTAG_DI/AC_ADCY/PG_EINT9
PG10/H_I2S2_MCLK/X32KFOUT/AC_MCLK/PG_EINT10
PG11/H_I2S2_BCLK/BIST_RESULT0/AC_SYNC/PG_EINT11
PG12/H_I2S2_LRCK/BIST_RESULT1/AC_ADCL/PG_EINT12
PG13/H_I2S2_DOUT0/H_I2S2_DIN1/BIST_RESULT2/AC_ADCR/PG_EINT13
PG14/H_I2S2_DIN0/H_I2S2_DOUT1/BIST_RESULT3/AC_ADCX/PG_EINT14
PG15/UART2_TX/TWI4_SCK/PG_EINT15
PG16/UART2_RX/TWI4_SDA/PG_EINT16
PG17/UART2_RTS/MCSI_SCK/TWI3_SCK/PG_EINT17
PG18/UART2_CTS/MCSI_SDA/TWI3_SDA/PG_EINT18
PG19/MCSI_MCLK/PWM1/PG_EINT19
VCC_PG
PH0/UART0_TX/CAN_TX/PWM3/TWI1_SCK/PH_EINT0
PH1/UART0_RX/CAN_RX/PWM4/TWI1_SDA/PH_EINT1
PH2/UART5_TX/SPDIF_CLK/PWM2/TWI2_SCK/PH_EINT2/EPHY-SPD-LED
PH3/UART5_RX/SPDIF_IN/PWM1/TWI2_SDA/PH_EINT3/EPHY-LINK-LED
PH4/SPDIF_OUT/PH_EINT4
PH5/UART2_TX/H_I2S3_MCLK/SPI1_CS0/PH_EINT5
PH6/UART2_RX/H_I2S3_BCLK/SPI1_CLK/TWI4_SCK/PH_EINT6
PH7/UART2_RTS/H_I2S3_LRCK/SPI1_MOSI/TWI4_SDA/PH_EINT7
PH8/UART2_CTS/H_I2S3_DOUT0/SPI1_MISO/H_I2S3_DIN1/PH_EINT8
PH9/H_I2S3_DIN0/SPI1_CS1/H_I2S3_DOUT1/PH_EINT9
PH10/IR_RX/TCON_TRIG1/PH_EINT10
PI0/RGMII_RXD3/RMII_NULL/DMIC_CLK/H_I2S0_MCLK/HDMI_SCL/PI_EINT0
PI1/RGMII_RXD2/RMII_NULL/DMIC_DATA0/H_I2S0_BCLK/HDMI_SDA/PI_EINT1
PI2/RGMII_RXD1/RMII_RXD1/DMIC_DATA1/H_I2S0_LRCK/HDMI_CEC/PI_EINT2
PI3/RGMII_RXD0/RMII_RXD0/DMIC_DATA2/H_I2S0_DOUT0/H_I2S0_DIN1/PI_EINT3
PI4/RGMII_RXCK/RMII_NULL/DMIC_DATA3/H_I2S0_DIN0/H_I2S0_DOUT1/PI_EINT4
PI5/RGMII_RXCTL/RMII_CRS_DV/UART2_TX/TS0_CLK/TWI0_SCK/PI_EINT5
PI6/RGMII_NULL/RMII_RXER/UART2_RX/TS0_ERR/TWI0_SDA/PI_EINT6
PI7/RGMII_TXD3/RMII_NULL/UART2_RTS/TS0_SYNC/TWI1_SCK/PI_EINT7
PI8/RGMII_TXD2/RMII_NULL/UART2_CTS/TS0_DVLD/TWI1_SDA/PI_EINT8
PI9/RGMII_TXD1/RMII_TXD1/UART3_TX/TS0_D0/TWI2_SCK/PI_EINT9
PI10/RGMII_TXD0/RMII_TXD0/UART3_RX/TS0_D1/TWI2_SDA/PI_EINT10
PI11/RGMII_TXCK/RMII_TXCK/UART3_RTS/TS0_D2/PWM1/PI_EINT11
PI12/RGMII_TXCTL/RMII_TXEN/UART3_CTS/TS0_D3/PWM2/PI_EINT12
PI13/RGMII_CLKIN/RMII_NULL/UART4_TX/TS0_D4/PWM3/PI_EINT13
PI14/MDC/UART4_RX/TS0_D5/PWM4/PI_EINT14
PI15/MDIO/UART4_RTS/TS0_D6/CLK_FANOUT0/PI_EINT15
PI16/EPHY_25M/UART4_CTS/TS0_D7/CLK_FANOUT1/PI_EINT16
VCC_PI
PL0/RSB_SCK/S_TWI0_SCK
PL1/RSB_SDA/S_TWI0_SDA
H616-BGA-284
bga284p65b1200_1400h125
CPUX-UTX
CPUX-URX
FD628-SCK
FD628-SDA
SPDIF-OUT
SYS-LED
USB0-DRVVBUS
RECOVERY
IR-RX
Reserve for DRAM para Identification
select_GPIO0
select_GPIO1
select_GPIO2
RS14 NC/1K R0402
RS13 1K R0402
RS12 1K R0402
VCC-IO
GND
PMU-SCK
PMU-SDA
CS1 NC C0402
CS2 NC C0402
RS3 33R R0402
RS4 33R R0402
RS5 33R R0402
eMMC-CMD
WL-SDIO-CLK
SDC0-D1
SDC0-D0
SDC0-CLK
SDC0-CMD
SDC0-D3
SDC0-D2
SDC0-DET
WL-SDIO-CMD
WL-SDIO-D0
WL-SDIO-D1
WL-SDIO-D2
WL-SDIO-D3
BT-UART-RX
BT-UART-TX
BT-UART-CTS
BT-UART-RTS
AP-CK32KO
BT-PCM-SYNC
BT-PCM-CLK
BT-PCM-DIN
BT-PCM-DOUT
WL-WAKE-AP
BT-WAKE-AP
AP-WAKE-BT
WL-REG-ON
BT-REG-ON
VCC-PC
VCC-PG
CS3 100nF C0402
CS4 100nF C0402
1
2
3
4
5
6
7
8

GPIO use guide:

1.Note that the voltage of SOC GPIO must matches the external IO voltage.

2.The pull up voltage of the GPIO is selected to correspond to the power field voltage of GPIO.

Reserve for DRAM para Identification

select_GPIO2	select_GPIO1	select_GPIO0	DRAM PARA
0	0	0	reserve
0	0	1	**Default**
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	reserve

Note: SDK version must be above 1.5!

SOC and peripheral circuit considerations-1

1.RS3 is the termination resistor at the source end of EMMC-CLK, which cannot be deleted.

2.RS4 is the termination resistor of SDC0-CLK source end, which cannot be deleted.

3.CS1 and CS2 are reserved for EMI suppression and need to be placed close to the Device.

4.RS5 is the termination resistor of SDIO-CLK source end, which cannot be deleted.

5.The default function of PH0 and PH1 is the UART print port, which is used for system software debugging and cannot be changed.

6.The DRAM para version identification reserved circuit cannot be deleted. For the purpose of software normalization management, the same firmware is compatible with multiple DRAM templates and DRAM materials. The way to read the hardware GPIO level in the boot phase, the software automatically calls the corresponding DRAM para. Pay special attention to the one-to-one correspondence between BOM and DRAM para.

7.boot sel: BROM will read the state of BOOT_Select, choose the external storage medium to boot, and speed up the boot time.
H616 has 4 boot sel pins multiplexed with the PC port, the configuration relationship is as follows:

bit[10]	bit[11]	bit[12]	bit[13]	Media	
1	1	1	1	MLC/SLC NAND	
0	1	1	1	eMMC USER	Default
1	0	1	1	eMMC BOOT	
1	1	0	1	SPI NOR	
1	1	1	0	SPI NAND	

The multiplexing relationship between 4 boot sel and PC port is as follows:
Bit[10]->PC3
Bit[11]->PC4
Bit[12]->PC5
Bit[13]->PC6

8.32K clock fanout, output low frequency clock, can be used by external wifi module, needs to surrounded by GND.

GPIO power domain list:

GROUP	Power Field	Voltage(V)
PC	VCC-PC	1.8/3.3
PF	VCC-PLL/VCC-IO	1.8/3.3
PG	VCC-PG	1.8/3.3
PH	VCC-IO	3.3
PI	VCC-PI	1.8/3.3
PL	VCC-PLL	1.8

Note: 1. When GPIO is not used, it can be directly floated, and the software is set to Disable.
2. After changing the default voltage of the multi-voltage IO power supply, the corresponding configuration changes must be confirmed on the software.

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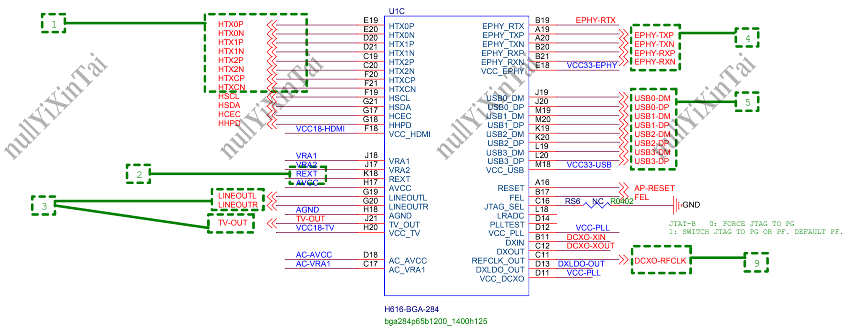
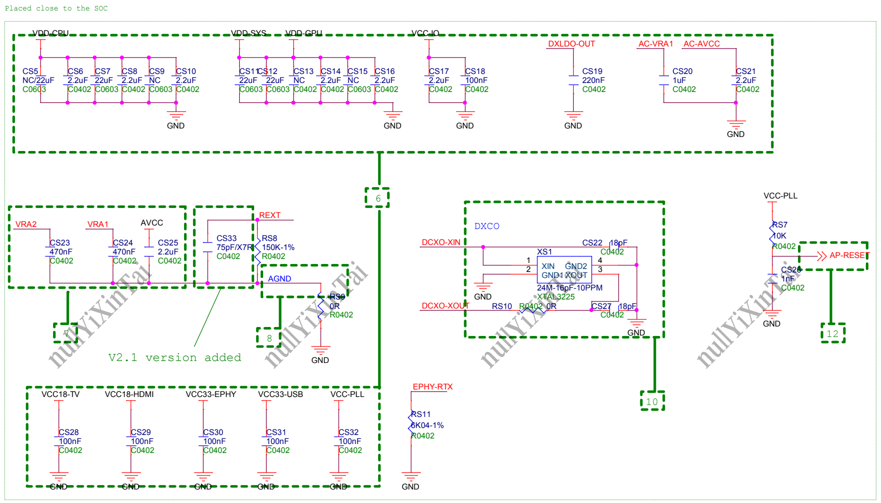
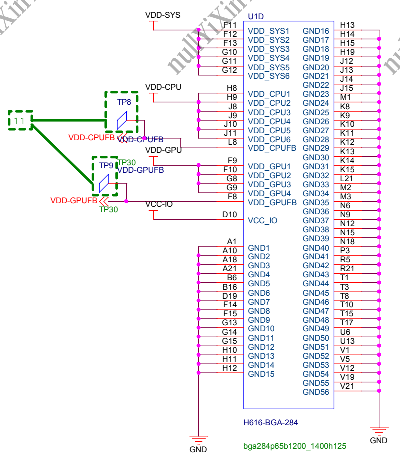
SOC and peripheral circuit considerations-2







1. The HDMI differential signal controls the differential impedance of 100ohm.

2. REXT is a sensitive signal, and the layout path is kept to the shortest.

3. Lineout, TVOUT individually ground; TVOUT trace control impedance 37.5ohm.

4. ePHY differential signal control differential impedance 100ohm.

5. USB differential signal control differential impedance 90ohm.

6. The decoupling capacitance of each module has been optimized by PI and cannot be modified.

7. The bypass capacitor of CODEC cannot be modified. These parameters will affect the internal power-on sequence.

8. The AGND trace should be as wide as possible, at least 12mil or more, and the copper skin should be widened after the BGA is released; the number of R99 GND vias should be guaranteed at least two.

9. 24Mfanout clock, can be used for wifi module, and the wiring needs to be isolated with ground.

10. The crystal matching capacitor is the reference value, the actual capacitance value can be modified according to the test; in addition, the series resistance needs to be reserved to facilitate debugging the oscillation amplitude.

11. The voltage feedback test point should be placed near the projection area of the back of the power pin.

12. The system reset signal AP-reset is far away from the board edge and interference signals.

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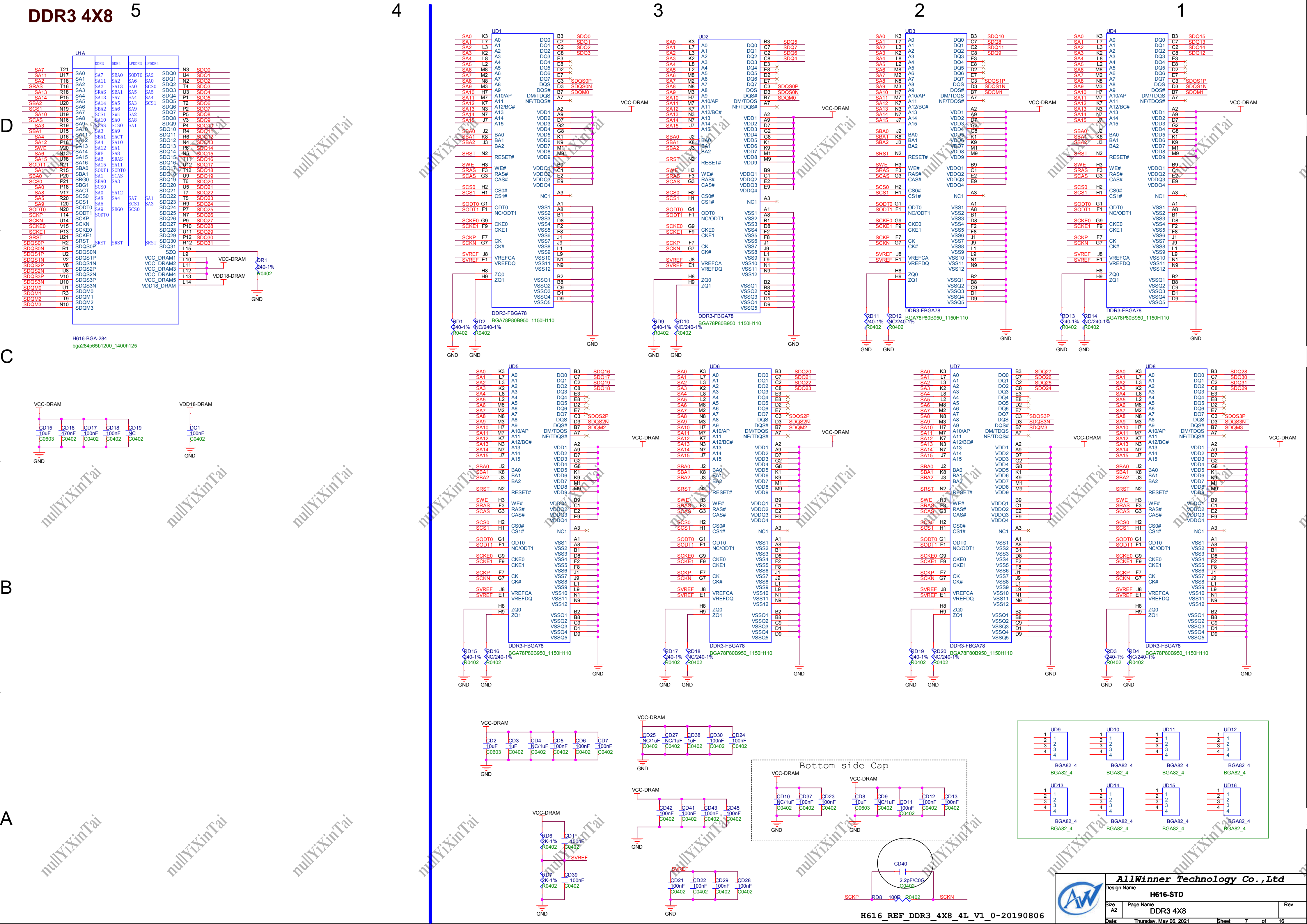
DDR3 4X8



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H616_REF_DDR3_4X8_4L_V1_0-20190806

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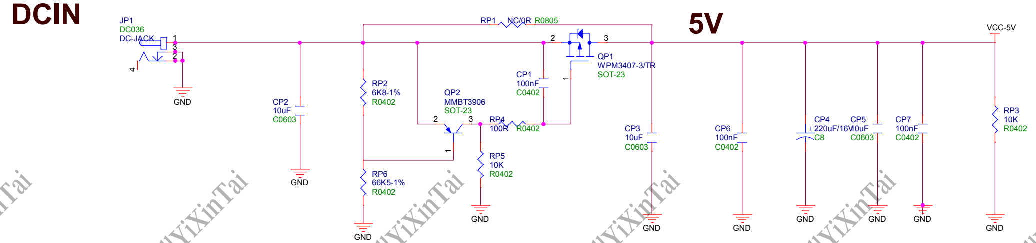
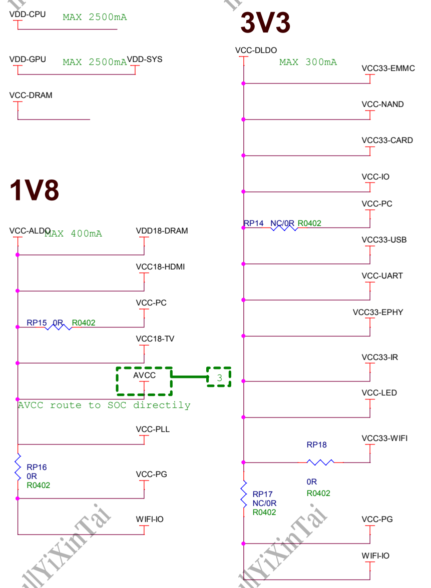
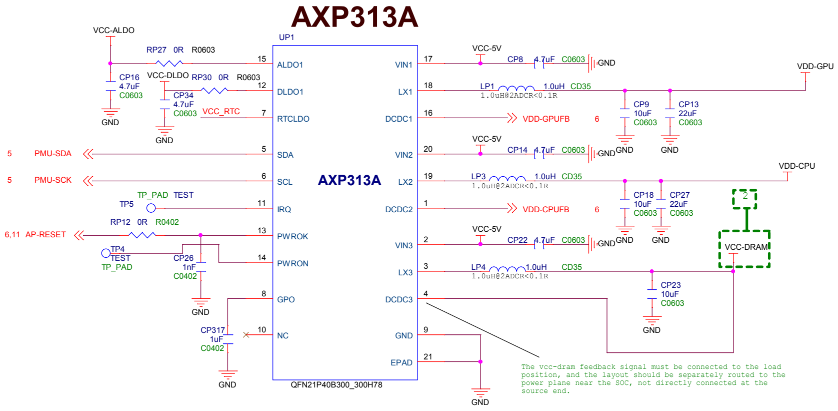
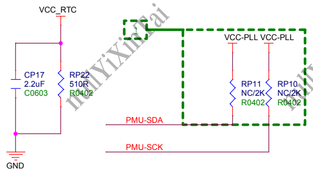
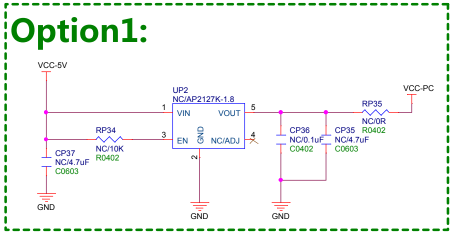


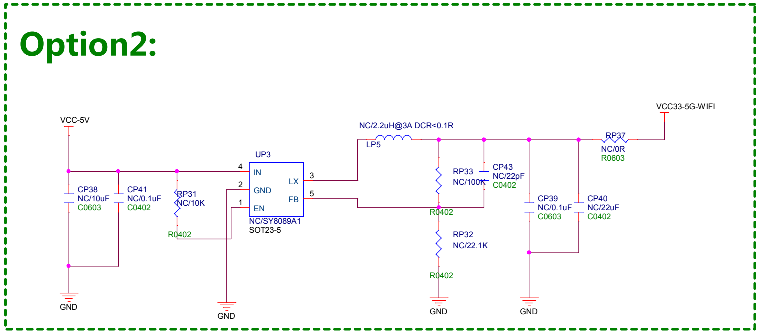








Reserve for EMMC which 1.8V current greater than 300mA.



Reserved for 5g WiFi power supply.

Power design considerations

1. AXP313A is controlled by the I2C signal of the PL port, and the external needs to be reserved for pull-up to VCC-PLL.

2. VCC-DRAM can support DDR3, DDR4, LPDDR3, LPDDR4 different DRAM power supply, different DRAM types through software
The identification is automatically matched to the appropriate supply voltage.

3. AVCC supplies power for analog modules such as Audio codec, T-senor, etc. The accuracy must be +/- 1%, and the minimum power supply voltage cannot be lower than 1.78V.
Otherwise, it will affect Audio performance and sensor accuracy.

Important:

The stability of the power supply directly affects the stability of the system. Please be sure to refer to the relevant guide in the "Hardware Design Guide" for the schematic diagram and PCB design!

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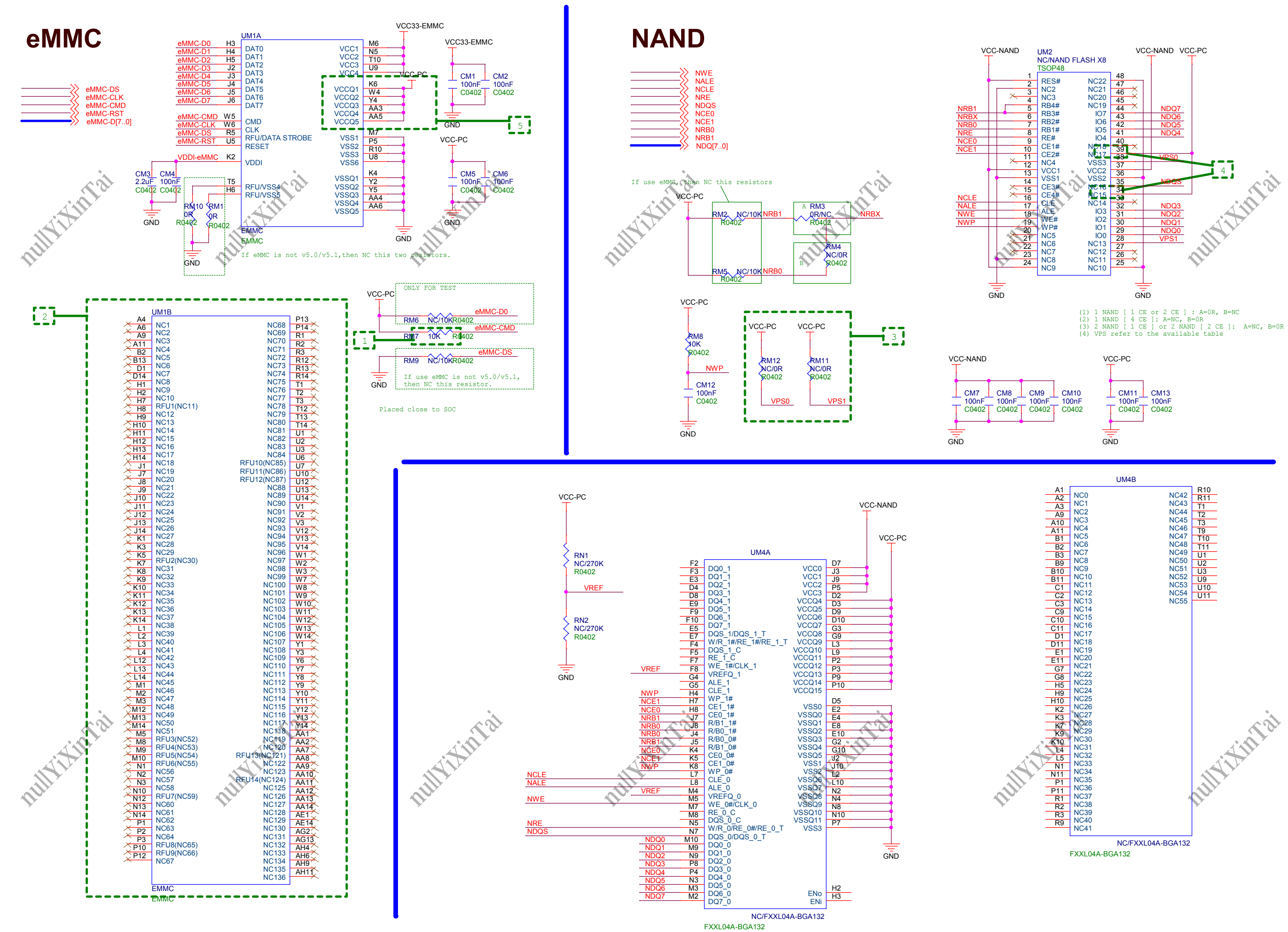

If eMMC is not v5.0/v5.1,then NC this two resistors.

ONLY FOR TEST

If use eMMC is not v5.0/v5.1, then NC this resistor.

Placed close to SOC

If use eMMC, then NC this resistors

(1) 1 NAND [1 CE or 2 CE] : A=0R, B=NC
(2) 1 NAND [4 CE]: A=NC, B=0R
(3) 2 NAND [1 CE] or 2 NAND [2 CE]: A=NC, B=0R
(4) VPS refer to the available table

Flash design considerations

1. CMD needs to be pulled up to VCC-PC.

2. The reserved pins, such as eMMCNC / RFU, are left unconnected. Do not connect these signals with power, ground, or other eMMC signals for easy fanout.

3. If you use Sandisk or Toshiba's nandflash, you need to pull up VPS0 and VPS1, and the other is left floating by default.

4. Some nand have 1.8V power supply, these two pins need to be connected to VCC-PC.

5. The EMMC IO power supply voltage matches the power domain voltage of the SOC GPIO.

Important:

For the PCB design of the Flash module, please refer to the layout guide in the Hardware Design Guide,
The guide has detailed impedance, timing and crosstalk requirements;
Note that when EMMC and NAND are dual-layout, a daisy-chain topology is used, and EMMC is used as a routing terminal.

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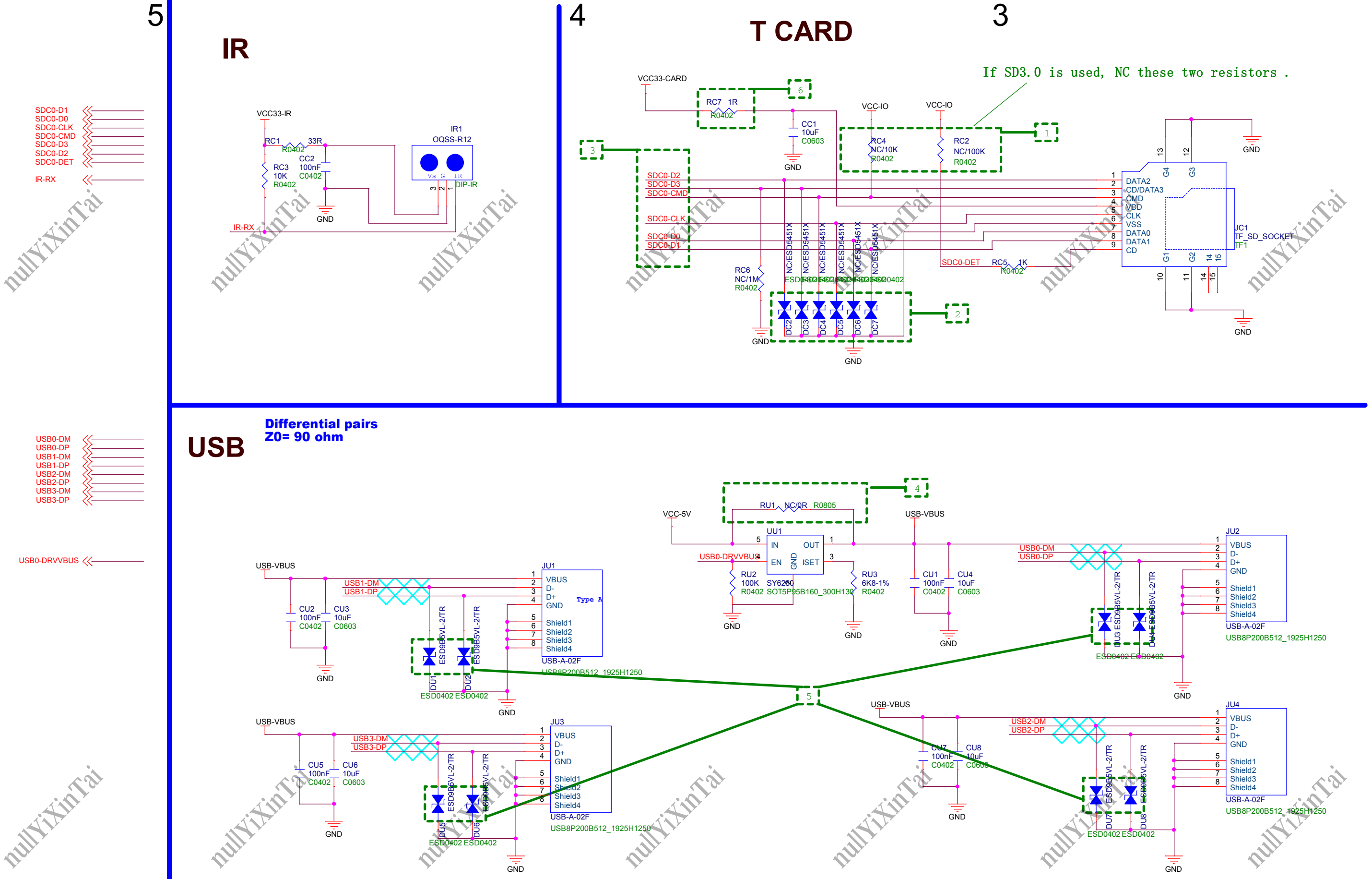

Peripheral interface considerations-1

1.card IO supports internal 1.8V / 3.3V automatic switching, the default is 3.3V, SDC0_CMD and SDC0_DET signals have weak pull-ups internally,
External pull-ups need to be reserved to prevent insufficient internal pull-ups.

2. The parasitic capacitance of the ESD device cannot be greater than 10pF, otherwise it will affect the signal quality.

3. Please refer to the relevant guide of "Hardware Design Guide" for the design of SDIO signal layout. The guide has detailed impedance, timing and crosstalk requirements.

4. Reserve 0R resistor for easy debugging.

5. USB2.0 interface signal lines USB0-DM, USB0-DP, USB1-DM, USB1-DP, USB3-DM, USB3-DP are high-speed signal lines, and connected ESD devices
Low capacitance value is required, otherwise it will affect data transmission, it is better to be less than or equal to 4pF. The USB differential signal controls the differential impedance of 90ohm and is isolated around the ground.

6.Connect a 1 ohm resistor in series to prevent the card from causing the power to drop instantly.

Important:

For ESD device layout related specifications, please refer to the relevant guides in the "Hardware Design Guide" for detailed instructions.

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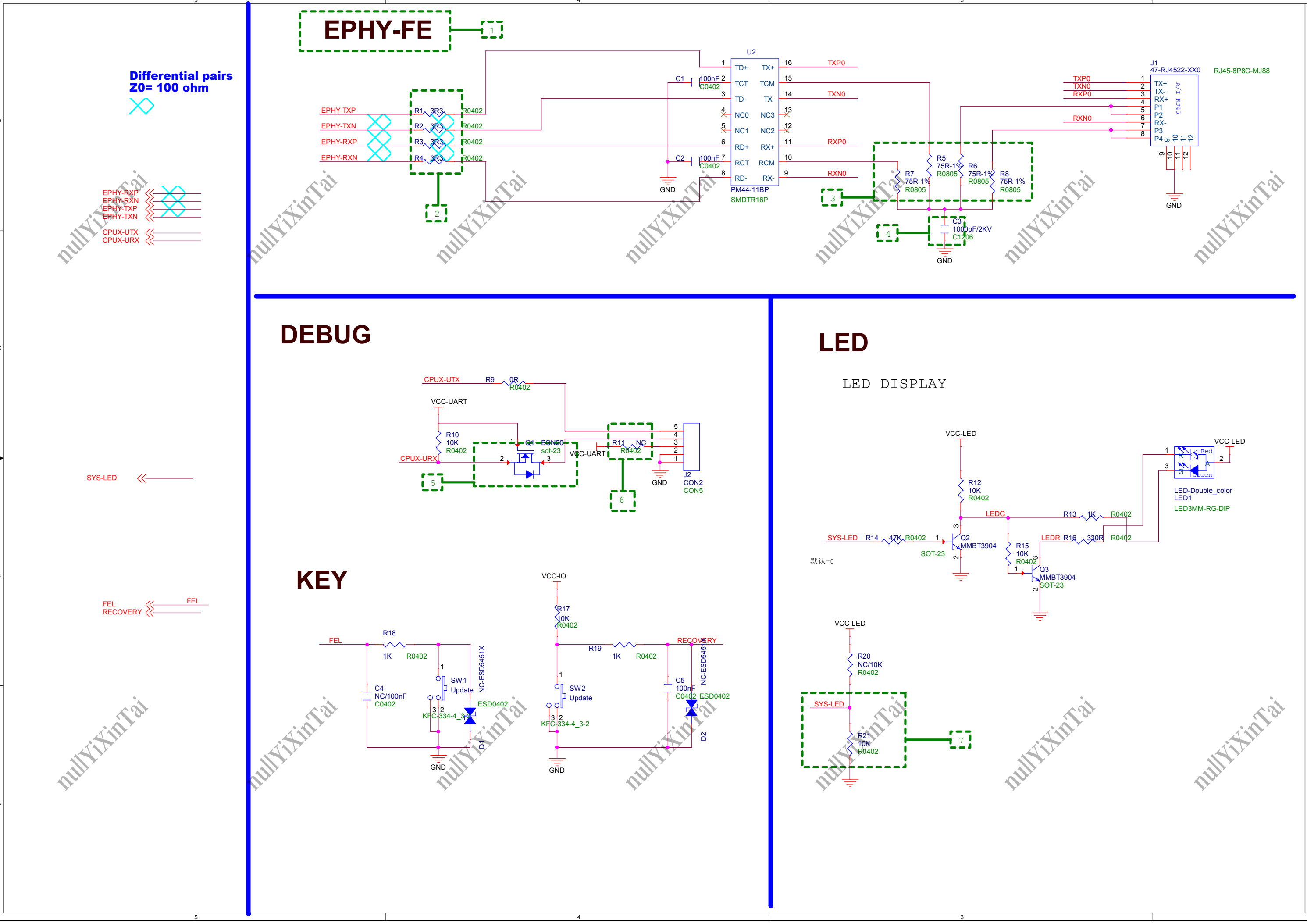

Peripheral interface considerations-2

1. H616 internally integrates 100M EPHY, if you need to use 1000M GPHY, you need to use PI port RGMII interface and external PHY chip.

2. The resistance of the serial resistor on the Ethernet differential line should not be too large. It is recommended to reserve 0 ohms to help improve the lightning test.

3. The four 75 ohm resistors of the interface are packaged in 0805, because the small package will be burned when struck by lightning.

4. The high voltage capacitor package cannot be less than 1206, and the withstand voltage of the high voltage capacitor cannot be less than 2KV.

5. CPUX-RX needs to add MOS tube for anti-backflow design, it needs to be added in the early debugging, and can be deleted in the later mass production.

6. R11 depends on the actual serial port used for debugging, and the default is NC.

7. The SYS-LED power-on default is low, add a pull-down resistor to stabilize the level.

Important:

For the differential signals of the network port and the layout of the high-voltage part, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.

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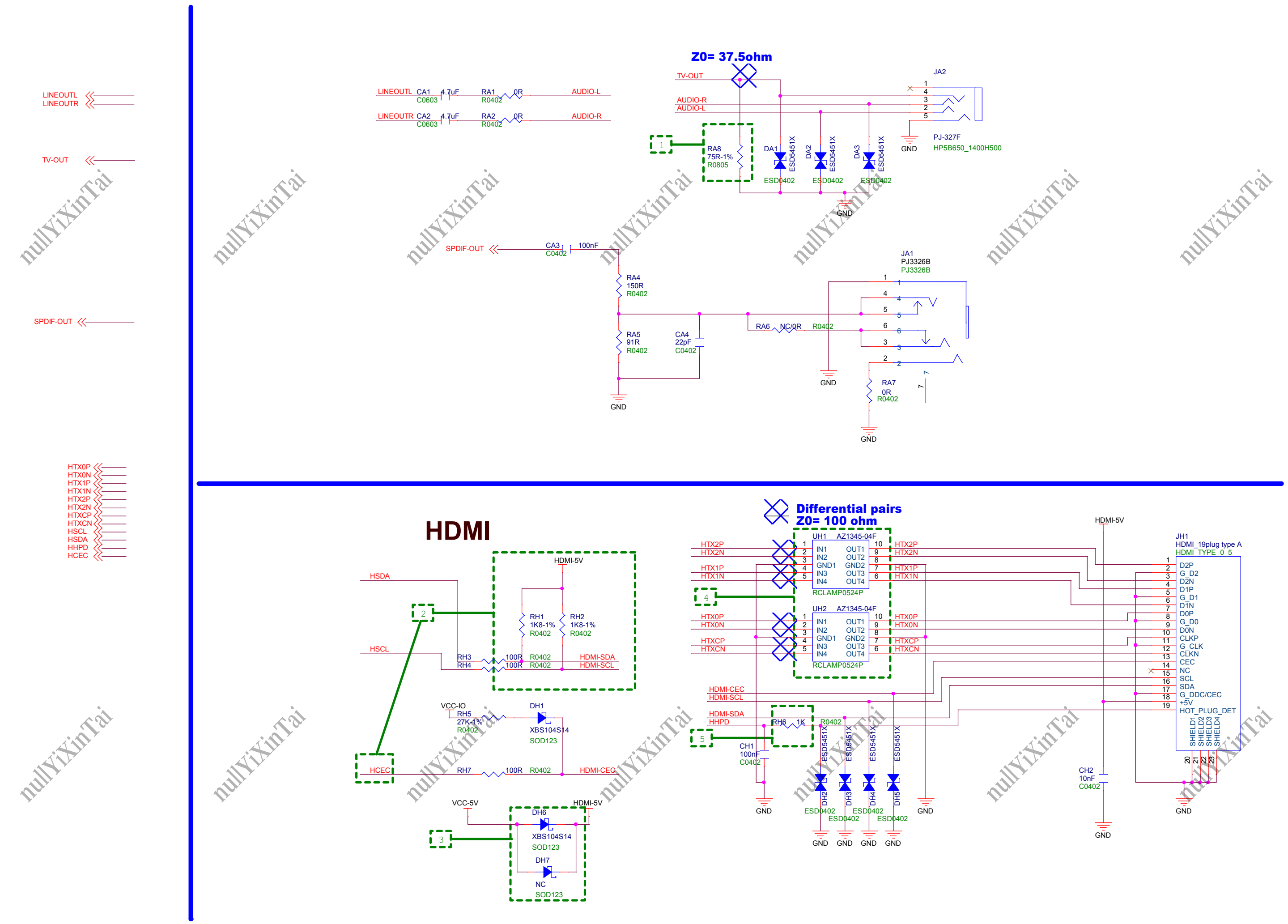

Audio&HDMI Interface considerations

1. The 75 ohm resistor of the CVBS port needs to use the 0805 package, because the CVBS output current type, the current will flow through the resistor, if the resistor package is too small ,The resistor will be burned by heat.

2. H616 HDMI IIC and CEC have built-in levelshift circuit, which supports direct connection to device.

3. The 5V power supply of HDMI must be connected in series with Schottky diodes to prevent leakage of the TV after shutdown. The voltage drop of ordinary diodes is high, which is easy to cause HDMI power supply is lower than 4.75v, to avoid compatibility problems, please choose a Schottky diode with reduced on-voltage.

4. The dynamic resistance (Rdyn) of the ESD device used on the HDMI differential line is less than 0.35 ohms, the operating voltage is 5v, and the parasitic capacitance is less than 0.35pF, It is recommended to use AZ1345-04F.

5. HPD has a built-in levelshift circuit in H616, which can withstand 5V, so it can be directly connected in series with no voltage division.

Important:

For audio and HDMI differential layout, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.

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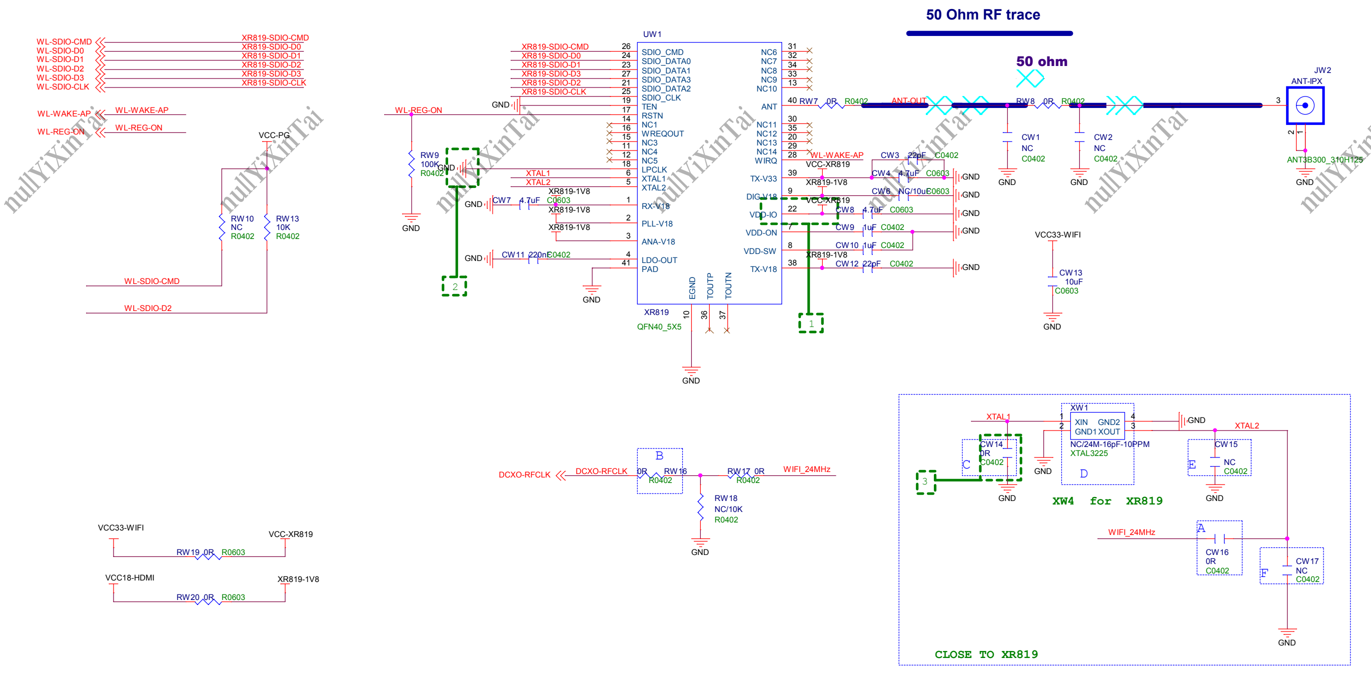
XR819



XR819 24M Crystal source	A	B	C	D	E	F
XW1	NC	NC	20pF	24M-16pF-10PPM	20pF	NC
DCXO-RFCLK	0R	0R	0R	NC	NC	NC

WIFI module design considerations

1. The IO power supply of WIFI is consistent with the power supply of the PG port of the SOC . Ensure that the levels of the SOC and peripherals match.

2. The 32.768K clock is provided inside XR819, and the pin is grounded.

3. When 24M Fanout is selected for crystal source, pay attention to XTAL1 grounding.

Important:

For SDIO and RF antenna layout, please refer to the relevant layout guide in the Hardware Design Guide for detailed instructions.

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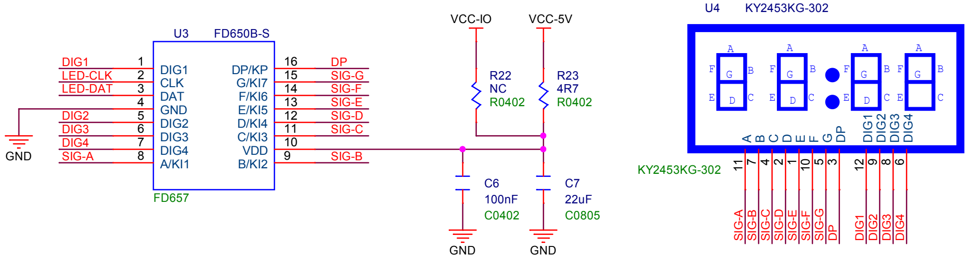

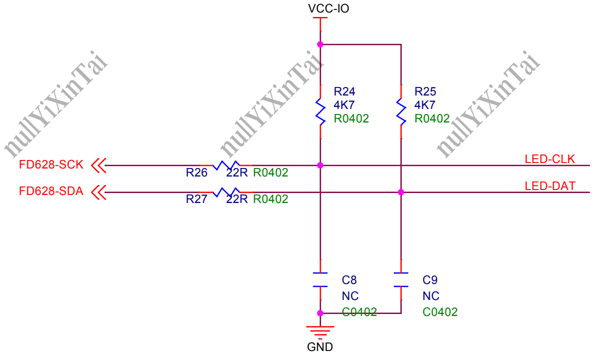

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