Lab 1: BCD-to-7segment decoder

Goals

- The objective of this lab is to implement a 7segment decoder that can also have a BCD input from a binary value to display the number in human readable base 10 format.
- The goal is that the student is familiarized with decoders and how they can be useful in hardware.

Introduction

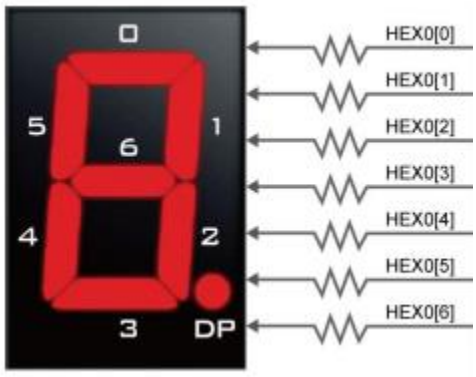
A decoder is a circuit that detects a specified combination of bits in the input and then generates a defined output based on different algorithms or conditions. The basic binary decoder is implemented in a way that a certain pattern or binary input is identified and then a low or high output is set to specify we are in that binary value or state.

Lab description

Design and implement a BCD-to-7segment decoder via gates and the provided double-dabble algorithm code.

Step 1.

The DE2-115 7 segment displays are common anode, this means that the corresponding connected line must be set to 0 in order for the display to light up that segment.



The board has HEX0 through HEX7, that means we have 7 7-segment displays we can utilize. The first step is to design a circuit that decodes a 4-bit input to a 7-bit output that satisfies the conditions for the right segments to be light up when the number is selected given this truth table:

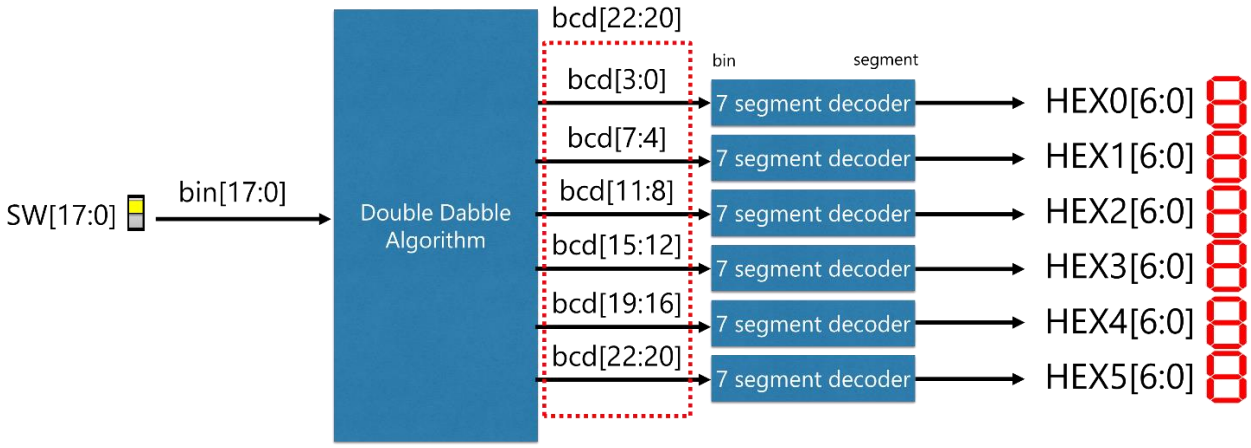
INPUTS				OUTPUTS							NUM
A3	A2	A1	A0	HEX[0](a)	HEX[1](b)	HEX[2](c)	HEX[3](d)	HEX[4](e)	HEX[5](f)	HEX[6](g)	
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0	0	0	1	0	0	1	0	
0	0	1	1	0	0	0	0	1	1	0	
0	1	0	0	1	0	0	1	1	0	0	
0	1	0	1	0	1	0	0	1	0	0	
0	1	1	0	0	1	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	1	0	0	

Step 2.

Connect the 4-bit input to the 4-bit output of the double dabble algorithm that can split any number from 0 to 9,999,999, and use the 18 slide switches to represent any number from 0 to 262,143 as the input of the double dabble algorithm.

Step 3.

The circuit should look a bit like this:



Step 4.

Implement the circuit on the FPGA.

- Use the following **switches** for input **bin**: **SW[17] to SW[0]**
- Use the following **7 segment displays** for outputs: **HEX7 to HEX0**

Submission

Implementation description

Generate a document providing a detailed description of the implementation. This should include an explanation of design decisions, challenges encountered, and how they were overcome. Include diagrams, schematics, tables, or equations used in the design development.

Video:

Upload a short video to the Teams group, recording the operation of the implemented circuit on the FPGA and providing a brief description of its functionality.