CPE 223 Computer Architectures 3 (2-2-6)

Second Semester 2023, RC Computer Engineering Students

Computer Engineering Department, KMUTT

Instructor Information		**Class Times**
Instructors:	Asst.Prof. Sanan Srakaew	Wed 8:30 – 12:30
E-mails:	sanan.sra@kmutt.ac.th	**Office Hours:** Wed 13.30 – 16.30, or with an appointment.
Website:	https://www.leb2.kmutt.ac.th/	
Telephone:	02-470-9083	
TAs	TBA	

Course Objectives

The key objective of this course is to provide students hands-on experiences in electrical circuits and electronics, analysis, design, and implementation. A project-based approach will be exploited.

The Computer Engineering Department has a new mission to use innovative hands-on, active learning techniques to develop 5 distinct student characteristics:

1) Self-Learner
   - prepare readings before class for group discussion/quiz
   - self-study for doing projects

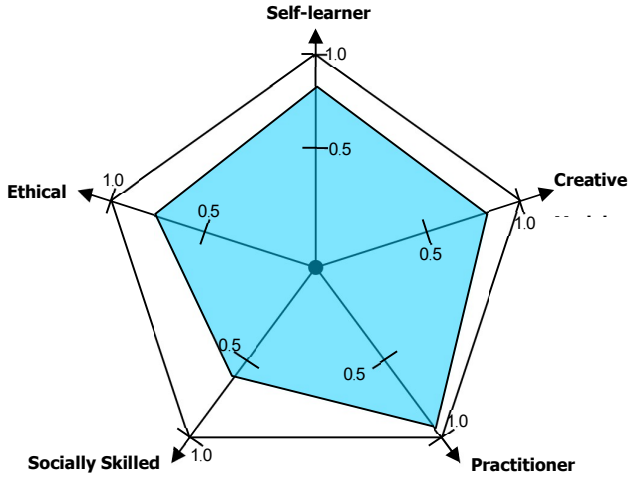
2) Creative Designer/Modeler
   - create models for projects and assignments of real-life problems

3) Practitioner
   - projects and assignments with real-life type problems.

4) Socially Apt
   - working in teams of 5 on projects
   - participating in group discussion

5) Ethical
   - focus on the importance of ethics and individual integrity

The shaded area in the graph is the goal of this course to develop you in each dimension. **Ethics** is a key characteristic we would like all our students to possess.



Five Desired Characteristics of CPE Students

Ethics means that any work you submit for credit is to be your work. For homework assignments and projects, general discussion with your classmates regarding the requirements or the approach to be taken is permitted.

Homework assignments and/or reports are due prior to the class time. Your submitted assignments/reports must be yours. **Class attendance** is very important. Showing up late causes 10% deducted in in-class exercises. **Cell-phones** must be **turned off** before you come to class and not allowed to use during class time. They are disruptive and annoying. If we hear a cell-phone ringing during a quiz, I will assume you are cheating. **Laptop** usage is for assigned classwork. **Facebook, Messenger, Line** and **game playing** are prohibited. If we see you playing game or using Facebook, Messenger, Line you will be asked to leave the room.

Course Description
Processor technology, input and output, memory hierarchy, interleaved memory, bus, cache, pipelined architectures, and computer arithmetic. Machine instructions, assembly language programming, microprocessor design and physical control. Communication and control of heterogeneous processors (on-chip, PCI, USB, SPI, CAN, RS-232/422, I2C, one-wire), communication and control of homogeneous processors (multi-core, cluster, GPU), introduction to specialized processors (vector, DSP). Experiments on microcomputer, microprocessor and microcontroller interfacing with physical devices.

Course Learning Outcomes
1. Understand the concept of computer architecture.
2. Able to design and evaluate a simple processor on emulator.
3. Able to write technical reports and give presentations.
4. Able to work as a team to build a practical project.

Required Texts
Computer Organization and Design: The Hardware/Software Interface 5th Ed., Patterson and Hennessy, Morgan Kaufmann, 2014, ISBN 978-0-12-407726-3.

Grading Policy
Final grades are based on performance indicated by student in-class exercises, lab reports, homework assignments, quiz, projects, and final exam. The final grade will be calculated according to the following weights:

Quiz and Final Exam:	50%
Homework assignments, in-class exercises, labs, and projects:	50%

CPE 223 Schedule (tentative)

Week#	Lectures	In-class/Labs topics
1 (Jan 17)	Introduction & History of computers On-line Zoom: 4976849195	IA-32 and IA-64 ISA review
2 (Jan 24)	Computer arithmetic, data representation, floating point arithmetic On-line Zoom: 4976849195	Floating-point representation exercise
3 (Jan 31)	Instruction Set Architecture and MIPS	Lab 1: Introduction to MIPS coding
4 (Feb 7)	MIPS instruction set	Lab 2: MIPS Assembly language
5 (Feb 14)	Datapath and control	Lab 3: MIPS Procedure calls
Feb 21	Quiz#1 (8:30-10:30, 22 Feb 2023)	
6 (Feb 28)	Datapath and control (Continued)	Mini-project proposal: Non-pipelined processor simulation
7 (Mar 6)	Control unit: Hardwired and microcoded	Mini-project presentation
8 (Mar 13)	Pipelining	Pipelining exercise
9 (Mar 20)	Pipeline control and hazards	Lab 4: MIPS data segment and arrays
10 (Mar 27)	Memory hierarchy: Caching schemes	Memory hierarchy exercise Final project proposal submitted
Mar 28 – Apr 5	Quiz#2 (8.30-10.30, 3 Apr 2024	
Apr 6 - 16	Class break	
11 (Apr 17)	Cache coherence, virtual memory	Lab 5: Modular programming in MIPS
12 (Apr 24)	Storage and I/O Systems	Storage and I/O system exercise
13 (May 1)	Parallel processing and cloud	
14 (May 8)	Project Presentation	
15 (May 15)	Reading Week	
May 20-30	Final period, Final (8:30-12:30, Wed 22 May 2023)	