


54321				
D	Version List			
	Version	Change List	Date	Author
	1.0.0	First Release	2022-7-19	Mark.Liu
C				
B				
A				
54321				



Title01_Cover

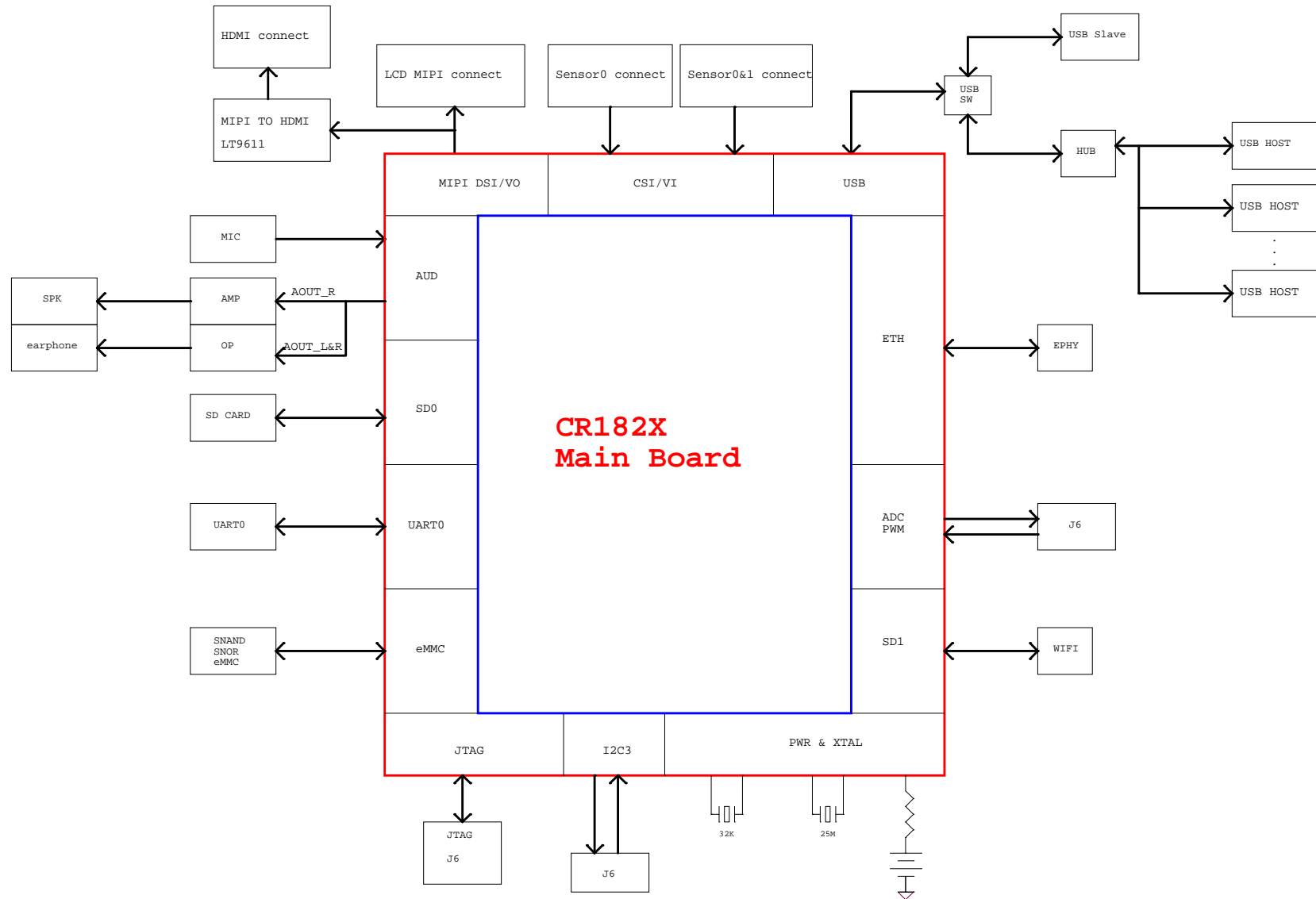
SizeCustom

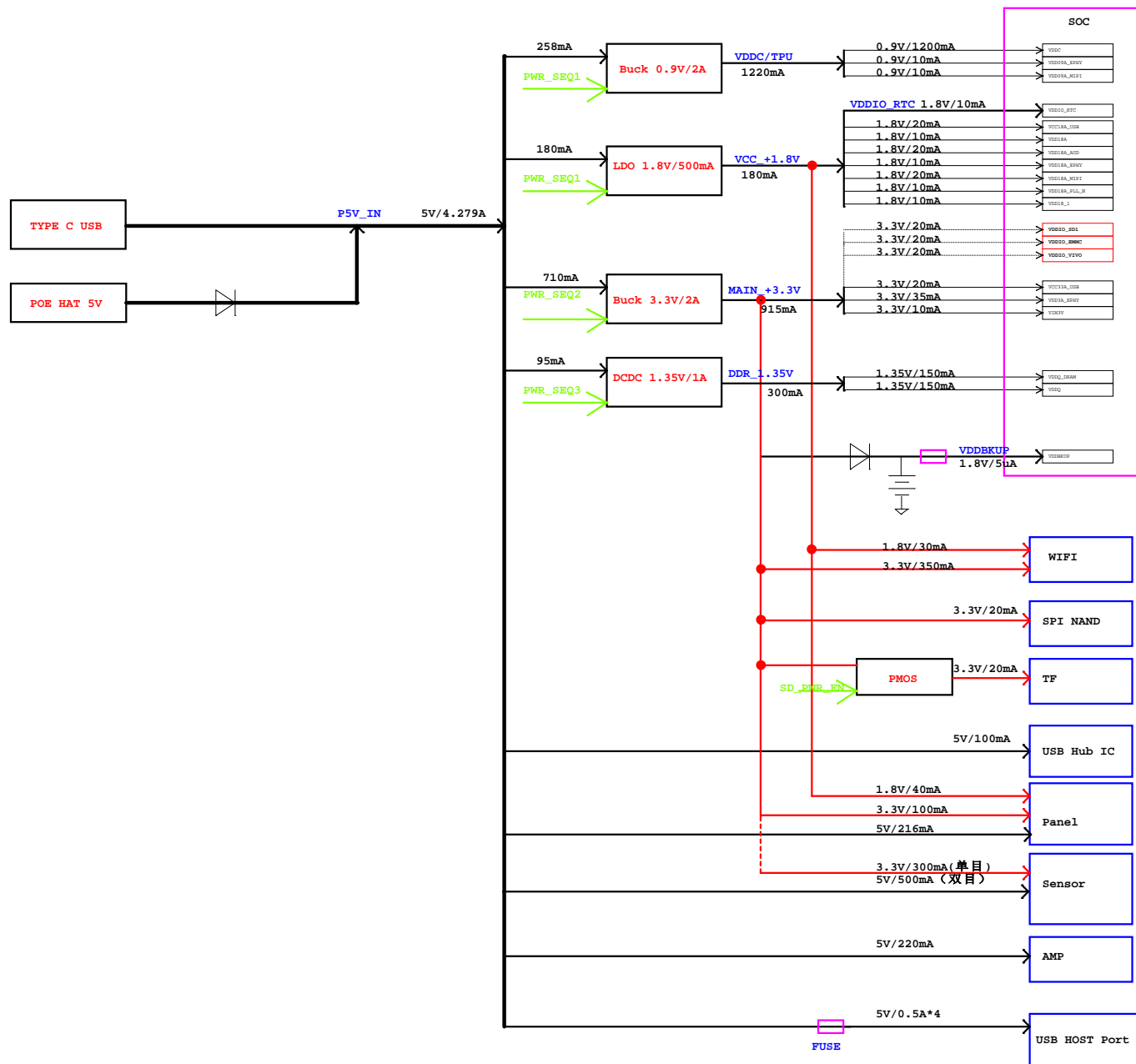
Document NumberCR182x_SIP_BGA

Rev1.0.0

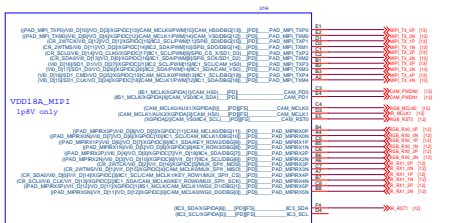
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Block Diagram for CR182x

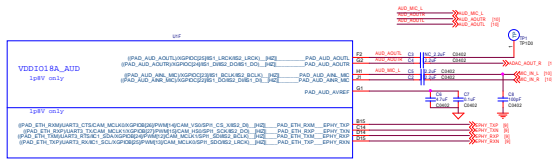




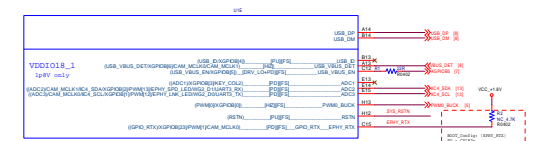
MIPI



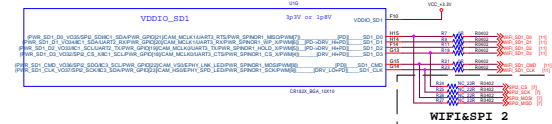
AUDIO&EPHY



USB&VDDIO18

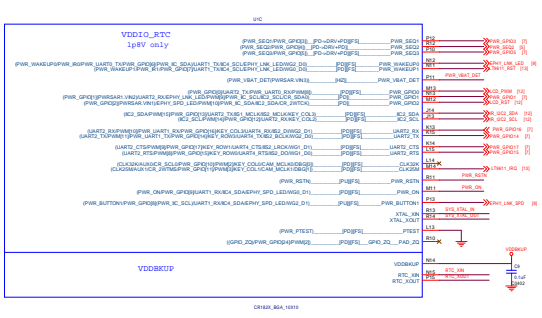


SDI

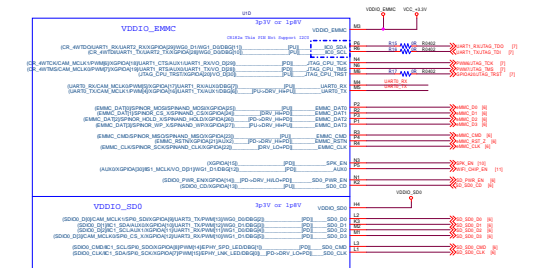


WIFI&SPI 2

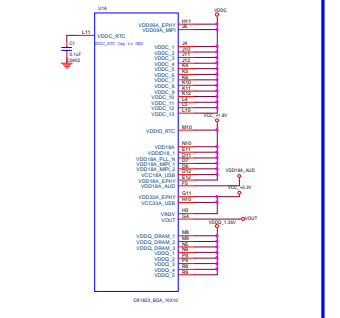
RTC&VDDBKUP



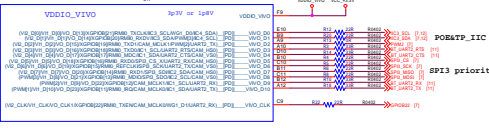
EMMC&SD0



POWER&GND



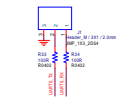
VIVO



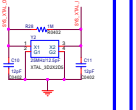
Pull Up



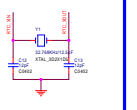
Debug



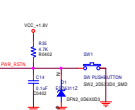
SYS XTAL



RTC XTAL



Reset

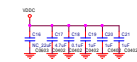


PWR DET



VBAT_DET Must be connect
Default 1.25V
When VBAT_DET< 1.0V
shutdown

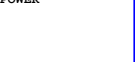
VDDC&TPU POWER



DDR3 POWER



SD0 POWER



BOOT CONFIG

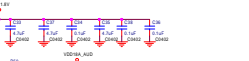
BOOT Config	Serial	Serial
X	1	Serial
1	0	Serial
0	0	Serial



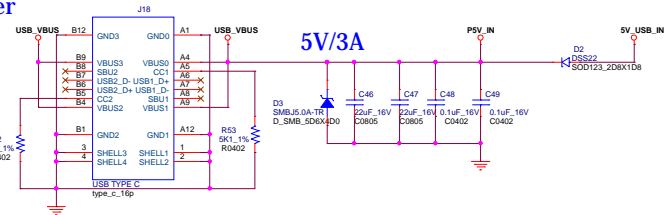
3.3V POWER



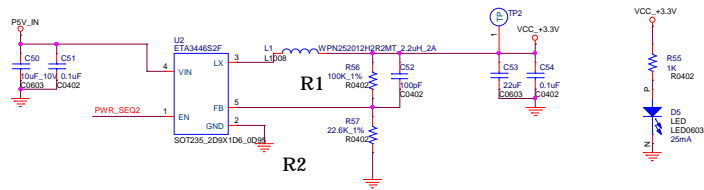
1.8V POWER



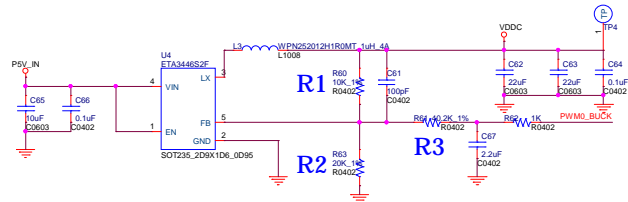
Power IN



PWR_SEQ02

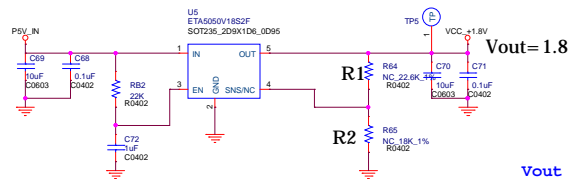


$$V_{out} = 0.6V * (R1/R2 + 1) = 3.25V$$



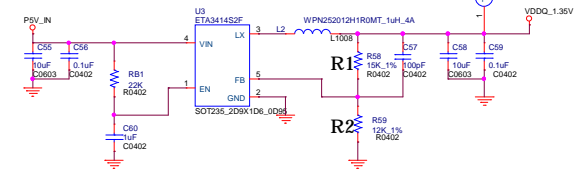
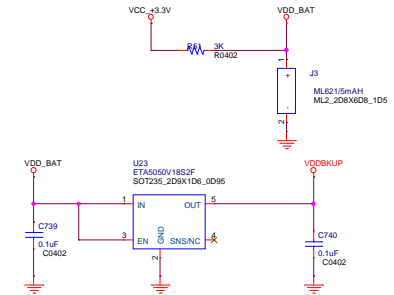
$$R2 \leq 20k\Omega \text{ for stability consideration.}$$

$$V_{out} = 0.6V * (R1/R2 + 1) = 0.9V$$



$$V_{out} = 0.8V * (R1/R2 + 1) = 1.8V$$

RTC

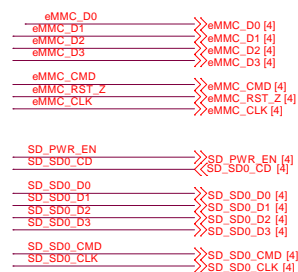


$$V_{out} = 0.6V * (R1/R2 + 1) = 1.35V$$

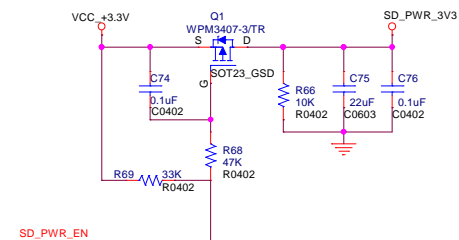
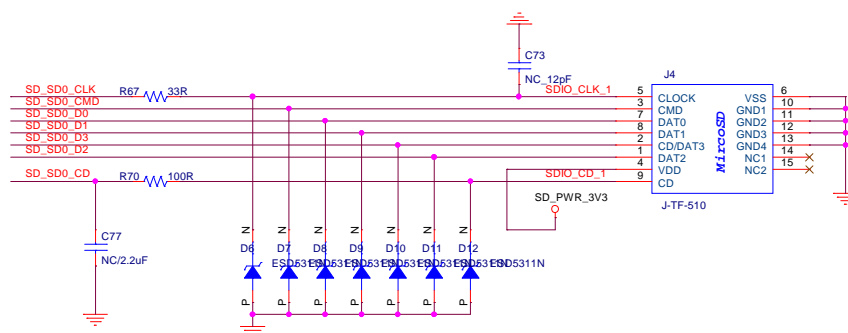
NET



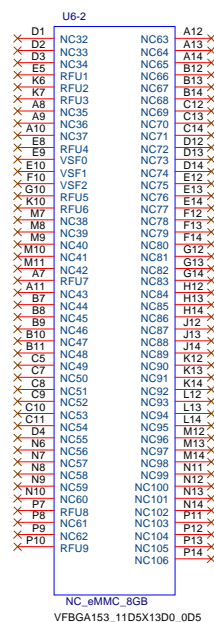
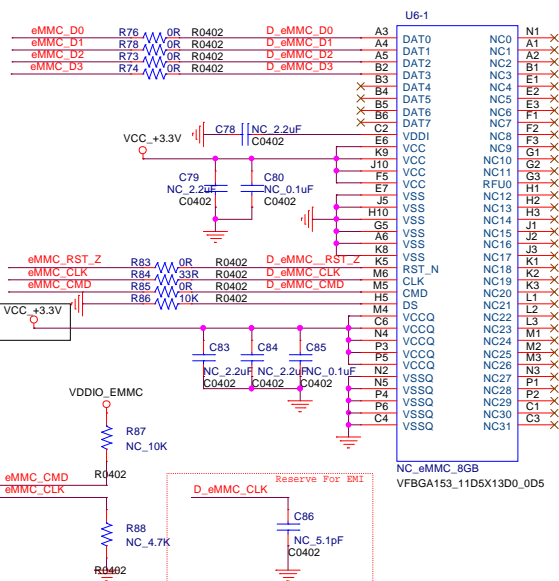
NET



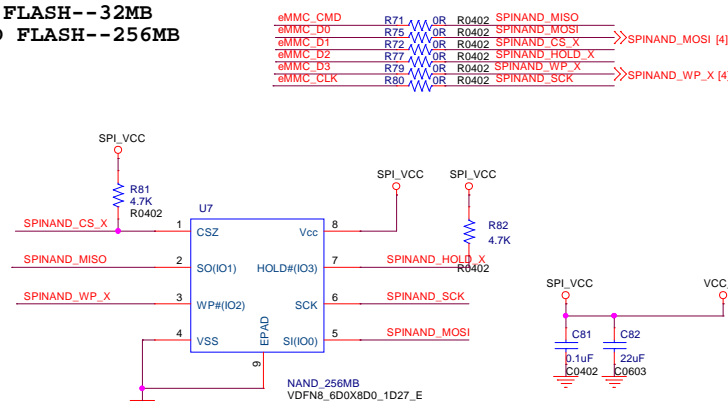
SD Card



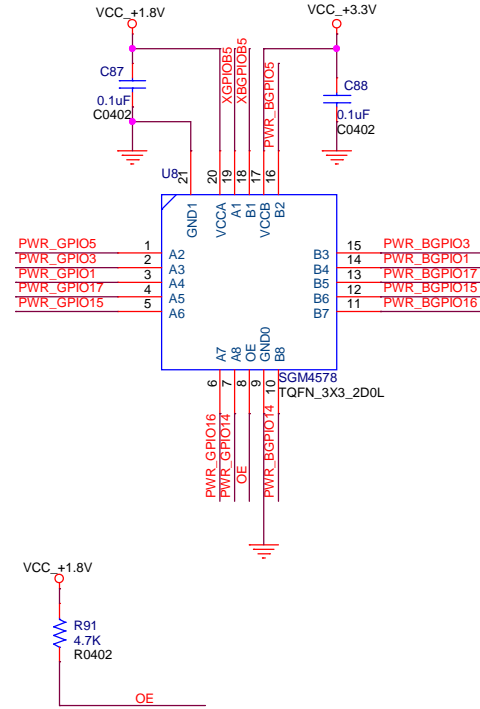
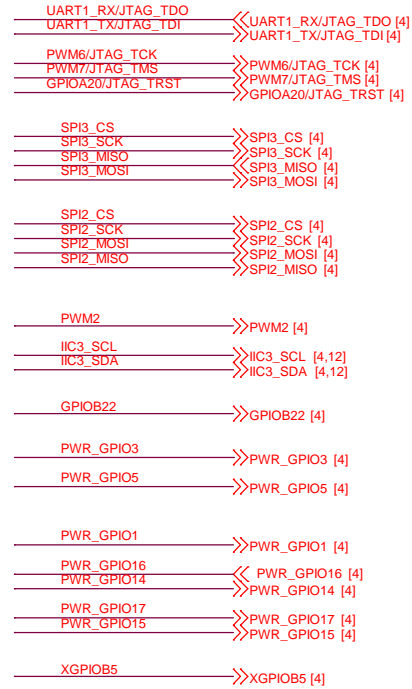
EMMC



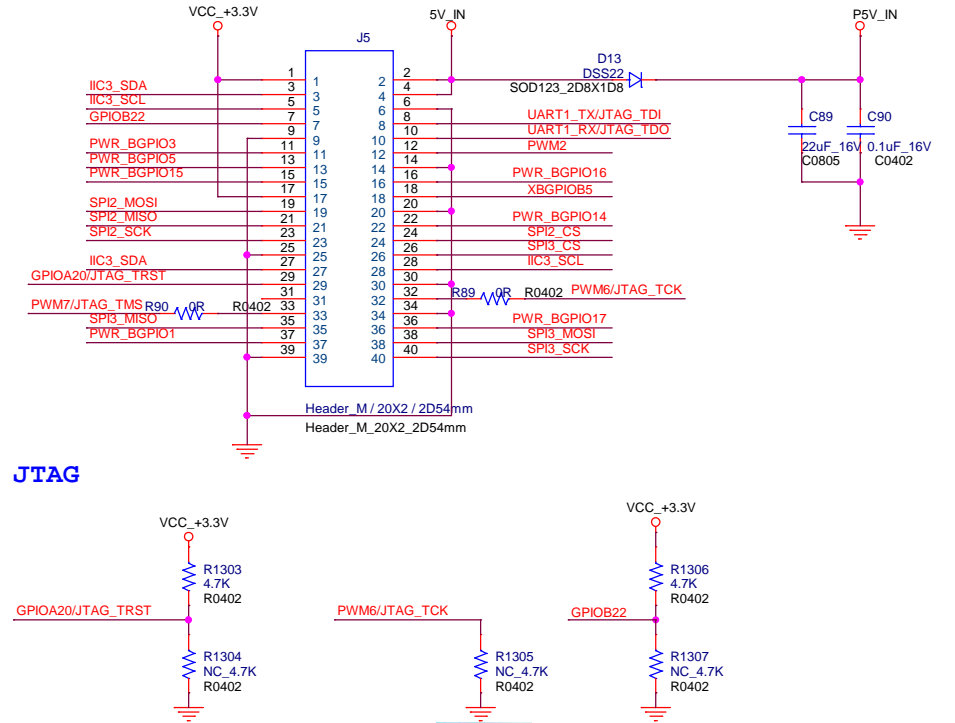
```
SPIFLASH
NOR FLASH--32MB
NAND FLASH--256MB
```



NET



JTAG

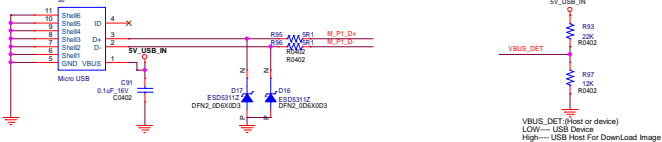


CVITEK		
Title 07_UART_WG		
Size Custom	Document Number CR182x_SIP_BGA	Rev 1.0.0
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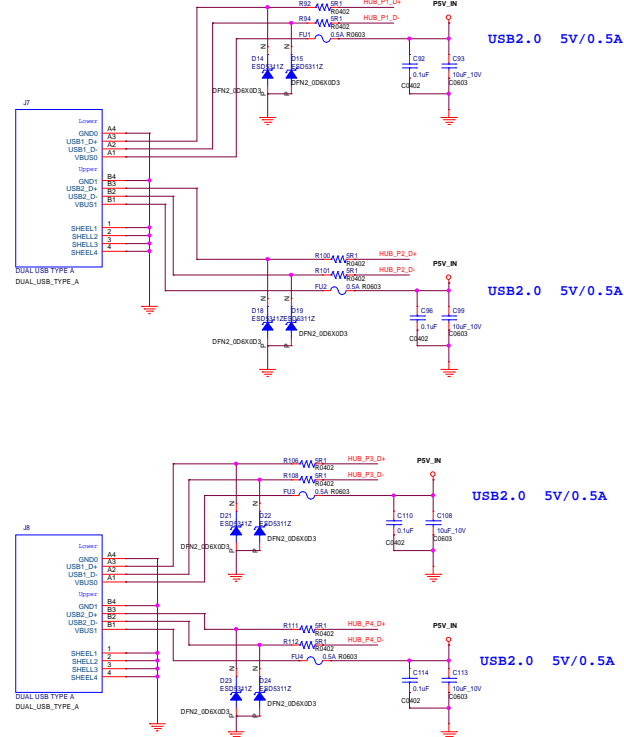
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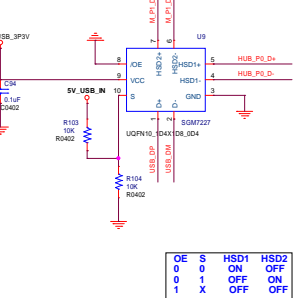
USB UPDATE



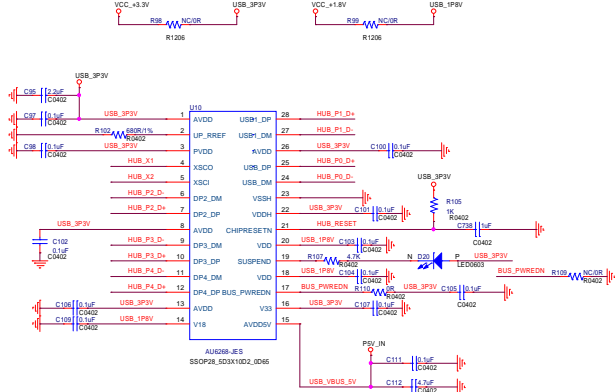
USB2.0 port 1/2/3/4



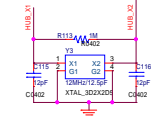
Port SEL



USB 2.0 HUB



USB HUB XTAL



C:\VITEP\		
File	08_USB	
Size	Document Number	Rev
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NET

EPHY_TXP
EPHY_TXN
EPHY_RXP
EPHY_RXN

EPHY_TXP [4]
EPHY_TXN [4]
EPHY_RXP [4]
EPHY_RXN [4]

EPHY_LNK_LED
EPHY_LNK_SPD

EPHY_LNK_LED [4]
EPHY_LNK_SPD [4]

ETH

U11
M1601AG
TF16_12D1X5D1_1D27

EPHY_TXP
EPHY_TXN
EPHY_RXP
EPHY_RXN

TX_D+
TX_D-
POE_TCM
RX_D+
RX_D-
POE_RCM

TXCT
RXCT
TX_D+
TX_D-
RX_D+
RX_D-
POE_45
POE_78
POE_78
POE_78

YEL_C-
YEL_A+
GRN_C-
GRN_A+
NC1
NC2
GND2
GND1

NC1
NC2
GND2
GND1

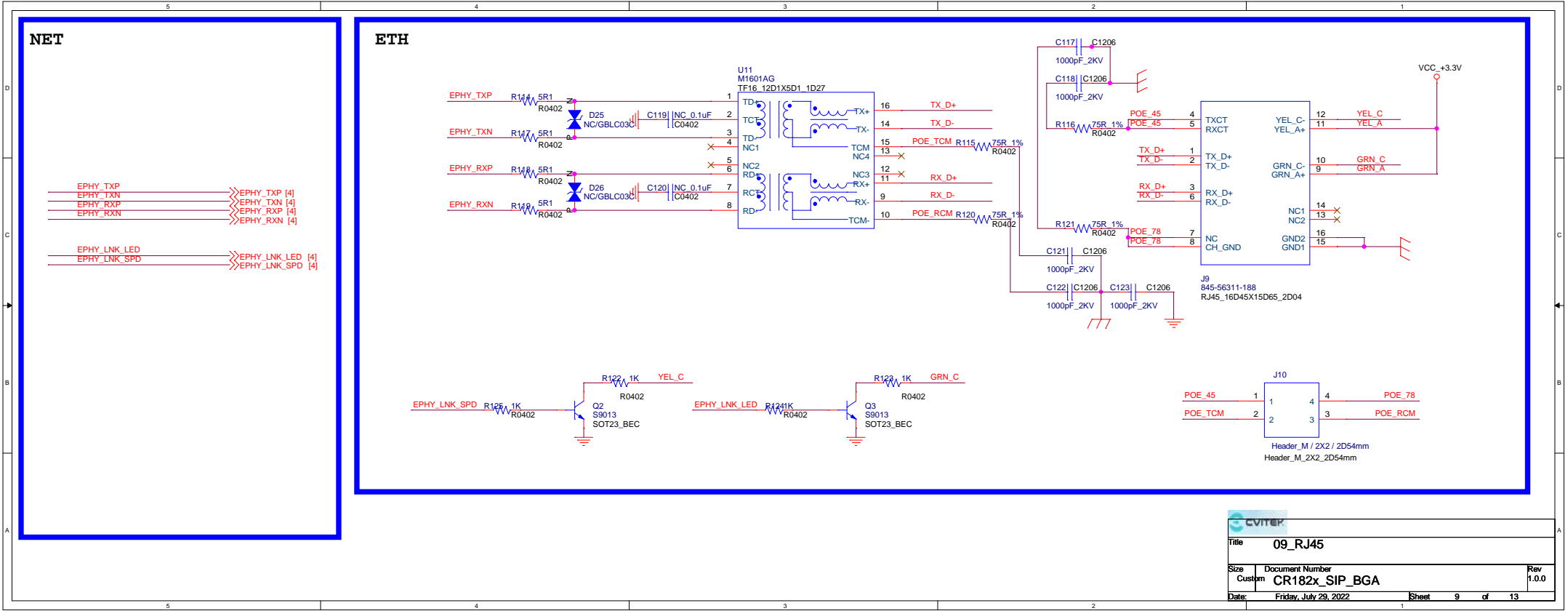
J9
845-56311-188
RJ45_16D45X15D65_2D04

J10
Header_M / 2X2 / 2D54mm
Header_M_2X2_2D54mm

POE_45
POE_TCM
POE_78
POE_78

Header_M / 2X2 / 2D54mm
Header_M_2X2_2D54mm

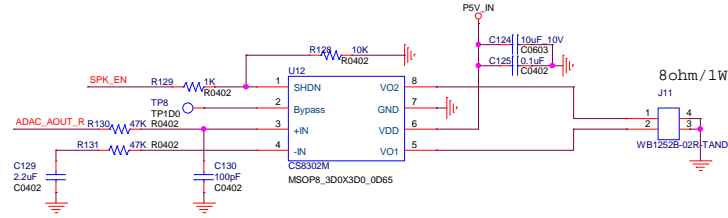
09_RJ45
CR182x_SIP_BGA
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1.0.0

[illegible][illegible]

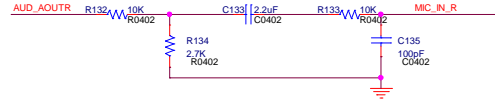
NET

ADAC_AOUT_R >>> ADAC_AOUT_R [4]
 MIC_IN_L <<< MIC_IN_L [4]
 MIC_IN_R <<< MIC_IN_R [4]
 SPK_EN >>> SPK_EN [4]
 AUD_AOUTL >>> AUD_AOUTL [4]
 AUD_AOUTR >>> AUD_AOUTR [4]
 AUD_MIC_L >>> AUD_MIC_L [4]

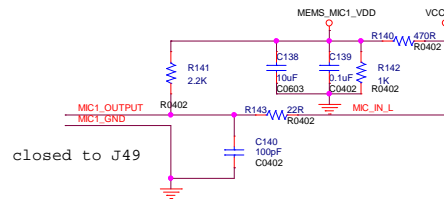
Audio AMP



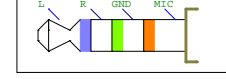
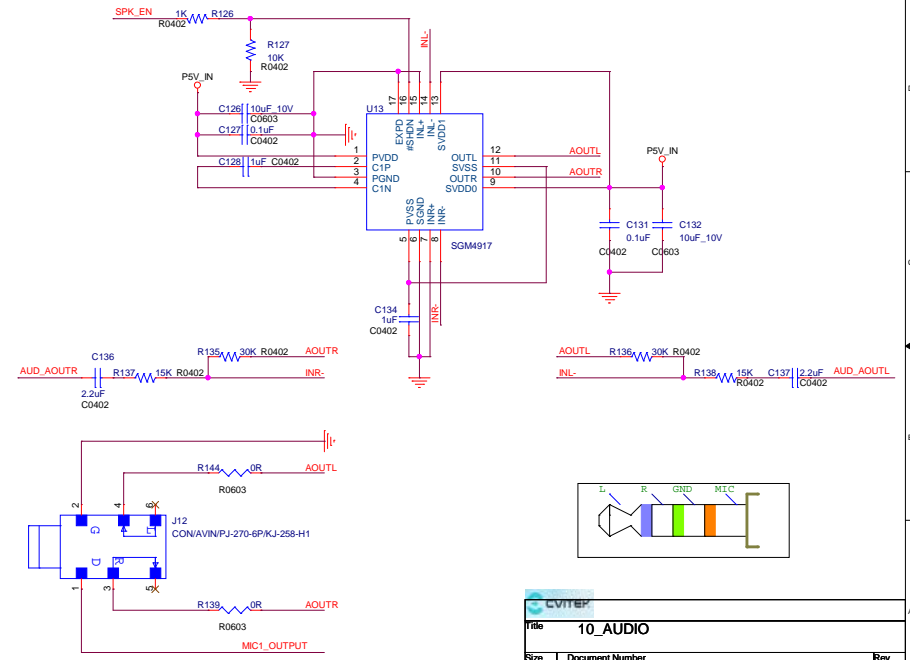
AEC



MIC



closed to J49



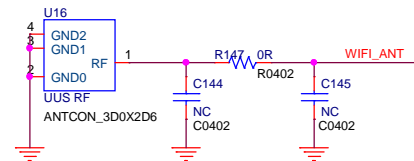
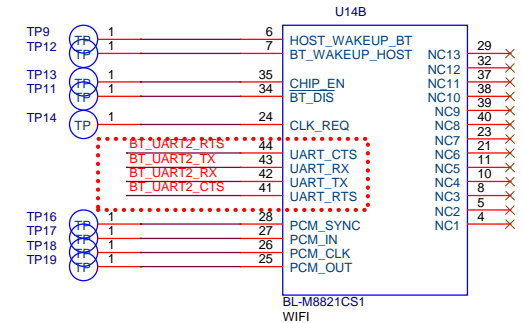
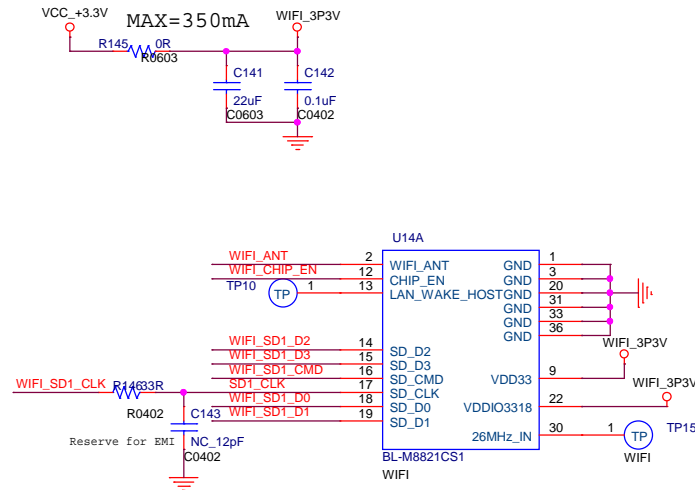
Title			
10_AUDIO			
Size	Document Number	Rev	
Customer	CR182x_SIP_BGA	1.0.0	
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NET

WIFI_SD1_D0 >>> WIFI_SD1_D0 [4]
WIFI_SD1_D1 >>> WIFI_SD1_D1 [4]
WIFI_SD1_D2 >>> WIFI_SD1_D2 [4]
WIFI_SD1_D3 >>> WIFI_SD1_D3 [4]

WIFI_SD1_CMD >>> WIFI_SD1_CMD [4]
WIFI_SD1_CLK >>> WIFI_SD1_CLK [4]
WIFI_CHIP_EN >>> WIFI_CHIP_EN [4]

BT_UART2_CTS >>> BT_UART2_CTS [4]
BT_UART2_RTS >>> BT_UART2_RTS [4]
BT_UART2_RX >>> BT_UART2_RX [4]
BT_UART2_TX >>> BT_UART2_TX [4]



CVITEK			
Title 11_WIFI_BT			
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Custom	CR182x_SIP_BGA		1.0.0
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NET

MIPI_TX_P0 >> MIPI_TX_P0 [4,13]
MIPI_TX_M0 >> MIPI_TX_M0 [4,13]
MIPI_TX_P1 >> MIPI_TX_P1 [4,13]
MIPI_TX_M1 >> MIPI_TX_M1 [4,13]
MIPI_TX_PCLK >> MIPI_TX_PCLK [4,13]
MIPI_TX_MCLK >> MIPI_TX_MCLK [4,13]
MIPI_TX_P3 >> MIPI_TX_P3 [4,13]
MIPI_TX_M3 >> MIPI_TX_M3 [4,13]
MIPI_TX_P4 >> MIPI_TX_P4 [4,13]
MIPI_TX_M4 >> MIPI_TX_M4 [4,13]

LCD_PWM >> LCD_PWM [4]
LCD_RST >> LCD_RST [4]

RGB_MCLK0 >> RGB_MCLK0 [4]
RGB_MCLK1 >> RGB_MCLK1 [4]
RGB_RST0 >> RGB_RST0 [4]
RGB_RST1 >> RGB_RST1 [4]

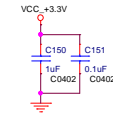
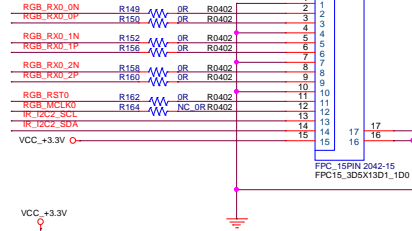
IR_I2C2_SCL >> IR_I2C2_SCL [4]
IR_I2C2_SDA >> IR_I2C2_SDA [4]

RGB_RX0_0P >> RGB_RX0_0P [4]
RGB_RX0_0N >> RGB_RX0_0N [4]
RGB_RX0_1P >> RGB_RX0_1P [4]
RGB_RX0_1N >> RGB_RX0_1N [4]
RGB_RX0_2P >> RGB_RX0_2P [4]
RGB_RX0_2N >> RGB_RX0_2N [4]
IR_RX1_0P >> IR_RX1_0P [4]
IR_RX1_0N >> IR_RX1_0N [4]
IR_RX1_1P >> IR_RX1_1P [4]
IR_RX1_1N >> IR_RX1_1N [4]
IR_RX1_2P >> IR_RX1_2P [4]
IR_RX1_2N >> IR_RX1_2N [4]
CAM_PWDN0 >> CAM_PWDN0 [4]
CAM_PWDN1 >> CAM_PWDN1 [4]

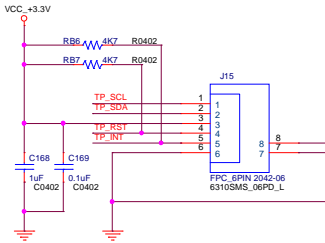
TP_INT R172 >> PWM/JTAG_TMS
TP_RST R173 >> PWM/JTAG_TCK

TP_SCL R175 >> IIC3_SCL [4,7]
TP_SDA R176 >> IIC3_SDA [4,7]

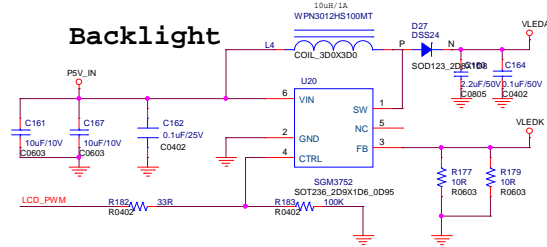
SENEORO



PANEL&TP



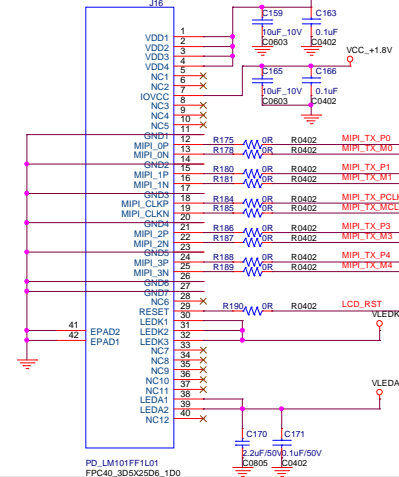
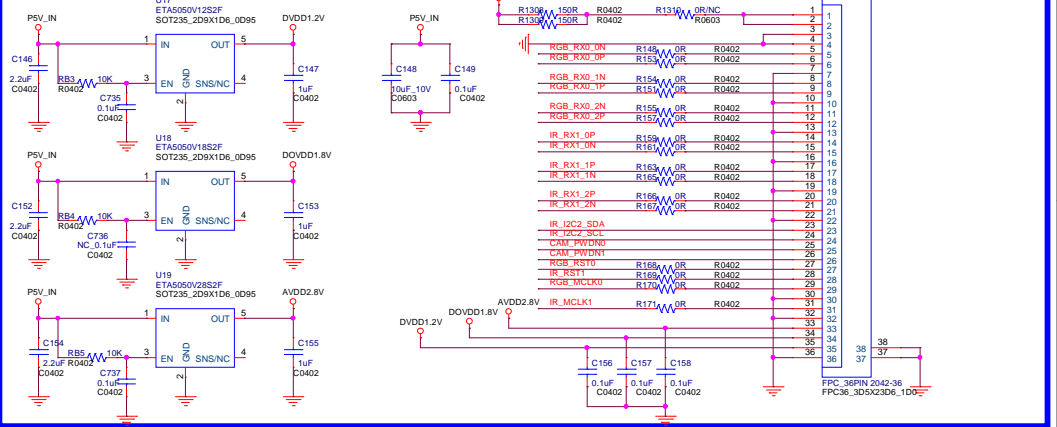
Backlight



VLED=18V
3*20=60mA
 $I_{ledmax} = V_{fb} / R_{set}$
 $V_{fb} = Duty * 200mV + 0.75mV$
200mV internal reference voltage

POWER

SENEOR 0&SENSOR 1

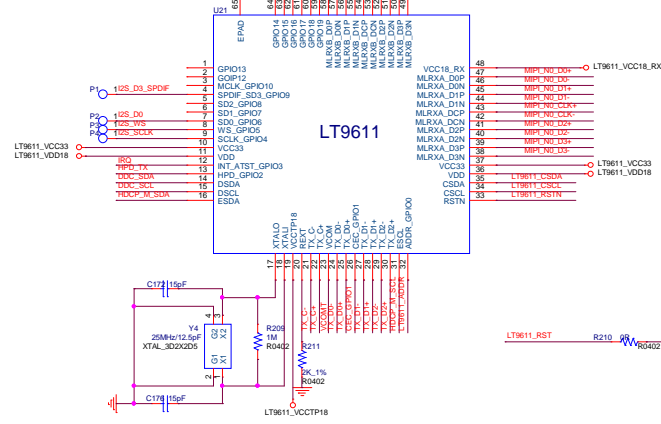


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Size	Custom
Document Number	CR182x_SIP_BGA
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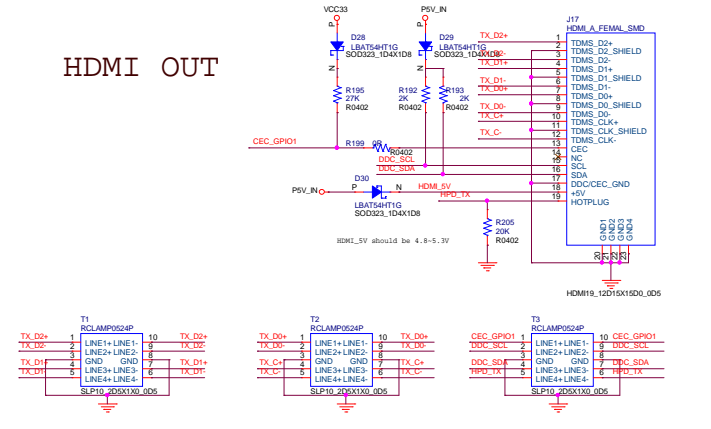
MIPI_IN



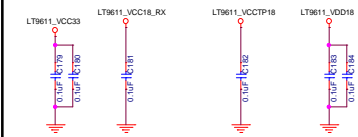
LT9611



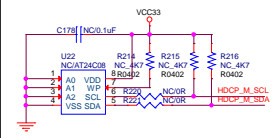
HDMI OUT



Decouple Cap: Close IC power pin



HDCP KEY



MIS

