Exercise 2

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1. 以 tool 產生分別可以測到 c17 電路中下列 faults 的 patterns、summary。

a. U2/out s-a-0

Summary

(Report 顯示需要 1 個 pattern)

```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          1
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
-------------------------------------------------
total faults                                 1
test coverage                           100.00%
fault coverage                          100.00%
-------------------------------------------------
            Pattern Summary Report
-------------------------------------------------
#internal patterns                           1
    #basic_scan patterns                     1
-------------------------------------------------
```

Patterns (test1_a_tp.v)

(Pattern 為: 01001)

```
Pattern "_pattern_" {
   W "_default_WFT_";
   "precondition all Signals": C { "_pi"=00000; "_po"=XX; }
   "pattern 0": Call "capture" {
      "_pi"=01001; "_po"=HH; }
}

// Patterns reference 2 V statements, generating 2 test cycles
```

test1_a.fault

```
test1_a.fault
1 sa0    NC    U2/Y
2
```

b. x16gat s-a-1

Summary

(Report 顯示需要 1 個 pattern)

```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          3
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
-------------------------------------------------
total faults                                 3
test coverage                           100.00%
fault coverage                          100.00%
-------------------------------------------------
            Pattern Summary Report
-------------------------------------------------
#internal patterns                           1
    #basic_scan patterns                     1
-------------------------------------------------
```

Patterns (test1_a_tp.v)

(Pattern 為: 01010)

```
Pattern "_pattern_" {
   W "_default_WFT_";
   "precondition all Signals": C { "_pi"=00000; "_po"=XX; }
   "pattern 0": Call "capture" {
      "_pi"=01010; "_po"=HH; }
}

// Patterns reference 2 V statements, generating 2 test cycles
```

test1_a.fault

```
test1_b.fault
1 sa1    NC    U3/Y
2 sa1    NC    U5/B
3 sa1    NC    U6/A
4
```

c. x19gat s-a-0 & s-a-1

Summary

(Report 顯示需要 2 個 pattern)

```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          4
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
-------------------------------------------------
total faults                                 4
test coverage                           100.00%
fault coverage                          100.00%
-------------------------------------------------
            Pattern Summary Report
-------------------------------------------------
#internal patterns                           2
    #basic_scan patterns                     2
-------------------------------------------------
```

Patterns (test1_a_tp.v)

(Pattern 為: 11110、00011)

```
Pattern "_pattern_" {
   W "_default_WFT_";
   "precondition all Signals": C { "_pi"=00000; "_po"=XX; }
   "pattern 0": Call "capture" {
      "_pi"=11110; "_po"=HL; }
   "pattern 1": Call "capture" {
      "_pi"=00011; "_po"=LH; }
}

// Patterns reference 4 V statements, generating 4 test cycles
```

test1_a.fault

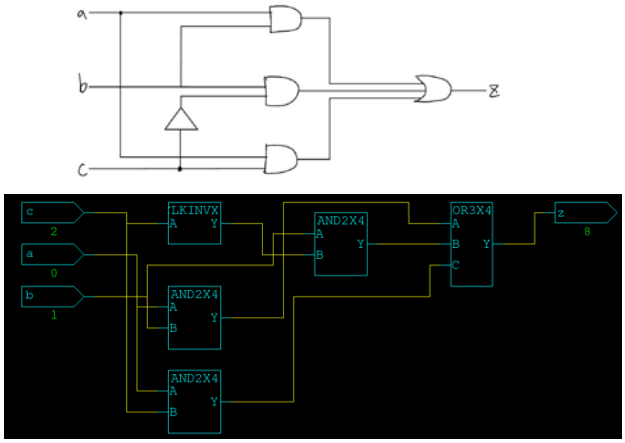
```
test1_c.fault
1 sa0    --    U4/Y
2 sa0    --    U6/B
3 sa1    NC    U4/Y
4 sa1    --    U6/B
5
```

2. 對 ISCAS85 c499 電路做 ATPG，觀看需要多少 patterns 及 fault coverage 為多少

```
Report Summaries (在 vlsicad6)
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT       1190
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
-----------------------------------------------
total faults                             1190
test coverage                          100.00%
fault coverage                         100.00%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                         78
    #basic_scan patterns                   77
    #full_sequential patterns               1
-----------------------------------------------
```

Report 顯示
Patterns : 需要 78 個 patterns
Fault Coverage 為 100.00 %

3. 設計一個 combinational circuit，這個電路至少包含一個 undetectable fault，使用本練習的方法做 ATPG



2_3.v

```
1   `timescale 1ns/1ns
2
3   module UNDETECTABLE ( a, b, c, z);
4   output z;
5   input a, b, c;
6
7   wire a_and_b, not_c, b_and_notc, a_and_c;
8     not I0 (not_c, c);
9     and I1 (a_and_b, a, b);
10    and I2 (b_and_notc, b, not_c);
11    and I4 (a_and_c, a, c);
12    or  I5 (z, a_and_b, b_and_notc, a_and_c);
13
14  endmodule
```

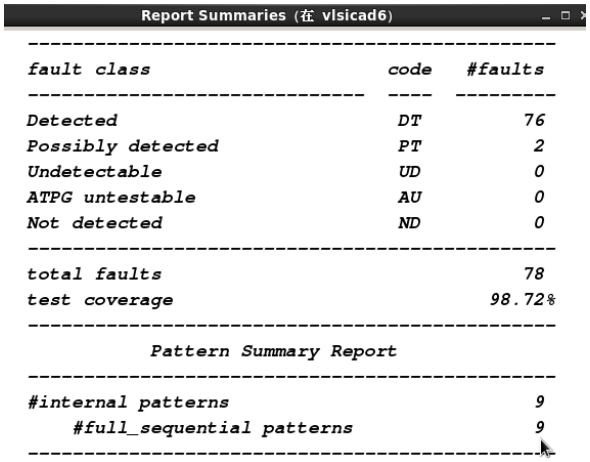
Summary

```
Report Summaries (在 vlsicad6)
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT         34
Possibly detected                PT          0
Undetectable                     UD          4
ATPG untestable                  AU          0
Not detected                     ND          0
-----------------------------------------------
total faults                               38
test coverage                          100.00%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                          6
    #basic_scan patterns                    6
-----------------------------------------------
```

Report 顯示
Detected : 34 個 faults
Undetectable : 4 個 faults

4. <Sequential circuit>

以 ISCA89 電路中的 s27 電路作為對象練習 ATPG，查看所需 patterns 數目及 fault coverage 為多少



Report 顯示

Patterns : 需要 9 個 pattern

Fault Coverage : 98.72 %