Exercise 1

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1. 以下圖 Summary report 結果可知，pattern 01100 輸入對 c17 電路做 Fault Simulation 查看對所有的 Stuck-at Faults 的 test coverage 為 26.00% (改寫檔案: c17.tbench.v //1-1)

```
Report Summaries (在 vlsicad6)
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT         13
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND         37
-----------------------------------------------
total faults                                50
test coverage                            26.00%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                           0
#external patterns (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)    1
    #basic_scan patterns                     1
-----------------------------------------------
```

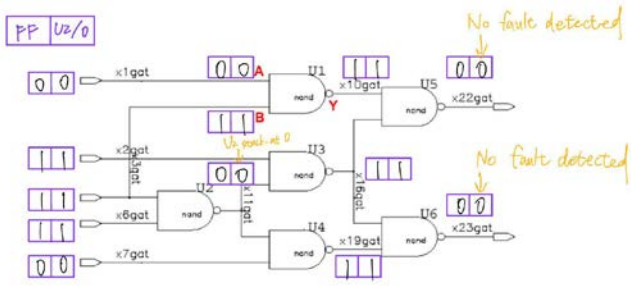
2. 以 tool 查看下列 5 個 patterns 中哪些可以測到 U2 的輸出 stuck-at 0 fault。
(改寫檔案: c17.tbench.v //1-2、test2.fault)

Tool result　　Parallel Fault Simulation

a. 01110

(Summary report 結果顯示 not detected)　　(PFS 分析結果為 not detected)

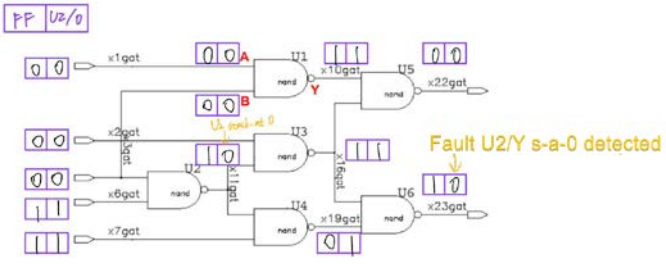
```
Report Summaries (在 vlsicad6)
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          0
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          1
-----------------------------------------------
total faults                                 1
test coverage                             0.00%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                           0
#external patterns (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)    1
    #basic_scan patterns                     1
-----------------------------------------------
```



b. 00011

(Summary report 結果顯示 detected)　　(PFS 分析結果為 detected)

```
Report Summaries (在 vlsicad6)
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          1
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
-----------------------------------------------
total faults                                 1
test coverage                            100.00%
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns                           0
#external patterns (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)    1
    #basic_scan patterns                     1
-----------------------------------------------
```

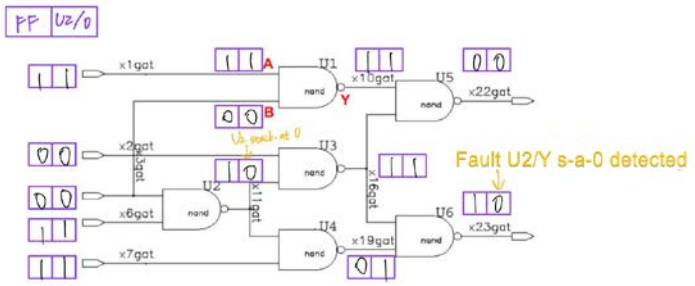


c. 10011

(Summary report 結果顯示 detected)

```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          1
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
-------------------------------------------------
total faults                                 1
test coverage                           100.00%
-------------------------------------------------
          Pattern Summary Report
-------------------------------------------------
#internal patterns                           0
#external patterns  (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)      1
    #basic_scan patterns                     1
-------------------------------------------------
```

(PFS 分析結果為 detected)

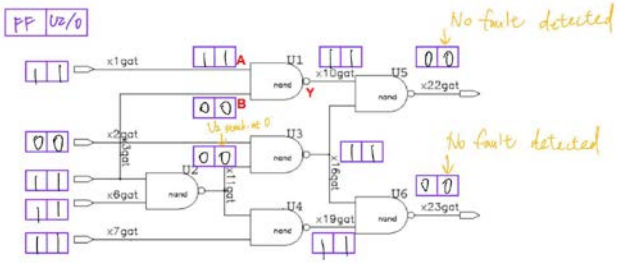


d. 10111

(Summary report 結果顯示 not detected)

```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          0
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          1
-------------------------------------------------
total faults                                 1
test coverage                            0.00%
-------------------------------------------------
          Pattern Summary Report
-------------------------------------------------
#internal patterns                           0
#external patterns  (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)      1
    #basic_scan patterns                     1
-------------------------------------------------
```

(PFS 分析結果為 not detected)

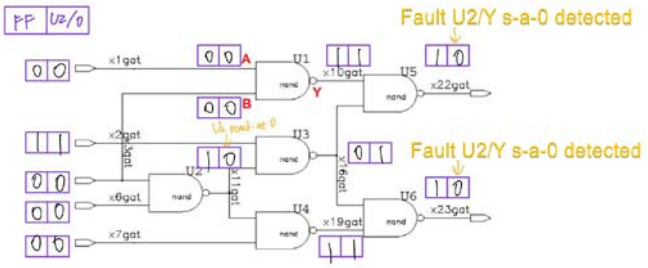


e. 01000

(Summary report 結果顯示 not detected)

```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT          1
Possibly detected                PT          0
Undetectable                     UD          0
ATPG untestable                  AU          0
Not detected                     ND          0
-------------------------------------------------
total faults                                 1
test coverage                           100.00%
-------------------------------------------------
          Pattern Summary Report
-------------------------------------------------
#internal patterns                           0
#external patterns  (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)      1
    #basic_scan patterns                     1
-------------------------------------------------
```

(PFS 分析結果為 detected)



3. 以 tool 檢查 pattern 01011 可以測到下列 faults 中的哪些 faults，並以 Parallel fault Simulation 與 Deductive fault Simulation 自行分析，看結果是否相同。

a. x16gat s-a-1 (改寫檔案: c17.tbench.v //1-3、test3_a.fault)

Tool result

(Summary report 結果為 2 個 fault detected / 1 個 fault not detected)

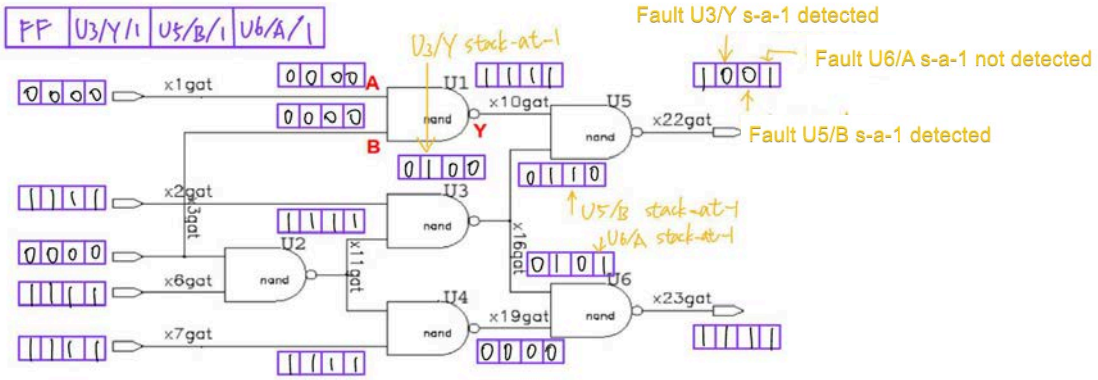
```
Report Summaries (在 vlsicad6)
fault class                    code   #faults
------------------------------ ----  ---------
Detected                       DT          2
Possibly detected              PT          0
Undetectable                   UD          0
ATPG untestable                AU          0
Not detected                   ND          1
------------------------------------------------
total faults                               3
test coverage                          66.67%
------------------------------------------------
          Pattern Summary Report
------------------------------------------------
#internal patterns                         0
#external patterns (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)    1
    #basic_scan patterns                   1
------------------------------------------------
```

test3_a.fault

```
test3_a.fault
1 sa1   NC   U3/Y
2 sa1   NC   U5/B
3 sa1   NC   U6/A
```

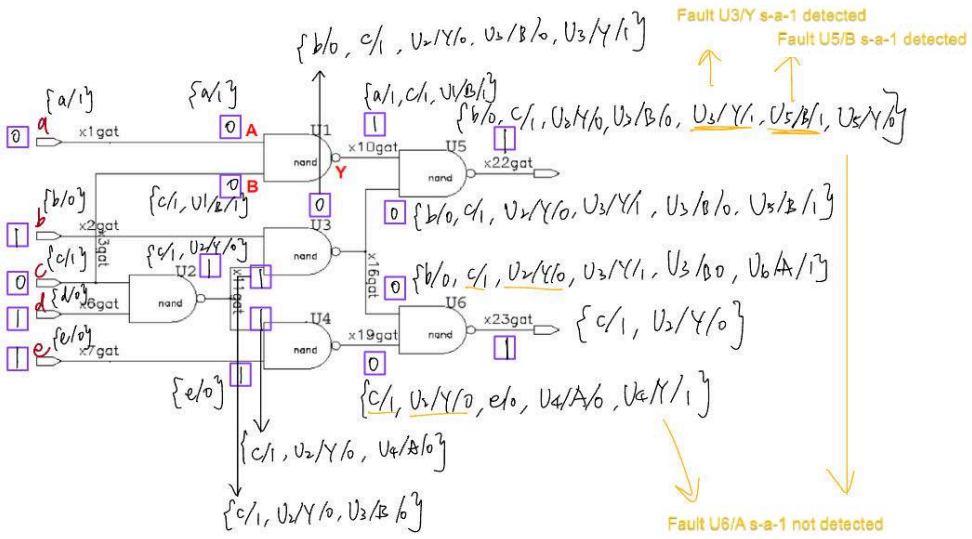
Parallel Fault Simulation

(PFS 分析結果為 Detected : Fault U3/Y s-a-1、Fault U5/B s-a-1
Not detected : Fault U6/A s-a-1)



Deductive fault Simulation

(Deductive fault Simulation 分析結果為 Detected : Fault U3/Y s-a-1、Fault U5/B s-a-1
Not detected : Fault U6/A s-a-1)



b. x7gat s-a-1

Tool result

(Summary report 結果為 1 個 fault not detected)

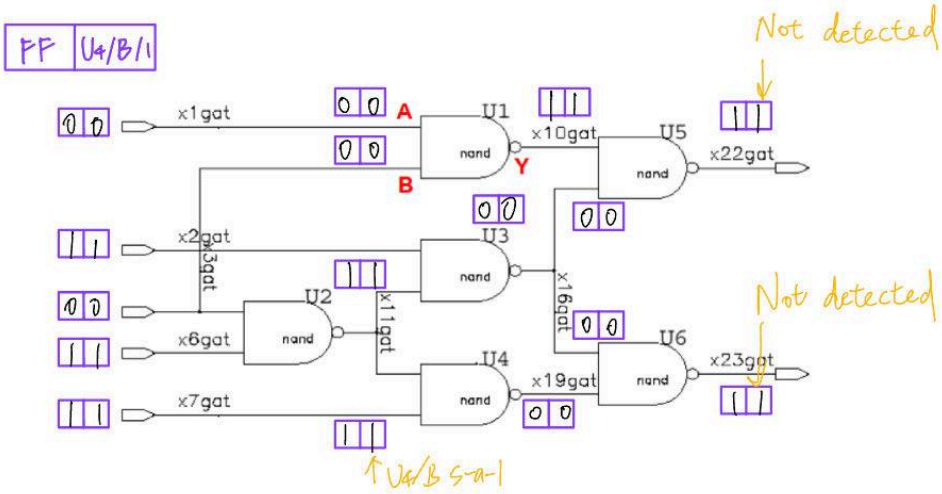
```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                    code   #faults
------------------------------ ----  ---------
Detected                        DT          0
Possibly detected               PT          0
Undetectable                    UD          0
ATPG untestable                 AU          0
Not detected                    ND          1
-------------------------------------------------
total faults                                1
test coverage                           0.00%
-------------------------------------------------
          Pattern Summary Report
-------------------------------------------------
#internal patterns                          0
#external patterns  (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)   1
    #basic_scan patterns                    1
-------------------------------------------------
```

test3_b.fault

```
test3_b.fault
1 sa1    --    U4/B
2
```

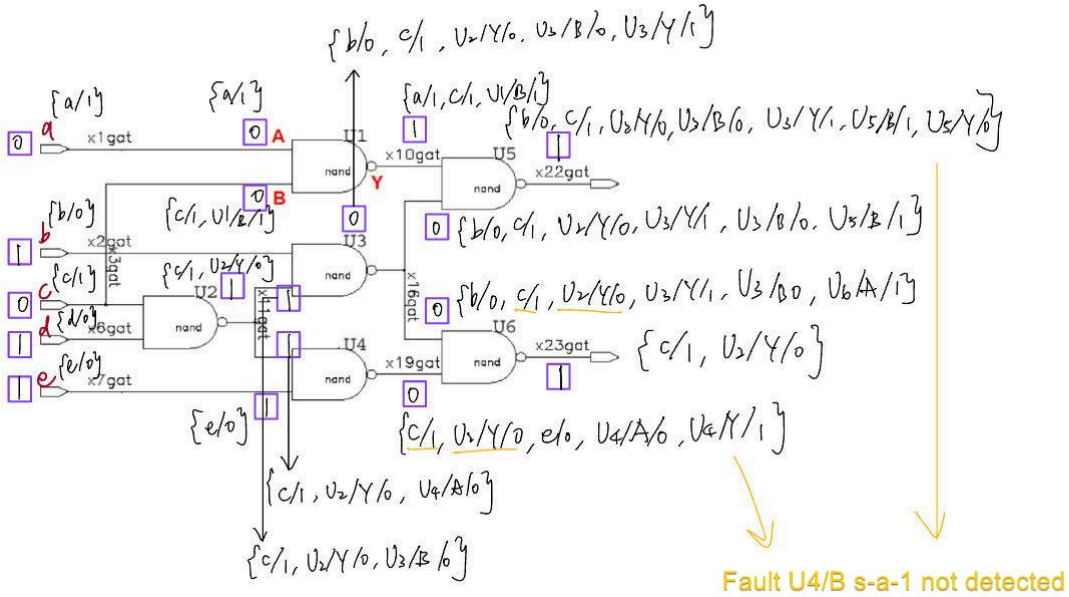
Parallel Fault Simulation

(PFS 分析結果為 Not detected : Fault U4/B s-a-1)



Deductive fault Simulation

(Deductive fault Simulation 分析結果為 Not detected : Fault U4/B s-a-1)



c. x11gat s-a-0

Tool result

(Summary report 結果為 2 個 fault detected / 1 個 fault not detected)

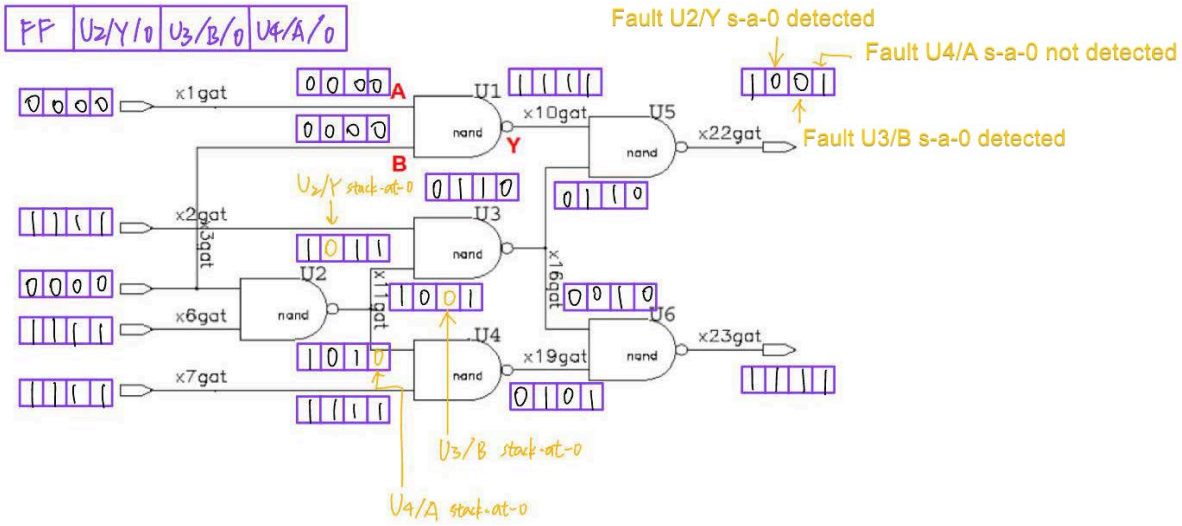
```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                    code   #faults
------------------------------ ----  ---------
Detected                       DT          2
Possibly detected              PT          0
Undetectable                   UD          0
ATPG untestable                AU          0
Not detected                   ND          1
-------------------------------------------------
total faults                               3
test coverage                          66.67%
-------------------------------------------------
          Pattern Summary Report
-------------------------------------------------
#internal patterns                         0
#external patterns  (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)      1
    #basic_scan patterns                   1
-------------------------------------------------
```

test3_c.fault

```
test3_c.fault
1 sa0   NC   U2/Y
2 sa0   --   U3/B
3 sa0   --   U4/A
```

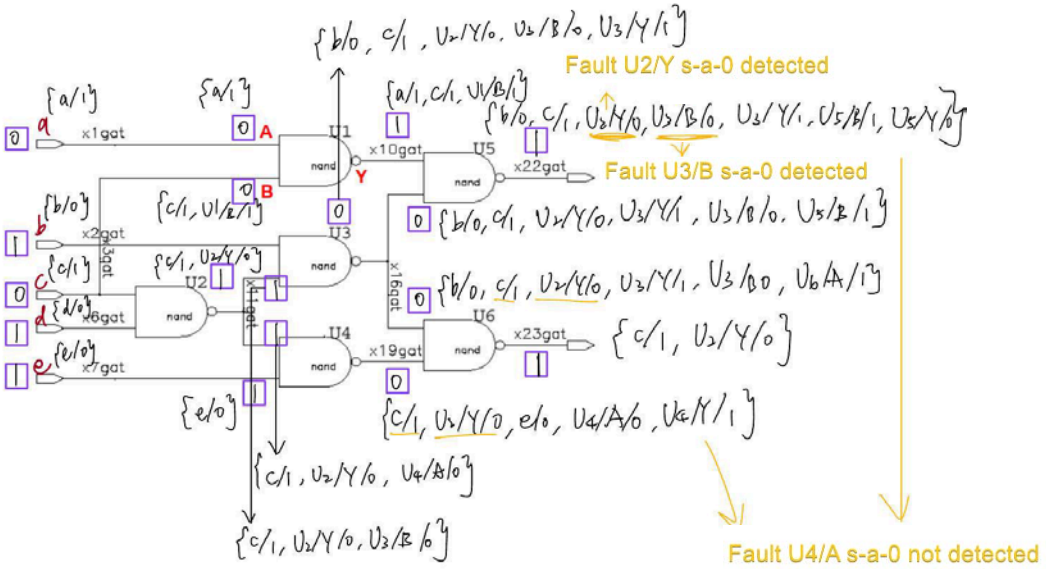
Parallel Fault Simulation

(PFS 分析結果為 Detected : Fault U2/Y s-a-0、Fault U3/B s-a-0
Not detected : Fault U4/A s-a-0)



Deductive fault Simulation

(Deductive fault Simulation 分析結果為 Detected : Fault U2/Y s-a-0、Fault U3/B s-a-0
Not detected : Fault U4/A s-a-0)



d. x22gat s-a-0

Tool result

(Summary report 結果為 1 個 fault detected)

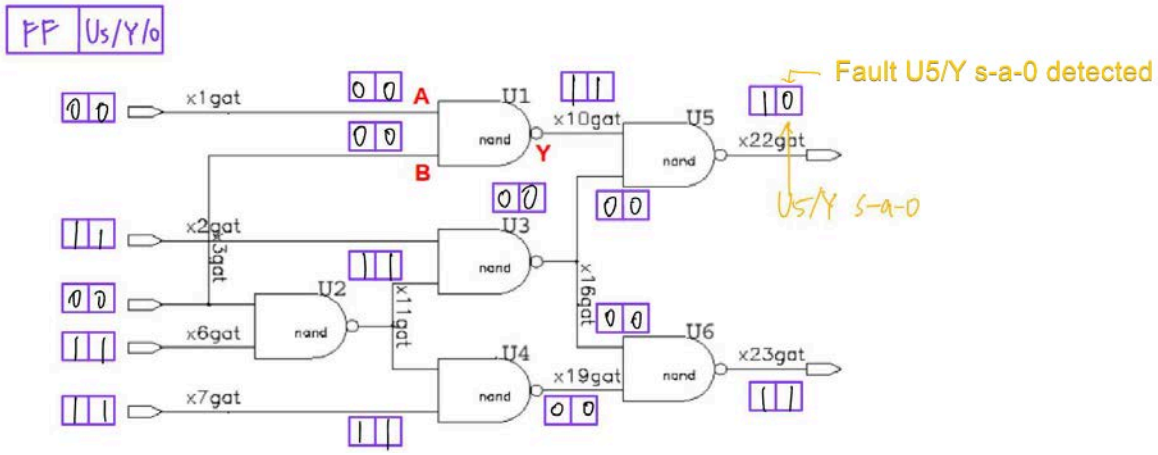
```
Report Summaries (在 vlsicad6)
-------------------------------------------------
fault class                    code   #faults
------------------------------ ----  ---------
Detected                        DT          1
Possibly detected               PT          0
Undetectable                    UD          0
ATPG untestable                 AU          0
Not detected                    ND          0
-------------------------------------------------
total faults                                1
test coverage                          100.00%
-------------------------------------------------
          Pattern Summary Report
-------------------------------------------------
#internal patterns                          0
#external patterns (/home/user2/test22/test2225/exercise/exercise_1/c17_tbench.v)      1
    #basic_scan patterns                    1
-------------------------------------------------
```

test3_d.fault

```
test3_d.fault
1 sa0    --    U5/Y
```

Parallel Fault Simulation

(PFS 分析結果為 Detected : Fault U5/Y s-a-0)



Deductive fault Simulation

(Deductive fault Simulation 分析結果為 Detected : Fault U5/Y s-a-0)