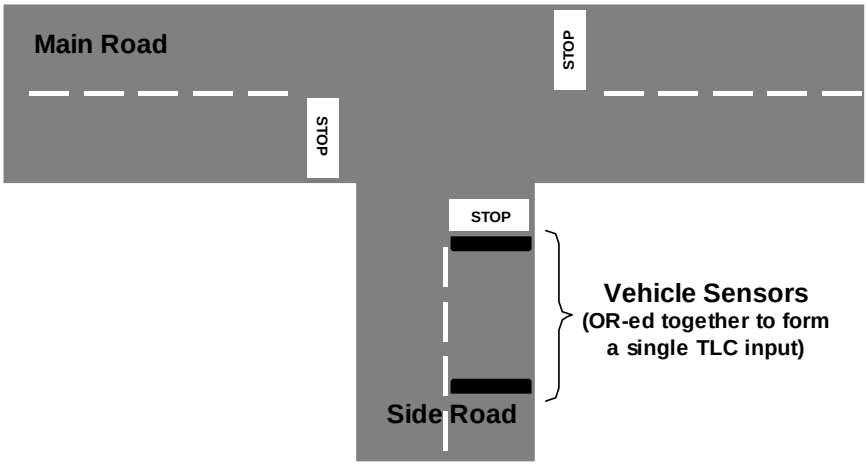
Technical Objective:

Creating timers or delays based on an input is a typical requirement of a design. The technical objective of this laboratory is to determine the feasibility of using counters to create a real world timed delay. In addition the use of a counter, using a state machine will be explored to create a system that will respond to an external input. In this lab, a Traffic Light Controller will be used as a prototype to demonstrate the system response the delays from external input. Special attention will be given to design size, re-usability and maintainability.

Pre-Laboratory:

1. Design a Traffic Light Controller (TLC) for a Tee intersection of a Main Road and a Side Road. The TLC needs to control RED-YELLOW-GREEN light configurations for both the Main Road and a Side Road. Additionally, the TLC needs to control two delay units. The Traffic Light Controller needs to operate under the following specifications…
    - The Main Road has priority over the Side Road.
    - If the Main Road has the right-of-way (i.e. Main Road is **GREEN**, Side Road is **RED**), it should remain this way until a vehicle is detected on the Side Road, indicated by the sensors in the side road.
    - If a vehicle is detected on the Side Road the TLC should cycle the lights to give the Side Road the right-of-way (i.e. Main Road is **RED**, Side Road is **GREEN**)
    - The Side Road will have the right-of-way for only 20 seconds regardless of the presence of any additional vehicles on the Side Road. This delay is controlled by an external timer.
    - To prevent backups, the Main Road will never have the right-of-way for less-than 30 seconds, regardless of the presence of a vehicle on the Side Road. This delay is controlled by an external timer.
    - When the lights are cycling, the **YELLOW** light should be on for 8 seconds and the **RED** light should be on simultaneously for the last 2 seconds the yellow light is on.



2. Using VHDL, and targeting the Altera DE2 Board, design the multiple-output function implementation for the Clock Divide-by Controller. Your VHDL design should use LEDs to simulate the traffic light and display the time delay to the seven-segment display. If no time is delay is being timed then the seven-segment display should be blank.
3. Your design must use the 50MHz clock as it clock source.
4. You design should use less than 60 registers You will lose 2 point for every 10 extra registers your design has when design is signed off.
5. Submit your VHDL code and the generated state transition diagram to the dropbox in MyCourses prior to your lab section.

Procedure:

1. Using the testbench provided, simulate your design in Modelsim and obtain a signoff.
2. Download your design and verify operation. Obtain a signoff.

Documentation:

Submit a report that includes the following:

1. Abstract
2. State transition diagram
3. Finite state machine output table
4. Simulation Results
5. Compilation report

Lab 10

Signoffs

Name Cliff Chapman

1. **Simulation results** _____
2. **Working board** RJ 11/13/13