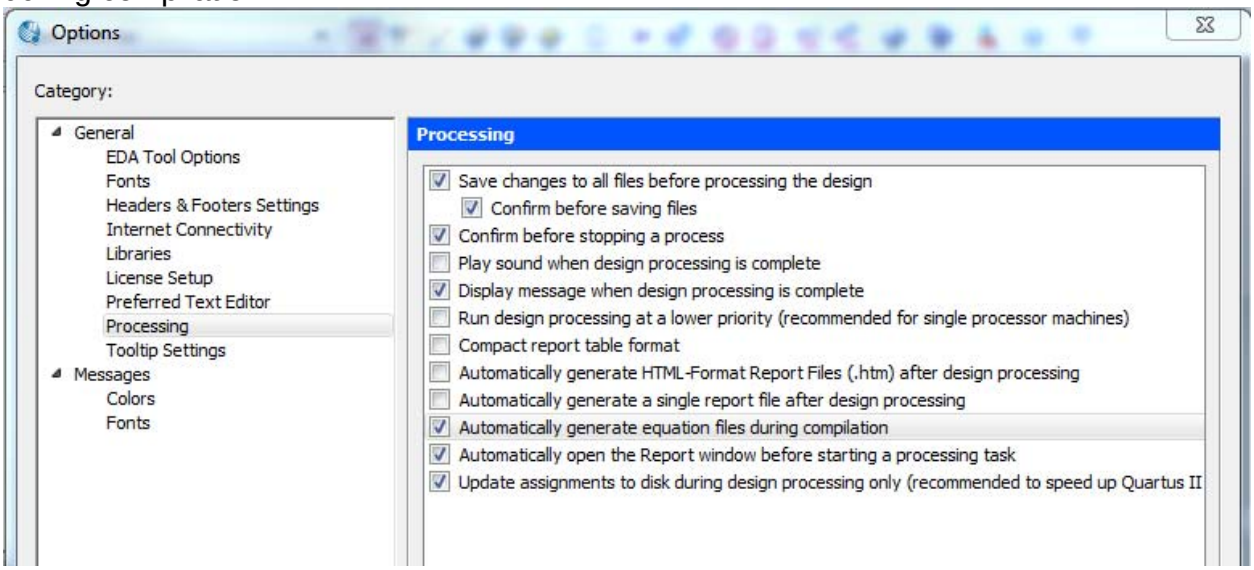
Technical Objective:

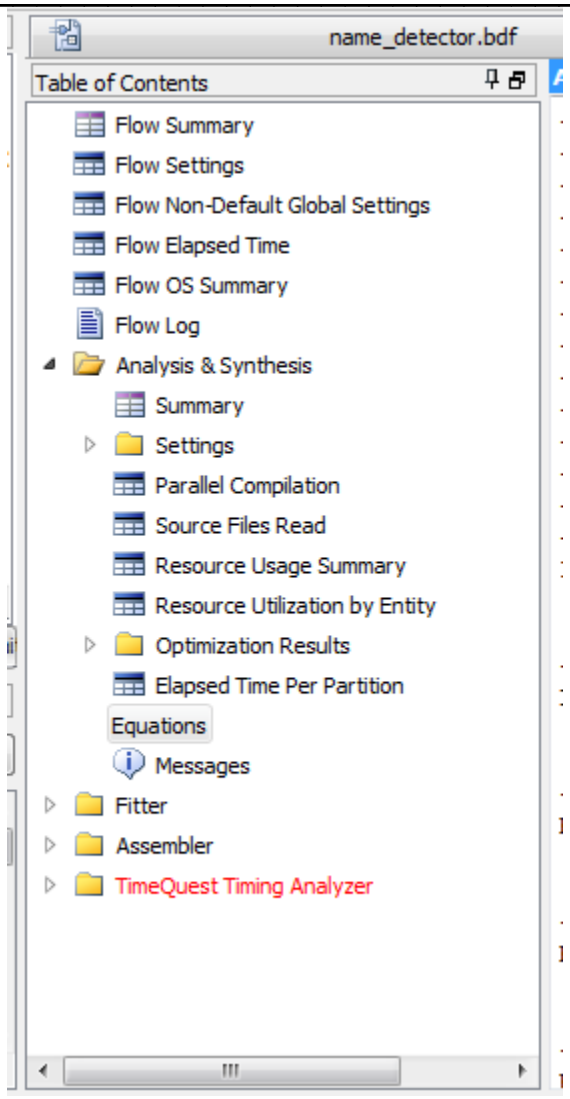
Today, programmable devices can be used to replace many SSI devices. The technical objective of this laboratory is to determine if an FPGA device can be used to implement combinational logic and replace SSI logic.

Pre-Laboratory: (20%)

1. Review lab 2 and open your Quartus II project. Choose tools > options and then click on Processing. Check the box entitled “Automatically generate equation files during compilation”



2. Compile the schematic. In the Table of Contents, click on Analysis & Synthesis and then Equations (see below). Examine the equations and save them to a word document.



3. Write the VHDL entity and architecture for the **Name Detector** that uses Conditional Signal Assignments (WHEN..ELSE). Name the outputs first_cond and last_cond.

4. Compile this implementation. Review the compilation errors and warnings and fix any problems.

5. Add two outputs to the entity. Name them first_case and last_case. Drive these outputs with an implementation for the **Name Detector** that uses Selected Signal Assignments (WITH, SELECT). This implementation should go in the same architecture as the conditional assignment.

6. Compile this implementation. Review the compilation errors and warnings and fix any problems.

7. Submit to the dropbox prior to lab:
    - Equations from step 1
    - Truth table with unsimplified equations for **first** and **last**
    - Final VHDL both implementations

Procedure: (60%)

1. Compile the VHDL version of the **Name Detector.**

2. Choose tools > Netlist Viewer > RTL Viewer of your design and examine the Quartus II generated schematic. Check the implementation equations for both VHDL implementations to see if they are the same. Compare the equations to those obtained in step 2 of the prelab.

3. Using the Altera U.P. simulator, test your design for all input combinations.

4. Assign pins, download your design and verify operation on DE2 board. If the circuit does not perform as expected, your implementation could be wrong. Troubleshoot the circuit and make any necessary changes. Obtain a signoff for the working board.

Documentation: (20%)

This will be a formal lab report that covers labs 2, 3 and 4. Your report must include the following:

- Abstract – objective, how the objective was met, summary of result
- Detailed discussion. This includes all pertinent design work
    - Truth tables, k-maps
    - Schematics
    - Vhdl code
    - Modelsim waveforms
    - Other data collected
- Discussion and conclusion section that includes, but is not limited to, a comparison all four implementations. What conclusion can you draw from this lab?

Name Cliff Chapman

Name Detector (VHDL)

Signoffs

1. **Simulation results** 9/18/13
2. **Working board** 9/18/13

*Make sure that the signoffs from lab 2 and lab 3 are included in your report.