

CPET-242 Digital Systems Design Fall 2013

Technical Objective:

This lab continues the investigation of designing "real-time" timers and counters in VHDL. In this lab, the concept of designing a mechanism to time an event will be created. The circuit to be developed is a reaction time game. A millisecond timer will be used to measure the amount of time it takes for the player to press a button after the appearance of an LED.

Pre-Laboratory: (20%)

- 1. Using VHDL, and targeting the Altera DE2 Board, create a VHDL circuit that acts as a reaction-timer. The circuit operates as follows:
 - The circuit is reset by pressing the pushbutton switch KEY0.
 - After an elapsed time, the red light labeled LEDR0 turns on and a four-digit BCD counter starts counting in intervals of milliseconds. The amount of time in seconds from when the circuit is reset until LEDR0 is turned on is set by switches SW7-0. (You can reuse your 1-second timer from lab 7).
 - A person whose reflexes are being tested must press the pushbutton KEY3 as quickly as possible to turn the LED off and freeze the counter in its present state.
 The count which shows the reaction time will be displayed on the 7-segment displays HEX3-0.
- 2. Your VHDL MUST adhere to the following guidelines:
 - a. ONLY 1 output per process. This means only one signal is assigned in the process. This is important so that processes can be re-used.
 - b. No integers types
 - c. No latch warnings
- 3. Submit your VHDL code to the dropbox prior to your lab section

Procedure: (60%)

- 1. Synthesize your design using Altera Quartus II.
- 2. Using the testbench provided on MyCourses, simulate your design in Modelsim. Note that it will take forever to simulate if your 1 second and 1 millisecond timers are included. The best way to get around this is to change the constant in the timers from its very large number to 10 (or less). Make print outs of simulation events of interest. Receive a signoff for the simulation.
- Change your one second constant back. Add pins to your design, compile and download to the DE2 board. Verify that your reaction timer works as expected. Obtain a signoff.



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Documentation: (20%) This is a formal lab report and should discuss labs 7 and 8. Be sure to include and discuss simulation waveforms (annotate comments on them), fully documented VHDL code and any other documentation useful in explaining what was done in the lab. Keep in mind that your target audience for the lab report is a person who has not read the lab handout. From your report they should be able to understand what the lab was about. Do not write the lab report with the instructor as your target audience.



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Name Class Chypnon Signoffs	
Reaction Timer	
1. Simulation results	
2. Working board	