Technical Objective:

The technical objective of this laboratory is to design a "real-time" clock using timers and counters in VHDL. In this lab, the concept of designing mechanism to keep track of time will be investigated. In a digital design, there are many applications that require a mechanism that is capable of tracking time. A timer and/or counter are useful for a variety of tasks where a timer or delay is required. In this lab special attention will be given to design partitioning the design into blocks or modules in VHDL.

Pre-Laboratory: (30%)

1. Using VHDL, and targeting the Altera DE2 Board, create a VHDL circuit that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays *HEX7-6*, the minute (from 0 to 59) on *HEX5-4* and the seconds (from 0 to 59) on *HEX3-2.* Use the switches *SW*15−0 to preset the hour and minute parts of the time displayed by the clock (the preset time will be entered in BCD via 16 switches). Use KEY1 'lock in' the time indicated by SW15-0. Use KEY0 to reset the entire system to 00:00:00.
2. Your VHDL **MUST** adhere to the following guidelines:
    a. ONLY 1 output per process. This means only one signal is assigned in the process. This is important so that processes can be re-used.
    b. No integers types
    c. No latch warnings
3. In order for your clock to only update once per second, a one second timer will need to be developed using the 50 MHZ clock (we covered this in class). How can you measure that this timer circuit to verify that it is one second? Propose a solution and include it with your prelab. Hint: you should use the o'scope.
4. Submit your VHDL code to the dropbox prior to your lab section

Procedure: (70%)

1. Synthesize your design using Altera Quartus II.

2. Using the testbench provided on MyCourses, simulate your design in Modelsim. Note that it will take forever to simulate if your 1 second timer is included. The best way to get around this is to change the constant in the timer from its very large number to 10. That way your time-of-day clock will increment every 10 clock cycles. Make print outs of several locations where each of the seconds, minutes and hours roll over. Capture the rollover from 23:59:59 to 00:00:00. Receive a signoff for the simulation.

3. Change your one second constant back. Add pins to your design, compile and download to the DE2 board. Verify that your clock works as expected. Obtain a signoff.

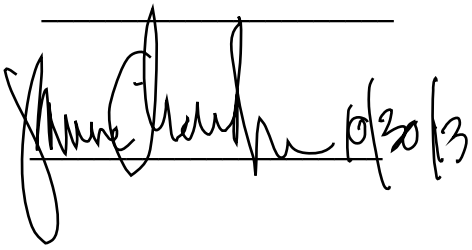
4. Include circuitry that will allow you to check the accuracy of your one second timer and verify it on the oscilloscope. Also verify that the clock still works. Obtain a signoff. You will have to take a picture of the o'scope screen for your report.

Documentation: There is no documentation for this lab. Save everything for lab #8 report.

Signoffs

Time of Day Clock

1. **Simulation results** _____

2. **Working board**  10/30/13

3. **Oscilloscope results** _____