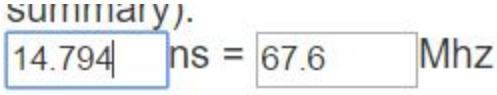
The total number of bytes required to store both Euclid's algorithm and relPrime as well as any memory variables or constants. 0x89->2*137=274

The total number instructions executed when relPrime is called with 0x13B0 (the result should be 0x000B using the algorithm specified in the project specifications). 316509

The total number of cycles required to execute `relPrime under the same conditions as Step 2. 949662

The average cycles per instruction based on the data collected in Steps 2 and 3. 949662/316509=3.0004265

The cycle time for your design (from the Xilinx Synthesis report – look for the Timing summary). 14.794ns



The total execution time for relPrime under the same conditions as Step 2. 15.194744ms

The gate count for your entire design (from the Xilinx Map report). This appears to have changed/is omitted in recent version. Extra credit for any group that finds a reasonable way to estimate the equivalent gate count from the data in the Xilinx reports.
About 1800. See video to show the video to show how we count.

The device utilization summary (from the Xilinx Synthesis report).

Device utilization summary:

Selected Device : 3sd1800afg676-4

Number of Slices:	398 out of 16640	2%	
Number of Slice Flip Flops:	374 out of 33280	1%	
Number of 4 input LUTs:	796 out of 33280	2%	
Number of IOs:	147		
Number of bonded IOBs:	147 out of 519	28%	
Number of BRAMs:	1 out of 84	1%	
Number of GCLKs:	1 out of 24	4%	