**Journal:**

**Group 2D**

**Milestone 1** Meeting Sunday, October 1, 2017

Location: F217

Agenda:

* General design idea of the our assembly code

Work Done:

* Have a general design of our assembly code

Our design for assembly code: We decided to build a 16-bit accumulator and load-store based processor. We chose this design since it has nice structure and can take advantage of both load-store and accumulator design. Then, we decided to include 4 accumulators in our design for data storing and few other registers: $0, $ra, and $sp, etc.

**Milestone 1** Meeting Monday, October2, 2017

Location: F217

Agenda:

* Write assembly code for relprime
* Write machine code for relprime
* Improve our design

Work Done:

* Write assembly code for relprime
* Write machine code for relprime
* Add lra, sra and ja to our design

Work for the week:

Decide design we are going to use, decide call conventions and instructions we are going to use, write down description of the instructions, develop rules for translating assembly language instructions to machine language estimated 1 day. [All group members, done in 1].

Write assembly code and machine code for relprime and Euclid’s algorithm. [All group members, done in 2].

**Milestone2** Meeting Thursday, October 5, 2017

Location: CS Labs F217

Agenda:

* Redesign instruction set
* Redesign method call procedure
* Redesign registers

Work done

* Need to talk to Micah during 7th hour tomorrow(~12:30)
* Got instruction type, registers, and instructions set in stone

Work to be done for next time

* Finish revising design doc
* Redo euclids
* M2

We chose to change our design to a mix of accumulator and load-store. This allows for short instructions and all the functionality that we need.

**Milestone2** Meeting Sunday, October 8, 2017

Location: CS Lab F225

Agenda:

* Start RTL
* Fix any remaining stuff from bad design document

Work Done

* Constructed most of the RTL
* Started to find groupings of instructions based on the RTL

We wrote out the full RTL for each instruction individually, then we began to group together sections that were common among instructions.

Built the most of the RTL[Caleb and Brian, done in 2], revise the test code of milestone 1 with new instructions [Kevin and Anderson, done in 2], type everything to doc and transfer the assembly code to machine code [Kaiyu, done in 1]

**Milestone2** Meeting Monday, October 9, 2017

Location: CS Lab F225

Time: 4pm

Agenda:

* Finish grouping RTL
* Record RTL in design doc
* Record parts/controls in design doc
* Make RTL tests

Work Done:

* RTL groupings all found
* RTL recorded in design doc

We finished the groupings of RTL instructions and broke it down into eight categories. We chose to test our RTL by having group members that didn’t design the RTL write some assembly code and translate it out into our RTL to see if they thought it made sense.

Finish all the RTLs and group them together, describe all the RTL in English and in a chart [Caleb and Brian, done in 2], write a piece of code in assembly and manually run them with the RTL instructions to test it [Kevin and Anderson, done in 2] check and revise all the codes and type codes to the doc [Kaiyu, done in 1]

Write Assembler and start documenting pseudo instructions [Caleb, assign for over fall break]

**Milestone 3** Meeting Monday 10/16/17

Location: CSSE Lab F225

Time: 8pm

Agenda:

* Complete or nearly complete M3
* Fix any problems still unfixed from M2
* Caleb - continue working on assembler

Work Done:

* Completed prototype datapath
* Assembler almost working theoretically
* Design Document flaws from M2 fixed

**Milestone 3** Meeting Tuesday 10/17/17

Location: O259

Time: Classtime

Agenda:

* Ask Micah questions
* Figure out plan for rest of M3

Work Done:

* Asked Micah questions

Work Assigned:

Write about datapath tests[Yuankai and Kaiyu, one day]

Revise component list[Caleb, one day]

**Milestone 3** Meeting Tuesday 10/17/17

Location: CS Lab F225

Time: 4pm

Agenda:

* Draw digital datapath
* Finish datapath tests

Work Done:

* Write about datapath tests

**Milestone 3** Meeting Wednesday 10/18/17

Location: O259

Time: Classtime

Agenda

* Write a table about each control signal in the design doc
* Update this journal with questions from milestone
* Finish digital datapath

Work Done:

* Draw datapath
* Complete table on control signals
* Updated journal to include design and testing decisions

Strategy for creating tests:

We first test every single component. We did an exhaustive test for every possible inputs.

Then we test each instructions. For this one, we just test some main values and edge cases, because there are so many possibilities. We test from the easiest that only need two or three components to the more complicated ones.

Finally we use the test we wrote for RTL test to run it. If possible, we will use all the possible instruction inputs, which is from 0000 0000 0000 0000 to 1111 1111 1111 1111.

Errors during testing:

For addings, we are possible to meet an overflow. We may also jump to an invalid memory address. During branch or jump we may go to an address that is out of range. We think we need to throw exception at these cases.

Choice in architecture affected your datapath design and component specification:

We need to have a large mux at the data write, because we almost need to throw everything into the accumulator and work on that. We went about designing the whole processor by going cycle by cycle, starting with the two cycles shared amongst all the instructions. We then when across all the instructions and added to the datapath in order to facilitate for each instruction. We found that some instructions use very similar paths and some required a lot of separate work.

**Milestone 4** Meeting: Monday 10/23/17

Location: O259

Time: Classtime

Agenda:

* Fix mistakes from last milestone
* Start on control state diagram
* Delegate tasks so that we don’t have to all be in one place to work

Work Done

* Fixed Parts list and RTL table
* Started on Control Diagram
* Started on Control descriptions
* Started on fixing integration plan from last week

**Milestone 4** Meeting: Monday 10/23/17

Location F225

Time: 6:40

Agenda

* Wrap up integration plan
* Finish changing control diagram due to change with order stuff

Work Done:

* Build most of the components, including all muxes and constants, 4 bit ze to 16 bit, 8 bit ze to 16 bit, 8 bit se to 16 bit, 16 bit register, 16 bit comparator(Anderson), register File (Brian), ALU(Kevin)

**Milestone 4** Meeting: Tuesday 10/24/17

Location: F225

Time: 9:30

Agenda

* Finish control tests
* Work on parts

Work Done

* Design doc changes for M4 finished
* Parts worked on(some to completion)

Assembler having linker built in

During this milestone creating the control, our design process was as follows. We took each cycle from the RTL and drew out what it corresponded to in the datapath. We then set the control signals needed for the processor to take that path. We did this for each possible cycle to come up with our final finite state machine.

**Milestone 5** Meeting:Monday 10/30/17

Location: O259

Time: Class time

Agenda

* Finish control tests
* Fix design document
* Work on assembling Datapath

Work Done

* Parts continued to update
* Document updated

**Milestone 5** Meeting Monday 10/30/17

Location: F225

Time: 6:00

Agenda

* Finish fixing mistakes from previous milestone in design doc
* Finish up last components
* Continue putting data path together

Work Done

* Fixed all mistakes from past milestone
* Finished almost all parts
* Datapath has all parts that are finished

Meeting Tuesday, 10/31/17

Location: F225

Time: 6pm

Agenda

* Continue updating data path
* Finish remaining components
* Add information regarding datapath and tests to design doc

Work Done

* Finished Register File and comparator
* Adding more parts to datapath
* Started and Finished Control Unit

Meeting Wednesday, 11/1/17

Location: F225

Time: 1pm

Agenda

* Finish data path
* Finish remaining components
* Finish integration test
* Finish system test

Work Done

* Finish data path
* Finish remaining components
* Finish integration test

Meeting Monday, 11/6/2017

Location: Class

Time: 9:55am

Agenda

* Fixing synthesis bugs

Work Done

* Fixed most synthesis bugs

Meeting Monday, 11/6/2017

Location: F225

Time: 6pm

Agenda

* Fix remaining synthesis problems
* Try to locate synthesis report

Work Done

* Fixed remain synthesis problems
* Could not locate synthesis reports

Meeting Tuesday, 11/7/2017

Location: F225

Time: 6pm

Agenda

* Get instructions to go through data path
* Add I/O
* Fix bugs in assembler

Work Done

* Got some instructions to go through data path with correct values
* Edited Euclid's Algorithm
* Added I/O to prepare to put on board
* Found small bugs in the assembler
* After bugs fixed in assembler, ready to implement Euclid’s.

Meeting Wednesday, 11/8/2017

Location: Class

Time: 9:55

Agenda

* Fix bugs in Assembler associated with addi
* Fix old Eculid’s algorithms
* Update full datapath test plan with some small test cases used

Work Done

* Fixed old Eculid’s algorithms
* Finished modifying assembler
* Update full datapath test plan

Meeting Wednesday, 11/8/2017

Location: F225

Time: 1pm

Agenda

* Run Euclid’s algorithm

Work Done

* Fixed some bugs in the datapath

Meeting Thursday 11/9/2017

Location: F225

Time: 1am

Agenda

* Run Euclid’s algorithm

Work Done

* Fixed bugs in the assembler about the location of labels
* Fixed bugs in assembly code about the sub instruction

Meeting Thursday 11/9/2017

Location: F225

Time: 10am

Agenda

* Add invert to the memory clock cycle

Work Done

* Successfully run Euclid’s algorithm

Meeting Saturday 11/11/2017

Location: F225

Time: 3pm

Agenda

* Finish M6
* Work on the final report and final presentation

Work Done

* Finished M6

Meeting Sunday 11/12/2017

Location: F225

Time: 3pm

Agenda

* Keep working on the final report and final presentation
* Fix the problems existed in previous design document

Work Done

* Finished Final report and final presentation
* Finished design document