ANDI (I type)

RegDst: 0   opcode: 12

Jump: 0

Branch: 0

MemtoRead: X

Memto Reg: 0

ALUOp: 11 (output: 000 - and)

MemWrite: 0

ALUsrc: 1

Regwrite: 1

Link: 0

Link_r: 0

Reg_31: 0

Reg-31_r: 0

b-invert: X

balv: 0

jump_mem: 0

jmp_mem: 0

SRLV (R type)

RegDst: 1   funct = 6

Jump: 0

Branch: 0

MemtoRead: X

Memto Reg: 0

ALUOp: 10 (output: 100 (shift))

MemWrite: 0

ALUsic: 0

RegWrite: 1

Link: 0

Link_r: 0

Reg_31: 0

Reg_31_r: 0

b-invert: X

balv: 0

jump_mem: 0

jmp_mem: 0

BNEAL (I type)   Opcode: 45

Reg Dst: X
Jump: 0
Branch: 1
Mem to Read: X
Mem to Reg: X
ALU Op: 01
MemWrite: 0
ALUsrc: 0
RegWrite: 1
Link: 1
Link-r: 0
Reg 31: 1
Reg-31-r: 0
b-invert: 1
balv: 0
jump-mem: 0
jmor-mem: 0

BALV (j type)   opcode: 33

Reg Dst: X
Jump: 0
Branch: 1
Mem to Read: X
Mem to Reg: X
ALUOp: XX
MemWrite: 0
ALUsrc: X
RegWrite: 1
Link: 1
Link_r: 0
Reg-31: 1
Reg-31-r: 1
b-invert: X
balv: 1
jump-mem: 0
jmor-mem: 0

JMOR (R type)

Funct: 37

Reg Dst: X
Jump: X
Branch: X
MemtoRead: 1
MemtoReg: 1 [Memto Reg R'larda 0]
ALU Op: 10 (output: 001-OR)
MemWrite: 0
ALUsrc: 0
RegWrite: 1
Link: 0
Link-r: 1
Reg-31: 0
Reg-31_r: 1
b-invert: X
balv: 0
jump_mem: 1
jmor-mem: 1

ALUOP = 10
sa ve FUNC=37
ise onalmem

JALR (R type)

Funct: 9

Reg Dst: 1
Jump: X
Branch: X
MemtoRead: X
MemtoReg: 0
ALUOp: 10 (output: 011)
MemWrite: 0
ALUsrc: X
Regwrite: 1
Link: 0
Link_r: 1
Reg-31: 0
Reg-31_r: 0
b-invert: X
balv: 0
jump_mem: 1
jmor_mem: 0