First Example
Keypad Seen on Leds

```
module keypad_ex (
                                                output reg [3:0] rowwrite,
                                                input [3:0] colread,
                                                input clk,
                                                output reg [3:0] data
                                                );

reg [25:0] clk1;
reg [3:0] keyread;
reg rowpressed;

always @(posedge clk)
                clk1<=clk1+1;

always @(posedge clk1[18])
                rowwrite <= {rowwrite[2:0], rowwrite[3]};

always @(*)
                if(rowwrite == 4'b1110 && colread == 4'b1110)
                        begin
                                keyread = 4'h1;
                                rowpressed = 1'b1;
                        end
                else if(rowwrite == 4'b1110 && colread == 4'b1101)
                        begin
                                keyread = 4'h2;
                                rowpressed = 1'b1;
                        end
                else if(rowwrite == 4'b1110 && colread == 4'b1011)
                        begin
                                keyread = 4'h3;
                                rowpressed = 1'b1;
                        end
                else if(rowwrite == 4'b1110 && colread == 4'b0111)
                        begin
                                keyread = 4'ha;
                                rowpressed = 1'b1;
                        end
                else if(rowwrite == 4'b1101 && colread == 4'b1110)
                        begin
                                keyread = 4'h4;
                                rowpressed = 1'b1;
                        end
                else if(rowwrite == 4'b1101 && colread == 4'b1101)
                        begin
                                keyread = 4'h5;
                                rowpressed = 1'b1;
                        end
```

```
else if(rowwrite == 4'b1101 && colread == 4'b1011)
	begin
		keyread = 4'h6;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b1101 && colread == 4'b0111)
	begin
		keyread = 4'hb;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b1011 && colread == 4'b1110)
	begin
		keyread = 4'h7;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b1011 && colread == 4'b1101)
	begin
		keyread = 4'h8;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b1011 && colread == 4'b1011)
	begin
		keyread = 4'h9;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b1011 && colread == 4'b0111)
	begin
		keyread = 4'hc;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b0111 && colread == 4'b1110)
	begin
		keyread = 4'he;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b0111 && colread == 4'b1101)
	begin
		keyread = 4'h0;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b0111 && colread == 4'b1011)
	begin
		keyread = 4'hf;
		rowpressed = 1'b1;
	end
else if(rowwrite == 4'b0111 && colread == 4'b0111)
	begin
		keyread = 4'hd;
		rowpressed = 1'b1;
	end
else
	begin
```

```
                        keyread = 4'hf;
                        rowpressed = 1'b0;
                end


always @(posedge clk1[18])
        if (rowpressed==1)
                data<=keyread;


initial
        begin
                rowwrite=4'b1110;
        end

endmodule
```

Example 2:
Keypad seen on one of the 7 segment Unit

```
module ssegkey (  output wire [3:0] rowwrite,
                                                input [3:0] colread,
                                                input clk,
                                                output wire [3:0] data,

                                                output wire [3:0] grounds,
                                                output wire [6:0] display
                                        );

reg [15:0] data_all;

reg [25:0] clk1;

always @(posedge clk)
        clk1<=clk1+1;

always @(posedge clk1[20])
        data_all<={data_all[15:4],data};

sevensegment ss1 (.datain(data_all), .grounds(grounds), .display(display), .clk(clk));

keypad_ex  kp1(.rowwrite(rowwrite),.colread(colread),.clk(clk), .data_out(data));

initial
data_all=0;

endmodule


module sevensegment(datain, grounds, display, clk);

        input wire [15:0] datain;
        output reg [3:0] grounds;
        output reg [6:0] display;
        input clk;

        reg [3:0] data [3:0];
        reg [1:0] count;
        reg [25:0] clk1;

        always @(posedge clk1[15])
                begin
                        grounds <= {grounds[2:0],grounds[3]};
                        count <= count + 1;
                end

        always @(posedge clk)
                clk1 <= clk1 + 1;
```

```
	always @(*)
		case(data[count])
0:display=7'b1111110; //starts with a, ends with g
1:display=7'b0110000;
2:display=7'b1101101;
3:display=7'b1111001;
4:display=7'b0110011;
5:display=7'b1011011;
6:display=7'b1011111;
7:display=7'b1110000;
8:display=7'b1111111;
9:display=7'b1111011;
'ha:display=7'b1110111;
'hb:display=7'b0011111;
'hc:display=7'b1001110;
'hd:display=7'b0111101;
'he:display=7'b1001111;
'hf:display=7'b1000111;
default display=7'b1111111;
		endcase

	always @*
		begin
			data[0] = datain[15:12];
			data[1] = datain[11:8];
			data[2] = datain[7:4];
			data[3] = datain[3:0];
		end

	initial begin
		count = 2'b0;
		grounds = 4'b1110;
		clk1 = 0;
	end
endmodule



module keypad_ex (
                                                output reg [3:0] rowwrite,
                                                input [3:0] colread,
                                                input clk,
                                                output reg [3:0] data_out
                                                );

reg [25:0] clk1;
reg [3:0] keyread;
reg rowpressed;

always @(posedge clk)
		clk1<=clk1+1;
```

```
always @(posedge clk1[20])
		rowwrite <= {rowwrite[2:0], rowwrite[3]};

always @(*)
		if(rowwrite == 4'b1110 && colread == 4'b1110)
			begin
				keyread = 4'h1;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1110 && colread == 4'b1101)
			begin
				keyread = 4'h2;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1110 && colread == 4'b1011)
			begin
				keyread = 4'h3;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1110 && colread == 4'b0111)
			begin
				keyread = 4'ha;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b1110)
			begin
				keyread = 4'h4;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b1101)
			begin
				keyread = 4'h5;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b1011)
			begin
				keyread = 4'h6;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b0111)
			begin
				keyread = 4'hb;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1011 && colread == 4'b1110)
			begin
				keyread = 4'h7;
				rowpressed = 1'b1;
			end
		else if(rowwrite == 4'b1011 && colread == 4'b1101)
			begin
				keyread = 4'h8;
```

```
                        rowpressed = 1'b1;
                end
        else if(rowwrite == 4'b1011 && colread == 4'b1011)
                begin
                        keyread = 4'h9;
                        rowpressed = 1'b1;
                end
        else if(rowwrite == 4'b1011 && colread == 4'b0111)
                begin
                        keyread = 4'hc;
                        rowpressed = 1'b1;
                end
        else if(rowwrite == 4'b0111 && colread == 4'b1110)
                begin
                        keyread = 4'he;
                        rowpressed = 1'b1;
                end
        else if(rowwrite == 4'b0111 && colread == 4'b1101)
                begin
                        keyread = 4'h0;
                        rowpressed = 1'b1;
                end
        else if(rowwrite == 4'b0111 && colread == 4'b1011)
                begin
                        keyread = 4'hf;
                        rowpressed = 1'b1;
                end
        else if(rowwrite == 4'b0111 && colread == 4'b0111)
                begin
                        keyread = 4'hd;
                        rowpressed = 1'b1;
                end
        else
                begin
                        keyread = 4'hf;
                        rowpressed = 1'b0;
                end


always @(posedge clk1[20])
        if (rowpressed==1)
                begin
                        data_out<=keyread;
                end

initial
        begin
                rowwrite=4'b1110;
        end

endmodule
```

Example 3:
Pressed keys are shifted and seen on 7 segment

```
module ssegkey (  output wire [3:0] rowwrite,
                                                input [3:0] colread,
                                                input clk,
                                                output wire [3:0] data,

                                                output wire [3:0] grounds,
                                                output wire [6:0] display
                                        );

reg [15:0] data_all;

reg [25:0] clk1;

always @(posedge clk)
        clk1<=clk1+1;

always @(posedge clk1[20])
        data_all<=data;

sevensegment ss1 (.datain(data_all), .grounds(grounds), .display(display), .clk(clk));

keypad_ex  kp1(.rowwrite(rowwrite),.colread(colread),.clk(clk), .data_out(data));

initial
data_all=0;

endmodule


module sevensegment(datain, grounds, display, clk);

        input wire [15:0] datain;
        output reg [3:0] grounds;
        output reg [6:0] display;
        input clk;

        reg [3:0] data [3:0];
        reg [1:0] count;
        reg [25:0] clk1;

        always @(posedge clk1[15])
                begin
                        grounds <= {grounds[2:0],grounds[3]};
                        count <= count + 1;
                end

        always @(posedge clk)
                clk1 <= clk1 + 1;
```

```
	always @(*)
		case(data[count])
0:display=7'b1111110; //starts with a, ends with g
1:display=7'b0110000;
2:display=7'b1101101;
3:display=7'b1111001;
4:display=7'b0110011;
5:display=7'b1011011;
6:display=7'b1011111;
7:display=7'b1110000;
8:display=7'b1111111;
9:display=7'b1111011;
'ha:display=7'b1110111;
'hb:display=7'b0011111;
'hc:display=7'b1001110;
'hd:display=7'b0111101;
'he:display=7'b1001111;
'hf:display=7'b1000111;
default display=7'b1111111;
		endcase

	always @*
		begin
			data[0] = datain[15:12];
			data[1] = datain[11:8];
			data[2] = datain[7:4];
			data[3] = datain[3:0];
		end

	initial begin
		count = 2'b0;
		grounds = 4'b1110;
		clk1 = 0;
	end
endmodule



module keypad_ex (
                                                output reg [3:0] rowwrite,
                                                input [3:0] colread,
                                                input clk,
                                                output reg [15:0] data_out
                                                );

reg [25:0] clk1;
reg [3:0] keyread;
reg rowpressed;
reg [15:0] addkey;

reg state;
```

```
always @(posedge clk)
		clk1<=clk1+1;

always @(posedge clk1[20])
		rowwrite <= {rowwrite[2:0], rowwrite[3]};

always @(posedge clk1[20])
	case (state)
	1'b0:
		if(rowwrite == 4'b1110 && colread == 4'b1110)
			begin
				keyread = 4'h1;
				rowpressed = 1'b1;
				state<=1;
			end
		else if(rowwrite == 4'b1110 && colread == 4'b1101)
			begin
				keyread = 4'h2;
				rowpressed = 1'b1;
				state<=1;
			end
		else if(rowwrite == 4'b1110 && colread == 4'b1011)
			begin
				keyread = 4'h3;
				rowpressed = 1'b1;
				state<=1;
			end
		else if(rowwrite == 4'b1110 && colread == 4'b0111)
			begin
				keyread = 4'ha;
				rowpressed = 1'b1;
				state<=1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b1110)
			begin
				keyread = 4'h4;
				rowpressed = 1'b1;
				state<=1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b1101)
			begin
				keyread = 4'h5;
				rowpressed = 1'b1;
				state<=1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b1011)
			begin
				keyread = 4'h6;
				rowpressed = 1'b1;
				state<=1;
			end
		else if(rowwrite == 4'b1101 && colread == 4'b0111)
```

```
		begin
			keyread = 4'hb;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b1011 && colread == 4'b1110)
		begin
			keyread = 4'h7;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b1011 && colread == 4'b1101)
		begin
			keyread = 4'h8;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b1011 && colread == 4'b1011)
		begin
			keyread = 4'h9;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b1011 && colread == 4'b0111)
		begin
			keyread = 4'hc;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b0111 && colread == 4'b1110)
		begin
			keyread = 4'he;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b0111 && colread == 4'b1101)
		begin
			keyread = 4'h0;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b0111 && colread == 4'b1011)
		begin
			keyread = 4'hf;
			rowpressed = 1'b1;
			state<=1;
		end
	else if(rowwrite == 4'b0111 && colread == 4'b0111)
		begin
			keyread = 4'hd;
			rowpressed = 1'b1;
			state<=1;
```

```
                end
        else
                begin
                        //keyread = 4'hf;
                        rowpressed = 1'b0;
                        state<=1;
                end
    1'b1:
        begin
                if (colread==4'b1111)
                begin
                state<=0;
                rowpressed<=0;
                end
        end
    endcase
always @(posedge clk1[20])
    if (rowpressed==1)
        begin
                data_out<=(data_out<<4)+keyread;
        end

initial
    begin
        rowwrite=4'b1110;
        state=0;
    end

endmodule
```