Project Exam #1

Objective:

You are provided with a Verilog-based ALU module (alu.v) including other module instances, its accompanying testbench, and related submodules. Your task is to analyze the simulation results, identify errors, locate and fix the bugs in the Verilog code, and document your corrections systematically.

Steps:

1. **Set Up the Project**
    a. Open **Quartus** and create a new project.
    b. Add all the provided Verilog files (e.g., alu.v, testbench, and submodules) to the project.
    c. Designate alu.v as the **Top Module**.
2. **Run Simulation**
    a. Set up and run a functional simulation using the testbench provided.
    b. Observe the output waveforms or logs generated during the simulation.
3. **Analyze the Results**
    a. Identify which function(s) are producing incorrect results.
    b. Record the names of the problematic function(s) of the ALU and describe the specific incorrect outputs.
4. **Locate and Correct the Errors**
    a. Inspect the Verilog code of the identified module(s).
    b. Determine the cause of the incorrect behavior.
    c. Make the necessary corrections to ensure the module functions correctly.
5. **Document Your Fixes**
    a. List each change made in the Verilog code.
    b. Include a brief explanation for each change, describing why it was necessary.
6. **Re-validate the Simulation**
    a. Re-run the simulation after applying the corrections.
    b. Confirm that all outputs are now accurate and consistent with the expected results.

Submission Instructions:

1. **Provide Detailed Answers to the Following Questions:**
    a. Which function(s) produced incorrect results in the simulation? (20 pts)
    b. What are the correct results for those outputs? (20 pts)
    c. What errors did you identify in the Verilog code? (20 pts)
    d. What corrections did you make? List them clearly, line by line, and include explanations. (30 pts)
    e. After correcting the Verilog code, rerun the simulation and take a screenshot of the resulting output. (10 pts)
2. **Upload Your Work:**
    a. Write your answers clearly and neatly in a text document. Save the file as *"Detailed Answers.txt"* and place it in your project folder.
    b. Ensure your project folder includes all required files, such as:
        - *"Detailed Answers.txt"*
        - *Corrected simulation screenshot*
        - Corrected Verilog files (e.g., `alu.v`, etc.)

    Upload the complete project folder.