1. 地址映射

   根据连接方式，可以确定地址映射为0x0010 0000 到 0x0017 FFFF。

2. 在程序Example_2833xDMA_xintf_to_ram.c指出相关的配置代码。指出XTIMING6、XINTCNF2寄存器各字段的数值及含义。

   该程序中与xintf相关的配置代码如下：

```
// Configure the timing parameters for Zone 6.
// Notes:
//    This function should not be executed from XINTF
//    Adjust the timing based on the data manual and
//    external device requirements.
void init_zone6(void)
{
    // Make sure the XINTF clock is enabled
    SysCtrlRegs.PCLKCR3.bit.XINTFENCLK = 1;

    // Configure the GPIO for XINTF with a 16-bit data bus
    // This function is in DSP2833x_Xintf.c
    InitXintf16Gpio();
    EALLOW;
    // All Zones---------------------------------
    // Timing for all zones based on XTIMCLK = SYSCLKOUT
    XintfRegs.XINTCNF2.bit.XTIMCLK = 0;
    // Buffer up to 3 writes
    XintfRegs.XINTCNF2.bit.WRBUFF = 3;
    // XCLKOUT is enabled
    XintfRegs.XINTCNF2.bit.CLKOFF = 0;
    // XCLKOUT = XTIMCLK
    XintfRegs.XINTCNF2.bit.CLKMODE = 0;
    // Disable XHOLD to prevent XINTF bus from going into high impedance state
    // whenever TZ3 signal goes low. This occurs because TZ3 on GPIO14 is
    // shared with HOLD of XINTF
    XintfRegs.XINTCNF2.bit.HOLD = 1;

    // Zone 6------------------------------------
    // When using ready, ACTIVE must be 1 or greater
    // Lead must always be 1 or greater
    // Zone write timing
    XintfRegs.XTIMING6.bit.XWRLEAD = 1;
    XintfRegs.XTIMING6.bit.XWRACTIVE = 2;
    XintfRegs.XTIMING6.bit.XWRTRAIL = 1;
    // Zone read timing
    XintfRegs.XTIMING6.bit.XRDLEAD = 1;
    XintfRegs.XTIMING6.bit.XRDACTIVE = 3;
    XintfRegs.XTIMING6.bit.XRDTRAIL = 0;

    // don't double all Zone read/write lead/active/trail timing
    XintfRegs.XTIMING6.bit.X2TIMING = 0;
```

```
    // Zone will not sample XREADY signal
    XintfRegs.XTIMING6.bit.USEREADY = 0;
    XintfRegs.XTIMING6.bit.READYMODE = 0;

    // 1,1 = x16 data bus
    // 0,1 = x32 data bus
    // other values are reserved
    XintfRegs.XTIMING6.bit.XSIZE = 3;
    EDIS;

   //Force a pipeline flush to ensure that the write to
   //the last register configured occurs before returning.
   __asm(" RPT #7 || NOP");
}
```

XTIMING6和XINTCNF2寄存器各字段的数值及含义如下：

XTIMING6：

```
// Zone 6------------------------------------
// When using ready, ACTIVE must be 1 or greater
// Lead must always be 1 or greater
// Zone write timing
XintfRegs.XTIMING6.bit.XWRLEAD = 1;
XintfRegs.XTIMING6.bit.XWRACTIVE = 2;
XintfRegs.XTIMING6.bit.XWRTRAIL = 1;
// Zone read timing
XintfRegs.XTIMING6.bit.XRDLEAD = 1;
XintfRegs.XTIMING6.bit.XRDACTIVE = 3;
XintfRegs.XTIMING6.bit.XRDTRAIL = 0;

// don't double all Zone read/write lead/active/trail timing
XintfRegs.XTIMING6.bit.X2TIMING = 0;

// Zone will not sample XREADY signal
XintfRegs.XTIMING6.bit.USEREADY = 0;
XintfRegs.XTIMING6.bit.READYMODE = 0;

// 1,1 = x16 data bus
// 0,1 = x32 data bus
// other values are reserved
XintfRegs.XTIMING6.bit.XSIZE = 3;
EDIS;
```

字段	数值	含义
XWRLEAD	1	写访问前导期为一个XTIMCLK周期
XWRACTIVE	2	写访问活动期为两个XTIMCLK周期

字段	数值	含义
XWRTRAIL	1	写访问尾部期为一个XTIMCLK周期
XRDLEAD	1	读访问前导期为一个XTIMCLK周期
XRDACTIVE	3	读访问活动期为三个XTIMCLK周期
XRDTRAIL	0	读访问尾部期为0
X2TIMING	0	值按 1:1 比例缩放
USEREADY	0	当访问该区域时，XREADY 信号将被忽略。
READYMODE	0	XREADY输入对于区域是同步的。
XSIZE	3	在这种模式下，区域将只使用16条数据线，XA0/WE1信号将表现为 XA0

XINTCNF2：

```
    // All Zones---------------------------------
        // Timing for all zones based on XTIMCLK = SYSCLKOUT
        XintfRegs.XINTCNF2.bit.XTIMCLK = 0;
        // Buffer up to 3 writes
        XintfRegs.XINTCNF2.bit.WRBUFF = 3;
        // XCLKOUT is enabled
        XintfRegs.XINTCNF2.bit.CLKOFF = 0;
        // XCLKOUT = XTIMCLK
        XintfRegs.XINTCNF2.bit.CLKMODE = 0;
        // Disable XHOLD to prevent XINTF bus from going into high impedance state
        // whenever TZ3 signal goes low. This occurs because TZ3 on GPIO14 is
        // shared with HOLD of XINTF
        XintfRegs.XINTCNF2.bit.HOLD = 1;
```

字段	数值	含义
XTIMCLK	0	XTIMCLK = SYSCLKOUT
WRBUFF	3	缓冲区最多可写3次
CLKOFF	0	已启用 XCLKOUT
CLKMODE	0	XCLKOUT = XTIMCLK

3. 根据存储器的读写时序（参数取值用表中-12一栏），能否优化DSP的XINTF配置？给出具体配置方案。

根据IS61LV12816存储器的读写时序，可得以下时序参数：

- TWC：写脉冲宽度，最小值为-12ns
- TRC：读脉冲宽度，最小值为-12ns

- TAA：读写地址到读写数据有效时间，最小值为-12ns
- TCE：读写地址到CE#变高时间，最小值为-12ns

可以看出，IS61LV12816存储器的时序参数与DSP的XINTF默认配置不完全匹配。在默认情况下，DSP的XINTF配置为XCLKOUT = SYSCLKOUT/2，即XINTF时钟频率为SYSCLKOUT/2，而IS61LV12816的最小TWC/TRC/TAA/TCE参数均为-12ns，这意味着存储器可以处理更高的时钟频率。因此，可以优化DSP的XINTF配置，提高时钟频率以减少存储器读写时的等待时间，从而提高系统的性能。

调整写时序参数，使其比IS61LV12816的最小值略大，以确保稳定性。

```
XintfRegs.XTIMING7.bit.XWRLEAD = 1;
XintfRegs.XTIMING7.bit.XWRACTIVE = 2;
XintfRegs.XTIMING7.bit.XWRTRAIL = 2;
```

调整读时序参数，使其比IS61LV12816的最小值略大，以确保稳定性。

```
XintfRegs.XTIMING7.bit.XRDLEAD = 1;
XintfRegs.XTIMING7.bit.XRDACTIVE = 3;
XintfRegs.XTIMING7.bit.XRDTRAIL = 2;
```

经过上述优化配置后，可以提高DSP与IS61LV12816存储器之间的数据传输速度，从而提高系统的性能。