designideas

READERS SOLVE DESIGN PROBLEMS

Auto pulse generator senses and responds to a probed load

Raju Baddi, Tata Institute of Fundamental Research, Pune, India

This automatic pulse generator (**figures 1** and **2**) is a test gadget that senses a probed contact to a pair of terminals under test and automatically issues a momentary power pulse to them once proper contact is made. These terminals could be the input of a logic gate, an LED on a circuit board, a transformer or relay coil, etc. The need for such a pulse often arises in the day-to-day engineering work of experimenting and testing.

The gadget is powered with a small 3.6V rechargeable NiCd battery. You can easily construct it in a glue-stick tube (**Figure 3**) with the special arrangement of probes shown. A regular arrangement of independent probes also may be used. The circuit has been tested with a 5V supply, as well.

Two versions are shown: **Figure 1** uses an NE555 timer IC as a monostable and is the easiest to get working. **Figure 2** eliminates the NE555 for a reduced parts count but could be affected by variations in the parameters and different manufacturers of the CD4069 CMOS hex inverter used in place of the NE555.

Transistors Q_1 and Q_2 are switches that connect the +ve and −ve probes to the 3.6V supply and ground when

turned on by the CD4069 and the NE555. R_3 and R_4 bias gate G_1's input just below the switching threshold to hold its output high, which holds the output of gate G_2 low. The time constant formed by C_1 provides a certain
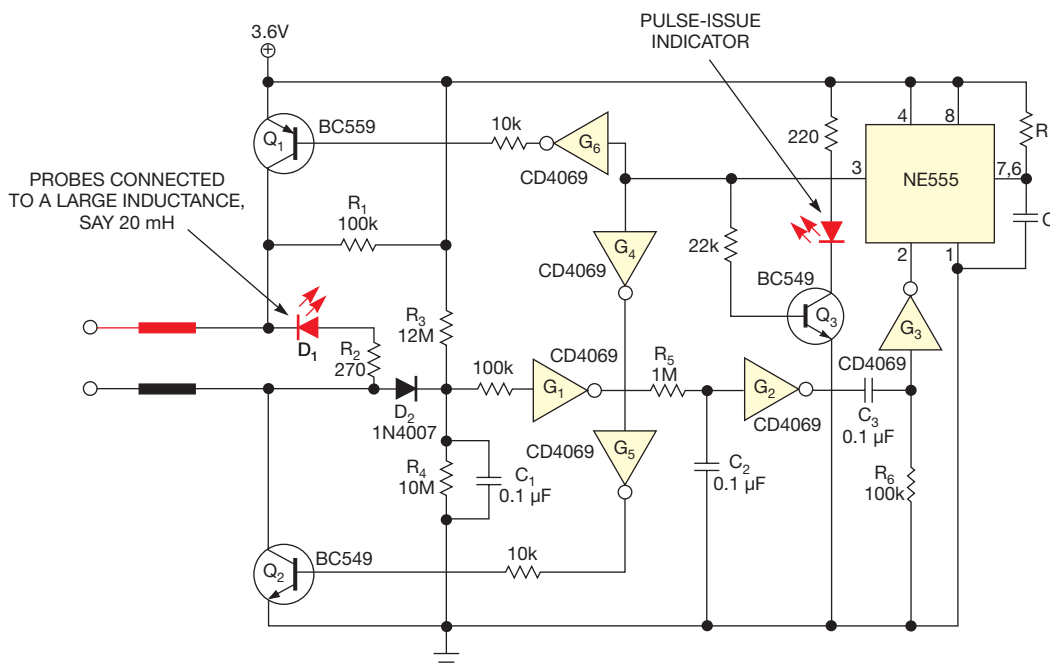
▶To see and comment on all of *EDN*'s Design Ideas, visit www.edn.com/designideas.

Figure 1 The NE555 version is easy to get working but has an increased parts count.
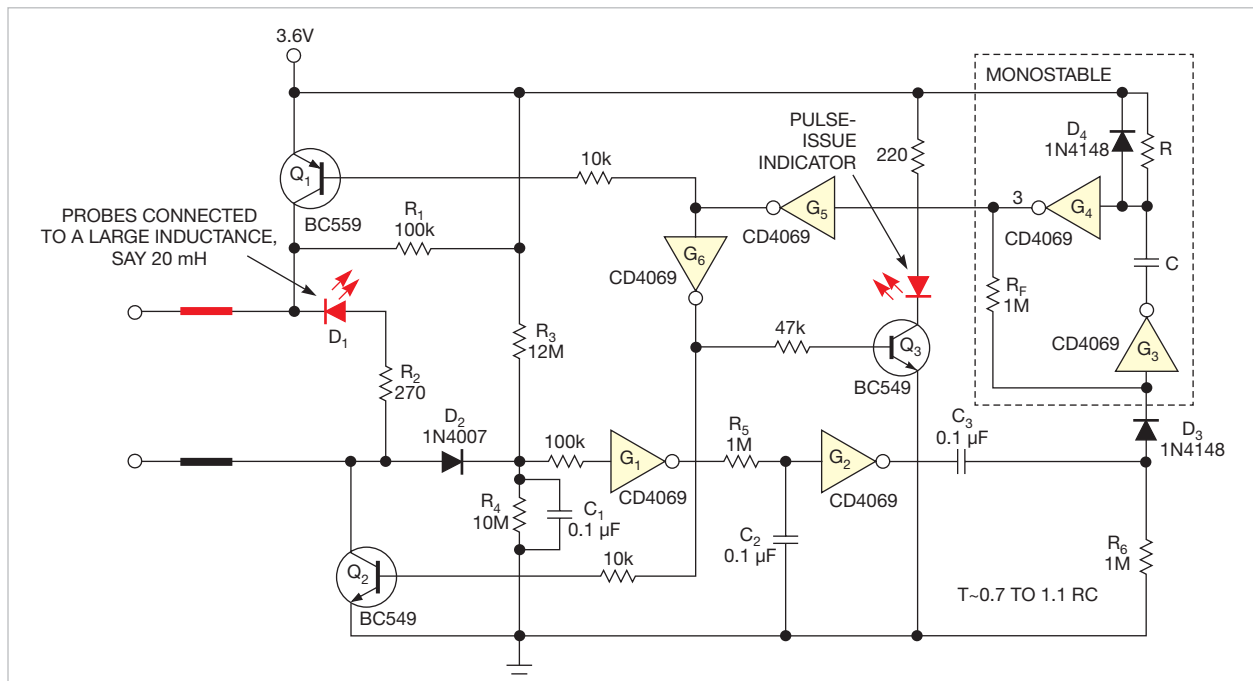
designideas

Figure 2 You can eliminate the NE555, but variations in the G_4 input switching threshold can affect the pulse duration.

amount of noise immunity and determines the minimum time for which the test circuit should be connected between the probes. The 100-kΩ resistor in series with the input of G_1 limits the input current in case the probe is accidentally connected to an active circuit.

R_1 connects to the junction of R_3 and R_4 through a reverse-biased diode, D_1. It normally has no effect as long as the probes are not connected through a load, because the series string of R_1, D_1, R_2, and D_2 is a high-resistance circuit compared with the 12 MΩ of R_3. As soon as you connect a passive test circuit such as a resistor/inductor/LED, however, D_1 and R_2 are paralleled by it. Thus, the branch in parallel with R_3 has a lower resistance and the G_1 input voltage increases such that it is now recognized as logic 1, driving G_1's output low.

R_5 and C_2 form a debounce-and-delay network to ensure that the probes are firmly con-

Figure 3 You can build the automatic pulse generator in a used glue-stick tube.

nected to the circuit under test before the power pulse is issued. When the output of G_1 goes low, capacitor C_2 begins to discharge through R_5. The logic input voltage of G_2 changes within a time on the order of R_5C_2.

In **Figure 1**, the rising output of G_2 immediately triggers the NE555 monostable through G_3 and the differentiator formed by C_3 and R_6. Once C_3 has finished charging through R_6, G_3's input returns to ground and its output returns high to allow the NE555 to complete its timing cycle with a duration that its R and C values determine.[1] The timed logic 1 output of the NE555 turns on Q_3 to light the "pulse issued" LED, and through G_4, G_5, and G_6 turns on Q_1 and Q_2 to present the power pulse to the circuit under test.

Only one pulse is generated per contact; removing the probes and then reconnecting them will issue a new pulse. If the circuit under test is inductive and greater than 20 mH at
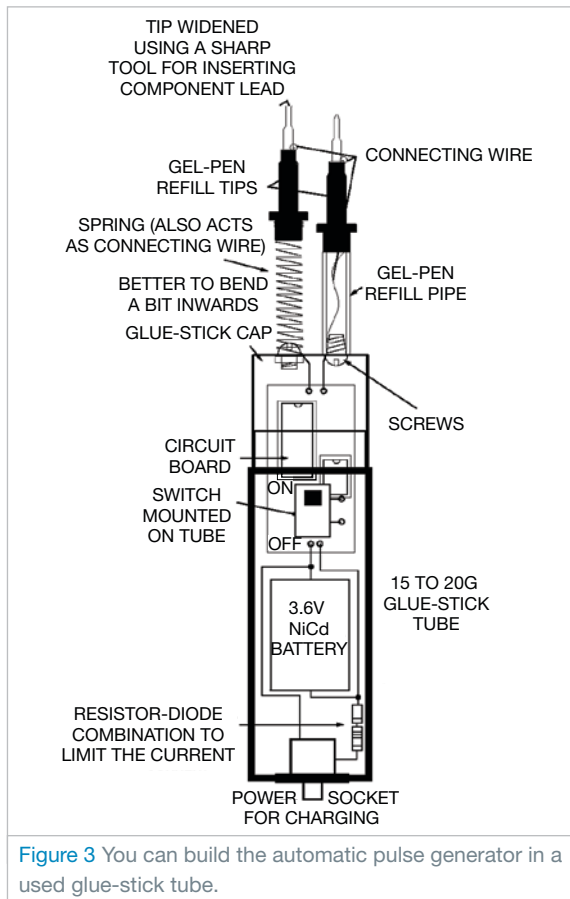
the end of the pulse, the inductive back EMF will flash LED D_1 if the probes are still connected.

In **Figure 2**, the NE555 has been replaced by a monostable comprising G_3 and G_4, D_4, and R_F. R_6 has been changed to 1 MΩ, and diode D_3 has been added to the input of G_3. Resistor R holds G_4's input high, which in the quiescent state causes G_4's output to hold G_3's input low. A rising edge from G_2 causes a low to couple through the initially discharged capacitor, C, to G_4, whose rising output is fed back to G_3 as positive feedback and holds G_3's input

high even if the probes are removed. If this happens, D_3 becomes reverse biased and prevents G_2's falling edge from affecting the monostable operation.

Capacitor C then slowly charges through resistor R until G_4's input rises above its switching threshold, and the positive-feedback process reverses. The pulse duration depends on the R×C time constant, and is about 0.7 to 1.1 RC, depending on the G_4 threshold voltage, which can vary between 0.33 and 0.67 of the supply voltage. The author suggests 1 MΩ for R and 40 nF for C, but R could be made variable,

as well. D_4 ensures that C discharges rapidly as G_3's output returns high.

In either case of **Figure 1** or **Figure 2**, the momentary high output of the monostable turns Q_3 on to flash the pulse-issued indicator LED. It also turns on both Q_1 and Q_2 to power the probes. D_2 serves to isolate the −ve probe from the primary input of the circuit at G_1 to avoid immediate self-suppression.**EDN**

REFERENCE

1 NE555 data sheet, Figure 11, Texas Instruments, June 2010, http://bit.ly/127p7kq.

Read 10 or more switches using only two I/O pins of a microcontroller

Aruna Prabath Rubasinghe, University of Moratuwa, Moratuwa, Sri Lanka

There are several ways to read multiple switch inputs using a reduced number of microcontroller-unit (MCU) pins. For example, you can use an analog MCU pin to read multiple switches by assigning a unique voltage to each switch through a resistor network, or you can use a one-wire device, such as the Maxim DS2408 8-channel addressable switch.

The first method has several disadvantages: The MCU has to have an ADC function, debounce wait times reduce the polling rate, and an error results if the switch is opened during the ADC sampling time. The second method also has the drawback of comparatively low speed; it uses 1-wire communica-
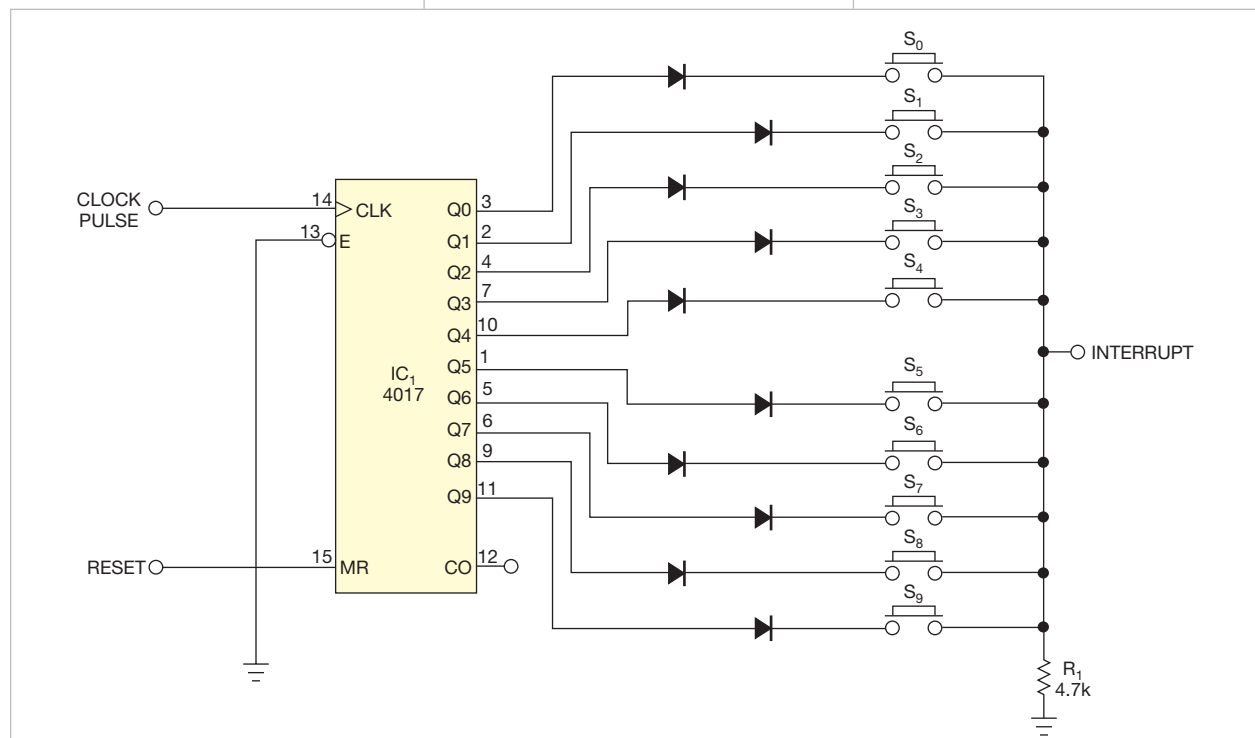

Figure 1 You can easily expand this circuit to many more than 10 switches, yet still use only two MCU I/O pins, by cascading multiple CD4017 counters through their carry-outs to the following enables.

LOGIC HIGH → HIGH IMPEDANCE=CLOCK PULSE
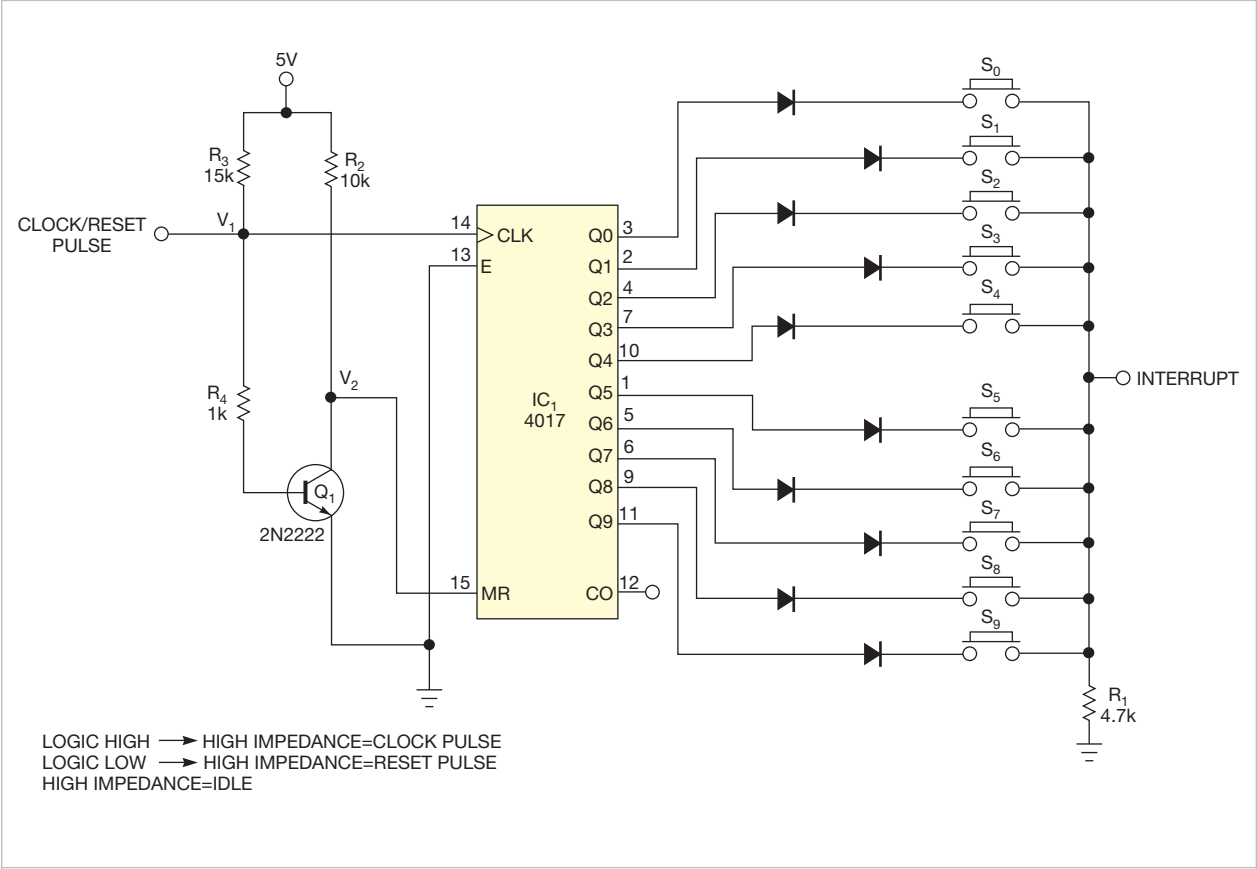LOGIC LOW → HIGH IMPEDANCE=RESET PULSE
HIGH IMPEDANCE=IDLE

Figure 2 You can add three resistors and a transistor to implement the occasional synchronizing reset without using a third I/O pin.
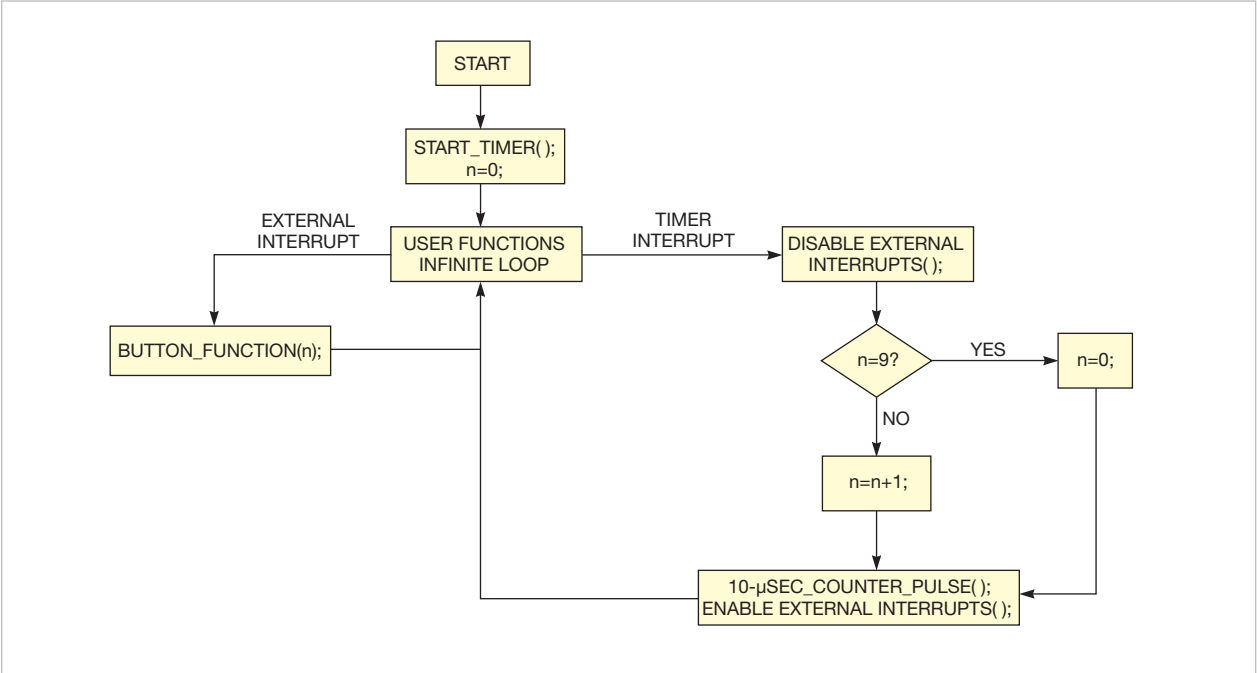

Figure 3 This flowchart displays the process for reading an all-pushbutton system. Only one button at a time should be pressed.

tion, which requires continuous polling; and each poll generates an 8-bit data sequence relevant to switch positions.

This Design Idea describes a method for reading multiple pushbuttons or open/closed switches using only two digital I/O pins and a timer interrupt of the MCU (**Figure 1**). Optionally, a third I/O pin can be assigned to periodically reset the CD4017 (a cascadable decoded 1-of-10 Johnson counter) for reliable operation should an EMI or ESD event occur that could falsely clock the counter, or you can use the circuit shown in **Figure 2** and retain the two-pin feature. The diodes isolate the counter outputs in the event that two or more switches are closed at the same time. You can increase the number of switches connected by cascading multiple CD4017 ICs using a carry-out signal (pin 12) and a clock signal (pin 14).

Reliable operation following the initial power-up reset depends on the CD4017 counter's remaining synchronized with the MCU counter. This synchronization can be upset by an ESD or EMI event such as a nearby cell phone, so it would be wise to include in the firmware a periodic hardware reset to the CD4017 to keep the counts synchronized. **Figure 2** shows how you can do this without having to use a third MCU pin.

For this function, you use the MCU's ability to keep its I/O pin in three different states: high, low, and, by temporarily changing the pin to an input, high impedance.

In the logic-high state, transistor Q_1 turns on through R_4, making the voltage on V_1 logic high and the voltage on V_2 below the logic-low level. This sets the clock pin to a logic high while keeping the reset pin at a logic low.

In the logic-low state, transistor Q_1 turns off, making the voltage on V_1 logic low and the voltage on V_2 above the logic-high level. This sets the reset pin to logic

high while keeping the clock in the logic-low state.

In the idle high-impedance state, transistor Q_1 is turned on through R_3 and R_4, making the voltage on V_1 and V_2 below the logic-low level. This sets both the clock and reset pins of the CD4017 to a logic-low state.

To send a clock edge, therefore, change the state in the following manner: high impedance > logic high > high impedance. Likewise, to reset the CD4017, change the state as follows: high impedance > logic low > high impedance.

The flowchart in **Figure 3** is for an all-pushbutton system and functions as follows: At the start, the MCU sets a counter variable to 0 and starts an interrupt-enabled timer, which is set to overflow and interrupt at 1-msec intervals. In the timer-interrupt routine, several tasks are carried out: External interrupts are disabled; the counter variable is incremented by 1; a 10-μsec clock pulse is sent to the CD4017; and the external interrupt is enabled.

A THIRD I/O PIN CAN BE ASSIGNED TO PERIODICALLY RESET THE CD4017 DURING AN EMI OR ESD EVENT.

As the MCU clocks the CD4017 every 1 msec and increments the counter variable by 1 if its value is less than 9, the CD4017 output corresponding to the counter-variable value goes to logic high from logic low; that is, if the counter-variable value is 2, then the decoded 2 output of the CD4017 (pin 4) is at logic high while all other outputs are at logic low. At this time, if the user pressed pushbutton S_2, it would send a logic-high signal to the external interrupt pin of the MCU. Pressing any other button does not generate external interrupts, because all other outputs of the CD4017 are in the logic-low state.

When the MCU receives the external interrupt, it gets the current counter-variable value (which is 2) from its memory, identifies the pressed button as S_2, and thus carries out the functions relevant to S_2. When the counter variable reaches 9, it is set to 0 through the software, as the CD4017 also resets automatically at the 10th pulse.

Note that only one button at a time should be pressed; if two consecutive buttons are pressed together, there may not be enough dropout time between successive counter states for the interrupt edge to register. You can resolve this issue by using the flowchart shown in **Figure 4**.EDN
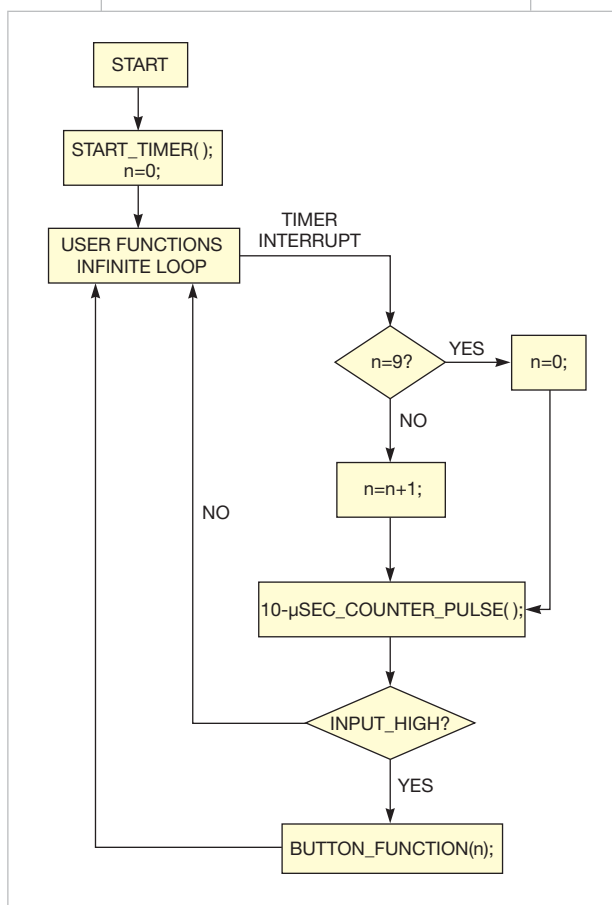

Figure 4 When non-momentary toggle switches are used, you can decode multiple combinations of switch closures by checking the state of the interrupt input.

Successfully choose complementary bipolar transistors

Peter Demchenko, Vilnius, Lithuania

For circuit designs that use complementary bipolar transistors, you sometimes need to sort the NPN and PNP transistors to have matching dc-current gains (β). One example of a circuit requiring matching is the output stage of an amplifier. The circuit in **Figure 1** shows a simple test fixture to achieve this match.

Transistors Q_1 and Q_2 are the devices being tested to see if they are matched. In the test fixture, Q_1 and Q_2 share the same base current (I_B); since there is no additional path where the current can flow, no additional compensation is needed. Note, however, that β should be high enough that $I_E \approx I_C$. With this detail in mind, resistors R_1 and R_2 should be equal.

To give the transistors a bit more headroom, an additional voltage drop is introduced between the transistors' base connections. A voltage differential of a few volts is desirable, so a blue LED is a good choice for D_1. Its presence helps to set the base voltage for Q_1 (V_{B1}) to about half of the supply voltage (V_S). Using an LED in the place of D_1 is preferable to using a zener diode due to the sharper knee at the low currents. Moreover, you can see the glow of many blue LEDs at currents below 10 µA; the glow indicates the presence of base current, which means the circuit

is working properly. **Equation 1** is used to determine the needed supply voltage:

$$V_{BE1}+V_D+V_{BE2}\approx V_S/2 \qquad (1)$$

A typical blue LED will have a forward voltage of about 3.5V; assuming $V_{BE1}=V_{BE2}=0.7V$, you get a value for V_S of about 9.8V.

Resistor R_1 sets the emitter current of Q_1; it is calculated using **Equation 2**:

$$R_1=(V_S-V_{BE1}-V_D-V_{BE2})/I_{E1} \qquad (2)$$

You should select an emitter current that matches the application in which the transistors will be used, because beta varies with emitter and collector current. With matching transistors ($\beta_1=\beta_2$)
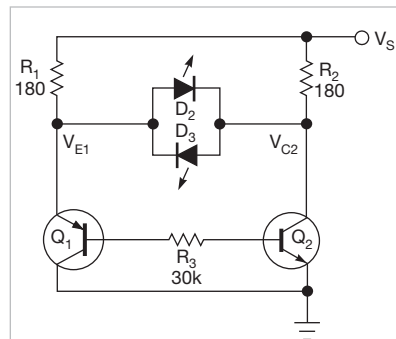

Figure 2 For a simpler version, replace the voltmeter with inverse-parallel-connected red LEDs.

installed in the test fixture, the voltage drops across R_1 and R_2 are equal, and the voltmeter will show 0.

The circuit in **Figure 2** is functionally equivalent but uses a simpler method to indicate when the circuit is in balance. With matched gains, neither of the red LEDs (D_2 and D_3) will be on. **EDN**
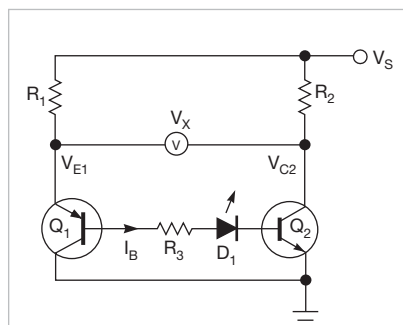

Figure 1 This circuit makes it easy to test and match the current gain of complementary bipolar transistors. Matched transistors will cause the voltmeter to read 0V.

designideas
CLASSICS

Synchronized regulator produces coherent noise

Jim Williams, Sean Gold, and Steve Pietkiewicz, Linear Technology, Milpitas, CA

By using a gated-oscillator archi-tecture instead of a clocked-PWM one, gated-oscillator-type switching regulators permit high efficiency over extended ranges of output current. This architecture eliminates the housekeeping currents associated with the continuous operation of fixed-frequency designs. Gated-oscillator regulators simply self-clock at whatever frequency is necessary to maintain the output voltage. Typically, loop-oscillation frequency ranges from a few hertz to the kilohertz region, depending on the load.

In most cases, this asynchronous, variable-frequency operation doesn't create any problems. However, some systems are sensitive to the asynchronous characteristics. The system in **Figure 1** slightly modifies a gate-oscillator-type switching regulator by synchronizing its loop-oscillation frequency to the system's clock. The oscillation frequency and its attendant switching noise, albeit variable, become coherent with system operation.

To analyze the system in **Figure 1**, temporarily ignore the flip-flop, and assume the circuit directly connects the A_{OUT} and FB pin of the LT1107 regulator. When the output voltage decays, the set pin drops below V_{REF}, causing A_{OUT} to fall. The internal comparator then switches to high, biasing the oscillator and output transistor into conduction. L_1 receives drive pulses, and the circuit deposits this inductor's flyback events into the 100-µF capacitor via the diode, ultimately restoring output voltage. This action overdrives the set pin, causing the IC to switch off until it requires another cycle. This oscillator cycle's frequency is load-dependent and variable.

Now, interposing a flip-flop into the path between the A_{OUT} and FB pins, as the **figure** shows, synchronizes the regulator to the circuit-generated clock.

When the output decays far enough, the A_{OUT} pin goes low. At the next clock pulse, the flip-flop's Q_2 output sets low, biasing the comparator-oscillator. This turns on the power switch, which pulses L_1. L_1 responds in flyback fashion and deposits its energy into the output capacitor to maintain output voltage. This operation is similar to the previously described case, except that the flip-flop now synchronizes the sequence of events with the system clock. Although the resulting loop's oscillation frequency is variable, the frequency and all attendant switching noise are synchronous and coherent with the system clock.

The circuit requires a start-up sequence because the output provides power for the clock. The circuit connects the flip-flop's remaining section as a buffer to furnish start-up. The flip-flop's connected CLR_1 and CLK_1 lines monitor output voltage via the 221-, 82.5-, and 100-kΩ resistor string. When power is applied, Q_1 sets CLR_2 low, which permits the LT1107 to switch, thereby raising the output voltage. When the output goes high enough, Q_1 sets CLR_2 high, and normal loop operation commences. Although this circuit uses a step-up regulator, the technique also works with other types.**EDN**
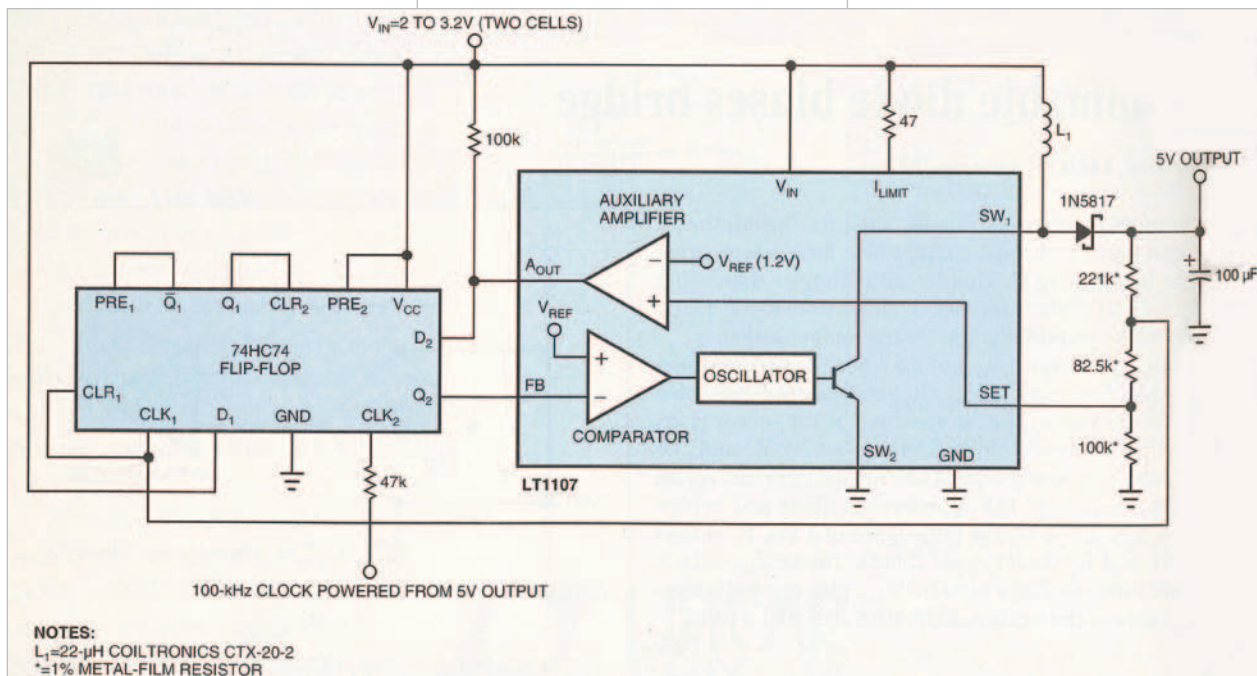

Figure 1 A synchronizing flip-flop forces the LT1107 gate-oscillator-type switching regulator's noise to be coherent with the 100-kHz clock.