KNN Acceleration Peripheral

IOB-KNN User Guide, V1 , Build 25f7cdb

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1 Introduction

The IObundle KNN core includes a configurable number of modules that can each solve the two most time consuming parts of the KNN algorithm: Distance calculation and neighbor sorting. It is written in Verilog and includes a C software driver. The IP is currently supported for use in FPGAs.

2 Symbol

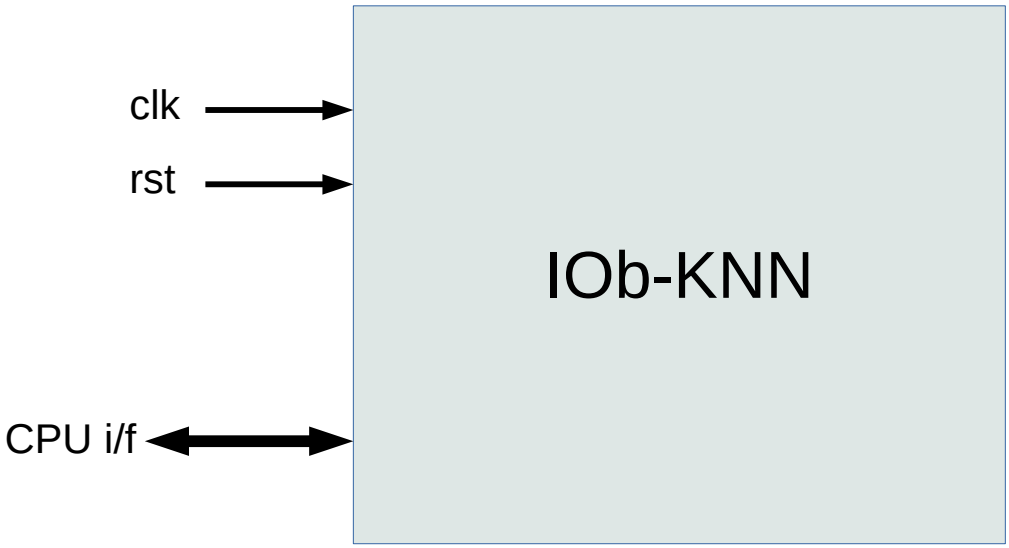

Figure 1: IP Core Symbol

3 Features

- 32-bit test point and dataset point inputs (16 bits for each coordinate).
- 16-bit index counter supports up to 2^{16} dataset points.
- Configurable number of hardware neighbors and modules.
- Flexible hardware can solve problems with any number of K neighbors independently of synthesized hardware.
- C software driver.
- Reset, set test point, set dataset point and get closest neighbors functions.
- IOb-SoC native CPU interface.

4 Benefits

- Compact hardware implementation
- Can fit many instances in low cost FPGAs
- Module can make use of bigger FPGAs, it is scalable.
- Low power consumption

5 Deliverables

- Verilog source code
- User documentation for easy system integration
- Example integration in IOb-SoC
- FPGA synthesis and implementation scripts

6 Block Diagram and Description

A high-level block diagram of the IOB-KNN core is presented in Figure 6 and a brief explanation of each block is given in Table 1.

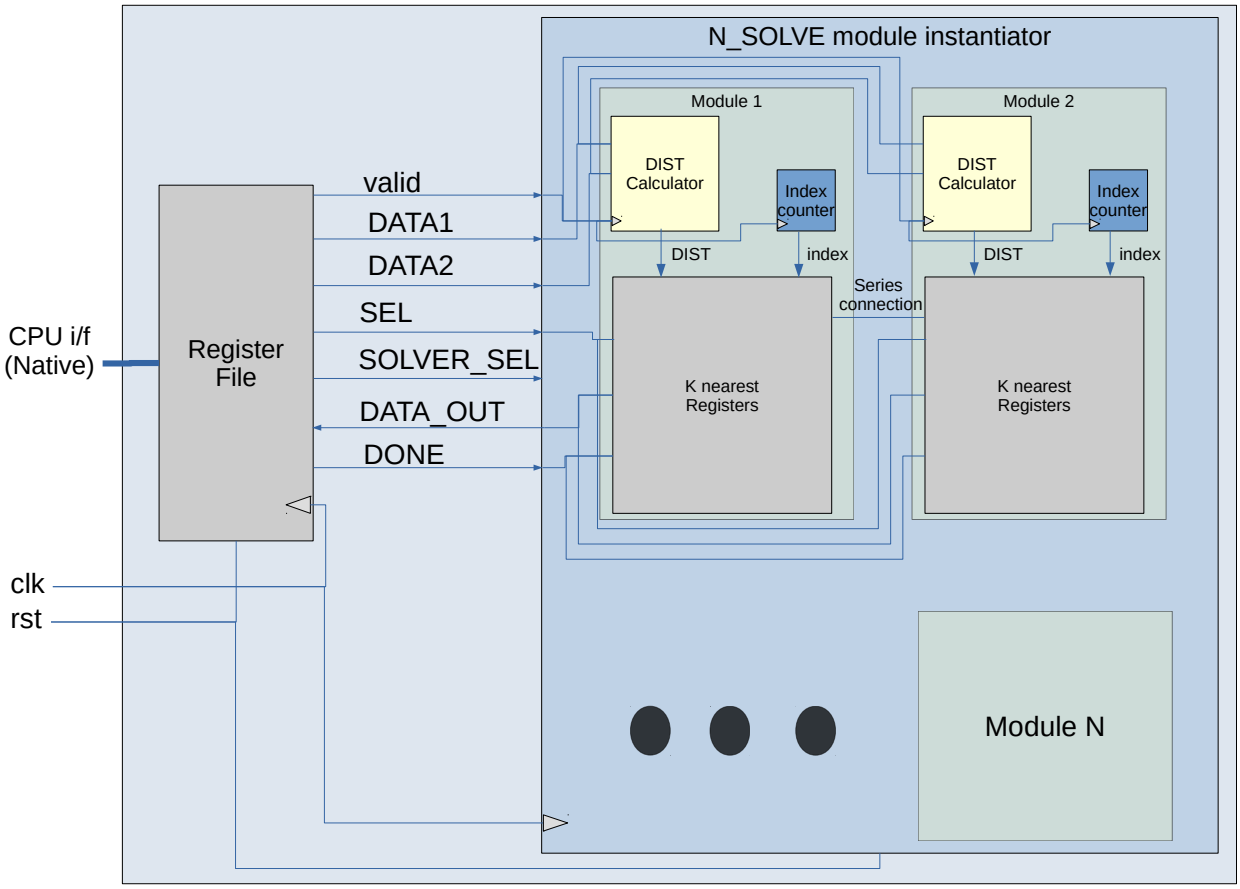

Figure 2: High-level block diagram

Block	Description
Register File	Configuration, control and status registers accessible by the sofware

Table 1: Block descriptions.

7 Interface Signals

The interface signals of the KNN core are described in the following tables.

Name	Direction	Width	Description
clk	input	1	System clock input
rst	input	1	System reset asynchronous and active high

Table 2: General Interface Signals

Name	Direction	Width	Description
valid	input	1	Native CPU interface valid signal
address	input	ADDR_W	Native CPU interface address signal
wdata	input	WDATA_W	Native CPU interface data write signal
wstrb	input	DATA_W/8	Native CPU interface write strobe signal
rdata	output	DATA_W	Native CPU interface read data signal
ready	output	1	Native CPU interface ready signal

Table 3: CPU Native Slave Interface Signals

8 Registers

The software accessible registers of the KNN core are described in Table 4. The table gives information on the name, read/write capability, word aligned addresses, used word bits and a textual description.

Name	R/W	Addr	Bits	Initial Value	Description
DATA_1	W	0x00	DATA_W-1:0	0	Test point input register
DATA_2	W	0x04	DATA_W-1:0	0	Dataset point input register
DATA_OUT	R	0x08	15:0	0	Index output register
DONE	W	0x0c	0:0	1	Signal if all dataset points have been sent
SOLVER_SEL	W	0x10	15:0	0	Solver module select
SEL	W	0x14	15:0	0	Neighbor select
SERIES_ENABLE	W	0x18	1:0	0	LSB is whether a module is working on it's own or chained to the one before through the series connection. MSB is enable
KNN_RESET	W	0x1c	0:0	0	Soft reset

Table 4: Software accessible registers.

9 FPGA Results

The following are FPGA implementation results for the Xilinx family of FPGA devices, for a peripheral with 30 solver modules and 10 neighbor registers each.

Resource	Used
LUTs	18210
Registers	24820
DSPs	30
BRAM	0

Table 5: Implementation Resources for Xilinx Artix-7 Devices