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CS61C

Great Ideas in **Computer Architecture** (a.k.a. Machine Structures)



UC Berkeley
Professor
Bora Nikolić

RISC-V Assembly Language

Great Idea #1: Abstraction (Levels of Representation/Interpretation)

High Level Language
Program (e.g., C)

```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

| Compiler

Assembly Language
Program (e.g., RISC-V)

lw	x3,	0 (x10)
lw	x4,	4 (x10)
sw	x4,	0 (x10)
sw	x3,	4 (x10)

Anything can be represented
as a number,
i.e., data or instructions

| Assembler

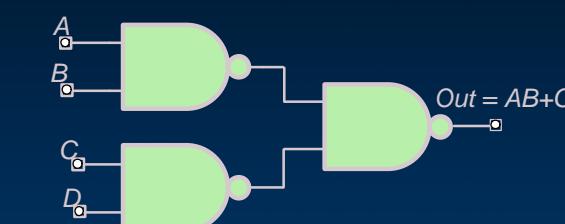
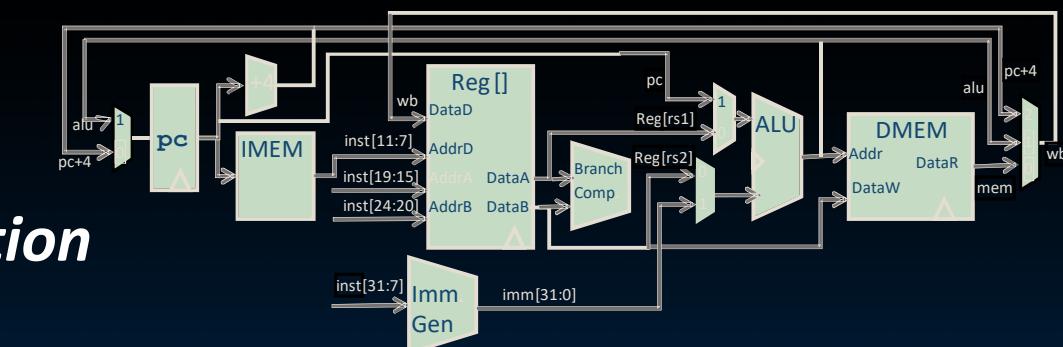
Machine Language
Program (RISC-V)

1000	1101	1110	0010	0000	0000	0000	0000	0000	0000
1000	1110	0001	0000	0000	0000	0000	0000	0000	0100
1010	1110	0001	0010	0000	0000	0000	0000	0000	0000
1010	1101	1110	0010	0000	0000	0000	0000	0000	0100

| Hardware Architecture Description
(e.g., block diagrams)

| Architecture Implementation

Logic Circuit Description
(Circuit Schematic Diagrams)



Assembly Language

- Basic job of a CPU: execute lots of *instructions*.
- Instructions are the primitive operations that the CPU may execute.
 - Like a sentence: operations (verbs) applied to operands (objects) processed in sequence ...
- Different CPUs implement different sets of instructions. The set of instructions a particular CPU implements is an *Instruction Set Architecture (ISA)*.
 - Examples: ARM (cell phones), Intel x86 (i9, i7, i5, i3), IBM Power, IBM/Motorola PowerPC (old Macs), MIPS, RISC-V, ...

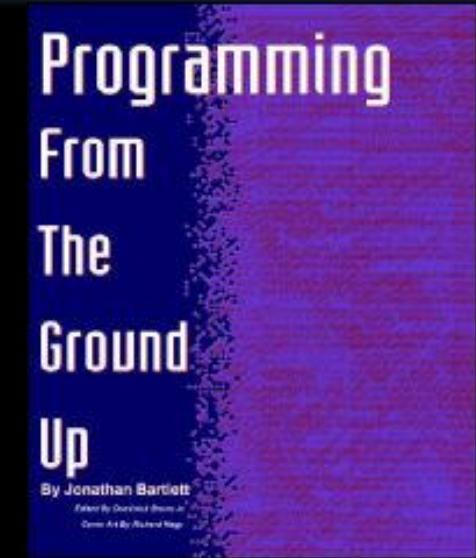
Book: Programming From the Ground Up

*“A new book was just released which is based on a new concept - teaching computer science through assembly language (Linux x86 assembly language, to be exact). This book teaches how the machine itself operates, rather than just the language. I've found that the key difference between mediocre and excellent programmers is whether or not they know assembly language. **Those that do tend to understand computers themselves at a much deeper level.** Although [almost!] unheard of today, this concept isn't really all that new -- there used to not be much choice in years past. Apple computers came with only BASIC and assembly language, and there were books available on assembly language for kids. This is why the old-timers are often viewed as 'wizards': they **had** to know assembly language programming.”*

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-- slashdot.org comment, 2004-02-05

RISC-V (4)



Instruction Set Architectures

- Early trend was to add more and more instructions to new CPUs to do elaborate operations
 - VAX architecture had an instruction to multiply polynomials!
- RISC philosophy (Cocke IBM, Patterson, Hennessy, 1980s) – Reduced Instruction Set Computing
 - Keep the instruction set small and simple, makes it easier to build fast hardware.
 - Let software do complicated operations by composing simpler ones.
 - This went against the convention wisdom of the time.
(he who laughs last, laughs best)

Patterson and Hennessy win Turing!





RISC-V Architecture

IBM 360 Green Card

- New open-source, license-free ISA spec
 - Supported by growing shared software ecosystem
 - Appropriate for all levels of computing system, from microcontrollers to supercomputers
 - 32-bit, 64-bit, and 128-bit variants
(we're using 32-bit in class, textbook uses 64-bit)

▪ Why RISC-V instead of Intel 80x86?

- RISC-V is simple, elegant.
Don't want to get bogged down in gritty details.
- RISC-V has exponential adoption

<https://cs61c.org/resources/>

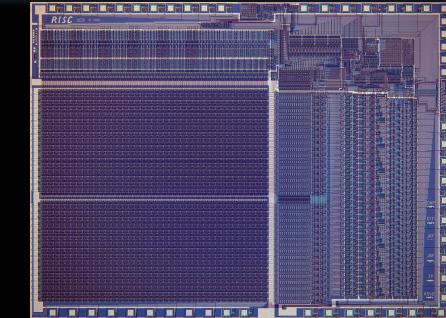
RISC-V (7)

IBM System/360 Reference Data					
<small>NAME MNEMONIC MODE OF MAT COMMENTS</small>					
Add	ADD	S,A	R/R	R/R	
Add Immediate	ADDI	A,P	R/R	R/R	
Add Logical	ADLI	A,P	R/R	R/R	
And	AND	S,A	R/R	R/R	
And Immediate	ANDI	A,P	R/R	R/R	
Branch	BRANCH	S,B	R/R	R/R	
Branch and Store	BRANCH&STORE	S,B	R/R	R/R	
Branch on Condition	BCR	S,B	R/R	R/R	
Branch on Condition or Equal	BCRE	S,B	R/R	R/R	
Component	C	R,R	R/R	R/R	
Component Load	CL	R,R	R/R	R/R	
Component Load/Store	CLC	R,R	R/R	R/R	
Convert to Floating	CVT	R,R	R/R	R/R	
Divide	DIV	R,R	R/R	R/R	
Divide Doubleword	DIVD	R,R	R/R	R/R	
Divide Floating	DIVF	R,R	R/R	R/R	
Divide Word	DIVW	R,R	R/R	R/R	
Insert One Key Swap	IWS	R,R	R/R	R/R	
Load Address	LAD	R,R	R/R	R/R	
Load Complement	LCR	R,R	R/R	R/R	
Load Multiple	LML	R,R	R/R	R/R	
Load Multiple Control	LMLC	R,R	R/R	R/R	
Load Pseudo	LPR	R,R	R/R	R/R	
Load Pseudo Address	LPRD	R,R	R/R	R/R	
Load Word	LW	R,R	R/R	R/R	
Move	MV	R,R	R/R	R/R	
Move Immediate	MVI	R,R	R/R	R/R	
Move Multiple	MML	R,R	R/R	R/R	
Move Multiple Control	MMLC	R,R	R/R	R/R	
Move Pseudo	MPR	R,R	R/R	R/R	
Move Pseudo Address	MPRD	R,R	R/R	R/R	
Not	NOT	R,R	R/R	R/R	
Not Immediate	NOTI	R,R	R/R	R/R	
Or	OR	R,R	R/R	R/R	
Or Immediate	ORI	R,R	R/R	R/R	
Shift Left	SHL	R,R	R/R	R/R	
Shift Right	SHR	R,R	R/R	R/R	
Swap	SWAP	R,R	R/R	R/R	
Xor	XOR	R,R	R/R	R/R	
Xor Immediate	XRI	R,R	R/R	R/R	

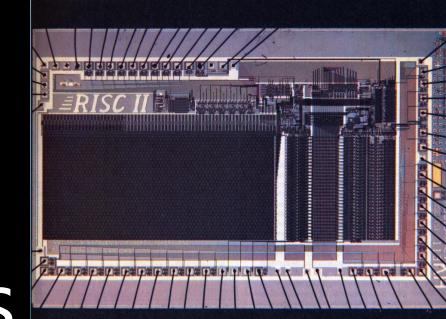
RISC-V Reference Data										
<small>RV32I BASE INTEGRAL INSTRUCTIONS, in alphabetical order</small>										
MNEMONIC	FMT	NAME	DESCRIPTION (in Verilog)	NOTE						
add	I	ADD (Word)	$R[rd] = R[r1] + R[r2]$	1)						
addi	I	ADD Immediate (Word)	$R[rd] = R[r1] + imm[16]$	1)						
and	I	AND	$R[rd] = R[r1] \& R[r2]$							
andi	I	AND Immediate	$R[rd] = R[r1] \& imm[16]$							
auipc	I	Add Upper Immediate to PC	$R[rd] = PC + imm[17:0]$							
beq	S	Branch EQ	$R[R[rs1]] == R[rs2]$							
bge	S	Branch Greater than or Equal	$R[R[rs1]] >= R[rs2]$							
bgeu	S	Branch Greater than	$R[R[rs1]] > R[rs2]$							
blt	S	Branch Less Than	$R[R[rs1]] < R[rs2]$							
bltu	S	Branch Less Than Unsigned	$R[R[rs1]] < R[rs2]$ PC-PC+imm[16]							
ne	S	Branch Not Equal	$R[R[rs1]] != R[rs2]$ PC-PC+imm[16]							
csrrc	I	Cont. Stat. RegRead&Clear	$R[rd] = CSR_CSR & CSR & -imm$							
csrrci	I	Cont. Stat. RegRead&Clear	$R[rd] = CSR_CSR & CSR & -imm$							
csrrs	I	Cont. Stat. RegRead&Set	$R[rd] = CSR_CSR & CSR R[rs1]$							
csrrwi	I	Cont. Stat. RegRead&Set	$R[rd] = CSR_CSR & CSR imm$							
csrrw	I	Cont. Stat. RegRead&Write	$R[rd] = CSR_CSR & CSR R[rs1]$							
csrrwi	I	Cont. Stat. Reg Read&Write	$R[rd] = CSR_CSR & imm$							
break		Environment BRAK	Transfer control to debugger							
ecall		Environment CALL	Transfer control to operating system							
fence	I	Synch thread	Synchronizes threads							
fence.i	I	Synch Inst & Data	Synchronizes writes to instruction							
jal	U	Jump & Link	$R[rd] = PC[4:1]; R[pc] = PC + imm[19:0]$							
jalr	I	Jump & Link Register	$R[rd] = PC[4:1]; R[pc] = R[rs1] + imm[19:0]$							
lb	I	Load Byte	$R[rd] = M[RS1][R[rs1]:R[rs2]]$							
lbu	I	Load Byte Unsigned	$R[rd] = M[RS1][R[rs1]:R[rs2]] + imm[7:0]$							
ld	I	Load Doubleword	$R[rd] = M[RS1][R[rs1]:R[rs2]] + imm[63:0]$							
lh	I	Load Halfword	$R[rd] = M[RS1][R[rs1]:R[rs2]] + imm[15:0]$							
lw	I	Load Halfword Unsigned	$R[rd] = M[RS1][R[rs1]:R[rs2]] + imm[15:0]$							
lui	I	Load Upper Immediate	$R[rd] = imm[31:0]$							
lw	I	Load Word	$R[rd] = M[RS1][R[rs1]:R[rs2]] + imm[31:0]$							
lwsr	I	Load Word Unsigned	$R[rd] = M[RS1][R[rs1]:R[rs2]] + imm[31:0]$							
or	I	OR	$R[rd] = R[r1] R[r2]$							
ori	I	OR Immediate	$R[rd] = R[r1] imm[16]$							
sb	S	Store Byte	$M[R[rs1]:R[rs2]] = R[rd]$							
sd	S	Store Doubleword	$M[R[rs1]:R[rs2]] = R[rd]$							
sh	S	Store Halfword	$M[R[rs1]:R[rs2]] = R[rd]$							
shll,shlw	I	Shift Left Immediate (Word)	$R[rd] = R[r1] << imm[1:0]$	1)						
shlti	I	Shift Left Immediate (Word)	$R[rd] = R[r1] << imm[1:0]$	2)						
shltiu	I	Shift Less Than Immediate Unsigned	$R[rd] = R[r1] << imm[1:0]$	2)						
slti	I	Set Less Than	$R[rd] = R[r1] < R[r2]$	1)						
sltiu	I	Set Less Than Unsigned	$R[rd] = R[r1] < imm[1:0]$	2)						
sr	I	Shift Right Immediate (Word)	$R[rd] = R[r1] >> R[rs2]$	1,5)						
srw,sw	I	Shift Right Immediate (Word)	$R[rd] = R[r1] >> imm[1:0]$	1)						
srl,slw	I	Shift Right Immediate (Word)	$R[rd] = R[r1] >> imm[1:0]$	1)						
sub,subw	I	SUBtract (Word)	$R[rd] = R[r1] - R[r2]$	1)						
sw	S	Store Word	$M[R[rs1]:R[rs2]] = R[rd]$							
xor	I	XOR	$R[rd] = R[r1] ^ R[r2]$							
xori	I	XOR Immediate	$R[rd] = R[r1] ^ imm[16]$							
sc	S	XOR Immediate	$R[rd] = R[r1] ^ imm[16]$							
Notes:	1) The Word operation only operates on the lower 32 bits of a 64-bit register 2) Operation assumes unsigned integers (instead of 2's complement) 3) The test bit significant bit of the branch address in jal is set to 0 4) Branch and Jump instructions extend the sign of data to fill the 64-bit register 5) Replicates the sign bit of imm to fill the 32-bit result during right shift 6) Multiplies with one operand signed and one unsigned 7) The Single version does a single-precision operation using the rightmost 32 bits of a 64-bit register 8) Classify writes a 16-bit mask to show which properties are true (e.g., -inf, 0, +inf, denorm, NaN) 9) Atomic memory operation; nothing else can interpose itself between the read and the write of the memory location The imm32 field is sign-extended in RISC-V									
ARITHMETIC CORE INSTRUCTION SET										
RV4M4 Multiplying Extension										
MNEMONIC	FMT	NAME	DESCRIPTION (in Verilog)	NOTE						
mul	R	MULiply (Word)	$R[rd] = R[r1] * R[r2]$	1)						
mulh	R	MULiply upper Half	$R[rd] = R[r1] * R[r2] > 17:0$							
mulhu	R	MULiply upper Half Unsigned	$R[rd] = R[r1] * R[r2] > 17:0$	6)						
mulhuu	R	MULiply upper Half Unsigned	$R[rd] = R[r1] * R[r2] > 17:0$	2)						
div	R	Divide (Word)	$R[rd] = R[r1] / R[r2]$	1)						
divu	R	Divide Unsigned	$R[rd] = R[r1] / R[r2]$	7)						
rem	R	REMinder (Word)	$R[rd] = R[r1] % R[r2]$	2)						
remu	R	REMinder Unsigned	$R[rd] = R[r1] % R[r2]$	7)						
RV4M4 and RV4D Floating-Point Extensions										
MNEMONIC	FMT	NAME	DESCRIPTION (in Verilog)	NOTE						
load		Load (Word)	$R[rd] = M[R[rs1]:R[rs2]]$	1)						
fmadd	S	Single Word	$R[rd] = R[r1] * R[r2] + R[r3]$	1)						
fadd	S	ADD	$R[rd] = R[r1] + R[r2]$	7)						
fsub	S	SUBtract	$R[rd] = R[r1] - R[r2]$	7)						
fmul	S	MULiply	$R[rd] = R[r1] * R[r2]$	7)						
fdiv	S	Divide	$R[rd] = R[r1] / R[r2]$	7)						
fneg	S	Negative	$R[rd] = -R[r1]$	7)						
fmadd.s	S	Single Word	$R[rd] = R[r1] * R[r2] + R[r3]$	7)						
fmadd.d	D	Double Word	$R[rd] = R[r1] * R[r2] + R[r3]$	7)						
fmul.s	S	Negative Multiply-Signed	$R[rd] = -R[r1] * R[r2]$	7)						
fmul.d	D	Negative Multiply-Double	$R[rd] = -R[r1] * R[r2]$	7)						
fdiv.s	S	Negative Divide-Signed	$R[rd] = -R[r1] / R[r2]$	7)						
fdiv.d	D	Negative Divide-Double	$R[rd] = -R[r1] / R[r2]$	7)						
fneg.s	S	Negative Negate-Signed	$R[rd] = -R[r1]$	7)						
fneg.d	D	Negative Negate-Double	$R[rd] = -R[r1]$	7)						
fmix.s	S	Normal source	$R[rd] = (R[r1] << 23) + R[r2] >> 23$	7)						
fmix.d	D	Normal source	$R[rd] = (R[r1] << 56) + R[r2] >> 56$	7)						
fmmax	S	Maximum	$R[rd] = R[r1] > R[r2]$	7)						
fmmin	S	Minimum	$R[rd] = R[r2] > R[r1]$	7)						
fcp1	F	Compuer Float 1/0	$R[rd] = R[r1] > 0$	7)						
fcp0	F	Compuer Float Less Than	$R[rd] = (R[r1] > 0) & (R[r1] < 1)$	7)						
fclans	S	Classify Type	$R[rd] = classType(R[rs1])$	7,8)						
fmove	S	Move from Integer	$R[rd] = move(R[rs1], R[rs2])$	7)						
fcvt.w	S	Convert from FP to IP	$R[rd] = convertFPtoIP(R[rs1])$	7)						
fcvt.d	D	Convert from FP to DP	$R[rd] = convertFPtoDP(R[rs1])$	7)						
fcvt.w,fcvt.d	S,D	Convert from FP to DP	$R[rd] = convertFPtoDP(R[rs1])$	7)						
fcvt.s,fcvt.l	S	Convert from FP to SP	$R[rd] = convertFPtoSP(R[rs1])$	2,7)						
fcvt.w,fcvt.l	S	Convert from FP to SP Unsigned	$R[rd] = convertFPtoSPUnsigned(R[rs1])$	7)						
fcvt.s,fcvt.d	S	Convert from FP to DP Unsigned	$R[rd] = convertFPtoDPUnsigned(R[rs1])$	7)						
fcvt.w,fcvt.u	S	Convert from FP to DP	$R[rd] = convertFPtoDP(R[rs1])$	2,7)						
fcvt.s,fcvt.u	S	Convert from FP to SP	$R[rd] = convertFPtoSP(R[rs1])$	2,7)						
fcvt.w,fcvt.u	S	Convert from FP to SP Unsigned	$R[rd] = convertFPtoSPUnsigned(R[rs1])$	2,7)						
fcvt.s,fcvt.l	S	Convert from FP to SP	$R[rd] = convertFPtoSP(R[rs1])$	2,7)						
fcvt.w,fcvt.l	S	Convert from FP to SP Unsigned	$R[rd] = convertFPtoSPUnsigned(R[rs1])$	2,7)						
fcvt.w,fcvt.u	S	Convert from FP to DP	$R[rd] = convertFPtoDP(R[rs1])$	2,7						

RISC-V Origins

- Started in Summer 2010 to support open research and teaching at UC Berkeley
 - Lineage can be traced to RISC-I/II projects (1980s)
- As the project matured, it migrated to RISC-V foundation (www.riscv.org)
- Many commercial and research projects based on RISC-V, open-source and proprietary
 - Widely used in education
- Read more:
 - <https://riscv.org/risc-v-history/>
 - <https://riscv.org/risc-v-genealogy/>



RISC-I



RISC-II



Elements of Architecture: Registers

Instruction Set

Preliminary discussion of the logical design of an electronic computing instrument¹

Arthur W. Burks / Herman H. Goldstine / John von Neumann

“instruction sets”

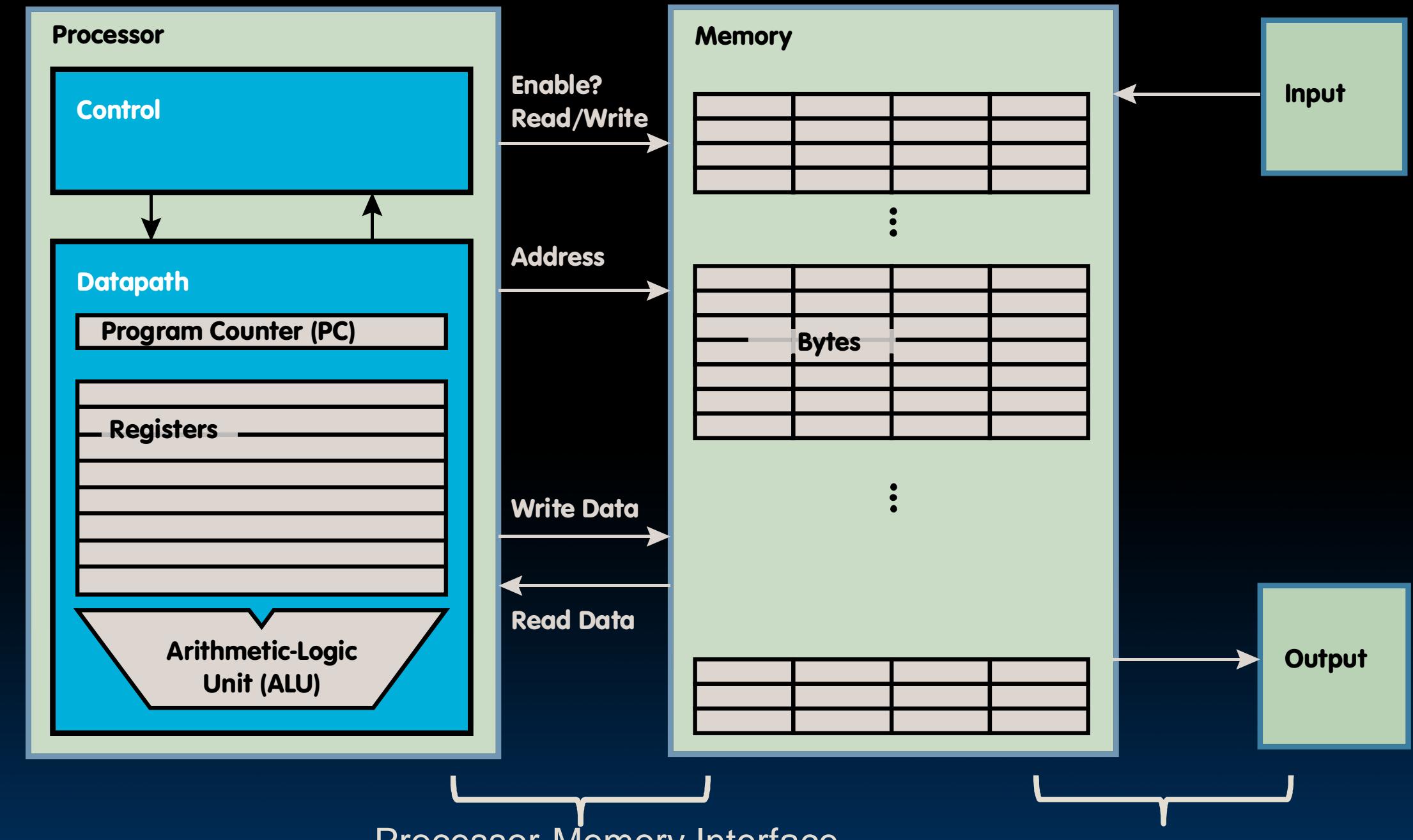
3.1. It is easy to see by formal-logical methods that there exist codes that are *in abstracto* adequate to control and cause the execution of any sequence of operations which are individually available in the machine and which are, in their entirety, conceivable by the problem planner. The really decisive considerations from the present point of view, in selecting a code, are more of a practical nature: simplicity of the equipment demanded by the code, and the clarity of its application to the actually important problems together with the speed of its handling of those problems. It would take us much too far afield to discuss these questions at all generally or from first principles. We will therefore restrict ourselves to analyzing only the type of code which we now envisage for our machine.

- Instruction set for a particular architecture (e.g. RISC-V) is represented by the Assembly language
- Each line of assembly code represents one instruction for the computer

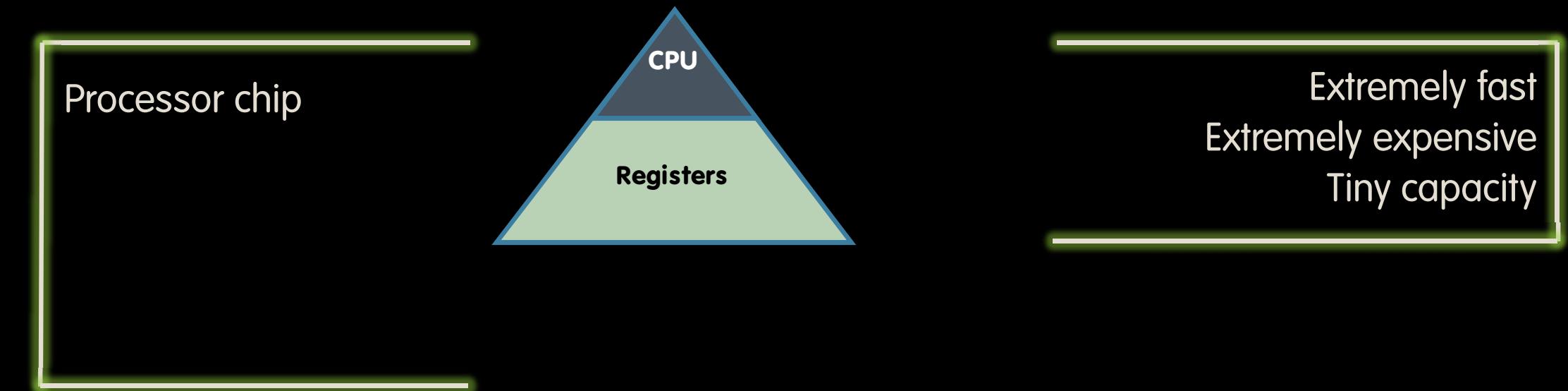
Assembly Variables: Registers (1/3)

- Unlike HLL like C or Java, assembly cannot use variables
 - Why not? Keep Hardware Simple
- Assembly operands are registers
 - Limited number of special locations built directly into the hardware
 - Operations can only be performed on these!
- Benefit: Since registers are directly in hardware, they're very fast (faster than 0.25ns)
 - Recall light is $3 \times 10^8 \text{m/s} = 0.3 \text{m/ns} = 30 \text{cm/ns} = 10 \text{cm}/0.3\text{ns}$!!!... where 0.3ns is the clock period of a 3.33GHz computer

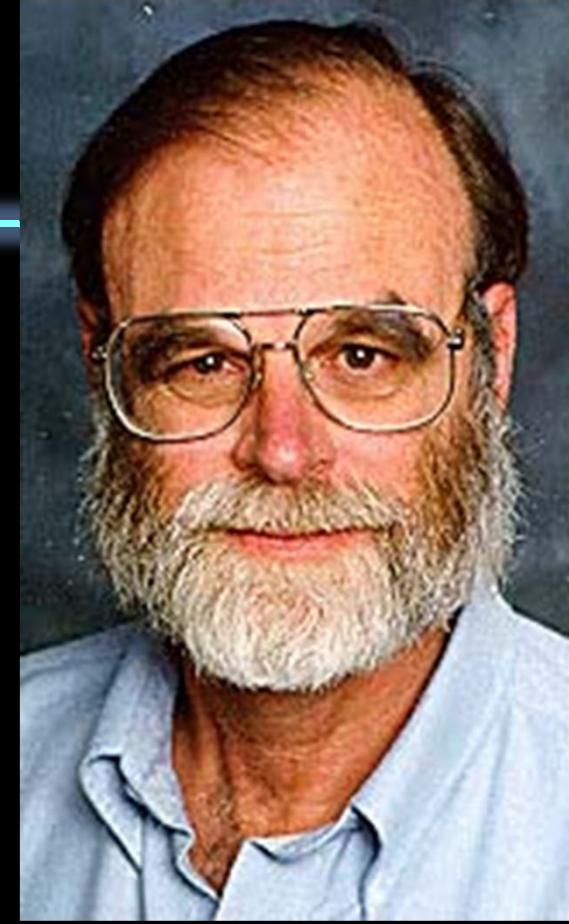
Aside: Registers are Inside the Processor



Great Idea #3: Principle of Locality / Memory Hierarchy



Jim Gray's Storage Latency Analogy: How Far Away is the Data?



Jim Gray
Turing Award
B.S. Cal 1966
Ph.D. Cal 1969

This Campus

1 Registers
[ns]



1 min

Assembly Variables: Registers (2/3)

- Drawback: Since registers are in hardware, there is a predetermined number of them
 - Solution: RISC-V code must be very carefully put together to efficiently use registers
- 32 registers in RISC-V
 - Why 32?
Smaller is faster, but too small is bad. Goldilocks principle ("This porridge is too hot; This porridge is too cold; this porridge is just right")
- Each RISC-V register is 32 bits wide (in RV32 variant)
 - Groups of 32 bits called a word in RV32
 - P&H textbook uses the 64-bit variant RV64

Assembly Variables: Registers (3/3)

- Registers are numbered from 0 to 31
 - Referred to by number **x0 – x31**
- **x0** is special, always holds value zero
 - So only 31 registers able to hold variable values
- Each register can be referred to by number or name
 - Will add names later

C, Java variables vs. registers

- In C (and most high-level languages) variables declared first and given a type. E.g.,

```
int fahr, celsius;
char a, b, c, d, e;
```
- Each variable can ONLY represent a value of the type it was declared as (cannot mix and match int and char variables).
- In assembly language, the registers have no type
 - Operation determines how register contents are treated

Comments in Assembly

- Make your code more readable: comments!
- Hash (#) is used for RISC-V comments
 - anything from hash mark to end of line is a comment and will be ignored
 - This is just like the C99 //
- Note: Different from C.
 - C comments have format
`/* comment */`
so they can span many lines

Aside: Apollo Guidance Computer



Margaret Hamilton
(Wikimedia commons)



```
179      TC      BANKCALL      # TEMPORARY, I HOPE HOPE HOPE
180      CADR    STOPRATE      # TEMPORARY, I HOPE HOPE HOPE
181      TC      DOWNFLAG     # PERMIT X-AXIS OVERRIDE
```

```
245      CAF      CODE500      # ASTRONAUT: PLEASE CRANK THE
246      TC       BANKCALL      #
247      CADR    GOPERF1
248      TCF     GOTOP00H      # TERMINATE
249      TCF     P63SPOT3      # PROCEED SEE IF HE'S LYING
250
251      P63SPOT4   TC      BANKCALL      # ENTER INITIALIZE LANDING RADAR
252          CADR    SETPOS1
253
254          TC      POSTJUMP      # OFF TO SEE THE WIZARD ...
255          CADR    BURNBABY
```

Assembly code with comments
(ABC News, 2018)

Assembly Instructions

- In assembly language, each statement (called an **Instruction**), executes exactly one of a short list of simple commands
- Unlike in C (and most other high-level languages), each line of assembly code contains at most 1 instruction
- Instructions are related to operations (=, +, -, *, /) in C or Java
- Ok, enough already...gimme my RV32!

RISC-V Add/Sub Instructions

- Syntax of Instructions:
 - one two, three, four
 - add x1 , x2 , x3**
 - where:
 - one = operation by name
 - two = operand getting result (“destination,” **x1**)
 - three = 1st operand for operation (“source1,” **x2**)
 - four = 2nd operand for operation (“source2,” **x3**)
 - Syntax is rigid:
 - 1 operator, 3 operands
 - Why? Keep hardware simple via regularity

Addition and Subtraction of Integers (2/4)

▪ Addition in Assembly

- Example: **add** **x1 , x2 , x3** (in RISC-V)
 - Equivalent to: $a = b + c$ (in C)
 - where C variables \Leftrightarrow RISC-V registers are:
 $a \Leftrightarrow x1$, $b \Leftrightarrow x2$, $c \Leftrightarrow x3$

■ Subtraction in Assembly

- Example: **sub** **x3, x4, x5** (in RISC-V)
 - Equivalent to: $d = e - f$ (in C)
 - where C variables \Leftrightarrow RISC-V registers are:
 $d \Leftrightarrow x3, e \Leftrightarrow x4, f \Leftrightarrow x5$

Addition and Subtraction of Integers (3/4)

- How to do the following C statement?

$$a = b + c + d - e;$$

- Break into multiple instructions

add x10, x1, x2 # a_temp = b + c

add x10, x10, x3 # a_temp = a_temp + d

sub x10, x10, x4 # a = a_temp - e

- Notice: A single line of C may break up into several lines of RISC-V.

- Notice: Everything after the hash mark on each line is ignored (comments).

Addition and Subtraction of Integers (4/4)

- How do we do this?

$$f = (g + h) - (i + j);$$

- Use intermediate temporary register

```
add x5, x20, x21 # a_temp = g + h
```

```
add x6, x22, x23 # b_temp = i + j
```

```
sub x19, x5, x6 # f = (g + h) - (i + j)
```

- A good compiler may do:

RISC-V

Immediates

- Immediates are numerical constants.
- They appear often in code, so there are special instructions for them.
- Add Immediate:
addi $x_3, x_4, 10$ (in RISC-V)
 $f = g + 10$ (in C)
 - where RISC-V registers x_3, x_4 are associated with C variables f, g
- Syntax similar to add instruction, except that last argument is a number instead of a register.

- There is no Subtract Immediate in RISC-V: Why?
 - There are **add** and **sub**, but no **addi** counterpart
- Limit types of operations that can be done to absolute minimum
 - if an operation can be decomposed into a simpler operation, don't include it
 - **addi ...,-x** = "subi ..., x" => so no "subi"
addi x3,x4,-10 (in RISC-V)
 $f = g - 10$ (in C)
 - where RISC-V registers **x3, x4** are associated with C variables f, g, respectively

Register Zero

- One particular immediate, the number zero (0), appears very often in code.
- So the register zero (**x0**) is 'hard-wired' to value 0; e.g.

add x3, x4, x0 (in RISC-V)

$f = g$ (in C)

- where RISC-V registers **x3, x4** are associated with C variables f, g
- Defined in hardware, so an instruction **add x0, x3, x4** will not do anything!