I²C Master Star

Revision History

Date	Revision	Revision
2010-01-28	Initial release	1.0
2010-07-22	Revised text. Added wormhole description	1.1
2012-12-12	The core of the I2C Master is changed to allow for multi-byte I2C cycles.	1.2
2015-01-29	Added chapter explaining star instantiation options. Added the reserved register 2 for the write acknowledge.	1.3
2015-04-02	Added the VC707 XDC file and updated control register 0x2.	1.4
2015-11-19	Added the sFMC820 XDC file.	1.5

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1 Introduction

This document gives the description of the I²C master star. The main features are:

- I²C Master 1, 2, 3 or 4 byte write access
- I²C Master 1, 2, 3 or 4 byte read access
- Selectable slave address through Stellar IP command
- Selectable sub address through Stellar IP command

2 Firmware Architecture

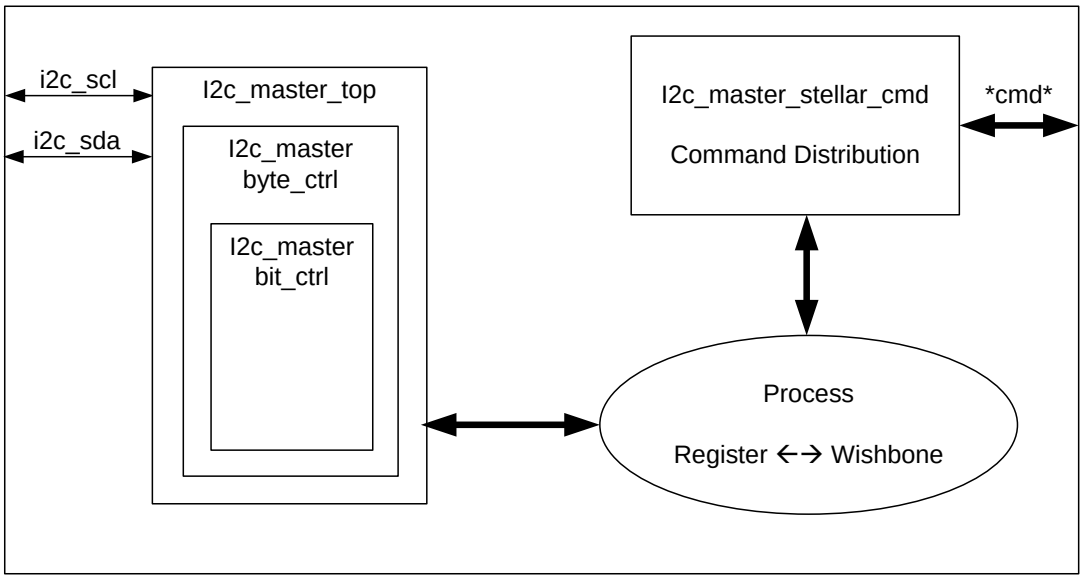

Figure 1: Firmware architecture

3 Star instantiation options

Depending on the target hardware configuration, it may be required to use different source and constraint files. This is supported by StellarIP through the .lst file. In most cases a different FPGA family requires a different FPGA type. Below is a list of the current lst files and their intended usage.

Table 1: Available lst files

File name	Target board	Description
sip_i2c_master.lst	All boards	This file works for all target boards

In StellarIP, the star index is used to target a specific UCF or XDC file for the star. StellarIP always searches for the UCF or XDC file that starts with the constellation name followed by target board name and then the star index. Not all possible combinations are available, but it does not necessarily mean a specific board/FPGA type cannot be supported.

Table 2: Available UCF files

File name	Target board	Target FMC Site/daughter card	Target FPGA type
sip_i2c_master_fc6301_0.ucf	FC6301	FMC 0	LX240T, LX365T, SX315T, SX475T, LX550T
sip_i2c_master_fm482_0.ucf	FM482	ADC250	LX80, SX55
sip_i2c_master_fm482_3.ucf	FM482	ADC224	LX80, SX55
sip_i2c_master_fm482_4.ucf	FM482	ADC250 Rear_fm_adapter	LX80, SX55
sip_i2c_master_fm489_0.ucf	FM489	ADC224	LX110T
sip_i2c_master_fm489_1.ucf	FM489	ADC110	LX110T
sip_i2c_master_fm680_0.ucf	FM680	ADC250	LX240T, LX365T, SX315T, SX475T, LX550T
sip_i2c_master_fm680_1.ucf	FM680	ADC110	LX240T, LX365T, SX315T, SX475T, LX550T
sip_i2c_master_fm680_2.ucf	FM680	FMC 0	LX240T, LX365T, SX315T, SX475T, LX550T
sip_i2c_master_fm780_0.ucf	FM780	FMC 0	X485T, X690T, X980T
sip_i2c_master_kc705_0.ucf	KC705	FMC HPC/LPC	K325T
sip_i2c_master_ml605_0.ucf	ML605	FMC HPC	LX240T
sip_i2c_master_ml605_1.ucf	ML605	FMC LPC	LX240T
sip_i2c_master_sp601_0.ucf	SP601	FMC 0	LX16
sip_i2c_master_sp605_0.ucf	SP605	FMC 0	LX45
sip_i2c_master_vc707_0.ucf	VC707	FMC HPC 1/2	X485T
sip_i2c_master_vc709_0.ucf	VC709	FMC	X690T
sip_i2c_master_vp680_0.ucf	VP680	FMC 0	LX130T, LX240T, LX365T, SX315T
sip_i2c_master_vp780_0.ucf	VP780	FMC 0	X485T, X690T, X980T
sip_i2c_master_zc702_0.ucf	ZC702	FMC LPC 1/2	Z020
sip_i2c_master_zc706_0.ucf	ZC706	FMC HPC/LPC	Z045
sip_i2c_master_zedb_0.ucf	ZEDBOARD	FMC HPC	Z020

For constellations that are targeting Vivado the star offers XDC files. The following table shows which XDC files are available and when they should be used.

Table 3: Available XDC files

File name	Target board	Target FMC Site	Target FPGA type
sip_i2c_master_kcu105_0.xdc	KCU105	FMC HPC/LPC	XCKU040
sip_i2c_master_vp780_0.xdc	VP780	FMC 0	X1140T
sip_i2c_master_kc705_0.xdc	KC705	FMC HPC/LPC	K325T
sip_i2c_master_fm780_0.xdc	FM780	FMC 0	X1140T
sip_i2c_master_vc707_0.xdc	VC707	FMC HPC 1/2	X485T
sip_i2c_master_sfmc820_0.xdc	sFMC820	FMC 0	XCKU040

4 Wormhole descriptions

4.1 Rst wormhole of type rstin

Signal Name	Direction	Width	Description
Rstin	Input	32	A vector that carries several reset signals. The I2C master star uses the following signals from the vector: Rstin(2) = reset for the command in and command out interface.

4.2 Cmdclk_in wormhole of type cmdclk_in

Signal Name	Direction	Width	Description
Cmdclk	Input	1	Command wormholes are synchronous to this clock.

4.3 Cmd_in wormhole of type cmd_in

Signal Name	Direction	Width	Description
Cmdin	Input	64	This signal caries the incoming command data packet [63..60] = command word [59..32] = address [31..0] = data
Cmdin_val	Input	1	When asserted high the cmdin carries a valid command packet.

4.4 Cmd_out wormhole of type cmd_out

Signal Name	Direction	Width	Description
Cmdout	Output	64	This signal caries the outgoing response data packet [63..60] = command word [59..32] = address [31..0] = data
Cmdout_val	Output	1	When asserted high the cmdout carries a valid response packet.

4.5 Ext_i2c wormhole of type ext_i2c

Signal Name	Direction	Width	Description
i2c_scl	Inout	1	I2C clock
i2c_sda	Inout	1	I2C data

4.6 Generic wormhole of type generic_def

Generic Name	Direction	Width	Description
global_start_addr_gen	N.A.	28	Start of the global address range of the constellation. All stars may act on a register access to the global address range.
global_stop_addr_gen	N.A.	28	End of the global address range of the constellation. All stars may act on a register access to the global address range.
private_start_addr_gen	N.A.	28	Start of the private address range of the star. The star may act on a register access to the private address range.
private_stop_addr_gen	N.A.	28	End of the private address range of the star. The star may act on a register access to the private address range.

5 Internal generics

In the star top level two generics are defined on the instantiation of the I²C master. These generics are preset to working values and should not be changed.

5.1 Generic parameter PRER - Clock Prescale Register

This register is used to prescale the SCL clock line. Due to the structure of the I²C interface, the core uses a 4*SCL clock internally. The prescale register must be programmed to this 4*SCL bit rate.

Example: CLK = 125MHz, desired SCL = 100kHz

Prescale = 125MHz / (4 * 100 kHz) = 312 (dec)

5.2 Generic parameter CTRL – Control Register

Bit 7 = I²C core enable bit

Bit 6 = I²C core interrupt enable bit

Bit 5:0 = Reserved

This value should be 0x80 (hex) = 128 (dec)

6 Registers Map

The I²C master core uses a 16-bit address range from private_start_addr_gen to private_stop_addr_gen. Within this range the I²C slave can be selected and the I²C slaves sub addresses can be selected. For example to write address 0x15 in an I²C slave with slave address 0x51 the register offset is calculated as follows:

private_start_addr_gen + (I²C Slave address << 8) + I²C Slave sub address

The address field (excluding the I²C master star offset) is build up as follows:

31 ..16	15	14..8	7..0
0	0	I²C Slave address	I²C Sub address

The data field is build up as follows:

31..24	23..16	15..8	7..0
I²C data byte 3	I²C data byte 2	I²C data byte 1	I²C data byte 0

The following registers addresses are reserved:

- Address 0x00000000 is reserved for PRER value. Default value = 0xF9.
- Address 0x00000001 is reserved for BYTE, selecting the number of data bytes in an I2C cycle (0 = 1 byte, 1 = 2 byte, 2 = 3 byte, 3 = 4 byte). Default value = 0.
- Address 0x00000002 is reserved for:
    - Bit0: enabling write acknowledge. When bit 1 is set the star will return a write acknowledge as soon as the I2C command finishes. Default value is write acknowledge off (0). This bit is legacy functionality. The I2C master, star revision 1.1 and higher, by default returns a write acknowledge when it receives a “write request ack” command from the sip command master or host interface.
    - Bit1: enabling direct read mode. By default this bit is set to ‘0’ which means that the I2C master always starts with a I2C write command to prepare the slave device for a read back. Some devices don’t support this write execution and should be read back immediately. To support those devices, set this bit to ‘1’ and the I2C master will directly execute a read command to the addressed slave.