FMC216 8Lane
A/D Daughter Card

Revision History

Date	Revision	Revision
2015-08-31	Initial Release	1.0
2016-03-16	Added 0x8 register for trigger out	1.1

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Table of Contents

1 Introduction

This document gives the description of the firmware Star FMC216 8lane. The main features are:

- 16 channel D/A conversion at 312.5 Msps*
- Channel control (enable/disable D/A)
- Burst control (number of bursts, burst size)
- Clock & Trigger control (internal/external source)

* Sampling rate can vary depending on configuration settings

2 Firmware Architecture

This firmware is designed to communicate with four DACs configured for JESD204B L=2, M=4,F=4, S=1,HD=0. Since each of the 4 DACs are configured as L=2 that gives a total of 8 tranceiver lanes being used.

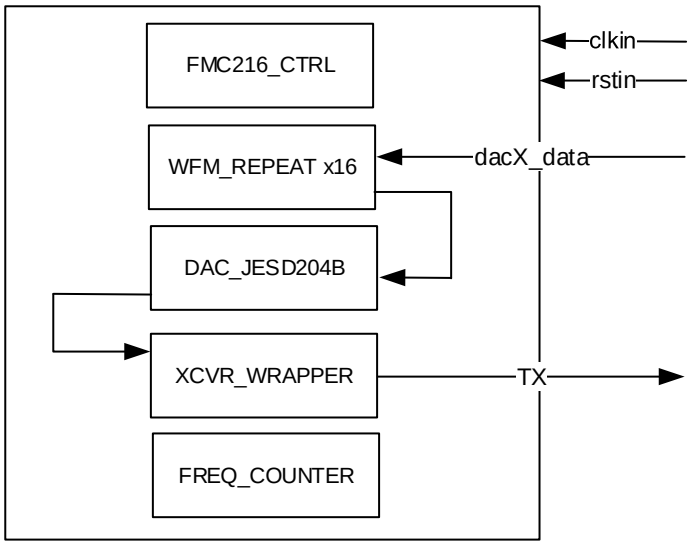

Figure 1: Firmware architecture

2.1 Example Configuration

For proper operation three devices need to be configured; the FPGA, the clocking chip and the DAC device. First the FPGA transceiver must be properly set to the desired line-rate, as an example the VC707 has a tranceiver line-rate limit of 10.3125 Gbps so we set this line-rate. Due to 10b/8b decoding this allows for 1.03125 GBytes/sec per lane. Each sample is 2 bytes so we get 515.625 Samples/Sec per lane. Each IC device is configured to use 2 lanes giving us 1031.25 Samples/sec per device. Each device has four DACs so we can send maximum of 1031.25/4 = 257.8125 Million Samples/second per converter on the VC707.

We use interpolation of x2 and get a sampling rate of 515.625 MSPS. The LMK clock device on the FMC216 needs to be configured to send out a 515.625 MHz sampling clock to each device and a 257.8125 MHz reference clock to the FPGA that will be used by all 8 transceivers. The reference clock can be anything supported by the FPGA PLL circuitry.

The configuration of the DAC can be involved please see the DAC39J84 datasheet for details, but as an example the following process is what is involved. You start with a line-rate (10.3125 Gbsps), DAC sampling rate (515.625 with x2 interpolation), and the JESD204B configuration (L=2, M=4,F=4, S=1,HD=0). The SerDes PLL is first configured, it must be set within a range of 1.5 GHz -3.15 GHz using either the DAC CLK or the internal DAC PLL. In this example we use the DAC CLK which is 515.625 MHz. We run the SerDes at full rate meaning the SerDes clock must be 0.25 the line-rate (10315.5 *.25 = 2578.125). To get there we divide the DAC CLK by 2 and get 257.812 and set the multiply factor (MPY) to 10. If the transceiver is working this alone causes the SerDes PLL to lock and the DAC can properly communicate with the FPGA. Next you configure the JESD settings L,M,F,S,HD, the interpolation is set to 2. Set JESDCLK_DIV given by the formula (interpolation * L / M) = 2 * 2 / 4 = 1. Please see device datasheets for further setting details.

2.2 Waveform Loading

To load a waveform you perform the following steps

1.	Se the number of bursts	0x0000002	0x1	1 burst
2.	Set the burst size	0x0000003	0x200	512 Samples
3.	Enable DACx	0x0000001	0xFFFF	enable all 16 channels
4.	WFM Load	0x0000000	0x8	Configure the waveform memories to accept data
5.	Send Data	DMA Write		Send 512 samples to each waveform memory.
6.	ARM	0x0000000	0x1	Continously playback samples

3 Star instantiation options

Depending on the target hardware configuration, it may be required to use different source and constraint files. This is supported by StellarIP through the .lst file. In most cases a different FPGA family requires a different FPGA type. Below is a list of the current lst files and their intended usage.

Table 1: Available lst files

File name	Target board	Description
sip_fmc216_8lane_vivado.lst	VC707	This lst file is required when targeting boards with a V7 (485t) FPGA .

In StellarIP, the star index is used to target a specific UCF or XDC file for the star. StellarIP always searches for the UCF or XDC file that starts with the constellation name followed by target board name and then the star index. Not all possible combinations are available, but it does not necessarily mean a specific board/fpga type cannot be supported.

Table 2: Available Constraint files

File name	Target board	Target FMC Site	Target FPGA type
sip_fmc216_8lane_vc707_0.xdc	VC707	FMC1 HPC	X485T

4 Wormhole descriptions

4.1 Rst wormhole of type rst_in

Signal Name	Direction	Width	Description
Rstin	Input	32	A vector that carries several reset signals. The FMC14x star uses the following signals from the vector: Rstin(2) = reset for all the internal logic.

4.2 Clk wormhole of type clkin

Signal Name	Direction	Width	Description
Clkin	Input	32	This is a vector that carries several clock signals. The FMC14x star uses none of these clock signals.

4.3 Cmdclk_in wormhole of type cmdclk_in

Signal Name	Direction	Width	Description
Cmdclk	Input	1	Command and data wormholes are synchronous to this clock.

4.4 Cmd_in wormhole of type cmd_in

Signal Name	Direction	Width	Description
Cmdin	Input	64	This signal caries the incoming command data packet [63..60] = command word [59..32] = address [31..0] = data
Cmdin_val	Input	1	When asserted high the cmdin carries a valid command packet.

4.5 Cmd_out wormhole of type cmd_out

Signal Name	Direction	Width	Description
Cmdout	Output	64	This signal caries the outgoing response data packet [63..60] = command word [59..32] = address [31..0] = data
Cmdout_val	Output	1	When asserted high the cmdout carries a valid response packet.

4.6 DACx wormhole of type wh_in

The DACx wormhole accepts 4 16-bit samples in each 64-data bus that is synchronised to the cmd_clk clock domain.

Signal Name	Direction	Width	Description
dacX_stop	Input	1	Out_stop is asserted by the receiving star when its internal FIFO is almost full. The FMC14x star will stop transferring data to the receiving star when out_stop is asserted.
dacX_dval	Output	1	Asserted when out_data holds valid data that needs to be written to the receiving star.
dacX_data	Output	64	Output data bus.

4.7 Ext_FMC144

Signal Name	Direction	Width	Description
ext_trigger_n/p	In	1	Representation of the signal connected to the external trigger input.
refclk_n/p	In	2	Reference clock used by the transceivers
serdin_n/p	In	8	RX transceiver data
serdout_n/p	Out	8	TX transceiver data
dac_syncb_n/p	Out	4	JESD SYNCB signal for DACs

pg_m2c	In	1	Active high signal that indicates all FMC power supplies are within valid range
prsnt_m2c_l	In	1	Active low signal indicating that an FMC is present.
lmkclk_n/p	In	1	Clock coming into FPGA from LMK chip
lmk_sync	Out	1	Sync signal going from FPGA to LMK chip

4.8 Generic wormhole of type Generic_def

Generic Name	Direction	Width	Description
global_start_addr_gen	N.A.	28	Start of the global address range of the constellation. All stars may act on a register access to the global address range.
global_stop_addr_gen	N.A.	28	End of the global address range of the constellation. All stars may act on a register access to the global address range.
private_start_addr_gen	N.A.	28	Start of the private address range of the star. The star may act on a register access to the private address range.
private_stop_addr_gen	N.A.	28	End of the private address range of the star. The star may act on a register access to the private address range.

5 Registers Map

Register	Address	Description
FMC216_CTRL – 0x0		
COMMAND	0x0000000	**BIT 0:** Writing a '1' arms the selected DAC. Enables waveform repeat. This bit is self-clearing. **BIT 1:** Writing a '1'disarms the selected DAC. Disables the waveform repeat. This bit is self-clearing. **BIT 3**: Writing a '1' allows waveform loading . A data transfer to the board should follow. *** All these bits are self-clearing.
CONTROL	0x0000001	**BIT 0-BIT 15:** DACX waveform enable **BIT 17-16:** "00" - External trigger disabled, software trigger enabled "01" - Enable external trigger, rising edge sensitive "10" - Enable external trigger, falling edge sensitive "11" - Enable external trigger, both edge sensitive
NB_BURSTS	0x0000002	Number of burst to be acquired. Each burst has a size of BURST_SIZE and will be captured on a trigger event. One trigger event per burst is required.
BURST_SIZE	0x0000003	Number of samples per burst; 512, 1K, 2K, 4K, 8K, 16K, 32K
FMC_INFO	0x0000004	**BIT 0:** PRSNT M2C **BIT 1:** PG M2C
TRANSCEIVER_CTRL	0x0000005	**BIT 0:** Tranceiver Reset **BIT 4:** RXRESET_IN(0) **BIT 4:** RXRESET_IN(1) **BIT 5:** RXRESET_IN(2) **BIT 6:** RXRESET_IN(3) **BIT 7:** RXRESET_IN(4) **BIT 8:** RXRESET_IN(5) **BIT 9**: RXRESET_IN(6) **BIT 10:** RXRESET_IN(7) **BIT 11:** TXRESET_IN(0) **BIT 12:** TXRESET_IN(1) **BIT 13:** TXRESET_IN(2) **BIT 14:** TXRESET_IN(3) **BIT 15:** TXRESET_IN(4) **BIT 16:** TXRESET_IN(5) **BIT 17:** TXRESET_IN(6) **BIT 18:** TXRESET_IN(7)
STATUS	0x0000006	**BIT 0 - BIT 7:** PLL used for X transceiver locked **BIT 8 - BIT 15:** Tranceiver X Ready
DAC_CTRL	0x0000007	**BIT 5 - BIT 4:** Data Select 00 - Waveform Repeat Output 01 – Repeating pattern for DAC short pattern test

		10 – Fixed four point sine wave 11 – Waveform Repeat output with byte swap
FMC_CTRL	0x00000008	**BIT 0: SYNC Out** **BIT 3-1: Trigger Out Select** 000 - fmc_ctrl(0) 001 - test_count(5) 010 - test_count(4) 011 - sysref_bufg 100 - fmc_ctrl(4) 101 - lmkclk_bufg 110 - ext_trigger_buf
FREQ_CNT- 0x10		
SELECT	0x0000010	**BIT 0- 2:** "000" – Clock command "001" – Transceiver Clock "010" – SYSREF "011" – LMK Clock "100" – External Trigger
VALUE	0x0000011	Result of the frequency measurement. The frequency in MHz can be calculated as follows: `Fclk = Fref * (CNT + 1) / 8192` Fref is the reference clock in MHz which is 125 MHz.

6 I2C Device Communication

To save pins on the FMC connector an I2C interface is used to communicate with a CPLD on the FMC216 which has a SPI interface to communicate with each of the four DAC38j84s and the LMK04828. The CPLD address is defined as "00111" & GA1 & GA0, for the VC707 HPC1 this is "001_1100" (0x1C).

6.1 CPLD Register Map

Register	Address	Description
ADDR_COMMAND	0x00	Selects which device to communicate with. **BIT 0:** LMK04828 **BIT 1:** DAC38j84 DAC0 **BIT 2:** DAC38j84 DAC1 **BIT 3:** DAC38j84 DAC2 **BIT 4:** DAC38j84 DAC3 BIT 5-7: Reserved
ADDR_CONTROL0	0x01	**BIT 0:** osc100_en **BIT 1:** osc491_en **BIT 2:** reset_dacs_L **BIT 3:** lmk_reset **BIT 4-7: Reserved**

ADDR_CONTROL1	0x02	**BIT 0:** DAC0 Amplifier Sleep **BIT 1:** DAC1 Amplifier Sleep **BIT 2:** DAC2 Amplifier Sleep **BIT 3:** DAC3 Amplifier Sleep **BIT 4:** DAC0 Sleep **BIT 5:** DAC1 Sleep **BIT 6:** DAC2 Sleep **BIT 7:** DAC3 Sleep
ADDR_CONTROL2	0x03	**BIT 0:** DAC0 TX_EN **BIT 1:** DAC1 TX_EN **BIT 2:** DAC2 TX_EN **BIT 3:** DAC3 TX_EN **BIT 4:** sync_src_sel_0 **BIT 5:** sync_src_sel_1 **BIT 6:** ga0_cc_out **BIT 7:** ga1_cc_out
ADDR_STATUS_1	0x04	**BIT 0:** DAC0 ALARM **BIT 1:** DAC1 ALARM **BIT 2:** DAC2 ALARM **BIT 3:** DAC3 ALARM **BIT 4:** PMTA ALARM **BIT 5:** I2C GA0 **BIT 6:** I2C GA1 **BIT 7:** Reserved
ADDR_VERSION	0x05	0x10
ADDR_I2C_DATA_0	0x06	LSB byte to send to the selected SPI device
ADDR_I2C_DATA_1	0x07	2nd byte to send to the selected SPI device
ADDR_I2C_DATA_2	0x08	3rd byte to send to the selected SPI device
ADDR_I2C_DATA_3	0x09	MSB byte to send to the selected SPI device
ADDR_STATUS_2	0x0A	**BIT 0:** lmk_clkin_sel(0) **BIT 1:** lmk_clkin_sel(1)
ADDR_I2C_READ_0	0x0E	LSB byte read from SPI device
ADDR_I2C_READ_1	0x0F	MSB byte read from SPI device