Reversible Logic-Based Concurrently Testable Latches for Molecular QCA

Himanshu Thapliyal, *Student Member, IEEE*, and Nagarajan Ranganathan, *Fellow, IEEE*

***Abstract*—Nanotechnologies, including molecular quantum dot cellular automata (QCA), are susceptible to high error rates. In this paper, we present the design of concurrently testable latches (*D* latch, *T* latch, *JK* latch, and *SR* latch), which are based on reversible conservative logic for molecular QCA. Conservative reversible circuits are a specific type of reversible circuits, in which there would be an equal number of 1's in the outputs as there would be on the inputs, in addition to one-to-one mapping. Thus, conservative logic is parity-preserving, i.e., the parity of the input vectors is equal to that of the output vectors. We analyzed the fault patterns in the conservative reversible Fredkin gate due to a single missing/additional cell defect in molecular QCA. We found that if there is a fault in the molecular QCA implementation of Fredkin gate, there is a parity mismatch between the inputs and the outputs, otherwise the inputs parity is the same as outputs parity. Any permanent or transient fault in molecular QCA can be concurrently detected if implemented with the conservative Fredkin gate. The design of QCA layouts and the verification of the latch designs using the QCADesigner and the HDLQ tool are presented.**

***Index Terms*—Concurrent testing, conservative reversible logic, sequential circuits.**

I. Introduction

QUANTUM dot cellular automata (QCA) is one of the emerging nanotechnologies that exhibit a small feature size, high clock frequency, and ultra low-power consumption [1], [2]. QCA provides an alternative way of computation, in which the logic states ("0" and "1") are defined by the positions of the electrons. Due to the significant error rates in nanoscale manufacturing and nanotechnologies, including the QCA, there is a critical need to maintain extremely low device error rates [3]. In the manufacturing of QCA, defects can occur in the synthesis and deposition phases. However, defects are more likely to take place during the deposition phase [4]. *QCA devices are also prone to transient faults caused by thermodynamic effects, radiation, and other effects, as the energy difference between the ground and the excited state is small [13].*

To the best of our knowledge, the concurrent testing of faults in QCA and QCA-based sequential circuits has not been addressed in the literature. In this paper, we propose novel designs for concurrently testable latches for molecular QCA using conservative reversible logic. Reversible computation in a system can be performed only when the system comprises reversible gates. Reversible circuits do not lose information, and can generate unique output vector from each input vector and *vice versa* (i.e., there is a one-to-one mapping between the input and the output vectors). Landauer has shown that for irreversible logic computations, each bit of information lost generates $kT\ln 2$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed [7]. Bennett showed that $kT\ln 2$ energy dissipation would not occur if a computation is carried out in a reversible way [8]. The testing properties of reversible logic are utilized in a 1-D array of molecular QCA in [3], which is considered to be the earliest effort toward applying reversible logic in molecular QCA.

In this paper, we propose a class of novel designs for the implementation of concurrently testable sequential circuits for molecular QCA based on a special type of reversible logic called conservative reversible logic. In conservative reversible logic, in addition to one- to-one mapping, there would be an equal number of 1's in the outputs as there would be on the inputs. We performed the fault pattern study of conservative reversible Fredkin gate due to the single missing cell defect or the additional cell defect in QCA. We found that when there is a permanent fault due to the aforementioned defects, there is a parity mismatch between the inputs and the outputs of the Fredkin gate. Due to the parity-preserving property, any permanent or transient fault in molecular QCA that leads to parity mismatch can be concurrently detected. It is stated in [11], that multiple defects are difficult to detect; however, single fault detection can be effectively accomplished. Like in most of the existing works reported in the literature, our work is also based on *single missing/additional cell defect model.* We present several new designs for concurrently testable latches (*D* latch, *T* latch, *JK* latch, and *SR* latch) that are based on the reversible conservative Fredkin gate, and are applicable in molecular QCA. It is to be noted that in existing literature, the design of conventional irreversible latches for molecular QCA have been proposed [17], [19]; however, these designs are not concurrently testable. Thus, the main contribution of this paper is a class of concurrently testable latches for use in the design of concurrently testable complex sequential circuits in molecular QCA.

This paper is organized as follows. Section II presents the conservative reversible logic Fredkin gate, the basic QCA devices, and the QCA design of Fredkin conservative logic gate. Section III presents the discussions on QCA defects, related work, and concurrent testing. Section IV presents concurrently testable reversible latches. Section V describes the simulation conditions used to verify the designs along with simulation results, and the QCA layout of the proposed designs. Some conclusions are provided in Section VI.

Manuscript received November 10, 2008; revised February 25, 2009. First published June 10, 2009; current version published January 8, 2010. The review of this paper was arranged by Associate Editor D. Hammerstrom.

The authors are with the Department of Computer Science and Engineering, University of South Florida, Tampa, FL 33620-5399 USA (e-mail: hthapliy@cse.usf.edu; ranganat@cse.usf.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2009.2025038

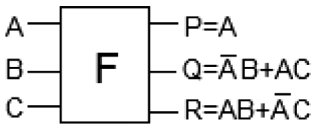

Fig. 1. Fredkin gate.

TABLE I
TRUTH TABLE OF FREDKIN GATE

A	B	C		P	Q	R
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	0	0
1	0	1		1	1	0
1	1	0		1	0	1
1	1	1		1	1	1

II. CONSERVATIVE REVERSIBLE FREDKIN GATE

The designs presented in this paper are based on conservative reversible (three inputs: three outputs) Fredkin gate shown in Fig. 1 [9]. Fredkin gate can be described as mapping (A, B, and C) to ($P = A, Q = \mathrm{A'B} + \mathrm{AC}$, and $R = \mathrm{AB} + \mathrm{A'C}$), where A, B, and C are the inputs, and P, Q, and R are the outputs, respectively. Table I shows the truth table of Fredkin Gate, and it can be seen that Fredkin gate produces the same number of 1's in the outputs as on the inputs, in addition to the one-to-one mapping feature of reversibility. Moreover, it is parity-preserving: its input parity is equal to the output parity. Before showing the QCA design of Fredkin gate, we present the QCA cell and the basic QCA logic devices: the majority voter (MV), the inverter (INV), binary wire, and the INV chain. Fig. 2 shows the QCA cell and the basic QCA devices.

The proposed designs are based on the Landauer four-phase clocking scheme, which is common in most QCA designs. A simple and elegant tutorial on QCA can be found in [5]. The QCA design of Fredkin gate is shown in Fig. 3 that uses the four-phase clocking scheme in which the clocking zone is shown by the number next to D (D0 means clock 0 zone, D1 means clock 1 zone, etc.).

III. BACKGROUND AND RELATED WORK

In the manufacturing of QCA, defects can occur during the synthesis and the deposition phase, more likely during the deposition phase [4]. Researchers assume that QCA cells have no manufacturing defects, and in metal, QCA faults occur due to cell misplacement. These defects can be characterized as cell displacement, cell misalignment, and cell omission [10]. Researchers have shown that molecular QCA cells are more susceptible to missing and additional QCA cell defects [11]. The additional cell defect is because of the deposition of an additional cell on the substrate, and the missing cell defect is due to the missing of a particular cell.

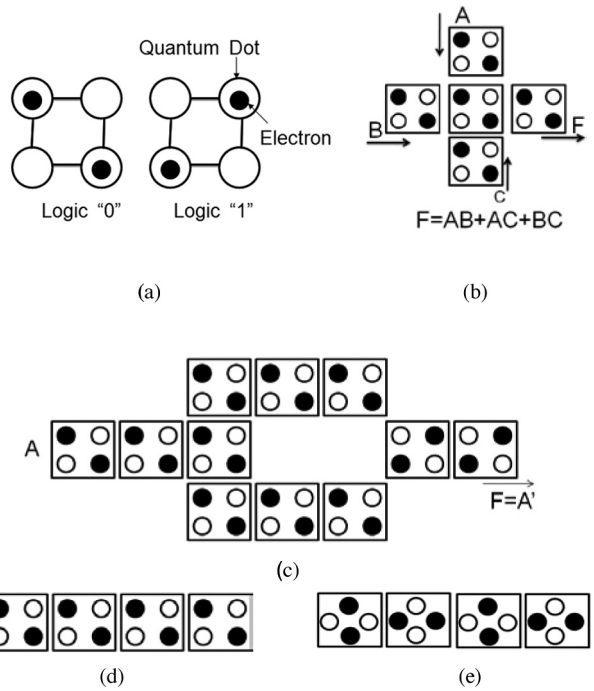

Fig. 2. Basic QCA devices. (a) QCA cell. (b) MV. (c) INV. (d) Binary wire. (e) INV chain.

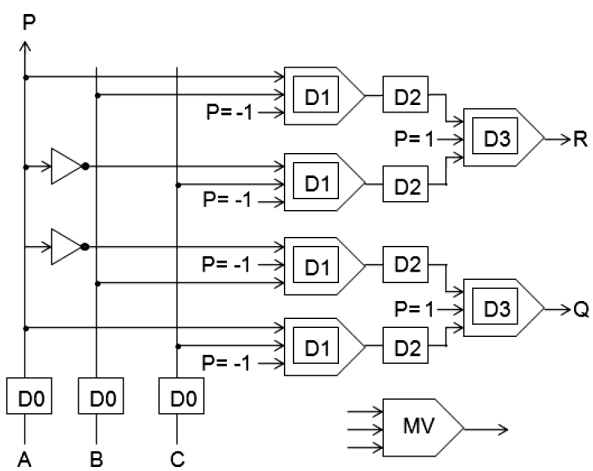

Fig. 3. Fredkin gate QCA design (D0–D3 represent clock zones 0–3).

A. Related Work

The testing of QCA was addressed for the first time in a seminal work reported in [4], where the defect characterization of QCA devices was investigated, and it was shown how the testing of QCA was different from conventional CMOS. The modeling of QCA defects at molecular level was done for combinational circuits in [11]. Fault characterization was done for single missing/additional cell defect on different QCA devices such as MV, INV, fan-out, crosswire, and L-shape wire. The test generation framework for QCA was presented in [10]. It was shown that additional test vectors can be generated for detecting QCA defects that remain undetected by the stuck-at fault model. Bridging fault on QCA wires was also addressed.

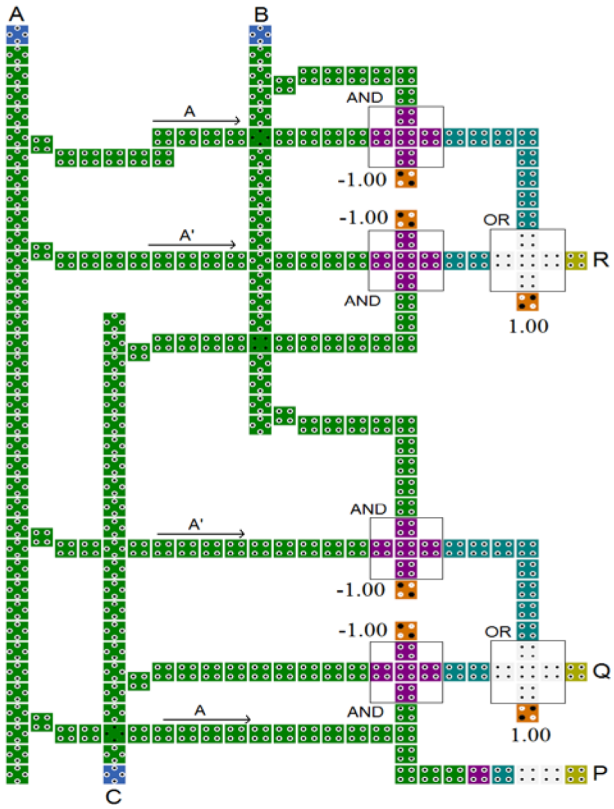

Fig. 4. QCA layout of Fredkin gate.

Reversible logic was proposed in [3] as a means to detect single missing/additional cell defects. It was shown that reversible 1-D array is C-testable. Fault-tolerant QCA designs were presented in [6] using triple-modular redundancy with shifted operands. The strategy considers the wire delay and the faults in the wires in QCA. The defect characterization and tolerance of the QCA SR latch, and the sequential circuit based on it were presented in [17] and [19]. The robust coplanar crossing in QCA was addressed in [22], and it was also proved that wires having rotated cells are thermally more stable. The exhaustive testing of single stuck-at faults (SSFs) in combinational logic is presented in [18]. There has been also numerous seminal works on the testing of reversible logic circuits such as those presented in [20] and [25], but they have not targeted fault testing of molecular QCA technology. Moreover, reversible sequential circuits are also discussed in existing literature such as [14]–[16], but none of these circuits are designed for molecular QCA and with concurrent testing in consideration. We have proposed two vector-testable reversible latches for molecular QCA in [21]. The work in [21] is based on stuck-at fault model and does not target concurrent testing of faults due to single missing/additional cell defects.

B. Concurrent Testing of Molecular QCA

The proposed QCA layout of the Fredkin gate is shown in Fig. 4. The Fredkin gate QCA layout is modeled to include the presence of all possible single missing/additional cell defects in MV, INV, fan-out, crosswire, and L-shape wire [11]. The modeling is done using HDLQ [12], a design tool that provides the Verilog hardware description language (HDL) library of QCA devices, i.e., MV, INV, fan-out, crosswire, and L-shape wire with fault injection capability. The design was simulated in Verilog HDL simulator in the presence of faults to determine the corresponding outputs. The exhaustive testing of the Fredkin gate with eight input patterns and all possible single missing/additional cell defects was performed using the Active HDL simulator. The exhaustive testing generated 20 unique fault patterns at the outputs, as shown in Table II. In the fault patterns study in Table II, ai is the 3-bit pattern having an equivalent decimal value of i, for example, a0 represents 000 (decimal 0) and a7 represents 111(decimal 7).

A careful observation of each fault pattern indicates that in the occurrence of a fault, there is parity mismatch between the outputs and the inputs of the Fredkin gate (i.e., parity of the input vector is not equal to the output vector). This led us to conclude that Fredkin gate can concurrently detect a permanent fault by matching the parity. Since Fredkin gate is logically parity-preserving, it can also detect the transient faults that result in parity mismatch between inputs and outputs. Hence, Fredkin gate can concurrently detect permanent, as well as transient fault based on parity preserving in molecular QCA.

IV. Design of Concurrently Testable Latches for Molecular QCA

In this section, we present the design of concurrently testable latches based on concurrently testable Fredkin gate.

A. D Latch

The characteristic equation of the D latch can be written as $Q^+ = DE + \bar{E}Q$. The equation can be mapped onto the Fredkin gate (F). Fig. 5(a) shows the design of the concurrently testable D latch using Fredkin gate. It is to be noted that fan-out is not allowed in reversible logic, but allowed in molecular QCA. Therefore, the design shown in Fig. 5(a) is valid for molecular QCA. However, it does not produce Q' (the complement of Q), which may be required in a number of places while designing the sequential circuits. Thus, we are also showing another design of D latch in Fig. 5(b), a design that also produces the complement output.

B. T Latch

The characteristic equation of the T latch can be written as $Q^+ = (T \oplus Q)E + \bar{E}Q$. However, the same result can also be obtained from $Q^+ = (TE) \oplus Q$. Fig. 6 shows the proposed design of concurrently testable T latch in which the first Fredkin gate produces (TE), and the second and third Fredkin gates generate $(TE) \oplus Q$ (second and third Fredkin gates together generate the XOR function).

C. JK Latch

The characteristic equation of the JK latch can be written as $Q^+ = (J\bar{Q} + \bar{K}Q)E + \bar{E}Q$. After computing the equation $J\bar{Q} + \bar{K}Q$, it can be mapped on the D Latch to design the JK

TABLE II
FAULT PATTERNS IN FREDKIN GATE

Input Vector	Fault Free	Fault Patterns																			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
a0	a0	a0	a0	a1	a1	a0	a0	a1	a2	a1	a1	a0	a2	a0	a2	a2	a0	a0	a0	a2	a4
a1	a1	a1	a1	a1	a1	a0	a1	a0	a1	a1	a1	a1	a3	a1	a3	a3	a3	a1	a3	a3	a5
a2	a2	a3	a2	a2	a3	a2	a0	a3	a2	a3	a3	a2	a0	a0	a2	a2	a2	a2	a2	a0	a6
a3	a3	a3	a3	a3	a3	a2	a1	a2	a1	a3	a3	a3	a1	a1	a3	a3	a3	a3	a3	a1	a7
a4	a4	a4	a5	a5	a5	a4	a4	a4	a4	a5	a4	a4	a4	a4	a4	a6	a4	a6	a4	a6	a0
a5	a6	a6	a7	a7	a7	a7	a6	a6	a6	a6	a6	a6	a6	a6	a6	a6	a4	a4	a6	a6	a2
a6	a5	a4	a4	a5	a4	a5	a5	a5	a5	a5	a5	a4	a5	a7	a5	a5	a5	a7	a5	a7	a1
a7	a7	a6	a6	a7	a6	a7	a7	a7	a7	a7	a7	a6	a7	a7	a7	a7	a5	a5	a7	a7	a3

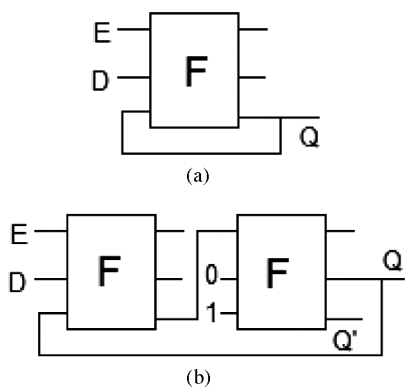

Fig. 5. Concurrently testable D latch design using Fredkin gates. (a) Fredkin D latch. (b) Fredkin D latch with complement output.

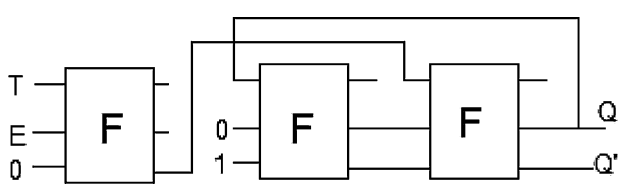

Fig. 6. Concurrently testable T latch design.

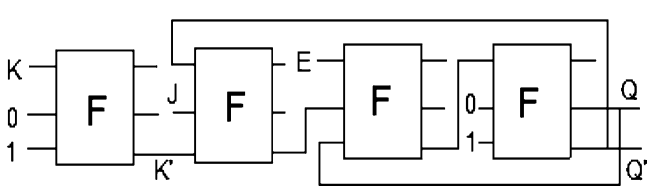

Fig. 7. Concurrently testable JK latch design.

Latch. Fig. 7 shows the proposed design of concurrently testable JK latch. The first Fredkin gate produces K', which is passed to the second Fredkin gate to generate $J\bar{Q} + \bar{K}Q$. The output $J\bar{Q} + \bar{K}Q$ produced by the second Fredkin gate is passed to the third and fourth Fredkin gates working as a D latch.

D. SR Latch

The characteristic equation of the SR latch can be written as $Q^+ = (S + \bar{R}Q)E + \bar{E}Q$. After computing the equation $S + \bar{R}Q$, it can be mapped on the D Latch to design the SR latch.

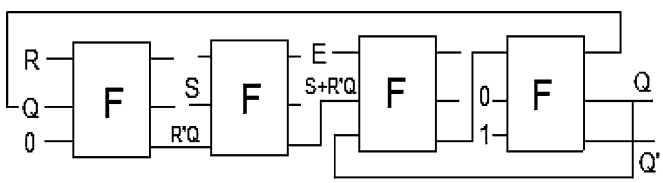

Fig. 8. Concurrently testable SR latch design.

Fig. 8 shows the proposed design of the concurrently testable SR latch. The first Fredkin gate produces $\bar{R}Q$, which is passed to the second Fredkin gate to produce $S + \bar{R}Q$. The $S + \bar{R}Q$ is passed to the third and fourth Fredkin gates working as a D latch to finally generate the SR latch.

V. SIMULATIONS FOR FUNCTIONAL VERIFICATION

All the designs were verified using QCADesigner version 2.0.3 [5]. In the bistable approximation, we used the following parameters: cell size = 18 nm, number of samples = 182 800, convergence tolerance = 0.001000, radius of effect = 41 nm, relative permittivity = 12.9, clock high = 9.8e − 22, clock low = 3.8e − 23, clock amplitude factor = 2.000, layer separation = 11.5000 nm, and maximum iterations per sample = 1000. In our QCA layouts, we set out to create workable designs with compact layouts. Each Fredkin gate in the layouts (in the critical path) will delay the output by one cycle since Fredkin gate is designed from four clocking zones (see Fig. 4). Fig. 9 shows the simulation results of the Fredkin gate QCA layout shown in Fig. 4, which has been verified using the QCADesigner tool, and it can be seen that the output is produced after a delay of one clock cycle, as the inputs are applied to the Fredkin gate at clock zone 0 while the outputs are available at clock zone 4 (the simulation waveforms is same as the truth table of Fredkin gate shown earlier in Table I that verifies the correctness of the design). An important objective in our designs was to ensure that the designs are practical and usable, and hence, through the QCA designer simulation, it was verified that the signals arrive properly without degradation. For example, in order to work correctly, all signals should arrive simultaneously at the QCA majority gate [23]. We also observed that there is a limit on the maximum number of QCA cells that can be connected to

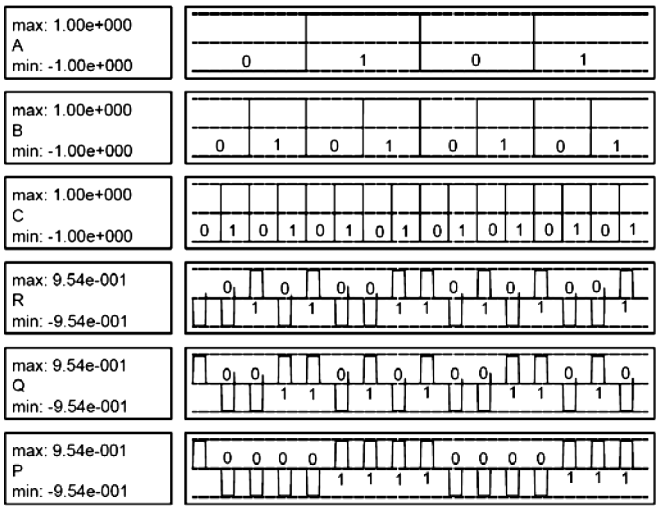

Fig. 9. Simulation of Fredkin gate.

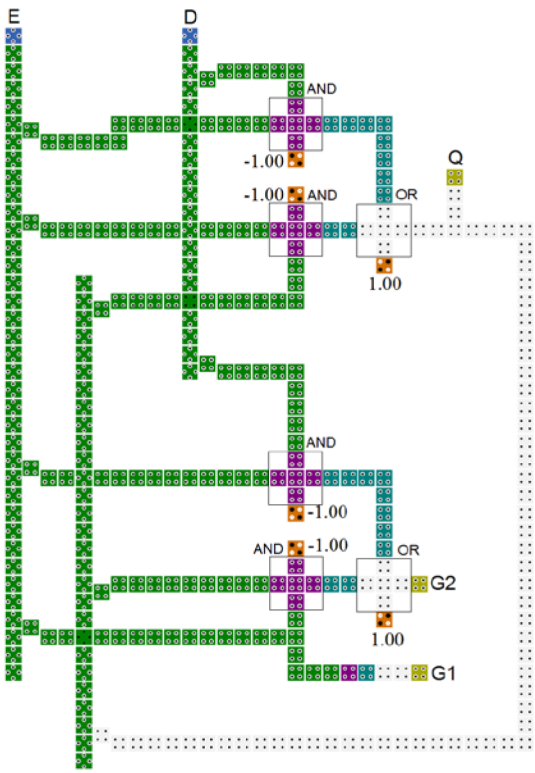

Fig. 10. QCA layout of D latch with output Q.

the same clock zone because the signal deteriorates beyond the limit.

A. QCA Layout and Simulation of Proposed Latches

Figs. 10 and 11 show the QCA layout and simulation of the D latch with output Q, but it does not produce the complement output (QBAR). In Fig. 11, the arrow A and arrow C show that when $D = 0$ and $E = 1$, we will have output as $Q = 0$ (the input $D = 0$ will be reflected in the output), and in the next cycle since $E = 0, Q$ will maintain its value of 0. Arrow B shows that when

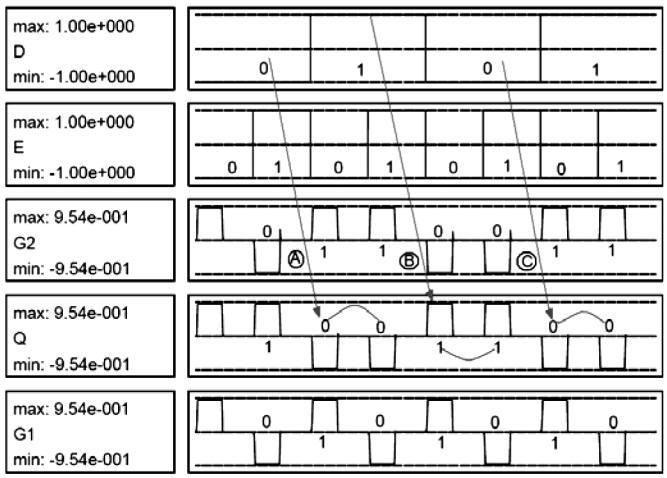

Fig. 11. Simulation of D latch with output Q.

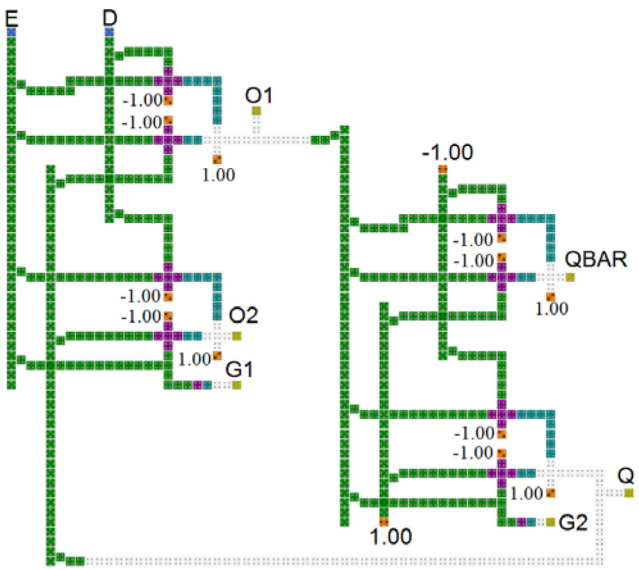

Fig. 12. QCA layout of D latch with output Q as well as complement output QBAR.

$E = 1$ and $D = 1, Q$ will become 1 (the value of $D = 1$ will be reflected in the output), and in the next cycle since $E = 0, Q$ will maintain its value 1. All the output will be delayed by one clock cycle as Fredkin gate has the output delayed by one clock cycle.

Figs. 12 and 13 show the QCA layout and simulation of the D latch with normal output Q, as well as the complement output QBAR. In Fig. 12, O1 and O2 represent the intermediate output. We have used the intermediate output so that the readers can better understand the simulation results, and the work can be reproduced by others (the actual output is named Q and QBAR). In Fig. 13, we get the correct output after the delay of two cycles after passing the input, as we have two Fredkin gates cascaded in series. Table III summaries the working of D latch having the output Q, as well as complement output QBAR (summarization of Fig. 11). The tip of the arrows A, C, and E in Fig. 13 represent that the value at the input D is reflected at the output Q after two

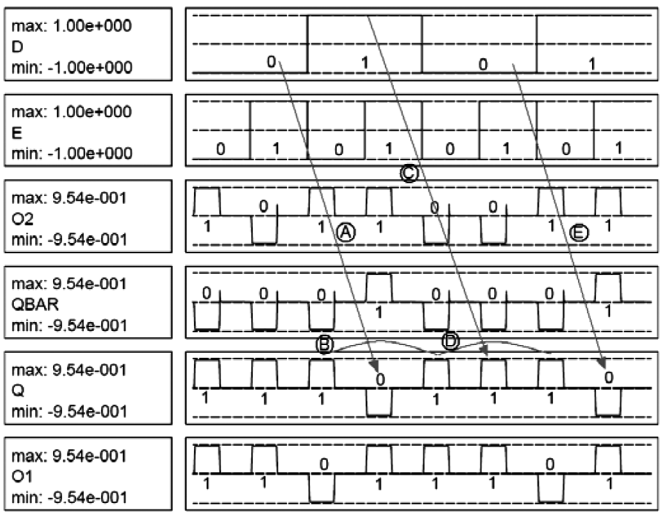

Fig. 13. Simulation of D latch with output Q and complement output QBAR.

TABLE III
VERIFICATION OF D LATCH

Arrow	Input	Output (after two cycles)
A	E=1 D=0 Q=1	Q=0
B	E=0 D=1 Q=1	Q=1
C	E=1 D=1 Q=0	Q=1
D	E=0 D=0 Q=1	Q=1
E	E=1 D=0 Q=1	Q=0

clock cycle delay. Arrows B and D represent that when $E = 0$, the output Q is same as the old value of Q (which is reflected two cycles after passing of inputs). This verifies the working of the D latch.

Figs. 14 and 15 show the QCA layout and simulation results of JK latch, respectively. We are providing the detailed analysis of JK latch QCA layout as it demonstrates special characteristic of QCA sequential circuits and the efforts required to design functionally correct sequential circuit in QCA. In the QCA layout of JK latch, YKB represents the complement of input K generated after a delay of one clock cycle. Now, the next Fredkin gate has three inputs: one of them is YKB, and others two are QBAR and J. Since YKB is produced after delay of one clock cycle; thus, in order to have all the input arrive simultaneously to the Fredkin gate to produce the correct result, we have delayed the input QBAR and J to the Fredkin gate by one clock cycle, as shown in Fig. 14. This produces $YJKQ$ output having the value as $JQ' + K'Q$ after a delay of two clock cycles. This is passed to the third Fredkin gate having other two input as E and Q. Since $YJKQ$ is available after the delay of two clock cycle, we have inserted two clock cycles delay to the input E and Q to make all the signals arrive simultaneously to the Fredkin gate. In the proposed JK latch, we will get the correct output after delay of four clock cycles, as four Fredkin gates forms the critical path to the output Q. Table IV summarizes the working of the JK latch, as shown in Fig. 15. Arrow A shows that when $J = 1$ and $K = 0$, output Q becomes 1, arrow B shows that when $J = 0$ and $K = 1$, we will get the output $Q = 0$, and arrow C shows

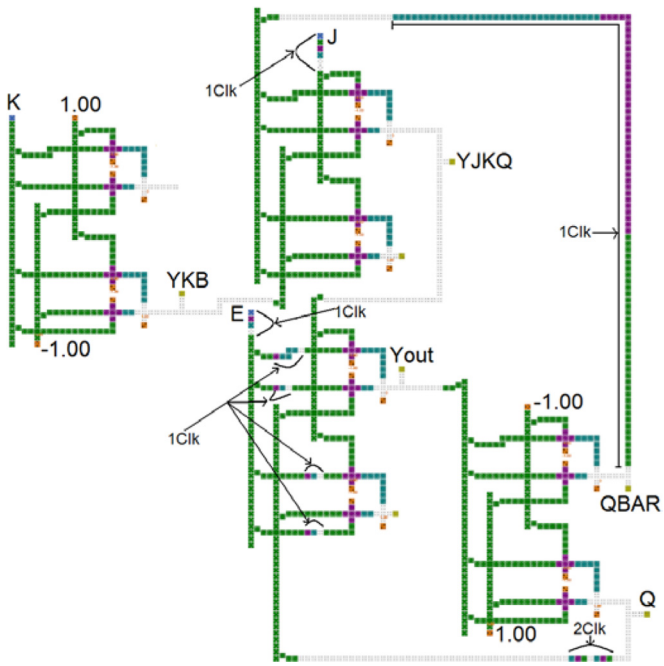

Fig. 14. QCA layout of JK latch.

TABLE IV
VERIFICATION OF JK LATCH

Arrow	Input	Output (after four clock cycles delay)
A	E=1 J=1 K=0 Q=1	Q=1
B	E=1 J=0 K=1 Q=1	Q=0
C	E=1 J=1 K=1 Q=1	Q=0

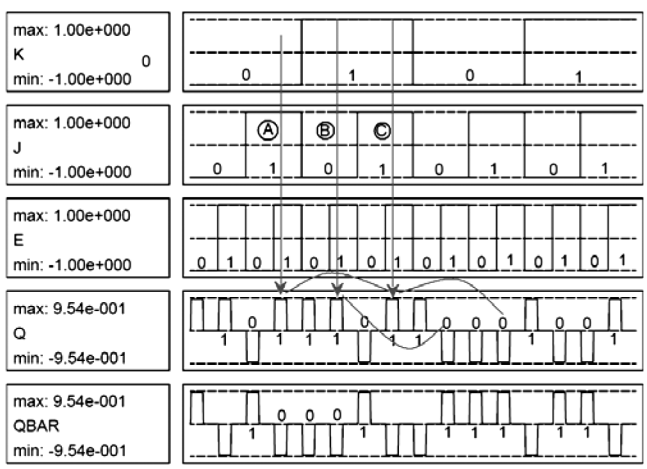

Fig. 15. Simulation of JK latch.

that when $J = 1$ and $K = 1$, the output toggles of its current value.

We simulated and verified the T latch and SR latch designs in QCADesigner tool. In the T latch, the output Q will reflect the input values after a delay of two clock cycles as the critical path to Q has two Fredkin gates. Similarly, in the SR latch, it takes four clock cycles to produce the correct output due to four

TABLE V
SUMMARY OF VERIFICATION OF LATCHES

	# of Fredkin Gates in Critical Path	# of Clock Cycles after which inputs reflect at outputs
D Latch with Output Q	1	1
D Latch without Fan-out	2	2
T Latch	2	2
JK Latch	4	4
SR Latch	4	4

Fredkin gates in the critical path. Table V shows the number of Fredkin gates in the critical path for various latches (each Fredkin gate in the critical path has a delay of one clock cycles, which means that having four Fredkin gates in the critical path will delay the output by four clock cycles). Thus, the number of clock cycles after which output Q reflects the values of inputs in various latches is shown in Table V.

As discussed in Section II, the QCA design of the Fredkin gate requires six MVs with four clocking zones. The Fredkin-gate-based D latch with enable signal having only the output Q requires one Fredkin gate for its design, as shown in Figs. 5(a) and 10, thus needing six MVs and four clocking zones. From Figs. 5 and 12, it can be seen that the D latch with enable signal having both Q and QBAR outputs requires two Fredkin gates for its design, thus requiring 12 MVs and eight clock zones. While the nontestable D latch design with enable signals converted from gate level schematic in [24] to its corresponding QCA design will require four MVs and four clock zones. The Fredkin-gates-based JK latch with enable signal shown in Figs. 7 and 14, has four Fredkin gates in its design, thus requiring a total of 24 MVs and eight clocking zones, while the nontestable design as converted from gate level schematic in [24] to its equivalent QCA design will require six MVs and four clocking zones. Thus, the advantages associated with proposed Fredkin-gate-based latches regarding concurrent testing come with some area overhead.

VI. CONCLUSION

We propose the use of conservative reversible logic based on Fredkin gate to design concurrently testable sequential circuits for molecular QCA. The proposed concurrent testing methodology is based on parity-preserving property of Fredkin gate, and is beneficial for both permanent and transient faults that results in parity mismatch between inputs and outputs. The concurrently testable designs for the latches (D latch, T latch, JK latch, and SR latch), their QCA layouts, and the simulation details are presented. The proposed approach is applicable for the concurrent detection of single missing/additional cell defect model or unidirectional faults. In unidirectional faults, there are only either $1 \rightarrow 0$ or $0 \rightarrow 1$ faults, and both types of faults cannot occur simultaneously. For unidirectional faults, comparing the number of 1's in the inputs with the number of 1's in the outputs could be used for fault detection. The proposed approach is not suitable for the detection of bidirectional multiple faults, for example, if we are expecting the outputs to be 011, but due to bidirectional faults, the outputs are flipped to 101, the parity of the outputs is still the same. We feel that one of the possible solutions to concurrently detect multiple faults is to regenerate the inputs at the outputs by using reversible logic. Since reversible logic has one-to-one mapping between the input and output vectors, it is possible to determine the inputs from the outputs. Thus, the regenerated inputs can be checked with the original inputs for the detection of multiple faults For example, in the Fredkin gate, if its outputs P, Q, and R are fed to another Fredkin gate cascaded in series, the original inputs will be regenerated at the outputs of the second Fredkin gate. This property of Fredkin gate can be beneficial for the detection of multiple faults, as multiple faults or single fault in either first or second Fredkin gate, or in both will result in incorrect values of regenerated inputs. Therefore, the original input vector can be compared with the regenerated input vector for detection of faults. We intend to direct our future efforts toward multiple fault detection in QCA computing. In conclusion, we have designed a class of novel latches for the implementation of concurrently testable sequential circuits for molecular QCA based on conservative reversible logic. The proposed paper will have impact on fault susceptible molecular QCA nanocomputing.

ACKNOWLEDGMENT

The authors would like to express their sincere thanks to the anonymous reviewers for their helpful suggestions that helped in improving the paper.

REFERENCES

[1] P. Tougaw and C. Lent, "Logical devices implemented using quantum cellular automata," *J. Appl. Phys.*, vol. 75, no. 3, pp. 1818–1825, 1994.
[2] A. O. Orlov, I. Amlani, G. H. Bernstein, C. S. Lent, and G. L. Snider, "Realization of a functional cell for quantum-dot cellular automata," *Science*, vol. 277, pp. 928–930, 1997.
[3] X. Ma, J. Huang, C. Metra, and F. Lombardi, "Reversible gates and testability of one dimensional arrays of molecular QCA," *Springer J. Electron. Testing*, vol. 24, no. 1–3, pp. 297–311, Jun. 2008.
[4] M. B. Tahoori, J. Huang, M. Momenzadeh, and F. Lombardi, "Testing of quantum cellular automata," *IEEE Trans. Nanotechnol.*, vol. 3, no. 4, pp. 432–442, Dec. 2004.
[5] QCADesigner. (2008). [Online]. Available: http://www.qcadesigner.ca/
[6] T. Wei, K. Wu, R. Karri, and A. Orailoglu, "Fault tolerant quantum cellular array (QCA) design using triple modular redundancy with shifted operands," in *Proc. 2005 Conf. Asia South Pacific Des. Autom.*, Shanghai, China, Jan., pp. 1192–1195.
[7] R. Landauer, "Irreversibility and heat generation in the computational process," *IBM J. Res. Dev.*, vol. 5, pp. 183–191, 1961.
[8] C. H. Bennett, "Logical reversibility of computation," *IBM J. Res. Dev.*, vol. 17, pp. 525–532, Nov. 1973.
[9] E. Fredkin and T. Toffoli, "Conservative logic," *Int. J. Theor. Phys.*, vol. 21, pp. 219–253, 1982.
[10] P. Gupta, N. K. Jha, and L. Lingappan, "A test generation framework for quantum cellular automata circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 1, pp. 24–36, Jan. 2007.
[11] M. Momenzadeh, M. Ottavi, and F. Lombardi, "Modeling QCA defects at molecular level in combinational circuits," in *Proc. DFT VLSI Syst.*, Monterey, CA, Oct. 2005, pp. 208–216.
[12] M. Ottavi, L. Schiano, and F. Lombardi, "HDLQ: A HDL environment for QCA design," *ACM J. Emerging Technol. Comput. Syst.*, vol. 2, no. 4, pp. 243–261, Oct. 2006.

[13] R. K. Kummamuru, A. O. Orlov, R. Ramasubramaniam, C. S. Lent, G. H. Bernstein, and G. L. Snider, "Operation of a quantum-dot cellular automata (QCA), shift registers and analysis of errors," *IEEE Trans. Electron. Devices*, vol. 50, no. 9, pp. 1906–1913, Sep. 2003.
[14] H. Thapliyal and A. P. Vinod, "Design of reversible sequential elements with feasibility of transistor implementation," in *Proc. 2007 IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, May, 2010, pp. 625–628.
[15] M. L. Chuang and C. Y. Wang, "Synthesis of reversible sequential elements," in *Proc. 2007 IEEE Asia South Pacific Des. Autom. Conf.*, Yokohama, Japan, pp. 420–425.
[16] J. E. Rice, "A new look at reversible memory elements," in *Proc. 2006 Int. Symp. Circuits Syst.*, Kos, Greece, May, pp. 243–246.
[17] M. Momenzadeh, J. Huang, and F. Lombardi, "Defect characterization and tolerance of QCA sequential devices and circuits," in *Proc. Defect Fault Tolerance VLSI Syst.*, Oct. 2005, pp. 199–207.
[18] S. Sultana, S. A. Imam, and K. Radecka, "Testing QCA modular logic," in *Proc. 13th IEEE Int. Conf. Electron., Circuits Syst.*, Nice, France, Dec. 2006, pp. 700–703.
[19] J. Huang, M. Momenzadeh, and F. Lombardi, "Analysis of missing and additional cell defects in sequential quantum-dot cellular automata," *Integr., VLSI J.*, vol. 40, no. 1, pp. 503–515, Jan. 2007.
[20] K. N. Patel, J. P. Hayes, and I. L. Markov, "Fault testing for reversible circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 8, pp. 1220–1230, Aug. 2004.
[21] H. Thapliyal and N. Ranganathan, "Testable reversible latches for molecular QCA," in *Proc. 8th IEEE Int. Conf. Nanotechnol.*, Arlington, VA, Aug. 2008, pp. 699–702.
[22] S. Bhanja, M. Ottavi, S. Pontarelli, and F. Lombardi, "Novel designs for thermally robust coplanar crossing in QCA," in *Proc. 2006 Des. Autom. Test Eur.*, Munich, Germany, Mar., pp. 786–791.
[23] K. Kim, K. Wu, and R. Karri, "Quantum-dot cellular automata design guideline," *IEICE Trans. Fund.*, vol. E89-A, no. 6, pp. 1607–1614, Jun. 2006.
[24] S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, 2nd ed. New York: McGraw-Hill, 1999, pp. 326–335.
[25] D. P. Vasudevan, P. K. Lala, and J. P. Parkerson, "Reversible-logic design with online testability," *IEEE Trans. Instrum. Meas.*, vol. 55, no. 2, pp. 406–414, Apr. 2006.

Himanshu Thapliyal (S'08) received the B.Tech. degree in computer engineering from G.B. Pant University of Agriculture and Technology, Pantnagar, India, in 2004, and the M.S. (by research) degree in very large-scale-integrated (VLSI) and embedded system technologies from the International Institute of Information Technology (IIIT), Hyderabad, India, in 2006. He is currently working toward the Ph.D. degree at the Department of Computer Science and Engineering, University of South Florida, Tampa.

For one year, he was a Research Assistant in the School of Computer Engineering, Nanyang Technological University, Singapore, where he was engaged in reversible/adiabatic computing at metal–oxide–semiconductor level. He has authored or coauthored more than 25 reviewed conferences and journal papers. He is a Reviewer of the Springer Journals, the World Scientific Journals, and the Association for Computing Machinery (ACM) Transactions. His current research interests include reversible logic, conservative logic, emerging technologies, Vedic mathematics, design of efficient arithmetic units, design of field-programmable gate array (FPGA) architectures for emerging nanotechnologies, and FPGA-based system design.

Mr. Thapliyal is a Reviewer of the IEEE Transactions, and various other prestigious conferences. He has delivered invited talks in the area of Vedic mathematics and reversible logic. He received the Distinguished Graduate Achievement Award by the Graduate and Professional Student Council, University of South Florida, in March 2009, for his outstanding academic and research accomplishments. Two of his research publications were student best paper award finalist at the Midwest Symposium on Circuits and Systems (MWSCAS) 2006. He was the Workshop Co-Chair of the First International Workshop on Future Computing (FC 2006), Las Vegas, NV. He was awarded Rs. 100 000 by the State Government of Uttaranchal, India, for his research on Vedic mathematics.

Nagarajan Ranganathan (S'81–M'88–SM'92–F'02) received the B.E. (Hons.) degree in electrical and electronics engineering from the Regional Engineering College (National Institute of Technology), Tiruchirapalli, India, in 1983, and the Ph.D. degree in computer science from the University of Central Florida, Orlando, in 1988.

From 1998 to 1999, he was a Professor of electrical and computer engineering at the University of Texas at El Paso, El Paso. He is currently a Distinguished University Professor of computer science and engineering at the University of South Florida (USF), Tampa. He has developed many special-purpose very large-scale-integrated (VLSI) circuits and systems for computer vision, image and video processing, pattern recognition, data compression, and signal processing applications. He has authored or coauthored more than 240 papers in refereed journals and conferences, four book chapters and holds six U.S. patents and two pending. He has edited three books titled: VLSI *Algorithms and Architectures: Fundamentals, VLSI Algorithms and Architectures: Advanced Concepts* (IEEE CS Press, 1993), *VLSI for Pattern Recognition and Artificial Intelligence* (World Scientific, 1995). He has coauthored a book titled: *Low Power High Level Synthesis for Nanoscale CMOS Circuits* (Springer-Verlag, June 2008). He was a member of the editorial boards for the *Pattern Recognition* (1993–1997) and the *VLSI Design* (1994–present), and the *Association for Computing Machinery (ACM) Transactions on Design Automation of Electronic Systems* (2007–2009). His current research interests include VLSI circuit and system design, VLSI design automation, multimetric optimization in hardware and software systems, bioinformatics, computer architecture, and parallel computing.

Prof. Ranganathan was a Fellow of the IEEE in 2002 for his contributions to algorithms and architectures for VLSI systems. He is a member of the IEEE Computer Society, the IEEE Circuits and Systems Society, and the VLSI Society of India. He has been a member of the editorial boards of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (1997–1999), the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY (1997–2000), the IEEE TRANSACTIONS ON COMPUTERS (2008–2010), and the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS (2008–2010). From 1997 to 2001, he was the Chair of the IEEE Computer Society Technical Committee on VLSI. He was a member of the Steering Committee of the IEEE TRANSACTIONS ON VERY LARGE-SCALE-INTEGRATED (VLSI) SYSTEMS from 1999 to 2001, the Steering Committee Chair from 2002 to 2003, and the Editor-in-Chief for two consecutive terms from 2003 to 2007. He was the Program Co-Chair for International Conference on VLSI Design (ICVLSID)'94, IEEE Computer Society Annual Symposium on VLSI (ISVLSI)'96, ISVLSI'05, and ICVLSID'08 and the General Co-Chair for ICVLSID'95, IWVLSI'98, ICVLSID'98, ISVLSI'05, and ISVLSI'09. He was a member of the Technical Program Committees of International Conferences including the International Conference on Computer Design (ICCD), the International Conference on Parallel Processing (ICPP), the International Parallel Processing Symposium (IPPS), the Symposium on Parallel and Distributed Processing (SPDP), the International Conference on High Performance Computing (ICHPC), the International Symposium on High-Performance Computer Architecture (HPCA), the Great Lakes Symposium on VLSI (GLSVLSI), the International Symposium on Asynchronous Circuits and Systems (ASYNC), the International Symposium on Quality Electronic Design (ISQED), the International Symposium on Low Power Electronics and Design (ISLPED), the International Workshop on Computer Architectures for Machine Perception (CAMP), the International Symposium on Circuits and Systems (ISCAS), the International Conference on Microelectronic Systems Education (MSE), and the International Conference on Computer Aided Design (ICCAD). He received the USF Outstanding Research Achievement Award in 2002, the USF President's Faculty Excellence Award in 2003, the USF Theodore–Venette Askounes Ashford Distinguished Scholar Award in 2003, the SIGMA XI Scientific Honor Society Tampa Bay Chapter Outstanding Faculty Researcher Award in 2004, and the Distinguished University Professor honorific title and the University Gold Medallion Honor in 2007. He was a corecipient of the three Best Paper Awards at the International Conference on VLSI Design in 1995, 2004, and 2006, and the IEEE Circuits and Systems Society VLSI Transactions Best Paper Award in 2009.