Designing Partially Reversible Field-Coupled Nanocomputing Circuits

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***Abstract*—Energy scalability of future digital systems is bounded by fundamental thermodynamic limits. Even worse, emerging technologies and process improvements, without reversible techniques, cannot solve this problem. Approaches such as field-coupled nanocomputing allow computations near the fundamental energy limits. However, there is a demand for strategies that avoid information losses within logic gates, consequently improving energy efficiency. For that end, we propose a novel way to reduce such losses by embedding fan-outs in logic gates, making them partially reversible. Simulation results for state-of-the-art benchmarks indicate an average reduction of the fundamental energy limit by 44% without affecting the delay. If delay is not the main concern, the average reduction reaches even 77%. To the best of our knowledge, this paper presents the first post-synthesis strategy to reduce fundamental energy limits for field-coupled nanocomputing circuits by means of logic network changes.**

***Index Terms*—Reversible computing, nanocomputing, energy efficiency, low power.**

I. Introduction

RECENT studies indicate that there might be only four to eight generations left before reaching the energetic boundary for Complementary Metal-Oxide Semiconductor (CMOS) technology. Despite the tremendous progress of integrated technologies, and even with the uprising of promising emerging technologies, the advancement of future systems could be strongly restricted by energy dissipation issues [1]. That means, in order to assure continuous technology advancement energy efficiency must scale, too [2]. Surprisingly, the cause of this problem is not a device property, but a direct consequence of the Second Law of Thermodynamics called Landauer's limit [3]. This is the fundamental energy limit, related to the information loss in the form of heat which occurs when bits are irreversibly erased within logic devices. It is on the order of $k_B T$ joules per erased bit, where k_B is the Boltzmann constant and T is the temperature of the systems thermal environment. Despite the controversies around it, Landauer's idea was experimentally verified, confirming that there is a physical limit in irreversible computation [4]–[7].

The CMOS technology can never reach Landauers minimum. This is due to the Landauer-Shannon limit that is about 50 times higher than Landauers limit [8]. However, Field-Coupled Nanocomputing (FCN) technologies, like Quantum-dot Cellular Automata (QCA) or Nanomagnet Logic (NML), are not restricted by this bound [6], [9], [10]. Consequently, the fundamental energy limits of these technologies are determined by irreversible operations.

That means, it is not just a matter of going beyond CMOS. Landauer's principle poses a barrier that is independent of the actual device, circuit or material [4]. Hence, to assure continuous scaling of device dimensions as well as energy efficiency one must consider to turn future computation reversible [2].

The main motivation for designing reversible systems is to ensure energy scalability, i.e., to guarantee that also in next technology generations energy reduction is possible. Therefore, it is important to quantify any energy losses of the system, ideally including both fundamental and non-fundamental ones. In case of the QCA technology, QCAPro [11] is the first tool that enabled the energetic evaluation of QCA designs. It applies a model that estimates polarization errors within the QCA cells and energy loss in non-adiabatic switching operations. Hence, the QCAPro provides an upper-bound energy consumption.

Torres *et al.* [12] recently proposed a logical synthesis model for QCAs that incorporates the main physical aspects, such as energy dissipation. The authors also developed a tool, called QD-E, that performs the energy evaluation in QCA circuits. The tools uses an quantum-level model for QCA cells and enables the energy evaluation that arise in irreversible as well as in reversible elements like interconnection, such as wires and fan-outs. Consequently, the QD-E provides the total energy consumed by a QCA circuit.

Ercan and Anderson [13], [14] provide a method that solely extracts the fundamental losses and disregards any non-fundamental ones. This is an appropriate approach for studies focusing on the energy scalability of the designs, having in mind that non-fundamental losses can be reduced by technological advances, while fundamental losses must be treated in a different way [15].

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As for energy reduction techniques, a decade after Landauer's work, Bennett presented a way to circumvent Landauer's limit [16]. He showed that any logically irreversible function can be mapped onto a physically reversible circuit, i.e., to a circuit that is able to return to any previous state in reverse order. Lent *et al.* proposed a clocking scheme that exploits Bennett's idea for QCA circuits [17]. The major drawback of this solution, though, is the tremendous degradation of the circuit's throughput. Based on this initial idea, Ottavi *et al.* [18] presented a partially reversible approach that allows balancing energy dissipation and throughput by adding memory stages and a pipeline-like control scheme. It could be shown, though, that this approach turns to be less effective than Landauer clocking if higher number of pipeline zones are applied [19].

Here, we take a different approach based on layout changes instead of modifications of the timing. We propose an intermediary step towards fully reversible systems by introducing a post-synthesis strategy that reduces fundamental energy losses. Our main contribution is a novel technique that identifies exploitable fan-outs and uses them for the recovery of bit's energy in FCN circuits, and thus enabling the design of new types of *partially reversible systems*. This is done by embedding the fan-outs into a gate, creating what we call here as *bit recycling gates*. Moreover, we propose an algorithm that creates partially reversible systems while allowing the designer to choose between energy reduction with no effect on the delay (named *depth-oriented*), or to focus solely on energy and accepting a potential delay penalty (named *energy-oriented*).

The proposed approach has been implemented and tested on well-established benchmarks [20], [21]. Obtained results indicate that the fundamental energy limit could be reduced by 44% on average if performance remained constant. In case of the energy-oriented solution, an average reduction of 77% could be achieved, while the delay degraded by an average factor of 16. To the best of our knowledge, this work presents the first post-synthesis approach that explores the use of bit recycling gates to reduce the fundamental energy limits of logic circuits.

We organize the remainder of this paper as follows. Section II gives some insights on the methods and technologies explored in this work. Section III introduces the proposed approaches. Section IV discusses our simulations results. Finally, Section V concludes this work.

II. Background

This section introduces preliminary aspects of this work. First, we briefly present the FCN technology, followed by the discussion of Landauer's argument and finally we show how to estimate the energy bounds in logic networks.

A. Field-Coupled Nanocomputing

Field-Coupled Nanocomputing (FCN) [10] is a potential alternative to traditional CMOS technologies. It is based on nanoscale cells that interact via local fields in absence of any current flow. This enables tremendously low energy dissipation and motivated numerous contributions in the past. Several physical realization of FCN devices have been developed both for its electronic version, Quantum-dot Cellular Automata (QCA), and for its magnetic version, Nanomagnet Logic (NML) [22]–[26]. Moreover, recent studies show promising theoretical advances in the development of FCN designs [12], [27]–[30].

In case of QCA, each cell consists of four quantum dots, i.e., structures able to confine electric charges. These quantum dots are arranged in a square-like fashion such that free mobile electrons can move between them. Since these electrons impose mutual repulsion due to Coulomb interaction [31], they tend to locate themselves at opposite corners of the square. Thus, they assume stable states, called polarizations, which are energetically equal and interpreted as binary 0 and 1. When placed close to each other, the polarization of one QCA cell influences the polarization of the other–again by Coulomb interaction. One can exploit this effect to construct logic gates, such as the *NOT* and the *MAJ* gates. Finally, locking one of the inputs of a *MAJ* gate to 0 or 1-state creates an *AND* or an *OR* gate, respectively.

NML circuits operate in a similar fashion but, instead of cells with quantum dots, the technology has single-domain nanomagnets as basic blocks. The magnetization of each nanomagnet is associated with binary 0 and 1, where both states are energetically equal as in QCA. Again, when placed close to each other, the magnetization of one nanomagnet influences the magnetization of its neighbors. The *MAJ* gate has the same layout as its QCA counterparts, while the *NOT* gate is even simpler through antiferromagnetic coupling [32].

The clocking system is an important factor in the dynamics of FCN circuits. Its principal functions are the synchronization of data flows and the implementation of adiabatic operation, enabling circuits with high energy efficiency. In QCA circuits, this efficiency is archived by adiabatic switching typically divided in four phases [27], [31]. The dynamics of NML circuits can be controlled by clock signals with three and four phases. However, lowest energy consumption is also only possible with the latter [33], [34].

B. Irreversibility and Heat Generation

"The search for faster and more compact computing circuits leads directly to the question: What are the ultimate physical limitations on the progress in this direction?" [3]. This visionary statement of Landauer back in 1961 reveals that he was already concerned with how far computing devices could reach. In his groundbreaking work, he could show that the fundamental energy dissipation occurs when devices *irreversibly* erase information, i.e., bits. That means, an irreversible operation generates outputs that do not uniquely define the operation's input values, i.e., no bijective function is performed. For example, a binary device D executing a *RESTORE TO 1* operation, i.e., starting from an undefined initial state of 0 or 1 the state 1 is generated, causes irreversible erasure of information since it cannot return to its initial state.

Landauer's argument relies on the concept of physical entropy and on implications of the Second Law of Thermodynamics. First, consider the usual definition of entropy in Statistical Mechanics, $S = k_B \ln(W)$, where k_B is the Boltzmann constant and W is the number of possible states. Considering a

device such as D (detailed above) with two equiprobable initial states and in thermal equilibrium with the environment, the initial configuration has $0.6931\,k_B$ units of entropy, while the only possible final configuration has an entropy of 0. The Second Law of Thermodynamics indicates that this reduction of entropy of the device must necessarily occur with compensation of greater or equal intensity in the neighborhood entropy. Thus, the energy transferred in the form of heat is at least $0.6931\,k_B\,T$ joules where T is the temperature of the environment. That means, fundamental energy losses result from the erasure of information, and thus, cannot be reduced by any technological advances.

The calculation of the Landauer's limit is often erroneously understood. This led to recent efforts by the research community towards its clarification [7], [13], [14], [35], [36]. The main reason for the confusion is that the limit is not a unique value for each type of logic gate. Indeed, it is a measure of information losses of a gate in the context of a circuit and depends on its clocking scheme and on the distribution of the gate's input probabilities. Note that gates in different positions within the circuit may have different input probabilities. Consequently, gates which perform irreversible operations, e.g., *AND*, could operate reversible when the probability of its input combinations guarantee a 1-to-1 relation between initial and final states. This situation is called *conditional reversibility* [36]. As our main focus is Landauer clocking, we use Ercan and Anderson's energy evaluation framework [13]. For those readers also interested in Bennett clocking, which is beyond the scope of this work, we would like to refer to Anderson's generalization [14].

In order to compute a gate's unavoidable fundamental energy dissipation, one should calculate the difference between the entropies of the probabilities of the initial and final states of the gates. The Equations (1a) and (1b) presents the Shannon's entropy for a generic probability distribution $\mathcal{S}$. In many cases there is no knowledge about the probability $P(x_i)$ of each of its initial states $x_i \in X$, thus, although the formalism does not requires it, each combination is considered to be equiprobable. Given $P(x_i)$, we may now define the probability $P(y_i)$ of each of the gate's final states $y_i \in Y$. It is achieved by applying the gate's logic function $\mathcal{G}$ on each x_i and adding $P(x_i)$ to $P\big(\mathcal{G}(x_i)\big)$. Then, by calling Eq. (1a) on x_i, we evaluate the contribution $\mathcal{I}(x_i)$ that it adds to the overall Shannon's entropy of X. Hence, the entropy $\mathcal{H}(X)$ of X is the summation of the contributions of all initial states x_i (Eq. (1b)). The same is valid for Y, i.e., $\mathcal{H}(Y)$ is the summation of the contributions $\mathcal{I}(y_i)$ of all final states y_i. The Landauer's limit for this gate is the difference between Shannon's entropy of its initial states and final states, i.e., $\mathcal{H}(X) - \mathcal{H}(Y)$. Finally, the Landauer's limit of the circuit is the sum of all losses of the gate. Following example shall detail this energy assessment.

$$\mathcal{I}(s) = -P(s) \times \log_2\big(P(s)\big) \tag{1a}$$

$$\mathcal{H}(S) = \sum_{s \in S} \mathcal{I}(s) \tag{1b}$$

Example 1: Consider the *sample* circuit depicted in Fig. 1. As the *NAND* gate 1 receives two of the four primary inputs of the circuit, each of its possible input combinations has a probability of $4/16$. Therefore, the Shannon's entropy of its initial state is $\mathcal{H}(X) = 2$ bits, as listed in Table I a. Replicating this calculus for the final states of gate 1 (see also Table I a), the Shannon's entropy of the final state is $\mathcal{H}(Y) = 0.81$ bits. That means, gate 1 loses $\mathcal{H}(X) - \mathcal{H}(Y) = 1.19$ bits of information.

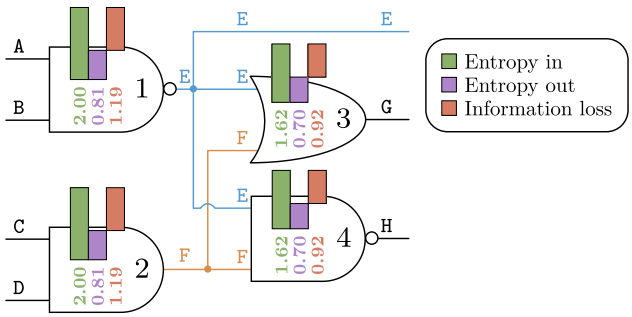


Fig. 1. *Sample* circuit and its information losses.

Table I b presents the same calculation for gate 2. As the initial and final states' probabilities are the same as those in gate 1, both dissipate the same amount of energy. Although, this is not the case for gates 3 and 4 (Tables I c and I d). Both gates operate with different initial states' probability due to their placement in the circuit (one of their input bits is produced by gate 1 and other by gate 2). Note that, despite gate 4 being a *NAND* like gate 1, it has distinct fundamental losses due to the different probabilities. Finally, adding up all gate's losses gives us the Landauer's limit for the *sample* circuit. Hence, we conclude that the *sample* circuit loses 4.22 bits of information or has a fundamental energy dissipation limit of $4.22\,k_B\,T\,\ln(2)$ joules.

Note that the exact evaluation of Landauer's limit requires a calculation for each gate and for all possible primary inputs combinations. For example, in the case of the *sample* circuit, which has 4 gates and 4 input bits, it requires 4 gates $\times\, 2^4$ combinations $= 64$ calculations. Hence, the runtime of this method grows exponentially with the number of primary inputs and linearly with the number of gates.

Another way to deal with this energy dissipation problem is to employ gates that avoid information losses. To that end, Lent *et al.* [17] indicated an approach that echoes the inputs of QCA gates to the output, turning these gates reversible even when the Bennett's strategy is not applied. Note that logic gates with a 1-to-1 relation between inputs' and outputs' states only guarantee the reversibility at the gate level, but this is not sufficient to enable reversibility at the circuit level. Data flow without discarding information between gates is also needed to accomplish arbitrarily small energy levels.

Consider Fig. 2 which depicts three different implementations of a QCA *AND* gate: (a) conventional, (b) unconditionally reversible (2-bit recycling gate) proposed by Lent *et al.* [17] and (c) conditionally reversible that recovers information of one input (1-bit recycling gate) proposed in this work. Lent *et al.* showed that the conventional QCA *AND* (Fig. 2(a)) must dissipate energy above $k_B\,T\,\ln(2)$ joules, when the value of one input differs from the output. They also demonstrated that the

TABLE I
ENTROPY CALCULATIONS FOR GATES IN FIG. 1'S CIRCUIT

Input					Output			
x_i	A	B	$P(x_i)$	$\mathcal{I}(x_i)$	y_i	E	$P(y_i)$	$\mathcal{I}(y_i)$
x_0	0	0	$4/16$	0.50		1		
x_1	0	1	$4/16$	0.50	y_0	1	$12/16$	0.31
x_2	1	0	$4/16$	0.50		1		
x_3	1	1	$4/16$	0.50	y_1	0	$4/16$	0.50
			$\mathcal{H}(X)$	2.00			$\mathcal{H}(Y)$	0.81

(b) Gate 2.

Input					Output			
x_i	C	D	$P(x_i)$	$\mathcal{I}(x_i)$	y_i	F	$P(y_i)$	$\mathcal{I}(y_i)$
x_0	0	0	$4/16$	0.50		0		
x_1	0	1	$4/16$	0.50	y_0	0	$12/16$	0.31
x_2	1	0	$4/16$	0.50		0		
x_3	1	1	$4/16$	0.50	y_1	1	$4/16$	0.50
			$\mathcal{H}(X)$	2.00			$\mathcal{H}(Y)$	0.81

(c) Gate 3.

Input					Output			
x_i	E	F	$P(x_i)$	$\mathcal{I}(x_i)$	y_i	H	$P(y_i)$	$\mathcal{I}(y_i)$
x_0	0	0	$3/16$	0.45	y_0	0	$3/16$	0.45
x_1	0	1	$1/16$	0.25		1		
x_2	1	0	$9/16$	0.47	y_1	1	$13/16$	0.25
x_3	1	1	$3/16$	0.45		1		
			$\mathcal{H}(X)$	1.62			$\mathcal{H}(Y)$	0.70

(d) Gate 4.

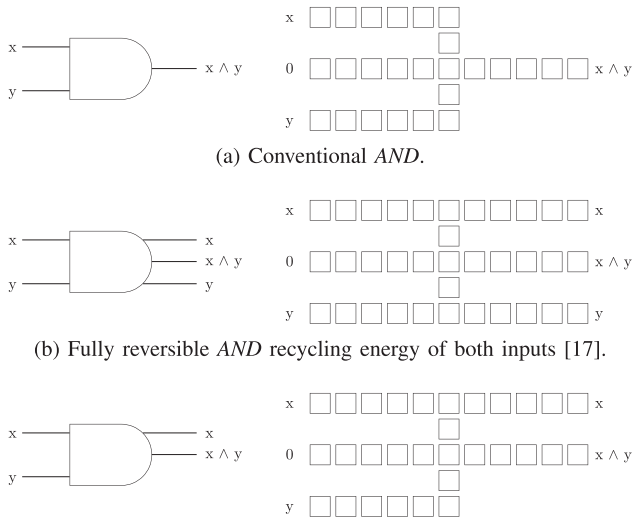
Input					Output			
x_i	E	F	$P(x_i)$	$\mathcal{I}(x_i)$	y_i	H	$P(y_i)$	$\mathcal{I}(y_i)$
x_0	0	0	$3/16$	0.45		1		
x_1	0	1	$1/16$	0.25	y_0	1	$13/16$	0.25
x_2	1	0	$9/16$	0.47		1		
x_3	1	1	$3/16$	0.45	y_1	0	$3/16$	0.45
			$\mathcal{H}(X)$	1.62			$\mathcal{H}(Y)$	0.70

dissipation of the fully reversible (2-bit recycling) QCA *AND* (Fig. 2(b)), which always guarantees a 1-to-1 relation between its initial and final states, can remain below $k_B\,T\,\ln(2)$ joules.

We propose here a generalization of the proposal of Lent *et al.* by echoing only a subgroup of inputs to the output, e.g., the QCA *AND* gate depicted in Fig. 2(c). Moreover, as showed in Section II-A, *AND* and *OR* gates are indeed *MAJ* gates with one input fixed. Therefore, the same layout also allows the recovery of 2 out of 3 bits on *MAJ* gates. Finally, the possibility of recovering 3 bits on *MAJ* gates remains for future investigation. Section III discusses these gates in more details.

III. IMPROVING FUNDAMENTAL ENERGY LIMITS

Information losses quantified by the Landauer's limit are the result of the local states' merging that happens within conventional logic gates, e.g., *AND*, *OR*, or *MAJ*. Thus, these losses directly depend on the probability distribution of the initial gate states. Such gate executes a reversible operation and consequently could spend less than $k_B\,T\,\ln(2)$ joules, when the probability of initial state allows a 1-to-1 relation with the probability of the final state [35].



(a) Conventional *AND*.

(b) Fully reversible *AND* recycling energy of both inputs [17].

(c) *AND* recycling energy of one input.

Fig. 2. Symbols and layouts of conventional as well as n-bits recycling QCA *AND* gates.

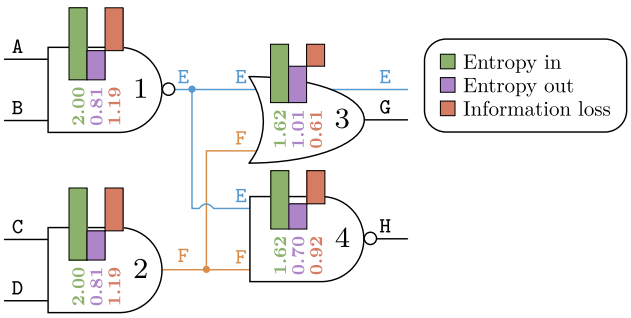
As introduced in Section II-B, we propose a generalization of the proposal of Lent *et al.* by allowing that only a subset of the n gate inputs is recycled, i.e., echoed to the output. That means, these modified gates only operate reversibly for a subset of the 2^n possible initial states, i.e., the ones that have a 1-to-1 relation with the final state. One should note that this proposal is in accordance with observations in related works which could show that such partial reversibility is indeed possible [13], [14], [35], [36].

We propose the exploitation of signals that are used more than once in the circuit. This gives us the ability to add gates that recycle input bits such that we can reduce the fundamental energy limit. Following example shall detail this approach.

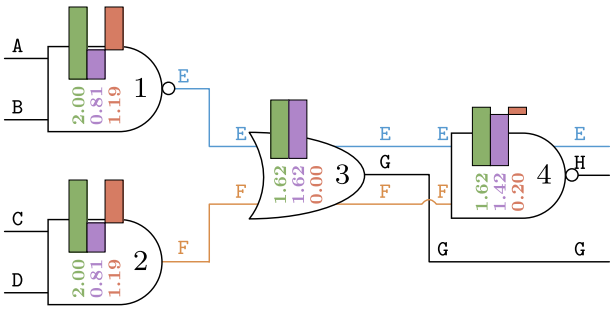
Example 2: Fig. 1 shows the *sample* circuit with its internal signals *E* and *F* highlighted in blue and orange, respectively. Note that this circuit solely applies conventional gates. As shown in Section II-B (Tables I a to I d), it dissipates 4.22 bits following Landauer's method.

Looking at the circuit, one can notice that some signals, i.e., *E* and *F*, feed different gates. Hence, instead of using a fan-out structure that multiplies the signal, one can feed it into gates that recycle its input energy and propagate the signal throughout them to the following stages. The resulting circuit is shown in Fig. 3 a. Here, gate 3 has been exchanged by its 1-bit recycling version that passes its input *E* to circuit's output (as in Fig. 2(c)). Table II a shows the new calculation for gate 3. Landauer's limit evaluation for this circuit results in a loss of 3.91 bits. The delay of this circuit is identical to the initial version.

If the delay is of lower priority, one can exploit that still some signals are inputs to more than one gate, e.g., signals *E* and *F*.



(a) *Sample* circuit that exploits fan-outs without degrading delay.



(b) *Sample* circuit that exploits fan-outs with delay penalty.

Fig. 3. Application of proposed method for the *sample* circuit.

Thus, instead of processing a signal in parallel, one can serialize the access and apply it as an echoed input to gates that recycle inputs. Fig. 3(b) depicts the resulting circuit, in which signal F also passes through the fully reversible gate 3 (as in Fig. 2(b)) before entering gate 4. Also, signal E traverses gate 4 (as in Fig. 2(c)) before being delivered as a primary output. Tables II b and II c show the new calculation for those gates. This additional modification comes at the costs of an increased delay from 2 to 3 stages. However, this reduces the fundamental energy loss down to 2.58 bits. The comparison of these results with those for Fig. 1 reveals that the gain is 1.64.

Algorithm 1 implements the proposed method for synthesized circuits given as netlist. It starts by iterating over all fan-outs (represented by nodes that distribute an output to different targets) in a reverse topological order so that nodes to be processed are not affected by a parent's recycling (Line 1). For each of these nodes, the algorithm builds chains of gates by selecting unique children from their outputs (Lines 2 to 8). The rank provided by the function topological-order, i.e., the node's distance from the primary inputs, is also fundamental for building those chains. The algorithm first iterates on a sorted-by-rank list containing sets of children nodes. Each set contains the children that are on a same rank, created by the function ranked-children (Line 4). Thus, each one of these sets is fed to a function choose which evaluates its nodes and selects a valid one that can be recycled and added to the chain (Line 5). Besides discarding invalid nodes, this function also enables the definition of gate's priorities, e.g., 1-bit recycling reversible gates over conventional ones. If energy shall be prioritized, it may even select multiple gates within same set (It will be clear in the following examples).

TABLE II
ENTROPY CALCULATIONS FOR GATES IN THE *sample* CIRCUIT DEPICTED IN FIG. 1

(a) New gate 3 (Fig. 3a).

Input					Output				
x_i	E	F	$P(x_i)$	$\mathcal{I}(x_i)$	y_i	E	G	$P(y_i)$	$\mathcal{I}(y_i)$
x_0	0	0	$3/16$	0.45	y_0	0	0	$3/16$	0.45
x_1	0	1	$1/16$	0.25	y_1	0	1	$1/16$	0.25
x_2	1	0	$9/16$	0.47	y_2	1	1	$12/16$	0.31
x_3	1	1	$3/16$	0.45		1	1		
			$\mathcal{H}(X)$	1.62				$\mathcal{H}(Y)$	1.01

(b) New gate 3 (Fig. 3b).

Input					Output					
x_i	E	F	$P(x_i)$	$\mathcal{I}(x_i)$	y_i	E	G	F	$P(y_i)$	$\mathcal{I}(y_i)$
x_0	0	0	$3/16$	0.45	y_0	0	0	0	$3/16$	0.45
x_1	0	1	$1/16$	0.25	y_1	0	1	1	$1/16$	0.25
x_2	1	0	$9/16$	0.47	y_2	1	1	0	$9/16$	0.47
x_3	1	1	$3/16$	0.45	y_3	1	1	1	$3/16$	0.45
			$\mathcal{H}(X)$	1.62					$\mathcal{H}(Y)$	1.62

(c) New gate 4 (Fig. 3b).

Input					Output				
x_i	E	F	$P(x_i)$	$\mathcal{I}(x_i)$	y_i	E	H	$P(y_i)$	$\mathcal{I}(y_i)$
x_0	0	0	$3/16$	0.45	y_0	0	1	$4/16$	0.50
x_1	0	1	$1/16$	0.25		0	1		
x_2	1	0	$9/16$	0.47	y_1	1	1	$9/16$	0.47
x_3	1	1	$3/16$	0.45	y_2	1	0	$3/16$	0.45
			$\mathcal{H}(X)$	1.62				$\mathcal{H}(Y)$	1.42

Algorithm 1: Building Chains of n-bits Recycling Gates.

```
   data : netlist ← circuit's netlist
1  foreach node ∈ reverse-topological-order(netlist) do
2      repeat
3          choices ← ∅
4          foreach set ∈ ranked-children(node) do
5              sel-children ← choose(set)
6              choices ← choices ∪ sel-children
7              set ← set ∖ sel-children
8          make-chain(node, choices)
9      until |choices| ⩽ 1
```

In this work, we employed a straightforward choose that only selects the first valid nodes. The selected nodes are added to the choices list (Line 6) and removed form the set (Line 7). Finally, when the chain is complete, i.e., there are no sets left, it selects a non-recyclable node, e.g., an output, to be at the bottom of the chain. After selection of the children, the algorithm links their inputs and outputs together (Line 8). This is done by the function make-chain. The execution stops when the choices list has at

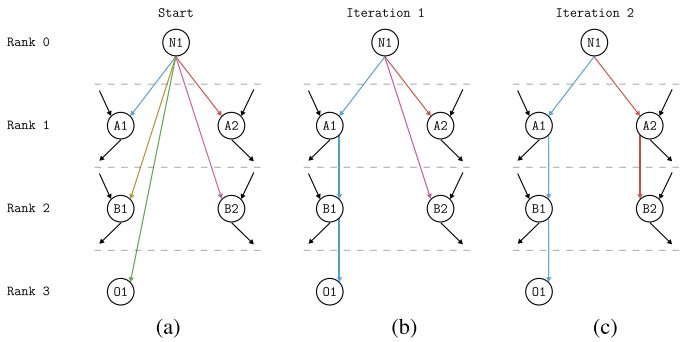


Fig. 4. Generations of chains in the depth-oriented strategy.

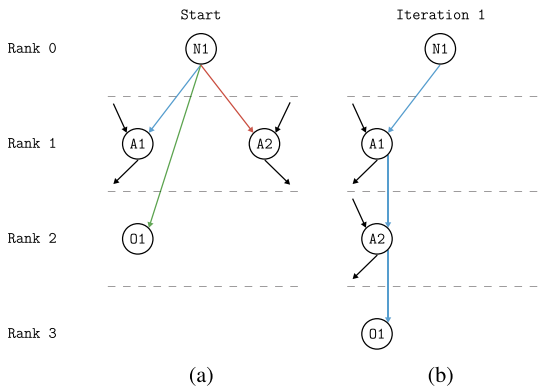


Fig. 5. Generations of chains in the energy-oriented strategy.

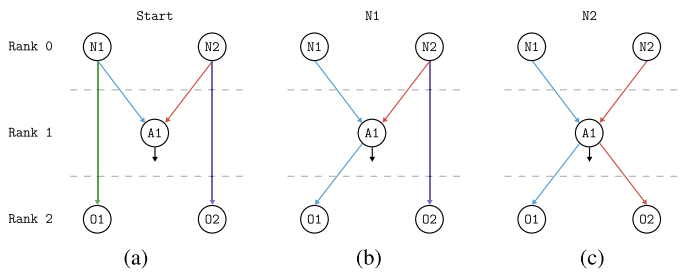


Fig. 6. Integration of fully reversible gates.

most one node left (Line 9), since at this point it cannot build any other chain from the fan-out.

The examples in Figs. 4 and 5 demonstrate the operation of the algorithm for two circuits.

Example 3: Fig. 4 shows the generation of chains in the depth-oriented strategy. In the initial version of the circuit (Fig. 4(a)) the output of node *N1* connects to all other nodes. During the first iteration (Fig. 4(b)), the algorithm selects and merges nodes *A1*, *B1* and *O1* into a chain that starts at node *N1* (marked as blue lines). Further, nodes *A1* and *B1* are changed to its 1-bit recycling versions. In the following iteration (Fig. 4(c)), a second chain consisting of nodes *A2* and *B2* is created (marked as red lines), and node *A2* is modified to a 1-bit recycling gate.

Fig. 5 shows the operation of the energy-oriented strategy in another circuit. In this case the algorithm only need one iteration to build the chain since it picks all children, despite some of them (*A1* and *A2*) being in the same rank.

Finally, the circuit from Fig. 6 illustrates how fully reversible gates are integrated. Initially, Fig. 6(a) shows two nodes, *N1* and *N2*, each one duplicating its outputs and having a common children, *A1*. In the first iteration (Fig. 6(b)), the connection between nodes *N1* and *O1* is placed between nodes *A1* and *O1* (blue lines). Further, node *A1* is modified to a 1-bit recycling gate. In the second iteration (Fig. 6(c)), the connection between nodes *N2* and *O2* is moved between nodes *A1* and *O2* (red lines). Now, node *A1* is changed to a fully reversible gate.

IV. Simulation Results

In order to assess our strategies, we evaluated the Landauer's limit for well-established benchmarks. Having in mind that the computational cost grows exponentially with the number of circuit's primary inputs (see also Section II-B), we analyzed circuits with up to 40 input bits of the MCNC [20] (154 circuits) and the EPFL [21] (6 circuits). Table III presents the obtained results for 14 circuits of MCNC and 6 majority-based circuits produced by Testa *et al.* [37] based on the EPFL benchmarks specifications. All benchmarks were evaluated *as they were*, i.e., we did not modify them before employing our technique.

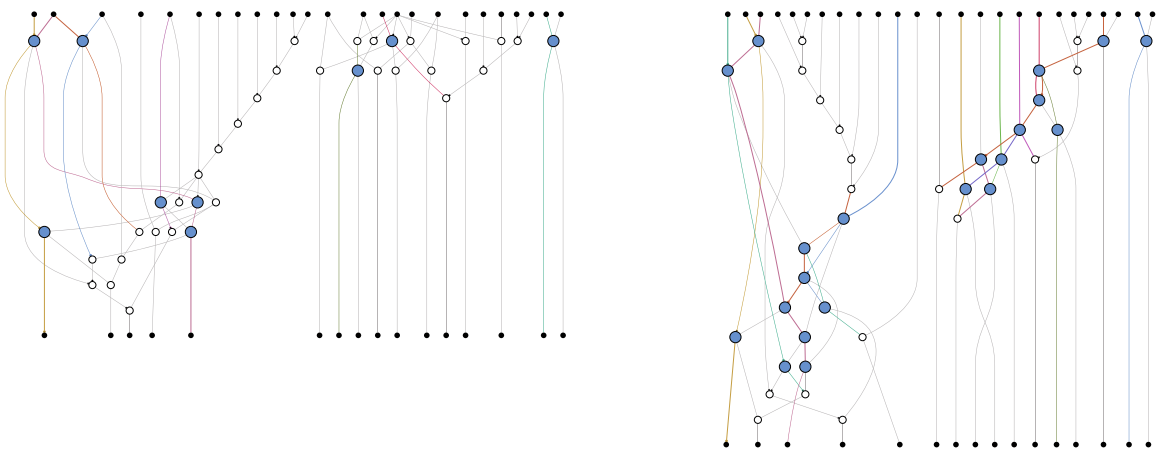
Table III lists the experiments results. Here, the first column shows the benchmark names. The second, third and fourth columns display the size of the circuit (number of gates) and the number of inputs and outputs, respectively. The fifth and sixth columns lists the exact Landauer's limit for an uniform input distribution applied to the original circuits, and its delay (number of levels). The next two columns refer to the depth-oriented results. That means, the seventh column shows the fundamental energy limit, while column eight lists the energy reduction resulting from our method. The remaining four columns relate to the energy-oriented results and list the Landauer's limit and its reduction as well as the new delay and its increase. We count the delay as the logic depth on the circuits' critical paths. Therefore, we are considering the best (minimum) possible delays. Note that both strategies come at no costs in terms of gate area. Hence, the circuit size is the same for the original and both modified cases.

The simulation results reveal that the fundamental energy limits could be reduced by, on average, 44% (up to 62%) on the depth-oriented case. If the delay was not restricted, i.e., the energy-oriented case, fundamental energy limits decreased by, on average 77% (up to 94%) at the costs of an average maximum delay increase of 16× (up to 73×).

For the sake of clarity, we choose a small circuit, not presented in Table III, to show the new logic networks produced by the proposed strategies. Fig. 7 shows the circuit produced by the proposed algorithms for the circuit *i1* (MCNC benchmark). Each color in the edges represents a signal for a specific fan-out, while the blue nodes highlight bit recycling gates. Black nodes represent the circuit's primary inputs and outputs. Fig. 7(a) displays the depth-oriented result for this circuit where 9 conventional gates were replaced by its recycling counterparts. This results into reduction of the fundamental energy dissipation by 20%

TABLE III
BENCHMARK RESULTS

				Original		*Depth-Oriented*		*Energy-Oriented*			
Benchmark	**Size**	**Inputs**	**Outputs**	**Energy**	**Delay**	**Energy**	**Reduction**	**Energy**	**Reduction**	**Delay**	**Increase**
log2	37 584	32	32	29 681.76	181	22 546.76	24 %	9377.48	68 %	1877	10.37 ×
sin	7895	24	25	6206.10	91	4642.82	25 %	1950.14	69 %	762	8.37 ×
cavlc	745	10	11	781.34	11	511.96	34 %	259.98	67 %	114	10.36 ×
dec	420	8	256	412.72	4	412.72	0 %	25.02	94 %	290	72.50 ×
int2float	246	11	7	259.10	9	188.88	27 %	88.55	66 %	52	5.78 ×
ctrl	127	7	26	135.60	5	92.31	32 %	38.42	72 %	36	7.20 ×
prom1	7803	9	40	6862.44	24	3560.18	48 %	1535.11	78 %	869	36.21 ×
mainpla	5346	26	54	4686.49	38	2211.91	53 %	1326.54	72 %	583	15.34 ×
xparc	5105	39	73	4642.60	47	1742.30	62 %	915.88	80 %	481	10.23 ×
bca	3669	16	46	3458.48	26	1334.85	61 %	546.24	84 %	402	15.46 ×
prom2	3513	9	21	3115.70	22	1696.55	46 %	731.23	77 %	481	21.86 ×
apex4	3452	9	19	3062.46	21	1645.90	46 %	825.64	73 %	404	19.24 ×
ex1010	3340	10	10	3038.40	24	1642.23	46 %	718.00	76 %	392	16.33 ×
bcb	3314	16	39	3117.99	26	1247.13	60 %	518.97	83 %	354	13.62 ×
bcc	3238	16	45	3073.95	25	1196.35	61 %	503.59	84 %	353	14.12 ×
C6288	2337	32	32	1665.15	120	1090.78	34 %	350.66	79 %	208	1.73 ×
bcd	2304	16	38	2182.07	25	934.01	57 %	391.27	82 %	243	9.72 ×
table3	2183	14	14	2009.57	24	950.47	53 %	432.81	78 %	258	10.75 ×
table5	1987	17	15	1841.59	26	841.46	54 %	390.88	79 %	211	8.12 ×
cps	1928	24	109	1883.59	31	812.68	57 %	430.58	77 %	226	7.29 ×
Average	4827	17	46	4105.86	39	2465.11	44 %	1067.85	77 %	430	15.73 ×



(a) Depth-oriented: 11 levels and 20 % of energy reduction.

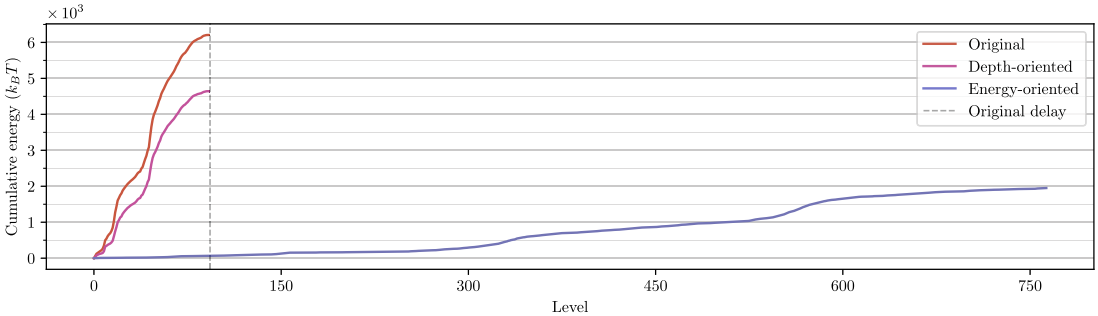
(b) Energy-oriented: 14 levels and 42 % of energy reduction.

Fig. 7. Circuit graphs resulting from the proposed strategies: the *i1* circuit's case.

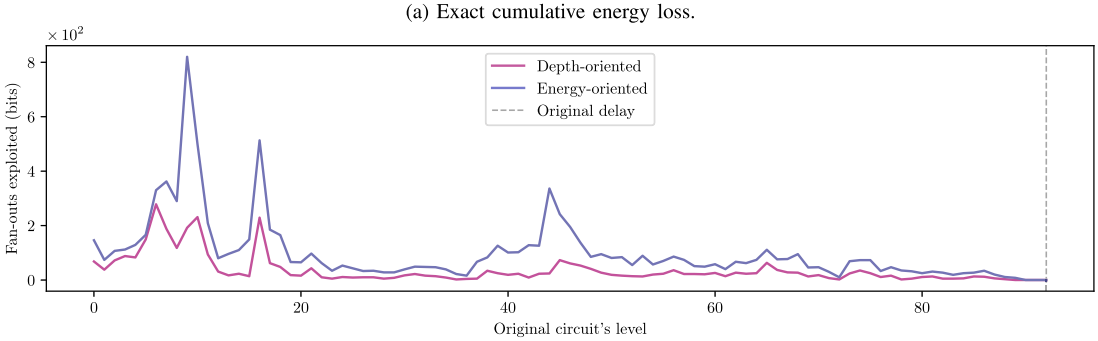
without any delay change. Fig. 7(b) depicts for the same circuit the outcome of the energy-oriented algorithm. Here, the fundamental energy dissipation can be reduced by 42% due to the serialization of some information transfer. Note that both graphs are aligned level by level allowing the comparison of the delay degradation (from 11 to 14 levels). Note that we do not consider input and output levels.

Fig. 8 presents the loss rate pattern and the fan-outs density for the EPFL circuit *sin*. First, Fig. 8(a) shows the accumulated energy losses for the original circuit version, the new depth-oriented version, which has the same delay as the original (vertical dashed line), and the energy-oriented version. Then, Fig. 8(b) presents the density fan-outs exploited by the depth-oriented and energy-oriented techniques.

It is interesting to note that circuits profit differently from both strategies, i.e., the ranking of the improvement of the energy limit for depth-oriented and energy-oriented results is not the same. This follows from the fact that the first approach takes advantage from the number of fan-outs that target different levels while the latter benefits only from the number of fan-outs. The *dec*



(a) Exact cumulative energy loss.



(b) Fan-outs exploited per level.

Fig. 8. *sin* circuit's evaluation.

benchmark is a good example for this observation. It has a high number of fan-outs that possess many targets on the same level. This explains the negligible improvement of the energy limits when delay is not impaired and the high gain when there is no such restriction.

V. Conclusions

Energy efficiency is of utmost importance for future technology scaling, which motivates the search for new computing paradigm that can circumvent the fundamental barrier defined by Landauer. We proposed in this work a step towards feasible partially reversible circuits designed in Field-Coupled Nanocomputing technologies that enable considerable reduction of its fundamental energy limits. Simulation results for established benchmark suites indicate that the presented technique can reduce the fundamental energy limits in average by 44% without any delay penalty. When delay is not a concern, energy can be decreased by up to 94% and on average by 77%, at an average performance penalty of $16\times$.

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