Logic and Memory Ferroelectric Field-Effect-Transistor Using Reversible and Irreversible Domain Wall Polarization

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***Abstract*— We propose a higher-κ non-hysteric ferroelectric field-effect transistor (FEFET) using reversible domain wall displacement. By separately stimulating reversible and irreversible domain walls, whose concepts have been experimentally suggested recently, our $HfZrO_x$-based FEFET showed remarkable performance as both a logic and a memory device. This was achieved by relatively low-temperature annealing, contributing to the formation of more reversible domain walls in the film. Finally, we demonstrated the feasibility of logic and memory co-integration by common fabrication process with complementary metal-oxide-semiconductor (CMOS) compatibility.**

***Index Terms*— Ferroelectrics, ferroelectric transistor, hafnium zirconium oxide, ferroelectric memory, reversible polarization.**

I. Introduction

THE discovery of ferroelectricity in HfO_2 accelerated the development of non-volatile memory such as ferroelectric field-effect-transistors (FEFET) [1], [2]. Recently, it has been found that some components of the polarization in HfO_2-based ferroelectrics can be volatile as well [3], [4]. In previous works, two fundamentally different concepts of domain wall displacement, reversible and irreversible domain wall polarization (P_{rev}, P_{irrev}), were suggested and electrically investigated. While P_{irrev} is the same concept as conventional ferroelectric polarization, P_{rev} is a newly proposed concept.

The conventional electrical characterization of ferroelectric materials is generally based on two methods—small-signal capacitance-voltage (C-V) measurement and polarization-voltage (P-V) measurement using bipolar pulses. Especially, a butterfly-shaped curve in C-V measurement has been considered an indicator of ferroelectric polarization switching. However, it should be noted that small-signal measurement observes responses of carriers induced by small signals only. This points out that there are real polarization responses generated by the small signal (<50 mV), which contributes to the formation of peaks in the butterfly-shaped curve. This is intriguing because it has generally been considered that only an electric field higher than the coercive field (E_c, generally >0.8 MV/cm in HfO_2-based ferroelectric materials at 300 K) can flip polarization in the ferroelectric layer [1].

In addition, it has been discovered that only P_{irrev} contributes to nonvolatile and hysteric behaviors of the ferroelectric film, while P_{rev} stays volatile and non-hysteric [3]. The large charge density ($\sim 10^{14}$ cm^{-2}) of P_{irrev} necessarily leads to significant hysteric charge trapping in the metal-ferroelectric-insulator-semiconductor (MFIS) structure, which is not desirable for a logic device [4], [5].

In fact, these concepts were already reported about thirty years ago in perovskite-based ferroelectrics [6], [7], [8]. Because perovskite ceramics in the preceding literature were single-crystal, the physical origin of P_{rev} is not attributed to the poly-crystal nature of HfO_2-based ferroelectrics. Nonetheless, no one has yet investigated the physical origin and effect of P_{rev}. Furthermore, most previous literature has considered only P_{irrev}, that is, the conventional concept of ferroelectric polarization.

In this letter, we suggest a proof-of-concept of P_{rev}-induced non-hysteric FEFET. We re-trace the fundamentals of ferroelectrics and provide FEFET with remarkably higher dielectric constant (κ) and non-hysteresis by stimulating P_{rev} only, which is a different concept from the minor loop because minor loops in the preceding literature considered only P_{irrev}, conventional ferroelectric polarization. It was understood that using P_{rev} is more desirable for a logic device because P_{irrev} inevitably induces significant charge trapping due to its high charge density. Furthermore, using ternary-content-addressable-memory (TCAM), we show the feasibility of co-integration of logic FEFETs and memory FEFETs with the same gate stack.

II. Device Fabrication

MFIS capacitors and partially depleted silicon-on-insulator (PDSOI) FEFET samples were fabricated. Highly doped silicon and SOI (channel thickness: 100 nm) wafers were

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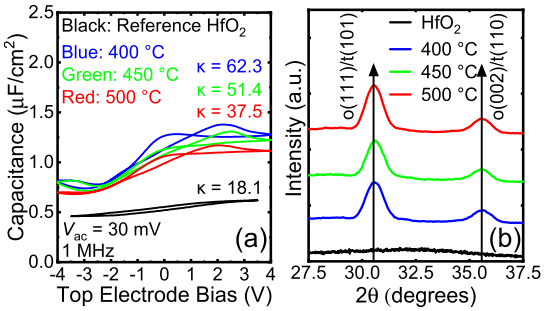

Fig. 1. (a) Double-swept *C-V* measurement with different annealing temperatures for MFIS$^+$ and reference MOS$^+$ capacitors. (b) GIXRD patterns of HfO_2 (reference) and HZO film annealed at 400 °C, 450 °C, and 500 °C.

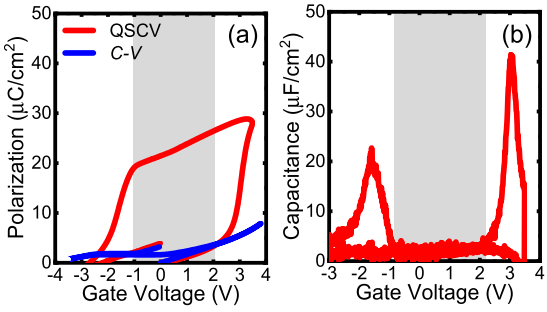

Fig. 2. (a) QSCV analysis with bias region of P_{rev} only (shadowed). This is a different concept from the minor loop. (b) Comparison between QSCV and *C-V* measurements.

prepared. The interfacial layer (SiO_x) was formed by sulfur peroxide mixture (H_2SO_4:H_2O_2:DI water = 1:1:5) and $Hf_{0.52}Zr_{0.48}O_2$ (HZO) was deposited by atomic layer deposition (ALD) at 250 °C. In this case, HZO (10.2 nm)/SiO_x(1.0 nm) was formed. Tungsten (30 nm) and aluminum (80 nm) were deposited for gate electrodes. Post-metallization-annealing (PMA) was carried out at different temperatures (from 400 °C to 500 °C) for 30 seconds in N_2 atmosphere by rapid thermal annealing (RTA) to crystallize the ferroelectric layer and to observe the PMA temperature dependence of P_{rev}.

A MOSFET sample for reference was also fabricated. Here, we adopted an SOI wafer with a thinner channel thickness (50 nm) and a gate oxide ($HfO_2$9.7 nm/SiO_x 1.0 nm) using different ALD equipment, to fabricate a high-quality reference MOSFET. PMA was conducted at 350 °C, which was optimized to reduce the contact resistance to the source and the drain, and to stabilize the HfO_2.

III. Results and Discussion

Fig. 1(a) shows the *C-V* characteristics in the MFIS$^+$ capacitors. All the MFIS$^+$ capacitors have higher capacitance than the MOS$^+$ capacitor, not only because of the higher κ of HZO but also because of the contribution of P_{rev}. Moreover, capacitor with 400 °C annealing showed higher P_{rev} responses (peaks of butterfly shape at biases ≈0 and 2 V). Larger P_{rev} responses were accomplished owing to the excellent ability to form orthorhombic phases at relatively low annealing temperatures (in previous work, ≥500 °C) [9], [10].

The κ values of the reference amorphous HfO_2 and HZO (500 °C, 450 °C, and 400 °C) were 18.1, 37.5, 51.4, and 62.3, respectively, while the κ value of SiO_x was only 1.6. This low κ value of SiO_x is typically attributed to the low density of the grown film. It should be noted that κ values of the HZO films include the contribution from P_{rev} as well as the linear dielectric response. The difference in contribution of P_{rev} to κ between 400 and 500 °C annealed HZO would be ∼24.8 if the grains and phases were not too different. In the grazing incident X-ray diffraction (GIXRD) patterns (Fig. 1(b)), the HZO films with different PMA temperatures showed dominant orthorhombic/tetragonal phase peaks different from the reference amorphous HfO_2.

Ferroelectric polarization in FEFET was electrically characterized by pulse-based quasi-static split *C-V* (QSCV) measurement [4], [5]. The capacitance peaks in Fig. 2(a) show the ferroelectric polarization switching, at approximately 3 V and −1.5 V. As experimentally suggested, pulse measurement such as QSCV measures both P_{irrev} and P_{rev} [3]. However, P_{irrev} switches only at an electric field higher than E_c, and P_{rev} is switched by a very small electric field. Thus, the capacitance peaks during QSCV involve polarization switching induced by both P_{irrev} and P_{rev}. This indicates that only P_{rev} is displaced in the region where there is no peak (shadowed region in Fig. 2(a)), in spite of the small response compared to the peaks. This is because most of the domain walls in our HZO film are irreversible [1], [11].

However, despite the weak responses, the capacitance enhancement induced by P_{rev} shown in Fig. 1(a) is already comparable to the typical oxide capacitance (C_{ox}) and inversion capacitance in conventional MOSFETs [11]. Because ferroelectric polarization already has 30-100 times higher charge density than the channel charge density, even a small amount of P_{rev} polarity can contribute to higher κ. To demonstrate P_{rev} in the bias region, *C-V* and QSCV measurements are shown for comparison in Fig. 2(b). At the bias region of −1.1 V < gate voltage < 2 V (shadowed in Fig. 2(b)), the two different measurement results showed similar polarization values, indicating that QSCV method also captured polarization switching by reversible domain wall displacement [3], [11], [12]. Hence, if FEFET works only in the bias region, without stimulating P_{irrev} but stimulating P_{rev}, steep-slope and non-hysteric I_D-V_G characteristics should be possible.

Double-sweep DC I_D-V_G characteristics of the fabricated FEFETs and reference MOSFET are shown in Fig. 3(a). Even though MOSFET with HfO_2 gate dielectric showed good characteristics of small hysteresis and steep slopes, FEFETs had even better slopes and negligible hysteresis. Furthermore, among two FEFETs with different annealing temperatures, the FEFET with lower annealing temperature showed much steeper I_D-V_G curves. Fig. 3(b) shows the calculated SS, extracted from Fig. 3(a). The FEFET with PMA at 400 °C shows excellent SS, despite its long channel. SS values less than 70 mV/dec were achieved over 6 orders of I_D.

These results are even comparable to those of previous studies about negative capacitance FET (NCFET); most devices have larger hysteresis because they used P_{irrev} [13], [14], [15]. Hence, it is understood that P_{rev} induced more polarity in the gate oxide, which resulted in higher κ and non-hysteresis, which, however, might be explained by charge compensation by trapped charges [16]. In this case, the trapped

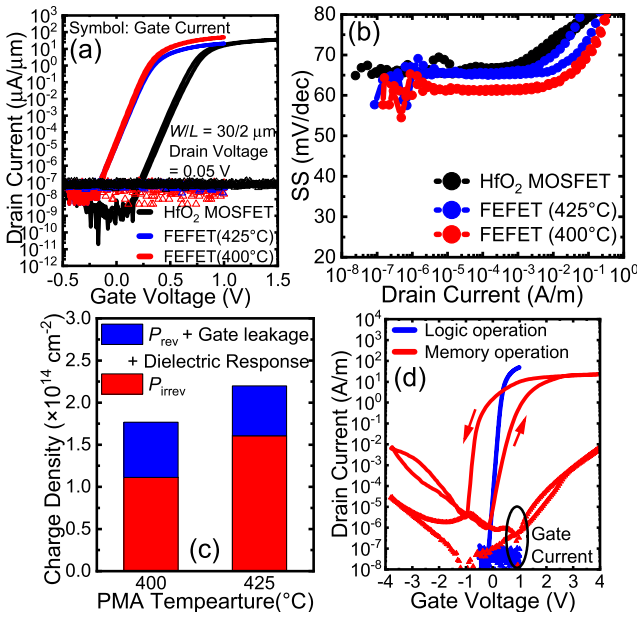

Fig. 3. (a) DC I_D-V_G of FEFETs and MOSFET. (b) Calculated SS as function of I_D from (a). (c) Sheet charge density of P_{irrev} and P_{rev} among total polarization. The 400 °C PMA device showed 1.77×10^{14} cm^{-2} of total polarization and 1.11×10^{14} cm^{-2} of P_{irrev}. (d) Logic and memory operations in DC I_D-V_G using same FEFET.

charges must be unstable and immediately de-trap when P_{rev} disappears.

The amount of P_{rev}, the dielectric response, and the gate leakage measured by double-pulsed QSCV in the two FEFETs with different PMA temperatures are quantitatively compared in Fig. 3(c) [11]. The FEFET with lower PMA temperature showed more desirable characteristics due to the larger value of P_{rev}, which can also be seen in Fig. 1(a).

Next, the characteristics of FEFET as a memory device were investigated. As mentioned, nonvolatile memory characteristics can be achieved by stimulating P_{irrev}. Fig. 3(d) shows DC I_D-V_G curves of the logic and memory operation, the concept of which has been reported by several groups [17], [18]. The case of the memory operation shows typical hysteresis (counter-clockwise) of n-channel Si FEFET, with high ON/OFF drain current ratio. Fig. 4(a) shows the retention characteristics of the FEFET. Device shows an excellent read property compared to those in previous studies in terms of stable retention properties and ultra-short read-after-write latency (<100 ns), considered challenging to achieve in MFIS FEFETs [19], [20]. This improvement is because polarization switching in the SOI FEFET operates by electron de-trapping mode [4]. Fig. 4(b) shows the write endurance behavior of the device. It has high cycling characteristics of 10^9 compared to previous studies [15], [21], [22], [23].

Fig. 5 describes reversible and irreversible domain wall displacements in the ferroelectric layer. When small biases are applied, reversible displacement (P_{rev}) occurs because the potential well of the domain wall is wide and shallow. However, as more biases are applied, the domain wall propagates and the potential energy locates in the deep well, which induces irreversible displacement (P_{irrev}). This is different from the concept of reverse switching in the previous literature because reverse switching is related to

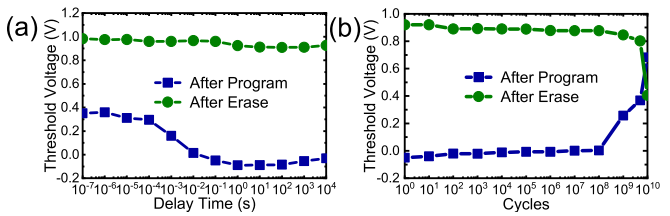

Fig. 4. (a) Retention and (b) write endurance characteristics of memory operation. 3.8 V/20 μs and -3 V/20 μs triangular pulses were used to write.

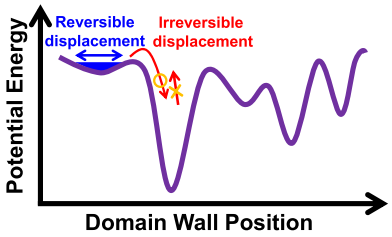

Fig. 5. Schematic of reversible displacement (P_{rev}) and irreversible displacement (P_{irrev}) of the ferroelectric domain wall.

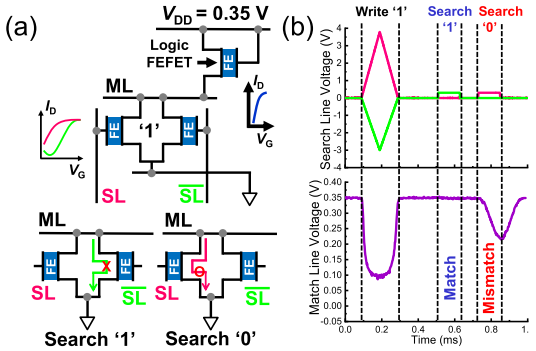

Fig. 6. (a) A Two-FEFET TCAM cell with logic FEFET. The search line (SL) and the match line (ML) are indicated. (b) Operation demonstration of TCAM unit cell.

carrier movement, while P_{rev} is the ferroelectric nature itself [24], [25].

Thanks to its complementary nature, P_{rev} can be used for higher-κ logic devices, and P_{irrev} for memory devices. This implies the potential integration of logic and memory devices in a common fabrication process. As proof-of-concept, Fig. 6(a) shows a schematic of a unit TCAM cell with two memory FEFETs and one logic FEFET formed using the same CMOS-compatible fabrication process [26]. Demonstration of searching '0' and '1' after writing '1' is shown in Fig. 6(b).

IV. Conclusion

The concept of higher-κ non-hysteric FEFET was suggested and examined based on the fundamental understanding of the ferroelectric domain nature. This was achieved by low-temperature annealing, which was likely to contribute to more reversible domain wall formation in the film. However, further studies of the origin of P_{rev} are required. Additionally, excellent memory performance was achieved using P_{irrev} and electron de-trapping mode. Finally, co-integration of memory and logic FEFETs by common CMOS-compatible fabrication process was demonstrated as a proof-of-concept.

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