Electrostatically Reversible Polarity of Dual-Gated Graphene Transistors

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***Abstract*—We developed dual-gated graphene transistors in which the transistor polarity (n-type or p-type) is electrostatically reversible by the gate bias of one of the top gates. In this device, a channel is defined as the region between a pair of top gates, where graphene is irradiated by an accelerated helium ion beam to form a defect-induced transport gap. This device features not only a large current ON–OFF ratio of four orders of magnitude but also unipolarity of transistors, which would otherwise be ambipolar. We also show how these polarity-reversible transistors can be used in logic circuits.**

***Index Terms*—Nanoelectronics, thin-film transistors.**

I. Introduction

GRAPHENE, a 2-D atomically thin-film of carbon [1], has attracted much attention due to its extremely high mobility of electrons and holes [2] and to its ultrathin body structure, which is ideal for overcoming short-channel effects in aggressively scaled-down devices [3]. It is well known, however, that, in addition to the lack of bandgap, the ambipolar nature of carrier conduction has been an issue for the application of graphene to complementary metal–oxide–semiconductor devices. On the other hand, electrostatic doping of carriers in graphene would be an advantage only if the issue of ambipolarity could be addressed, because, due to the electrostatic control of both electrons and holes, the transistor type (p-type of n-type) can be electrically flipped, which is impossible in silicon transistors with impurity doping. In this paper, we propose a novel concept graphene device with dual gates and a functionalized graphene channel. For graphene channel engineering, we adopted a technique of helium ion beam irradiation to graphene to generate a defect-induced transport gap [4]. We show that this device works as a unipolar transistor in which the transistor polarity can be controlled by the polarity of the gate bias of one of the two gates. The controllability of transistor polarity is expected to enhance the flexibility of circuit configurations. In particular, it should reduce the number of transistors in the circuits [5]. We also discuss the device structure suitable for circuits.

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II. Device Fabrication

A schematic illustration of the structure of the proposed device is shown in Fig. 1(a). The device has a pair of top gates and a helium ion beam irradiated between them. We exfoliated a crystal of highly ordered pyrolytic graphite with adhesive tape and deposited single-layer graphene flakes on a silicon chip with a 285-nm-thick surface SiO_2 layer. Source and drain electrodes were formed by Ti/Au (5/30 nm) thermal evaporation and lift-off. It was confirmed that the total contact resistance was lower than 1 kΩ and the back gate voltage of the Dirac point was within the range from 0 to 2 V. The top gates had a point contact structure with a gate gap of 20 nm, as shown in Fig. 1(b). These gates were fabricated by thermal evaporation of SiO_2 (5 nm) and Al (25 nm). This gate structure is based on the natural oxidation of Al, and the Al_2O_3 layer worked as an insulating layer [6]. The SiO_2 layer was added to the interface for increasing the spacing between the graphene channel and Al electrode. A helium ion beam was applied to the graphene region between the top gates with a controlled ion dose of 6.9×10^{15} ions/cm^2. Outside this region, the graphene was irradiated with a heavy dose of ions (2.0×10^{16} ions/cm^2) to make it insulating in order to separate the source and drain regions. The defect density of this region was estimated to be 2%. In a preliminary experiment, we confirmed that a heavily dosed graphene did not exhibit any detectable current ($<$100 fA) under a bias of 1 V. Therefore, the source and drain regions were completely separated. As a result, the current flows in the central part of the device with a width of 30 nm and length of 20 nm, as indicated in Fig. 1(d). This region is referred to as the "channel."

For helium ion irradiation to graphene, we used a helium ion microscope. A helium ion beam was first used in graphene

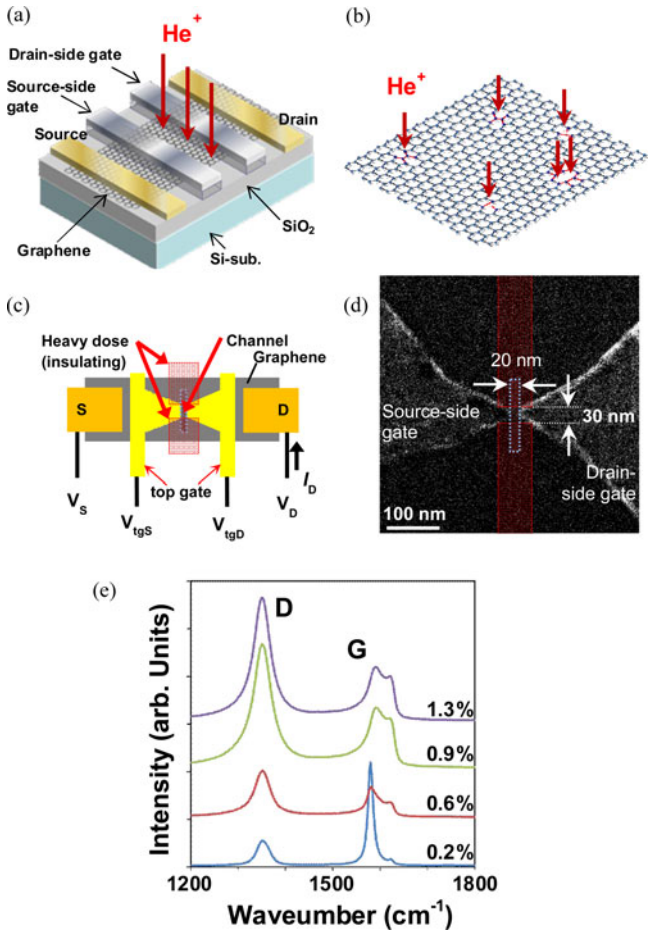

Fig. 1. (a) Schematic of the proposed graphene transistor consisting of pair of top gates. Graphene between top gates is irradiated with helium ion beam to form a transport gap. (b) Graphene with helium ion beam irradiation. Ion beam induces point defects that work as scatterers for electrons to be localized. (c) Top view of fabricated device structure. Measurement configurations are also given. (d) Helium ion micrograph of central part of one of fabricated devices. Central part within gate gap (channel) was irradiated with helium ion beam of 6.9×10^{15} ions/cm^2, and regions out of channel were irradiated with heavy ion dose to make it insulating. Channel length, $L_{\rm irr}$, and width, $W_{\rm irr}$, was 20 and 30 nm, respectively. (e) Raman spectra of samples with different defect density.

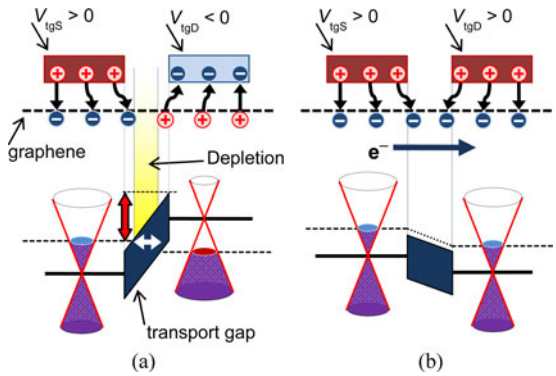

Fig. 2. Illustrations of charge distribution and corresponding band configurations in (a) OFF state and (b) ON state. In OFF state, channel region contains depleted region that works as barrier for carrier transport from source to drain regions, which can be much higher and longer than conventional graphene transistors. On state is generated with same polarity biasing of both gates.

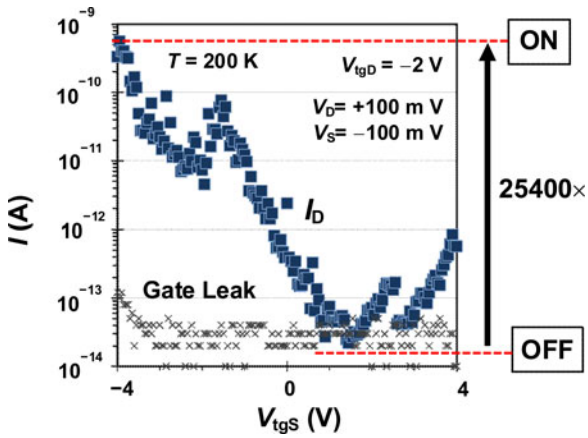

Fig. 3. ON–OFF switching operation of one of fabricated graphene devices at 200 K. The maximum ON–OFF ratio of 25400 was achieved. Gate leak current was also added.

for precision cutting of a nanoribbon [7], [8], and we applied this technique to graphene functionalization [4]. The primary effect of ion irradiation is that the impact of ions on carbon atoms will generate point defects in graphene, and the acceleration voltage of 30 kV is large enough to remove carbon atoms in graphene [9]. According to a calculation in [6], the density of generated point defects in the channel was estimated to be 0.7%. The introduction of defects was confirmed by Raman spectroscopy in which the D-mode peak grew by the application of the helium ion beam [see Fig. 1(e)]. Also, in the Raman spectra, the G-mode peak remained in the ion irradiated graphene, confirming that the basic hexagonal structure of graphene lattice survived ion irradiation. It is believed that these defects work as scatterers for electron waves to interfere with each other, and that electrons tend to be spatially localized, forming a transport gap for carrier conduction [10]. By controlling the band configurations, including the transport gap, the carrier transport through the device can be modulated.

III. Current ON–OFF Switching

The basic operation principle of current ON–OFF switching in our device is shown in Fig. 2. The original motivation of our concept of this device was to improve the cut-off property, as shown in Fig. 2(a). The OFF state is induced by applying gate biases of opposite polarity to each other so that a depletion region comes in the channel where the transport gap is generated by ion irradiation. In this case, the barrier height and length can be enhanced as compared to the conventional transistor structure [11]. On the other hand, the ON state can be generated by applying the gate bias of the same polarity. In Fig. 2(b), top gates are positively biased, and the graphene is negatively charged throughout the channel region, resulting in current flowing in the device. For this transistor operation, the distance between the graphene sheet and gate electrode was optimized by inserting a 5-nm-thick SiO_2 spacer layer between the graphene and Al electrode.

Current ON–OFF switching operation of a fabricated device was demonstrated at a temperature of 200 K, as shown in Fig. 3. The source and drain biases V_S and V_D were -100 and $+100$ mV, respectively. The gate bias of the drain-side gate

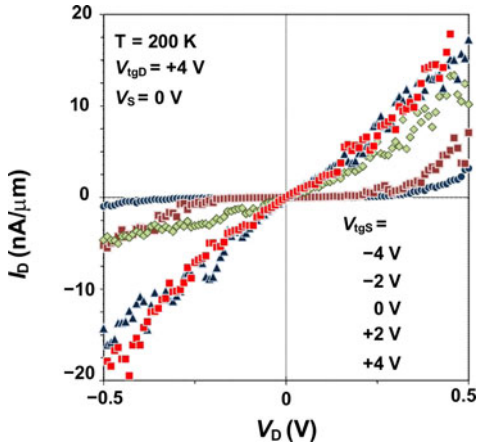

Fig. 4. Drain bias dependence of drain current. V_{tgD} was fixed to $+4$ V, so device went into on state when $V_{\mathrm{tgS}} > 0$.

V_{tgD} was fixed at -2 V, and the gate bias of the source-side gate V_{tgS}, was swept from -4 to $+4$ V. In this configuration, the device went into the OFF state when $V_{\mathrm{tgS}} > 0$ V [see Fig. 2(a)] and ON state when $V_{\mathrm{tgS}} < 0$ V [Fig. 2(b)]. The maximum ON–OFF ratio was about 25 400, as indicated in Fig. 3. This is the largest ON–OFF ratio that we have obtained with this device concept in the temperature region from room temperature to 200 K. Regarding the sweeping direction of V_{tgS}, hysteresis was observed when the V_{tgS} sweeping direction was reversed. It is believed that the hysteresis was induced by doping from the surface contamination such as the residue of resist, water, or oxygen. At temperatures higher than 200 K, the ON–OFF ratio became low mainly due to the increase in the off current. At room temperature, the ON–OFF ratio was one order of magnitude. The hysteresis became more noticeable at higher temperatures. We did not observe any detectable gate leakage during transistor operation, as shown in Fig. 3. The absence of gate leakage was also confirmed by comparing the drain current I_D to the source current I_S.

Drain bias dependence of current with different gate biases is shown in Fig. 4. The bias of the drain-side gate was fixed to be positive, and $I_D - V_D$ curves were taken at different source-side gate biases. As shown in the figure, the ON state is given by $V_{\mathrm{tgS}} > 0$, and it will be OFF state when $V_{\mathrm{tgD}} < 0$. The ON–OFF switching feature was found to depend strongly on the defect density, which is directly related to the size of the transport gap. We conducted an experiment on another device of the same structure with a lower defect density of 0.3%, the ON–OFF ratio was on the order of 10; on the other hand, if the defect density exceeds 1%, the current in this device will be almost zero. The channel length also has an effect on the device characteristics. In our previous work, we found that the current in ion-irradiated graphene decreased exponentially as the channel length increased [11]. The conductance of the devices showed a strong temperature dependence of thermally activated transportation in high temperatures, which deviated from Arrhenius fitting, suggesting variable range hopping in lower temperatures [12]. The activation energy of 380 meV was evaluated by Arrhenius fitting.

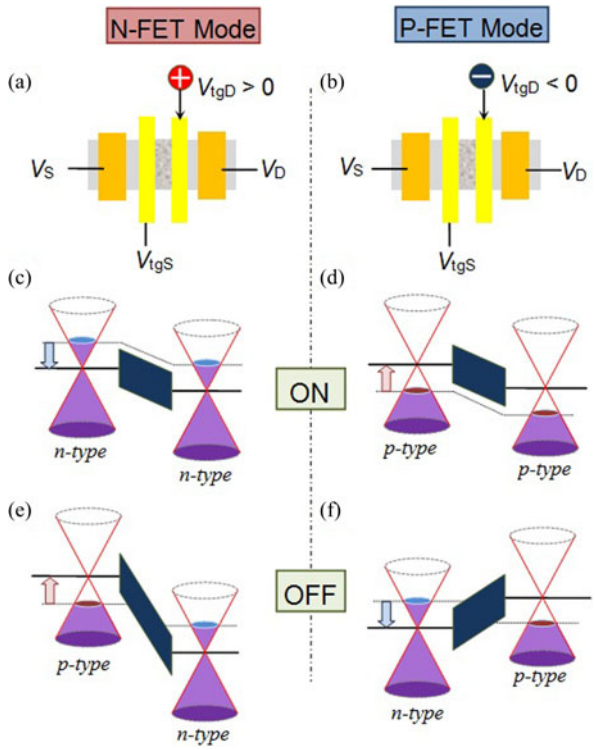

Fig. 5. Schematic illustration of polarity-reversible transistor operation. (a) When one of top gates is positively biased, device will be on by positive bias (b) and off by negative bias. This is n-type FET. (d) When one of top gates is negatively biased, then gate bias for on (e) and off (f) states will be inversed to be p-type FET.

IV. Polarity-Reversible Transistors

The concept of the proposed device enables a polarity-reversible transistor operation due to its dual-gated structure. With the band configuration shown in Fig. 2(a), V_{tgD} was fixed to negative. In this configuration, the device turns ON if $V_{\mathrm{tgS}} < 0$, as shown in Fig. 3. This is a p-type field-effect transistor (FET). If V_{tgD} is set to positive, on the other hand, the device turns ON if $V_{\mathrm{tgS}} > 0$, working as an n-type FET. The band configurations are summarized in Fig. 5. The role of each gate can be swapped. The device can also work similarly when the gate bias of the drain-side gate is swept while that of the source side is fixed. In any case, the device turns ON when $V_{\mathrm{tgS}} V_{\mathrm{tgD}} > 0$ and turns OFF when $V_{\mathrm{tgS}} V_{\mathrm{tgD}} < 0$.

Polarity-reversible transistor operation was demonstrated in a fabricated device at a temperature of 200 K, and $V_D = +100$ mV and $V_S = -100$ mV. Back gate bias was not applied in these measurements. Fig. 6(a) shows the N-FET mode with $V_{\mathrm{tgD}} > 0$, in which the device turns ON when $V_{\mathrm{tgS}} > 0$. The polarity of this device can be flipped just by reversing the polarity of one of the gate biases. Fig. 6(b) shows the P-FET mode operation with $V_{\mathrm{tgD}} < 0$ in the same device as that shown in Fig. 6(a). The maximum ON–OFF ratio in this device was nearly four orders of magnitude.

One of the advantages of the proposed device could be that it can reduce the channel length compared to conventional devices. The proposed device can reduce the channel length because the

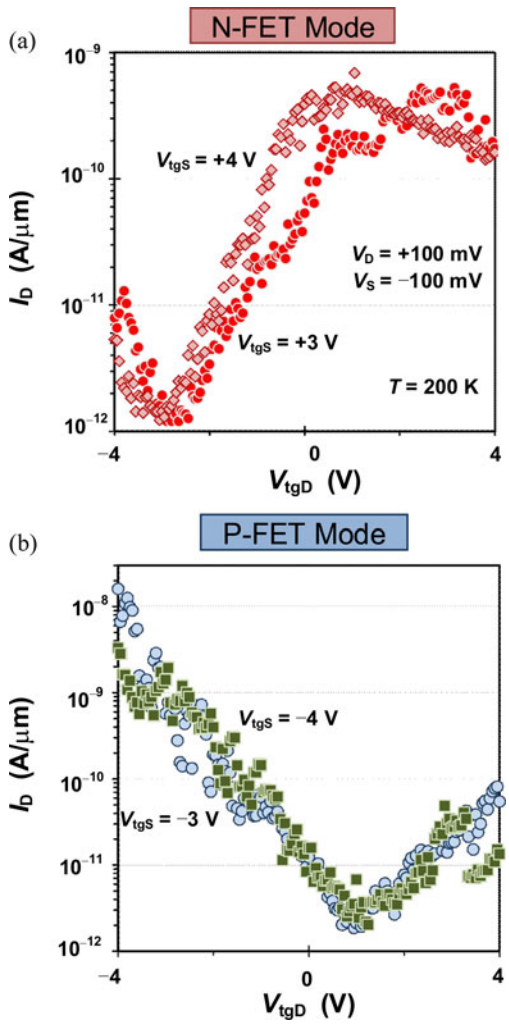

Fig. 6. Polarity-reversible transistor operation in one of fabricated devices at 200 K. The n-type FET mode with $V_{\mathrm{tgD}} > 0$ (a) and p-type FET with $V_{\mathrm{tgD}} < 0$ (b) are presented. Maximum on-off ratio was about four-orders of magnitude.

energy gap is required only in a small gap of a pair of split gates, which is easily fabricated by a self-aligned process. In the proposed device, the channel length was as short as 20 nm, which is quite difficult to fabricate in the conventional device structure in which the energy-gapped graphene region and a top gate are aligned. In graphene devices, the channel region must have an energy gap (band or transport gap) in order to control the carrier transport. However, mobility in a graphene nanoribbon (GNR), for example, will decrease by increasing the bandgap and narrowing the ribbon width [3]. If a GNR had a band gap of 1.1 eV, its mobility would be lower than that of silicon, suggesting that GNR cannot compete with silicon. This issue is also the same in the case of irradiated graphene; as the defect density increases, the transport gap will decrease. The tradeoff between mobility and energy gap implies that a novel device operating principle is required to overcome this tradeoff, and our device concept of the dual-gated structure could be a potential solution.

An inverter, which is one of the basic elements of logic circuits, can be formed using our proposed graphene device.

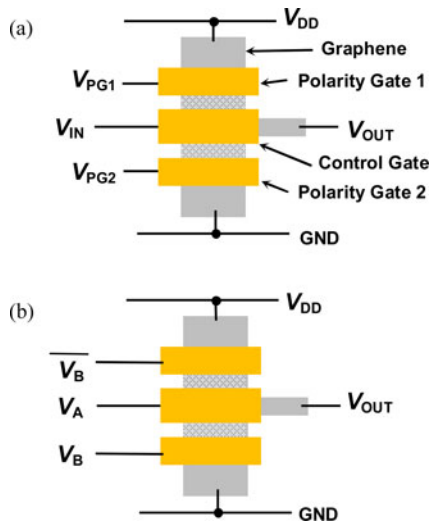

Fig. 7. (a) Triple-gated graphene inverter device. Graphene region is connected with V_{DD}, $\mathrm{V_{OUT}}$, and GND lines, and three top gates (polarity gates 1 and 2, control gate) can be independently biased. Every graphene region between top gates is irradiated with ion beams. Polarity gates can be replaced by impurity doping. (b) Same device structure as that in (a), but there are two inputs of gate bias working as the XOR logic circuit.

Fig. 7(a) is a schematic of a graphene inverter as a triple-gated device. In this device, two dual-gated transistors are combined; one gate of each device is merged into a single gate used as a control gate (V_{IN}), and two other gates are used as polarity gates (V_{pg1} and V_{pg2}). When $V_{\mathrm{pg1}} > 0$ and $V_{\mathrm{pg2}} < 0$, the device works as an inverter. In this device, $\mathrm{V_{DD}}$ and GND levels can be exchanged; the device also works as an inverter with $V_{\mathrm{pg1}} < 0$ and $V_{\mathrm{pg2}} > 0$. In any case, once the polarity gates are charged to fix the device configurations, the inverter requires only one gate to be charged. If the polarity control is not needed, the polarity gates can be replaced by impurity doping. In this case, an inverter can be fabricated with a single gating, which can reduce the total charge for inverter operation. The polarity-reversible transistors will be an advantage when it is used in the "exclusive OR" (XOR) logic [5]. In conventional devices, the XOR logic requires six transistors. In polarity-reversible transistors, on the other hand, the XOR logic requires only two double-gated transistors [5]. In our graphene device, only one triple-gated device, shown in Fig. 7(b), is required for XOR logic operation.

V. Summary

We proposed a transistor in which graphene has a pair of top gates and the graphene region between the top gates are irradiated with a helium ion beam to form a transport gap. We performed polarity-reversible transistor operations with the maximum on-off ratio of four orders of magnitude at 200 K. The features of the polarity reversibility are advantageous when several of these devices are applied to logic circuits so that the number of transistors and total charge required for calculations can be reduced, which can contribute to the reduction in power consumption in LSIs.

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