All-Optical Modified Fredkin Gate

Tanay Chattopadhyay

***Abstract*—Conventional digital circuits lose energy because the bits of information are destroyed during the operation. Reversible circuits are currently on the top approaches to power minimization with its application in all-optical-based systems. Fredkin gate is a very common reversible logic gate. In this paper, a modification of the Fredkin gate is proposed. All-optical circuit of this modified Fredkin gate (MFG) is also designed using semiconductor optical amplifier on the Mach–Zehnder interferometer switch. A 16-Boolean logical operational circuit is also shown using this MFG. The main advantage of this scheme is that we can design a 15-Boolean logical function using a single MFG unit. Only one operation (NAND) required two MFG units. Hence, complexity of the circuit can be reduced. Also, multivalued T-gate circuit using MFG is proposed.**

***Index Terms*—All-optical switch, Mach–Zehnder interferometer, multivalued logic (MVL), nonlinear optics, reversible logic.**

I. Introduction

ALL current computers are open dissipative systems requiring energy to run. Landauer [1] shows that for irreversible logic computation, each bit of information lost generates $kT \ln 2$ joules of heat energy, where k is the Boltzmann constant and T is the absolute temperature. The amount of dissipating heat is small ($\sim 2.9 \times 10^{-21}$ J) but not negligible. The design that does not lose any information is called "reversible." The reversible circuits offer an alternative that allows arbitrarily small energy dissipation. There are two types of reversible elements: one without memory, which is usually called a reversible logic gate and the other with memory, which is called rotary element [2]. The definitions of the reversible logic gate are as follows [3]–[7].

1) A gate or circuit is called "reversible" if there is one-to-one correspondence between its input and output assignment, i.e., the number of outputs is equal to the number of inputs. Each input pattern maps to a unique output pattern.
2) A gate with m inputs and n outputs is written as $m \times n$ logic gate, where reversible gates must have $m = n$. The output vector is a permutation of the number 0 to $2^n - 1$.
3) A gate is called "conservative" if hamming weight (number of logical ones) of its input is equal to the hamming weight of its output.

There are significant differences in the synthesis technique using a reversible gate which are [6], [7] as follows:

1) fan out is not permitted;
2) feedback is not permitted;
3) use minimum number of garbage outputs;
4) use minimum circuit level; and
5) use minimum number of gates.

Many reversible logic gates are proposed by different authors. Among them, Fredkin gate [8], Toffoli gate [8], Feynman gate [9], and Perers gate [10] are most common. Here, I am focusing on Fredkin gate in this paper because a modification of this gate is proposed. Furthermore, Fredkin gate is of major interest in quantum computing [11], optical computing [12]–[15], and low-power CMOS design [16]. For increasing transmission capacity, the modern electronic switches cannot handle the terabit-per-second datapulse. Also, optoelectronic switches increase the network cost and reduce the efficiency of wavelength-division multiplexing/optical time-division multiplexing (OTDM) optical networks. The capacity of these equipment is limited to a few hundred gegabites per second and cannot be easily extended. In order to overcome the electronic bottleneck and fully exploit the advantage of fibers, it is necessary to move toward the all-optical network. Here, an all-optical circuit of the modified Fredkin gate (MFG) is proposed and described using semiconductor optical amplifiers on the Mach–Zehnder interferometer (SOA-MZI) arms-based switch. This device is used because it can provide high speed, low energy requirement, short latency, high stability, fast switching time, low switching window (3.5–8 ps), easily fabricated in chip level, and commercial availability to that of other similar OTDM devices [17]–[20].

II. Background of Fredkin Gate and Its Modification

Fredkin gate is a popular 3×3 reversible and conservative logic gate. If (A, B, and C) and (X, Y, and Z) are the inputs and outputs of this gate, respectively, then we can say

$$\begin{aligned} X &= A \\ Y &= B \quad \text{iff } A = 0, \quad \text{otherwise } Y = C \\ Z &= C \quad \text{iff } A = 0, \quad \text{otherwise } Z = B. \end{aligned} \tag{1}$$

Logical operations [12], [13], [21] and arithmetical operations [6], [21], [22] can be performed using this gate.

Picton [23] made the first modification of the Fredkin gate. It is a 4×4 reversible gate. If (A, B, C, and D) and (P, Q, R, and S) are the inputs and outputs of this gate, respectively, then according to Picton's modification, we can write [23]

$$\begin{aligned} P &= A \\ Q &= B \\ R &= D \quad \text{iff } A \geq B, \quad \text{otherwise } R = C \\ S &= C \quad \text{iff } A \geq B, \quad \text{otherwise } S = D. \end{aligned} \tag{2}$$

Manuscript received September 4, 2010; revised November 18, 2010 and December 5, 2010; accepted January 1, 2011. Date of publication March 21, 2011; date of current version March 2, 2012.

The author is with Mechanical Operation (Stage-II), Kolaghat Thermal Power Station, West Bengal Power Development Corporation Ltd., Mecheda 721171, West Bengal, India (e-mail: tanay2222@rediffmail.com).

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Digital Object Identifier 10.1109/JSTQE.2011.2106111

TABLE I
TRUTH TABLE OF THE PROPOSED MFG

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	1	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1

In this paper, a new modification of the Fredkin gate is made. The advantage of this modification is that we can easily design 15-logical operations using a single MFG. Only NAND operation is done using two cascaded MFGs. Hence, this modification may make the logical operation simple and small in size. Also, we can design a multivalued logic (MVL) circuit using this MFG. The MFG is also a 4 × 4 reversible gate as given by Picton. If (A, B, C, and D) and (P, Q, R, and S) are the inputs and outputs of this gate, respectively, then outputs follow the logic

$$\begin{aligned} P &= A \\ Q &= B \\ R &= C \quad \text{iff } A \neq B, \quad \text{otherwise } R = D \\ S &= D \quad \text{iff } A \neq B, \quad \text{otherwise } S = C. \end{aligned} \tag{3}$$

Truth table is shown in Table I. From the drawn "Karnaugh map" (see Fig. 1), the Boolean equations of R and S can be written as

$$\begin{aligned} R &= C\,(A \oplus B) + D\,(A \odot B) \\ S &= C\,(A \odot B) + D\,(A \oplus B)\,. \end{aligned} \tag{4}$$

The schematic diagram of this MFG is shown in Fig. 2. In the next section, all-optical circuit of the MFG is proposed.

III. ALL-OPTICAL CIRCUIT OF THE PROPOSED MFG

A. Design and Operation

All-optical MFG can be easily designed using a single SOA-MZI switch with two control pulses. Two controlled SOA-MZI-based XOR operations are very common and are already proposed theoretically and experimentally by many authors [24]–[28]. My proposed all-optical circuit has also two controls like XOR operation. The main difference is that it has two incoming signals. But binary XOR operation has one incoming signal. The MFG circuit is shown in Fig. 3. MZI is formed by two 2 × 2 3-dB couplers for dividing and combining the data signals C and D. Two polarizing beam splitters (PBSs) have been introduced before and after SOAs to put in and out the control signals A and B. These optical control signals are introduced into two arms of the MZI to deplete the carriers in the corresponding SOA. This causes gain saturation and also the change in refractive index, which is used for switching. When one of the control pulses is turned on, the data signal is switched from the "cross" (×) into "bar" (∥) state. In this proposed circuit, the control pulse of vertically polarized light (↕) is applied and separated through a PBS according to Fig. 3. In PBS, s-polarized light is reflected and p-polarized light is transmitted. The polarization state of s-polarized light is vertical to the plane of incidence (↕) and p-polarized light is parallel to the plane of incidence, i.e., horizontally polarized light (•). The Jones matrix of the PBS is $M_i = R\,(-\alpha) \cdot P(0) \cdot R\,(\alpha)$, where $i = x$ and y

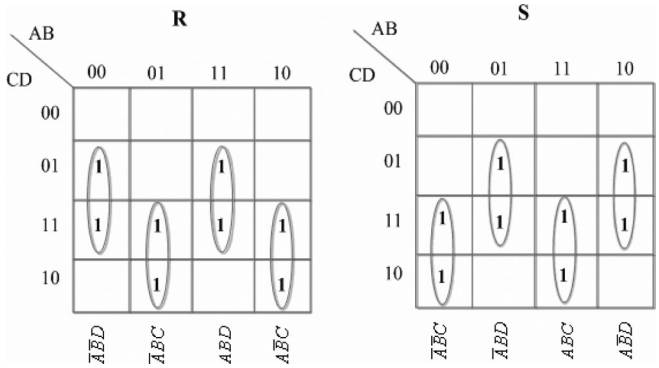

Fig. 1. "Karnaugh map" based on (3) and Table I.

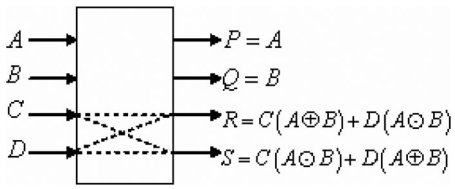

Fig. 2. Schematic diagram of MFG. "⊕" indicates binary XOR operation and "⊙" indicates binary XNOR operation.

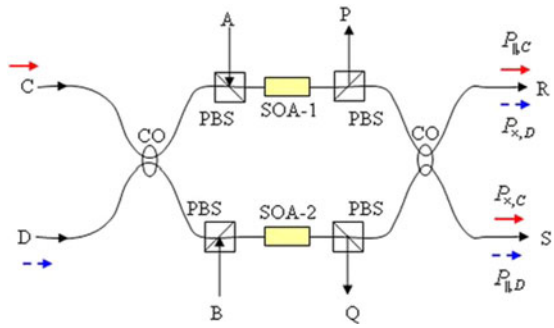

Fig. 3. All-optical modified Fredkin gate. SOA: semiconductor optical amplifier. PBS: polarizing beam splitter. CO: 2 × 2 3-dB beam splitter.

such that

$$M_x = \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix} \qquad M_y = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}.$$

When s-polarized and p-polarized lights fall on the PBS, they go into specific direction as follows.

For s-polarized light

$$\begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}\begin{pmatrix} 0 \\ 1 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \qquad \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix}\begin{pmatrix} 0 \\ 1 \end{pmatrix} = \begin{pmatrix} 0 \\ 1 \end{pmatrix}.$$

For p-polarized light

$$\begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}\begin{pmatrix} 1 \\ 0 \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \end{pmatrix} \qquad \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix}\begin{pmatrix} 1 \\ 0 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}.$$

Here, incoming and control signals are orthogonally polarized light. The switching window of the SOA-MZI switch is symmetric and can be determined by the corresponding change of phases ϕ_1 and ϕ_2 in SOA of both arms that can be adjusted by relative time delay between two control pulses as in XOR gate. With or without control signal, the data signals from input ports C and D are directed to the respective cross ports ($\times$) S and R. Suitable optical control signal A or B by means of carrier density is related to refractive index changes and induces the differential phase shift $\Delta\phi = \phi_1 - \phi_2$ of π in the MZI switch so as to switch the signals to their respective bar port ($\|$) R or S.

B. Theoretical Model

Some assumptions have to be considered in modeling of all-optical MFG using the SOA-MZI switch, such as, incoming signal does not affect the SOA gain dynamics. SOA is polarization independent of traveling wave type with null reflectivity. The gain and group-velocity dispersion is neglected, which is practically satisfied for pulse width in the picosecond range and SOA length is several micrometers long [29]. The length of the SOA is taken small such that the effect of amplified spontaneous emission (ASE) is neglected. Schares *et al*. [30] show that ASE becomes high enough and influenced the gain saturation only for SOA which is longer than 1500 μm. The energy of the control pulse is much lower than 1 pJ and pulse width is also narrow. So, two-photon absorption and ultrafast nonlinear refection are neglected [31]. Furthermore, the SOA small-signal gain, internal loss, and saturation energy are assumed to be wavelength independent and hence the same for both control and incoming signal; otherwise, we have to use a second-order polynomial of the gain spectrum [32] that could increase the model complexity. The saturation energy and unsaturated single-pass amplifier gain of the SOA can be expressed as [32]–[34]

$$E_{\rm sat} = \frac{\hbar\omega_0 wd}{a_N \Gamma} \tag{5}$$

$$G_0 = \exp\left[g_0 L - \alpha_D L\right] \tag{6}$$

$$g_0 = \Gamma a_N N_{\rm tr}\left(\frac{I\tau_e}{qwdLN_{\rm tr}} - 1\right) \tag{7}$$

where $E_{\rm sat}$ is the saturation energy of the SOA, G_0 is the unsaturated single-pass amplifier gain, Γ is the confinement factor, a_N is the differential gain, $N_{\rm tr}$ is the carrier density at transparency, q is the charge of an electron, w is the width of the active region of the SOA, d is the depth of the active region of the SOA, L is the active length of the SOA, α_D is the internal loss of the wave guide, $\omega_0 = 2\pi c/\lambda_0$ is the angular frequency, c is the velocity of light in vacuum, λ_0 is the wavelength of light, and $\hbar = h/2\pi$, where h is the Planck constant. Let us introduce a function $h(t) = \int_0^L g(z,t)dz$, where $g(z, t)$ is the model gain. A pulse when passes through SOA is amplified, and we obtain [29]

$$P_{\rm out}(t) = P_{\rm in}(t)\cdot G(t) = P_{\rm in}(t)\cdot\exp\left[h(t)\right] \tag{8}$$

where $P_{\rm in}(t)$ and $P_{\rm out}(t)$ are the powers of the input (it is also Gaussian in nature and the peak value is 0.2 mW) and output pulses, respectively

$$h(t) = -\ln\left[1 - \left(1 - \frac{1}{G_0}\right)\exp\left(-\frac{E_{\rm cp}(t)}{E_{\rm sat}}\right)\right]. \tag{9}$$

When a control pulse is injected into the MZI, it saturates the SOA at time t_s and changes its index of refraction. The gain of the SOA decreases rapidly. $E_{\rm cp}(t) = \int_{-\infty}^{t} P_{\rm cp}(t')dt'$ is the energy fraction contained in the leading edge of the pulse until the moment $t' \le t$. By definition, $E_{\rm cp}\,(t \to \infty) = E_c$ is the total energy of the control pulse. The gain recovers due to injection of carriers and can be obtained from the gain recovery formula [33], [34]

$$G(t) = G_0\left[\frac{G(t_s)}{G_0}\right]^{\exp[-(t-t_s)/\tau_e]}, \qquad t \ge t_s \tag{10}$$

where τ_e is the gain recovery time. When a periodic pulse train inserted in the SOA, there is no time to recover the gain to G_0, but to a lower one [35]. Here, we consider Gaussian pulse $P_{\rm cp}(t) = \frac{E_c}{\sigma\sqrt{\pi}}\exp\left(-\frac{t^2}{\sigma^2}\right)$ as a control signal. σ is related to full-width at half-maximum (FWHM) by $T_{\rm FWHM} \cong 1.665\ \sigma$. For the next pulse, gain starts to reduce again and the same process is repeated. The output power at bar port ($\|$) and cross port ($\times$) can be expressed as [27], [32]

$$P_{\|}(t) = \frac{P_{\rm in}(t)}{4}\cdot\{G_1(t) + G_2(t) - 2\sqrt{G_1(t)\cdot G_2(t)} \cdot\cos(\Delta\varphi)\} \tag{11}$$

$$P_{\times}(t) = \frac{P_{\rm in}(t)}{4}\cdot\{G_1(t) + G_2(t) + 2\sqrt{G_1(t)\cdot G_2(t)} \cdot\cos(\Delta\varphi)\} \tag{12}$$

where $G_1(t)$ and $G_2(t)$ are the gains of SOA-1 and SOA-2, respectively, at time t. Hence, the powers at the output ports R and S can be expressed as

$$P_R(t) = P_{\|,C}(t)\cdot\xi + P_{\times,D}(t)\cdot\zeta \tag{13}$$

$$P_S(t) = P_{\|,D}(t)\cdot\zeta + P_{\times,C}(t)\cdot\xi. \tag{14}$$

The terms $P_{\|,C}(t)$ and $P_{\times,D}(t)$ indicate the bar and cross port powers due to incoming signals coming from C and D, respectively. ξ and ζ are related to the logical states of A and B, respectively.

TABLE II
PARAMETERS USED IN THIS SIMULATION

Parameters	Symbol	Value
Injection current of SOA	I	600 mA
Confinement factor	Γ	0.48
differential gain	a_N	3.3×10^{-20} m^2
Line-width enhancement factor of SOA	α	6.5
Carrier density at transparency	N_{tr}	1.0×10^{24} m^{-3}
width of the active region of SOA	w	0.7 μm
depth of the active region of SOA	d	220 nm
Active length of SOA	L	150 μm
Internal loss of the wave guide	α_D	2700 m^{-1}
wave length of light	λ_0	1500 nm
Gain recovery time	τ_e	20 ps
Unsaturated single-pass amplifier gain	G_0	23.142 dB
Control pulse energy	E_c	15 fJ
Full width at half maximum of control pulse	σ	2 ps
Incoming pulse peak power		0.2 mW

C. Results and Discussions

Table II lists the values of the SOA parameters used in the simulation which are representative of bulk InGaAsP SOAs operating in the range of 1500-nm spectral region. Numerical simulation (with 50 Gb/s) for the output waveform is done using the parameter for SOA (shown in Table II). Fig. 4 shows the outputs *P, Q, R*, and S with the corresponding input $A =$ "0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1," $B =$ "0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1," $C =$ "0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1," and $D =$ "0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1." The gain variation of SOA-1 and SOA-2 of the MZI is shown in Fig. 5. In order to evaluate the performance of the gate, we define and calculate different metrics such as contrast ratio (CR), amplitude modulation (AM), extinction ratio (ER), etc.

The bit error rate (BER) in any optical system is set by the signal-to-noise ratio (SNR). BER cannot be easily calculated because the output waveform is not exact Gaussian in nature due to optical noise. If we assume that the output waveform is Gaussian, then BER is related to the quality factor Q of this circuit as follows [31]:

$$\mathrm{BER} = \frac{1}{2}\mathrm{erfc}\left(\frac{Q}{\sqrt{2}}\right) \tag{15}$$

where "erfc" is the complimentary error function and the quality factor Q is

$$Q = \frac{P_1 - P_0}{\delta_1 + \delta_0}. \tag{16}$$

Here, P_1 (P_0) and $\delta_1(\delta_0)$ are, respectively, the average power and standard deviation of the output at "1" state (0's state). I plot BER against control pulse energy E_c shown in Fig. 6. I found that BER is approximately 10^{-7} at $E_c = 15$ fJ. Also, the performance of the optical receivers depends on the SNR. It is

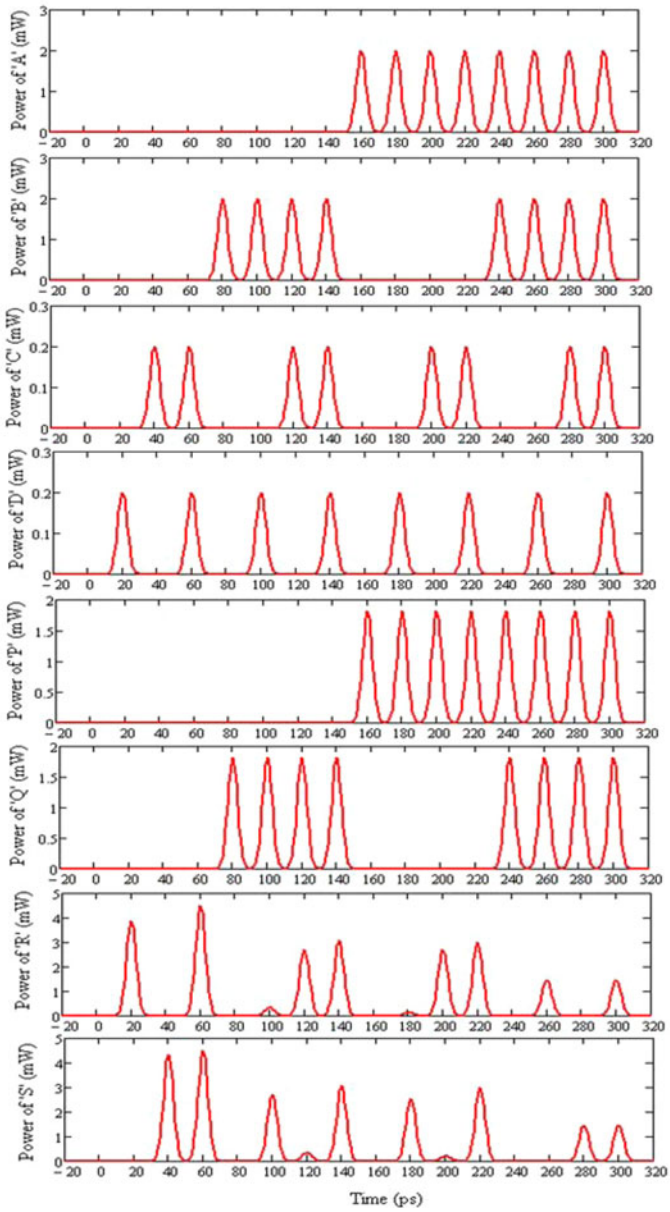

Fig. 4. Simulated waveform in 50 Gb/s (power in megawatt with time in picosecond) of the MFG modified Fredkin gate.

defined as [36]

$$\mathrm{SNR} = \frac{P_1^2}{\delta_1^2}. \tag{17}$$

The output CR is defined as the ratio of the mean value of the output peak power for "1," say P^1_{mean}, to the mean output peak power for "ZERO" (0), say P^0_{mean}, in decibels [29], [31], i.e.,

$$\mathrm{CR(dB)} = 10\log\left(\frac{P^1_{\mathrm{mean}}}{P^0_{\mathrm{mean}}}\right). \tag{18}$$

The AM is defined as [29], [31]

$$\mathrm{AM(dB)} = 10\log\left(\frac{P^1_{\mathrm{max}}}{P^1_{\mathrm{min}}}\right) \tag{19}$$

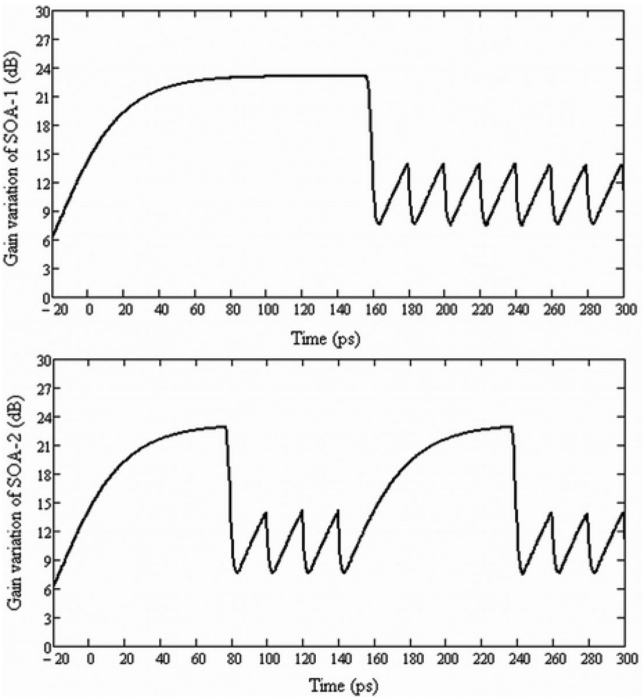

Fig. 5. Gain variation of SOA-1 and SOA-2 of the MZI-based MFG when control signals (A, B) are applied.

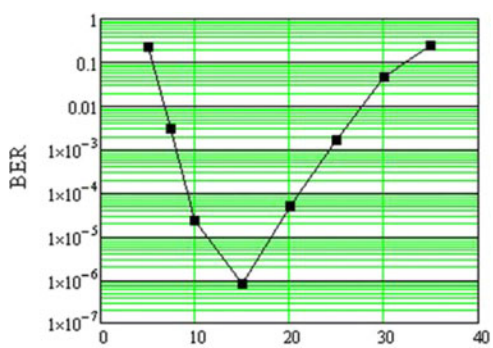

Fig. 6. BER against control pulse energy E_c.

where $P^1_{\max}$ and $P^1_{\min}$ are the maximum and minimum values of the peak power of "HIGH" (1). The ER is defined as [29], [31]

$$\mathrm{ER(dB)} = 10 \log \left(\frac{P^1_{\min}}{P^0_{\max}} \right) \tag{20}$$

where $P^1_{\min}$ and $P^0_{\max}$ are the minimum and maximum values of the peak power of "HIGH" (1) and "ZERO" (0), respectively. For optimum gate performance, first the CR must be as high as possible so that the largest fraction of input exists at the output; second, the AM must be as low as possible so that output "1" has the same level and the pattern effect is negligible; and third, the ER must be as high as possible so that the "1" level can be distinguishable from "ZERO" (0). The dependence on the outputs CR, AM, SNR, and ER with control signal energy E_c is shown in Fig. 7. At $E_c = 10$ fJ, we obtain low AM = 3.038 dB, high SNR = 12.046 dB, and CR $\cong$ 7.395 dB. Also, the peak

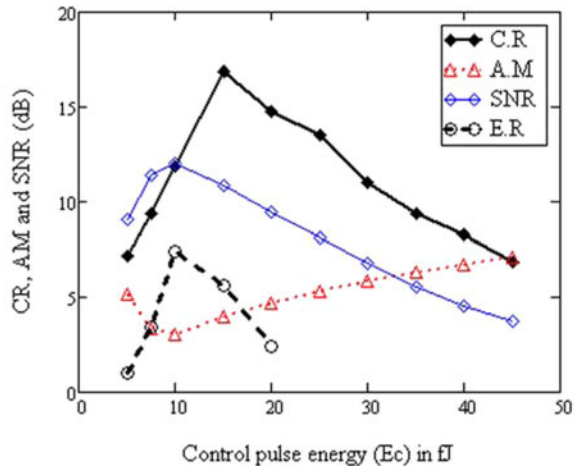

Fig. 7. Outputs CR, AM, SNR, and ER with control pulse energy E_c.

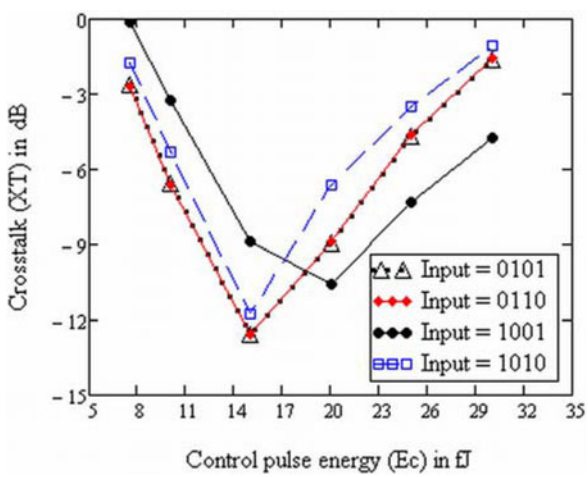

Fig. 8. Variation of XT with control pulse energy E_c.

value of CR ($\sim$16.904 dB) is obtained at $E_c = 15$ fJ. Leuthold *et al*. [37] experimentally showed that for SOA biasing current I_1 and I_2, if equal then, different extinction ratio (*E.R*) found. For control = "ON," we find ER = 29 dB, and for control = "OFF," we find ER = 13 dB. This can be optimized to 20 dB if $I_1 \neq I_2$ [37], [38] or by increasing the path length of one arm of MZI [39].

The switching crosstalk (XT) is defined as the ratio of P_{nt} to P_t, the power of switched nontargeted and targeted signals, respectively, and is given as [40], [41]

$$\mathrm{XT} = 10 \log \left(\frac{P_{\mathrm{nt}}}{P_t} \right). \tag{21}$$

The ratio can be calculated from (11) and (12). The variation of XT with control signal energy E_c is plotted in Fig. 8 for the inputs *ABCD = 0101, 0110, 1001,* and *1010*. Minh *et al*. experimentally shows that for a symmetric MZI, XT increases if the two control pulse energies are different [40]. In other paper, Ngah and Ghassemlooy show that using increased time delay between two control pulses, XT also increases [41]. When one data pulse transmits through the switching window, the next set of data cannot pass until the gain recovery of the SOA take

place. Hence, the switching time of our proposed circuit depends on the gain recovery time τ_e of the SOA. The performance of this circuit depends on the SOA carrier lifetime. This parameter is crucial and can impose the strict limitation on the performance of the gate, which can severely alter the pattern effect observed on the switched-out pulses. Hence, the carrier lifetime should be reduced. The most direct method to achieve the goal is by increasing SOA injection current and length [42] but the cost will be twice [29]. As the length of the SOA increases, we cannot neglect ASE [31]. Also, quantum-dot SOAs can be used for complex gain recovery enhancement technology to reduce carrier lifetime [43], [44]. Recently, high-speed operations have been successfully demonstrated in many literature using hybrid-integrated MZI all-optical switch, which can demultiplex 168-Gb/s data pulse [45]. Also, 320-Gb/s operations are successfully reported [46].

IV. Applications

A. All-Optical Logical Operation

All-optical MFG can be successfully used to design 16 logical operations. Binary logic (radix $= 2$) has two logical states 0 and 1. Depending on the radix and number of variables used, different logic functions can be generated. The number of possible function is [47]

$$N = R^{(R^n)} \tag{22}$$

where R is the radix and n is the number of variables. In binary logic of two variables ($R = 2, n = 2$), there are $2^{2^2} = 16$ possible functions as shown in Table III.

I can apply any one of the light sources A, B, 1 (constant pulsed light source), or 0 (no light source) to the four inputs (A, B, C, and D) of the MFG, and we get different logical operations of the Table III according to Fig. 9(a)–(g).

In Fig. 9(h), a NOR gate is implemented keeping the inputs A $= 1$, B $= (A + B)$ (combined beam of A and B by a beam combiner), C $= 0$, and D $= 1$. Hence, according to (4), we find the outputs $P = 1$, $Q = (A + B)$, $R = \bar{A}\bar{B}$, and $S = (A + B)$.

Two MFG units are cascaded to design NAND operation, which is shown in Fig. 9(i).

B. Multivalued Logical Operation

MVL (radix > 2) may be the best solution in future all-optical signal processing systems. It can increase the data-carrying capacities, large information storage, and high-speed arithmetical operations [48]–[50]. Binary logic is limited to only two logical states 0 and 1. But MVL has n logical states $\{0, 1, 2, \ldots, n-1\}$. T-gate is a "universal" gate in MVL operation. Any logic (MAX, MIN, Inverter, Literals, etc,) arithmetical operation and storage element can be easily designed with this T-gate [48]–[51]. T-gate has n inputs $\{A_0, A_1, \ldots, A_{n-1}\}$, a select input line "$x$," and one output "$T$," respectively. The property of the T-gate is

TABLE III
Sixteen Boolean Logical Functions (F1–F16)

Inputs	A	0	0	1	1	
	B	0	1	0	1	
Outputs	F1	0	0	0	0	False (0)
	F2	0	0	0	1	AB
	F3	0	0	1	0	$A\bar{B}$
	F4	0	0	1	1	A
	F5	0	1	0	0	$\bar{A}B$
	F6	0	1	0	1	B
	F7	0	1	1	0	$A \oplus B$
	F8	0	1	1	1	$A + B$
	F9	1	0	0	0	$\bar{A}\bar{B}$
	F10	1	0	0	1	$A \odot B$
	F11	1	0	1	0	$\bar{B}$
	F12	1	0	1	1	$A + \bar{B}$
	F13	1	1	0	0	$\bar{A}$
	F14	1	1	0	1	$\bar{A} + B$
	F15	1	1	1	0	$\bar{A} + \bar{B}$
	F16	1	1	1	1	True (1)

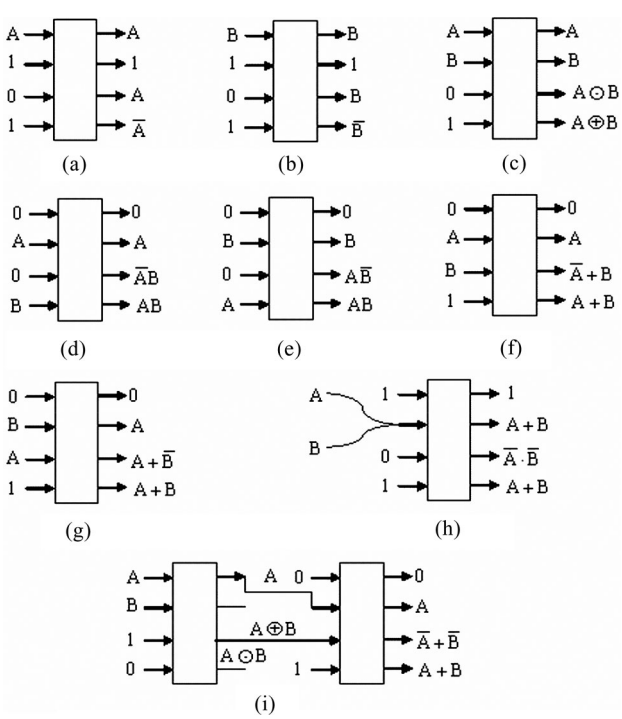

Fig. 9. 16-Boolean logical operation circuit by MFG.

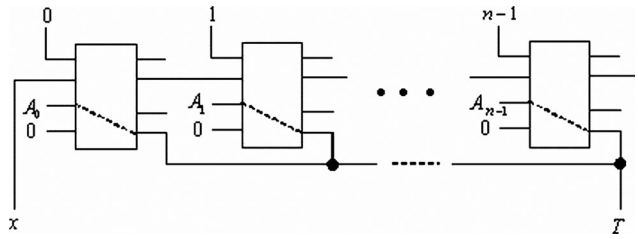

Fig. 10. Multivalued T-gate using MFG. x is the selected input and T is the output.

shown as follows:

$$T(A_0, A_1, \ldots, A_{n-1}; x) = \begin{cases} A_0, & \text{if } x = 0 \\ A_1, & \text{if } x = 1 \\ \vdots & \\ A_{n-1}, & \text{if } x = n-1. \end{cases} \tag{23}$$

In all-optical implementation, the logical states can be selected with different polarized state lights [51], [52]. "0" state is due to absence of light. Different circuits using all-optical T-gate in quaternary logic (radix = 4) are shown in my previous manuscript [51].

The proposed MFG has a 4×4 output system. So, it can also be successfully used to design MVL circuits. From (3), we find that when A = B, the input signals are directed to the cross port of MZI. Using this property, we can easily design a multivalued T-gate circuit. The schematic diagram of a multivalued T-gate is proposed using MFG, which is shown in Fig. 10. The operation of this circuit is easy. As an example, if $x = 1$, then A_1 input of the second MFG (from the left) is only connected to the output *T*. Other gates give "0" (no light) to the output. So, output $T = A_1$.

V. Conclusion

In this paper, a modification of the Fredkin gate is done and its all-optical circuit using SOA-MZI is proposed. Numerical simulation is done to calculate different metrics such as CR, ER, AM, BER, etc. The simulated values are BER $\sim 10^{-7}$, AM $\sim$3.038 dB, and CR $\sim$7.395 dB. This result is not satisfactory, so for better performance they should be less than 10^{-9}, below 1 dB, and over 10 dB, respectively. This happens due to the peak fluctuation at the outputs R and S which is shown in Fig. 4. To obtain satisfactory results, SOA design parameters should be thoroughly calibrated. Hence, the design of the proposed MFG is amenable to further improvements and this paper constitutes a preliminary effort toward this goal, which could possibly be extended and optimized in the future. Besides, a somewhat reduced rate than 50 Gb/s would produce better results without compromising the whole concept. However, such an MFG can be successfully used to design 16 Boolean logical operations and MVL circuits. All the outputs of these circuits (shown in Fig. 9) have any logical states of the 16 Boolean operations. Hence, we can say that there is no garbage in this case.

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Tanay Chattopadhyay was born in Kolkata, West Bengal, India, on January 15, 1977. He received the M.Sc. degree in physics with special paper electronics from the University of Calcutta, Kolkata, in 2002. He also received the Diploma in computer hardware maintenance and networking in 2006.

He is currently working as a Junior Manager at Kolaghat Thermal Power Station, Mecheda, West Bengal, India. He has more than 40 papers published/accepted in international/national journals and symposia proceedings and also writes one book chapter. He is also a reviewer of several international journals. His current research interests include optical logic-based information processing, multiple-valued logic, and laser and nonlinear optics.

Mr. Chattopadhyay joined as an Editorial Board Member in Optoelectronics and Photonics in the journal *Physics Express* on July 2010.