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A gate driver for parallel connected MOSFETs with crosstalk suppression

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ABSTRACT

New semiconductor materials offer several advantages for modern power systems, including low switching and conduction losses, excellent thermal conduction of a die, and high operation temperature. Avionics is one of the main beneficiaries of the progress in power devices, as it enables more compact and lighter converters for future More Electrical Aircraft. However, these advancements also come with new challenges that must be addressed to avoid potentially dangerous situations and fully utilize the capabilities of fast SiC MOSFETs. One such challenge is the high drain voltage rate during the switching process, which leads to a significant injection of current into the gate circuit (crosstalk effect). This increased current injection increases the risk of shoot-through conduction and thermal runaway. Although preventive measures are well-known, they offer limited protection in the case of parallel MOSFET connections. Therefore, this paper considers crosstalk features for parallel MOSFET connections, such as parasitic inductance of gate driver trace and gate voltage distribution. A special model is proposed to predict the magnitude of induced gate voltage under different conditions considering the nonlinear behavior of the MOSFET reverse capacitance. A new clamp circuit with an individual low-inductance path for each parallel switch is also proposed to suppress the consequences of crosstalk. The modified circuit operates independently from the main gate driver circuit; therefore, it does not change the switching time and electromagnetic interference pattern of the inverter. The efficiency of the new gate driver is confirmed through simulation and experimental results.

KEYWORDS

Power electronics, SiC MOSFET, parallel connection, gate driver, parasitic effects.

Over the last two decades, the continuous improvement of new semiconductor materials has greatly contributed to the popularity and variety of SiC power devices. Power converters have made a big step toward higher power densities, higher switching frequencies, and lower losses due to the outstanding characteristics of SiC devices[1,2]. The advantages of new power devices are especially welcomed with considerable interest in avionics, and many studies have confirmed the superiority of SiC converters in terms of increased efficiency and weight reduction[3]. With fast switching transient processes, SiC MOSFETs can operate at higher switching frequencies without deteriorating the system's efficiency. Therefore, weight optimizations of the cooling system and power filters can lead further toward the converter's miniaturization[4].

Another advantage of SiC devices is their high operational junction temperature, the upper limit of which is far beyond the capabilities of Si devices[5]. Fully SiC inverters can operate under harsh thermal conditions, which are common in jet engine housing environments. Thus, many mechanical apparatuses, which were the only options available to engineers several years ago, could be replaced with power electronics today, increasing reliability and efficiency.

Although power electronics prosper these days, conquering transportation and aviation confidently, the engineers experience new issues, which are downsides of SiC's incredible performance[6]. Fast switching and high maximum drain-source voltage led to extreme values of voltage rate, and a short pulse of current with a significant magnitude was injected through reverse transfer capacitance into the gate circuit when the drain-source voltage changed from one extremum to another. Although the mechanism generating the pulse exists in all types of MOSFETs regardless of their material, SiC devices suffer the most. If unaddressed, the generated voltage can easily reach the threshold level and cause a shoot-through or thermal runaway[7]. To increase the margin between the threshold level and gate voltage in a turn-off state, the negative shift of the minimal gate voltage became a rule of thumb if SiC devices were used in the design.

Although negative gate voltage helps in most applications, there are still special cases (i.e., unusually high rates of drain-source voltage (V_{ds}), high ambient temperature), where the safe margin is not large enough and additional measures are required to prevent spurious turn-on. Several researchers have studied this phenomenon focusing on methods to evaluate or predict the generated voltage level[8,9] and methods to reduce its amplitude. Some methods exploit separated turn-on and turn-off resistances (or modify them) to clamp gate voltage tightly to gate driver output[10–12]. The schematics of these gate drivers are simple and do not usually require any additional control signals. The direct proportion between the rate of V_{ds} and suppression efficiency is a feature of such structures, and it could be considered as a drawback for some applications. Another approach is an adaptive shift of gate voltage that can temporarily change the voltage level to satisfy safe conditions[13,14]. A sophisticated system of sensors and switches is included in the gate driver circuit to perform shift operations.

Although the problem is well covered for the case of a single device, there is a lack of solutions for parallel MOSFETs, and SiC MOSFETs connected in parallel are still exposed to high dV_{ds}/dt values. Parallel connection of discrete MOSFETs could be useful

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in inverter design, as discrete components are featured with compact packages that might increase the power density of the system or reduce values of parasitic components[15,16]. For optimization design techniques, paralleling scales the semiconductor area and conducting power[17]. Meanwhile, the parallel connection has several distinct features, which limit the efficiency of the solutions suitable to a single MOSFET. The parallel connection has nonzero trace parasitic inductance due to the spread gates' locations. The inductance limits dI/dt of bypassing circuits (clamps); thus, reducing its efficiency. Sometimes the gate circuit experiences a limit of free space, and its PCB cannot accommodate a large number of additional components if a complex auxiliary circuit is implemented for each MOSFET of the group.

Therefore, this paper presents a gate driver for a parallel MOSFET connection with a clamping auxiliary circuit to reduce the crosstalk between devices in a leg configuration. The circuit works independently of the main gate driving circuit; therefore, it does not affect switching times. Additionally, loop path for crosstalk current is near its MOSFET, so parasitic inductances have less influence on the performance of the clamp. The simulation model of $V_{ds}(t)$ based on the gate charge current and accurate C_{rss} calculation is developed to analyze the generated gate voltage and efficiency of suppression circuits. Section 1 describes the simulation model of $V_{gs}(t)$ during crosstalk and presents simulation results for different operating conditions or component values. Section 2 explains the structure of the proposed suppression circuit and its simulation model. Section 3 contains the experimental results, including the waveforms of the gate voltage of unmodified and modified circuits and comparisons of simulated and measured curves.

1 Modeling of crosstalk for parallel connection of MOSFETs

1.1 Gate drive circuit with parallel MOSFETs

The design of a gate driver circuit is challenging due to the distributed locations of gate inputs. Moreover, the stable operation of parallel MOSFETs requires individual gate resistance for each transistor, which makes it difficult to use conventional methods of crosstalk suppression. Distances between gates are usually determined by the dimensions of MOSFET's package, and parasitic trace inductance between the gate driver and the farthest gate always exists and could affect the gate signal significantly in case of a high inductance value.

Figure 1 shows a schematic of a distributed gate drive circuit and its simplified model. The prototype of the circuit and its printed circuit board (PCB) layout are shown in Figure 2.

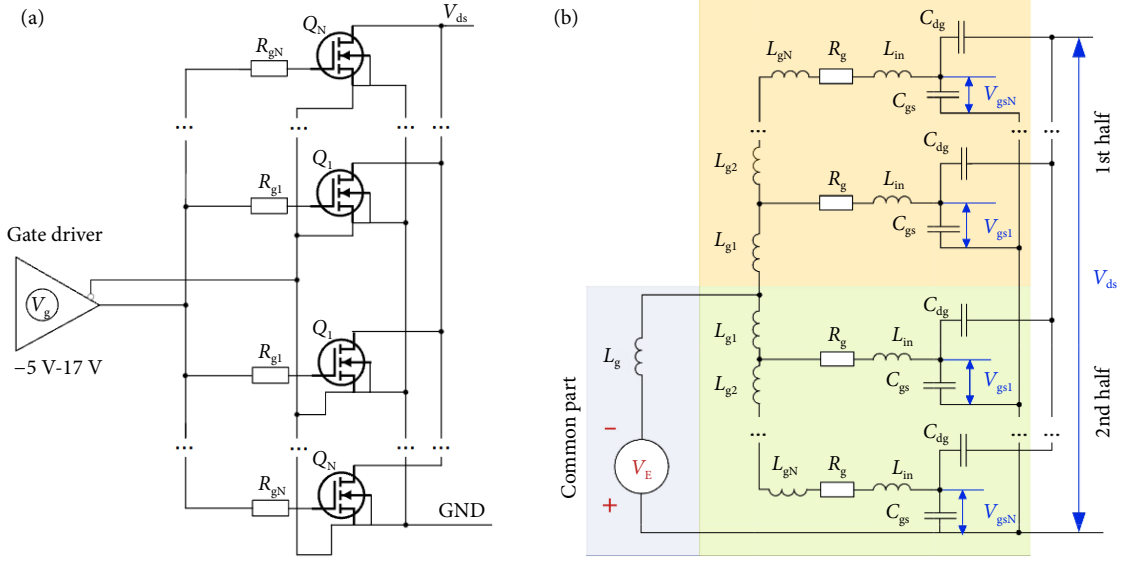

Fig. 1 Distributed gate drive circuit of parallel MOSFETs. (a) Schematic view and (b) simplified model.

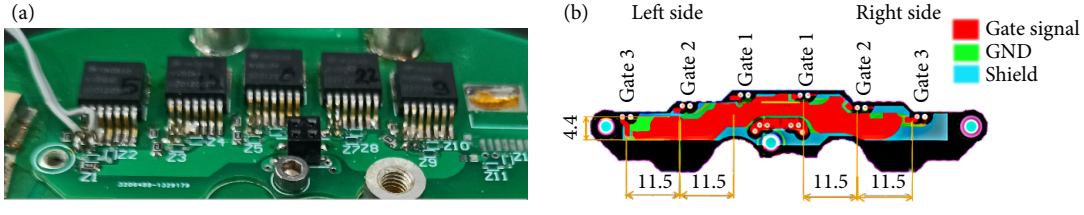

Fig. 2 Example of parallel MOSFET and layout of gate traces.

The model is considered symmetrical with respect to the center of the MOSFET group, so the output of a gate driver splits into two equal branches at the line of symmetry. Therefore, voltages and currents are the same in two branches (considering all components have equal values). The model also assumes that all MOSFETs have the same characteristics and parasitic elements. The model is suitable for MOSFETs with separated source pin that conducts only gate current (TO-263-7 or TO-247-4), as source parasitic inductance and drain current transients are not included in the calculation.

Each MOSFET and its gate resistor act as an individual input for the current I_{dg} through MOSFET's reverse transfer capacitance C_{dg} (see distribution of currents in Figure 3). A system of two differential equations expresses the gate voltage (V_{gs}) and gate resistor current (I_g) for each element with number k, $1 \leqslant k \leqslant N$:

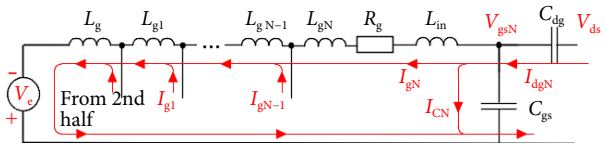

Fig. 3 A single element of a gate driver circuit.

$$\begin{cases} V_{gsk} = L_{in}\dfrac{dI_{gk}}{dt} + (R_{gin}+R_{gex})I_{gk} + \sum_{i=1}^{k}\left[L_{gi}\sum_{j=i}^{N}\dfrac{dI_{gj}}{dt}\right] + \\ \qquad 2L_g\sum_{j=1}^{N}\dfrac{dI_{gj}}{dt} - V_e \\ C_{dg}(V_{ds})\dfrac{dV_{dgk}}{dt} = I_{gk} + C_{gs}\dfrac{dV_{gsk}}{dt} \\ V_{gsk}(0) = -V_e; I_{gk}(0) = 0; \end{cases} \tag{1}$$

where R_{gin} and R_{gex} are the inner and external gate resistances, respectively. The parasitic inductance L_{in} includes the inductance of MOSFET leads and the inductance of traces between the wide trace of gate signal and the gate. The exact value for lead's inductance can be obtained using SPICE manufacturer models. In general, a value of approximately 15 nH is a good estimation for this parameter.

Other trace inductances are calculated based on the trace shape, structure, and materials of PCB. The equations for the inductance of a PCB trace consisting of two parallel strips with a dielectric between and for the inductances of two parallel wires with opposite currents are given as follows[18,19]:

$$L_{PCB} = \frac{\mu_0\mu_r HL}{W}, L_{2wire} = \frac{\mu_0 L}{\pi}\left(\ln\left(\frac{2D}{d_{wire}}\right) + \frac{1}{4}\right) \tag{2}$$

where μ_0 and μ_r are the permeability of free space and relative permeability of the PCB material, respectively; L, W, and H are the length, width of the trace, and distance between layers, respectively; D and d_{wire} are the distances between wires and their diameter, respectively. Values of trace inductances with various parameters are presented in Figure 4.

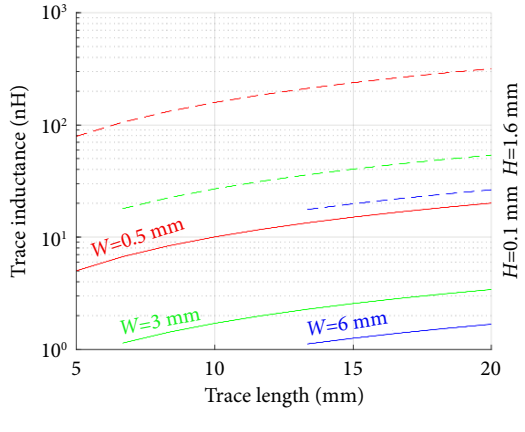

Fig. 4 Gate-to-gate trace inductances with different PCB trace characteristics.

The results show that in some cases, the inductance of traces between the gate driver and resistor is comparable to that of MOSFET leads. Inductance values used in the simulation are presented in Table 1.

Table 1 Trace parameters and inductance values of the simulation model

L (mm)	H (mm)	W (mm)	Relative permeability	L_{gk} (nH)	L_g (nH)	L_{in} (nH)
12	0.1	4.5	4	1.34	10	15+6.5

Note that L: gate to gate distance; H: layer thickness; W: trace width; L_{gk}: gate to gate inductance; L_g: common path inductance; L_{in}: MOSFET lead's inductance.

1.2 Transition of drain-source voltage

The change in drain-source voltage (V_{ds}) determines the amplitude and shape of the injected gate current (I_{dg}) and gate voltage (V_{gs}) during the crosstalk. In a real device, many factors influence the transient of V_{ds} and increase the complexity of the modeling process. In this paper, the parasitic inductances of the drain circuit, charging of output MOSFET capacitance, and reverse recovery of body diode are not included in the calculation to focus on processes in the gate circuit. The influence of these factors is described at the end of the chapter. There are no parasitic components across the power connections between the high and low sides of MOSFETs, and V_{DC} voltage source DC link voltage can be expressed as follows.

$$V_{DC} = V_{dsHS} + V_{dsLS} \rightarrow V_{dsLS} = V_{DC} - V_{dsHS} \tag{3}$$

According to the basics of MOSFET switching with inductive load, when gate voltage is applied, V_{dsHS} starts to decrease with the rate that is proportional to gate current $i_{gHS}(t)$ when V_{gsHS} reaches level of Miller plateau (V_{miller}):

$$V_{dsHS} = V_{dgHS} + V_{gsHS} = \int_{t_{start}}^{t_1}\frac{-i_{gHS}(t)}{C_{dg}(V_{dsHS})}dt + V_{miller}, V_{dgHS}(t_{start}) = V_{DC} - V_{miller} \tag{4}$$

$$i_{gHS}(t) = \frac{V_{gmax} - V_{miller}}{R_{gin} + R_{gex}} \tag{5}$$

Voltage value V_{miller} can be obtained using threshold voltage (V_{th}), the maximum drain current (I_{max}), and the forward transconductance (g)

$$V_{miller} = V_{th} + gI_{max} \tag{6}$$

In this study, SiC MOSFET NVBG020N120SC1 is used, and its characteristics are presented in Table 2.

Table 2 Characteristics of NVBG020N120SC1

C_{ISS} (pF)	V_{th} (V) (Id = 10 mA)	g (S)	R_{gin} (Ohm)	V_{gmax} (V)
2,943	2.7	34	1.6	25/−15

Although these data are clearly stated in the datasheet, figures must be adjusted to the operational point of MOSFETs because of high nonlinearity of transconductance characteristics. Datasheet table values for transconductance and gate threshold voltage are 34 A/V, and 2.7 V, respectively, and the adjusted values (to the point of $I_{max} = 40$ A) are 24.6 A/V and 6.96 V (see Figure 5).

$$V_{miller25\,°C} = V_{th25\,°C} + g_{app25\,°C}I_{max} = 6.96\text{ V} + 24.6\frac{\text{V}}{\text{A}}40\text{ A} = 8.59\text{ V} \tag{7}$$

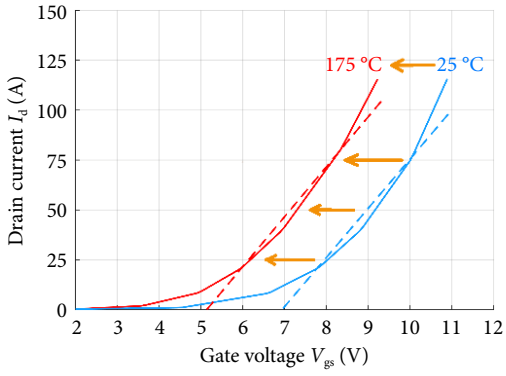

Fig. 5 Transfer characteristics and its linear approximation at different junction temperatures.

The drain-gate or reverse transfer capacitance (C_{dg} or C_{rss}) is a function of V_{DS} and cannot be used directly as a constant value. In this study, an instant value of C_{dg} is calculated with MATLAB by two-step (linear and logarithmic) approximation of datasheet plot (see Figure 6). At the first step, several points are acquired manually from the datasheet plot with software GetData Graph Digitizer, so linear approximation fits the required curve in log axis. Then, logarithmic approximation in MATLAB is used to transform copied linear approximation of logarithmic curve into normal linear approximation by calculating the following coefficient for each interval:

$$m_i = \frac{\log_{10}\left(\frac{C_{rssi+1}}{C_{rssi}}\right)}{\log_{10}\left(\frac{V_{dsi+1}}{V_{dsi}}\right)}. \tag{8}$$

Additional points can be obtained by applying this coefficient to any value of V_{ds} within the range $(V_{dsi}; V_{dsi+1})$ into the equation:

$$C_{rssj} = C_{rssi}\left(\frac{V_{dsj}}{V_{dsi}}\right)^{m_i} \tag{9}$$

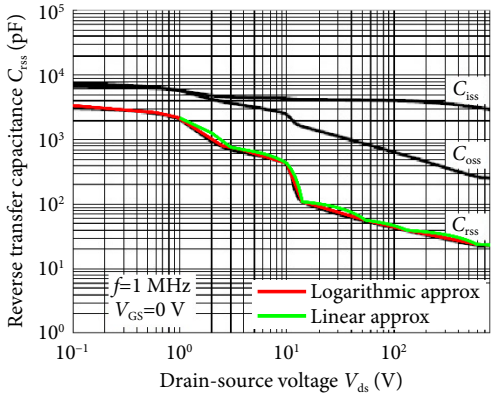

Fig. 6 Comparison of logarithmic, linear approximations, and datasheet curve[20] of $C_{rss}(V_{ds})$.

Simulink model of V_{ds} voltage source generating the waveform according to Eqs. (3–5) is shown in Figure 7.

Another approach to determine the instant value of V_{ds} is to use a simplified ramp model of voltage source (see "ramp model" in Figure 8) with dV_{dsHS}/dt calculated through total charge of $C_{dg}(V_{dg})$ that is required to discharge the capacitor from initial

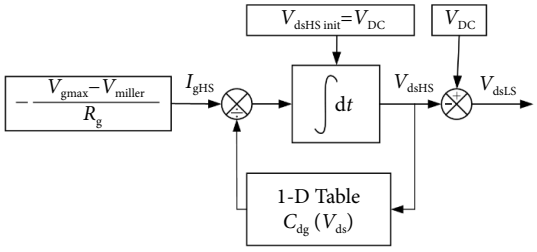

Fig. 7 Simulink model of the V_{ds} voltage source based on integration of i_{gHS} and varying value of $C_{dg}(V_{dg})$.

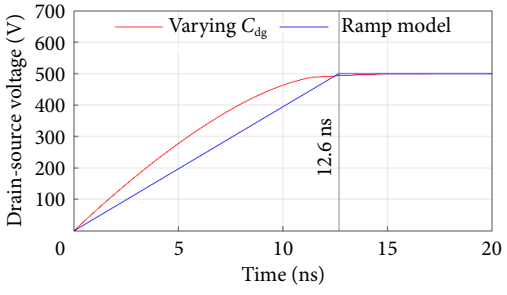

Fig. 8 Drain-source voltage generated using the two methods.

$V_{ds} - V_{miller}$ to the beginning of the ohmic region V_{dsmin}[9] without modification of C_{dg}

$$V_{dsmin} = I_{max}R_{don}(V_{gs} = V_{miller}) \tag{10}$$

$$Q_{dgsat} = \int_{V_{dsmin}}^{V_{dsmax}-V_{miller}} C_{dg}(V_{ds})\,dV \tag{11}$$

Switching time t_1 is determined using the charging capabilities of the gate driver circuit and drain-gate capacitance of MOSFET, and calculated as follows:

$$t_1 = \frac{Q_{dgsat}(V_{dsmax}, V_{dmsin})}{i_{gHS}} = \frac{Q_{dgsat}(V_{dgmax}, V_{dgmin})}{\frac{V_{gmax}-V_{miller}}{R_{gin}+R_{gex}}};$$

$$V_{dsLS}(t) = \begin{cases} \frac{V_{DC}-V_{dsmin}}{t_1}t, 0 < t < t_1 \\ V_{DC}-V_{dsmin}, t \geqslant t_1 \end{cases} \tag{12}$$

As dV_{ds}/dt is a constant value in this model throughout the transition period, $V_{ds}(t)$ has ramp shape starting from 0 V and reaching its maximum value $V_{dsmax} = V_{DC} - V_{dsmin}$ at time t_1. Figure 8 shows the waveforms of V_{ds} generated using the methods.

Due to the low value of C_{rssHS} at the beginning of the transition, the charging process is faster in case of varying C_{rss} with the same amount of gate current, and the dV_{ds}/dt is higher. Therefore, the current pulse through C_{rss} of low side MOSFET is higher. In further simulations, this method is used to generate $V_{ds}(t)$.

Although the parasitic components of drain and source circuits are omitted in this model, they affect the waveform of V_{ds} and V_{gs}. The parasitic inductance of the power lines (drains, sources of high and low sides MOSFETs, and traces between them) causes the voltage overshoot of $L_{par}\frac{dI_d}{dt}$. In this case, I_d includes load current, reverse recovery current, and charge current of the output capacitance. The overshoots extend the period of nonzero dV_{ds}/dt. Therefore, it increases injected charge and total value of V_{gs}, even though the rise is not significant with noticeable overshoot due to the low value of C_{rss} at high voltage. However, after the transition

of V_{ds}, the power trace's parasitic inductance starts to resonate together with C_{DS} passing the oscillation into gate circuit as well.

The output capacitance of the MOSFET and the reverse recovery process affect the MOSFET at a forced transient of V_{ds} by generating a short current pulse with significant amplitude. The pulse is responsible for oscillation in the drain circuit and can distort the external gate signal if any common inductivity between the gate and source (even in the presence of a Kelvin connection) exists. Common inductance creates an additional voltage pulse in the gate circuit, increasing the load on the gate driver and suppressing the circuits.

1.3 Crosstalk simulation

The simulated model includes six parallel MOSFETs (NVBG 020N120SC1 type), three per branch. The parameters of the traces are presented in Table 1. Simulations are performed in MATLAB Simulink by numerically solving the differential Eq. (4) for each MOSFET of one branch (waveforms are in Figures 9 and 10).

The results show that a spurious partial turn-on is possible with high voltage (> 400 V) and high junction temperature. Therefore, suppressing measures to reduce crosstalk should be applied to avoid excessive power losses and MOSFET thermal destruction.

Additionally, a smaller value of the gate resistor does not help to decrease the crosstalk but makes the pulse even higher. Although low R_{gex} can drain a higher amount of injected current from the gate, it also increases the rate of V_{ds} at turn-on/turn-off and the amplitude of the injected current. The situation could be improved if a second gate resistor is added to the gate circuit to separately discharge the gate and prevent the increase of dV_{ds}/dt at the turn-on. The drawbacks are higher parasitic inductances of the gate circuit (two lines share the same area of PCB) and higher dV_{ds}/dt at the turn-off. Latter results in higher ringing amplitude and may cause a problem with EMI compatibility on the inverter level[2]. Moreover, fast discharge requires a higher current capability of a gate driver that cannot be acceptable in a parallel configuration.

It is worth noting that there is no method to entirely remove the crosstalk influence due to the nonzero resistance and inductance inside the MOSFET package. For an ideal connection between the transistor and an ideal gate power supply, a voltage is still generated between the gate and source, even though the voltage is undetectable for external measurements and could be evaluated by the rate of V_{ds} only (see Figure 11). Clamping techniques cannot suppress the parasitic generation beyond this value. If the generated voltage exceeds the desired level, it is recommended to change the negative output voltage of the gate driver or apply active crosstalk protection using a voltage-shifting scheme.

2 The proposed gate driver with crosstalk suppression

The requirements for a new gate driver circuit are as follows:

- Does not change the output current of the gate driver or change the switching time.
- Effectively suppresses positive and negative crosstalk.
- Simple circuit due to limited space and a large number of parallel MOSFETs.
- Does not connect gates of MOSFETs to the same point directly, as it might cause stability problems.

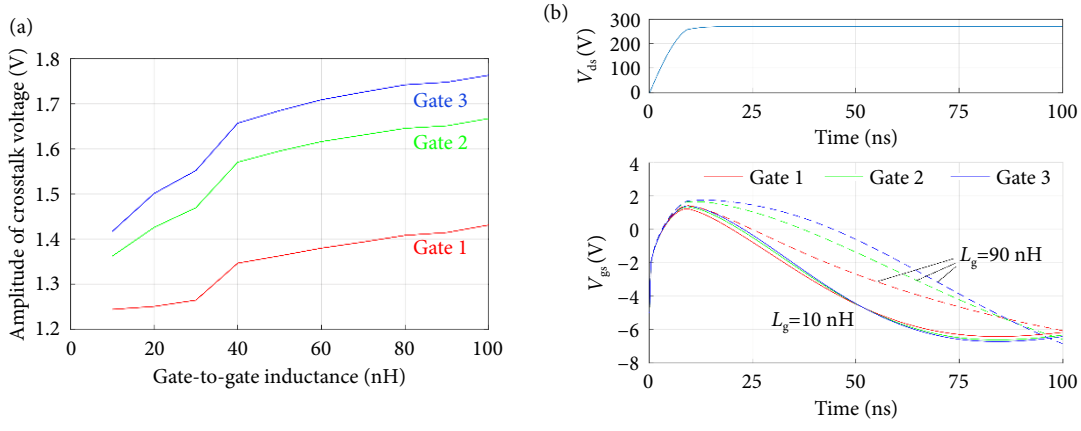

Fig. 9 Simulation of crosstalk-generated gate voltage. (a) Pulse's maximum voltage and **(b)** waveforms with different trace characteristics.

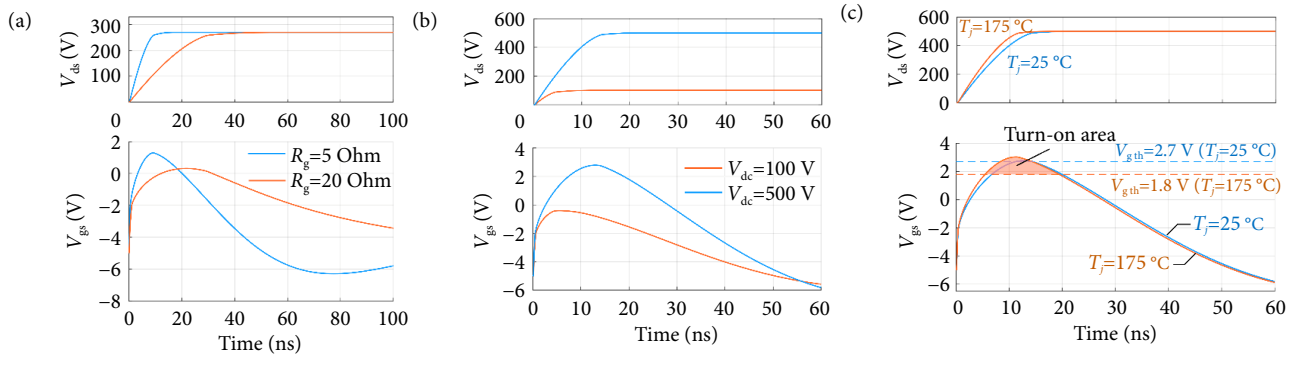

Fig. 10 Crosstalk-generated gate voltage under different operating conditions. (a) Variation in gate resistance, **(b)** variation in drain voltage (R_g = 5 Ohms) and **(c)** temperature variation (R_g = 5 Ohms).

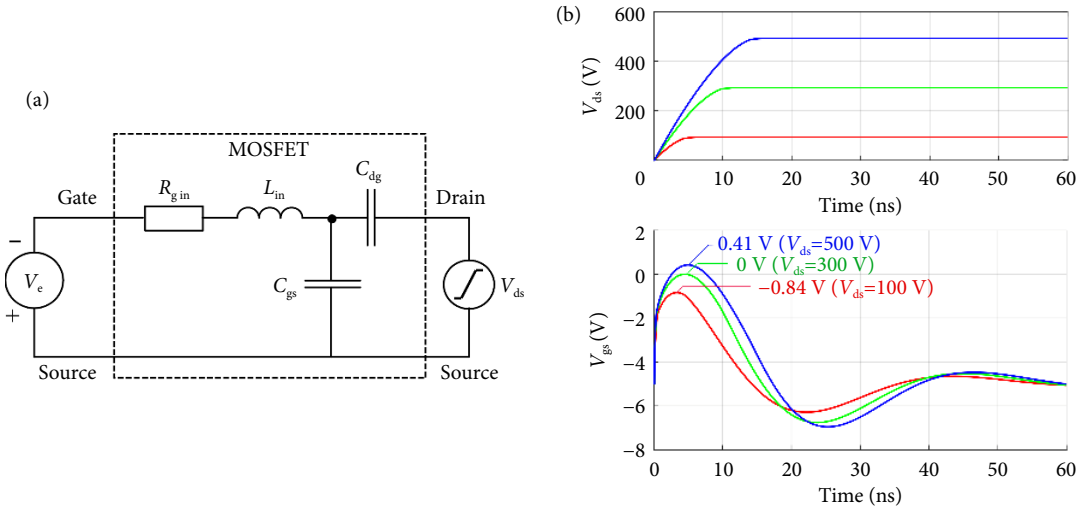

Fig. 11 Crosstalk-generated inner gate voltage with the gate shorted with V_e. (a) Electric scheme and **(b)** gate voltage waveforms.

The simplest possible solution ("V_E connected clamps") is to add a transistor next to each power MOSFET that clamps the gate to the negative voltage V_E of the gate driver (see schematic in Figure 12). The control signal of high-side switches determines the status of Q_{FN} by a second channel of isolation IC. The transistor Q_{FN} is already on during the turn-on of the high-side MOSFETs due to lower propagation delays in the control IC. Therefore, the current I_{dg} generated by the crosstalk flows through Q_{FN} to the gate driver's power supply directly. Again, due to the faster signal propagation switch, Q_{FN} normally turns off before V_{ds} starts to decrease. In this case, the current I_{dg} drained through C_{rss} is shorted by the body diode of Q_{FN} as V_{GS} of Q_F starts to decrease below V_E. If it requires an additional "fall edge," delay can adjust the turn-off time to accommodate the second transition of V_{ds} (falling edge) as well. In both cases, transistor Q_{FN} is already off at Q_N turn-on and does not affect its transient time, providing freedom to choose gate resistance independently. Waveforms of voltages and currents are shown in Figure 13.

Ideally, low active resistance of Q_{FN} should provide an effective bypass for injected current and reduce the amplitude of generated pulses at V_{gs}. However, the full impedance is significantly affected by the value of parasitic inductance between Q_{FN} and power supply's output. Considering that the gate signal trace and the additional "−5 V" trace share the same area, it is really challenging to keep total trace inductance for all MOSFETs below 15–20 nH. The effect of the trace parasitic inductance on the efficiency of "V_E connected clamps" is presented through simulation. The external gate resistor is set to 0 for low-side MOSFETs with two different values for trace parasitic inductance between gates L_g (10 and 30 nH) to simulate the bus connection of Q_{FN} to "−5 V" trace. Ideal clamping (Figure 11) and no-clamping (nonzero value of R_g) cases are added for reference. The simulation results show that high trace inductance cancels any advantages of skipping R_g and increases oscillation of V_{gs} (Figure 14).

If the PCB layout limits the size of traces, some modifications are required to reduce the length of the current path and value of trace parasitic inductance. The proposed modification is based on Ref. [21] designed for a single transistor structure, and its schematic is presented in Figure 15. A capacitor C_{FN} is added to the gate driver circuit, so current I_{dg} is shorted through C_{FN} and Q_{FN}. During the turn-off period, C_{FN} is charged to the minimum voltage of the gate driver with respect to source potential. Therefore, V_{gs} is clamped at the minimum of gate voltage. In that case, there is no need for a separate power line as it is for the scheme in Figure 12. The amplitude of crosstalk pulses depends on the capacitance of C_{FN} and the on-state resistance of Q_{FN}. The control of the additional transistor remains the same, as described earlier, with only difference in ground potential for the second channel of isolation IC due to different source connections of Q_{FN}.

The circuit should be connected as close as possible to the gate input of the power MOSFET. Although its efficiency is not affected by the parasitic inductance of traces between MOSFET and gate driver, inductances between C_{FN}, Q_{FN}, and Q_N still limit bypassing capabilities.

Figure 16 shows the equivalent circuit of the proposed driver for one of the parallel MOSFET. The transistor Q_{FN} could be

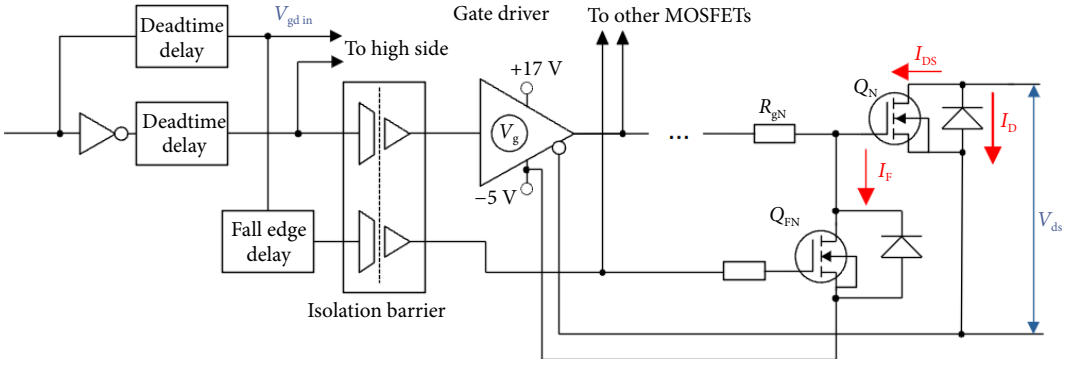

Fig. 12 Structure of a driver with external clamping.

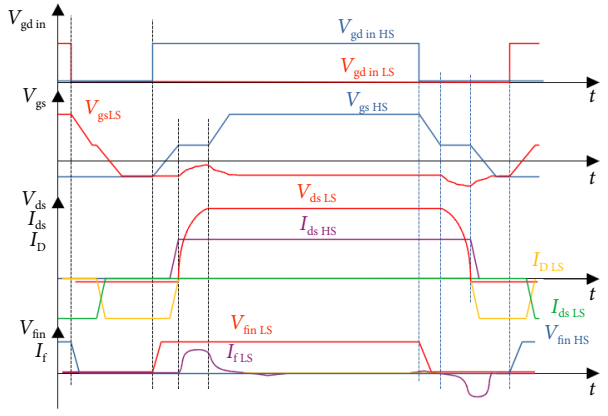

Fig. 13 Waveforms of voltages and currents during a single cycle.

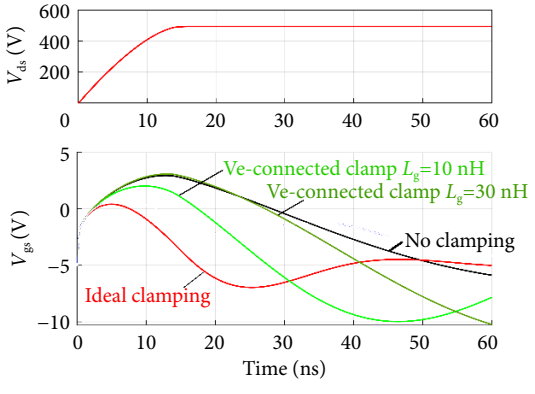

Fig. 14 Crosstalk with different suppression techniques (R_g = 5 Ohm, central clamp #1 – $L_{g1,2,3}$ = 30 nH, central clamp #2 – $L_{g1,2,3}$ = 10 nH).

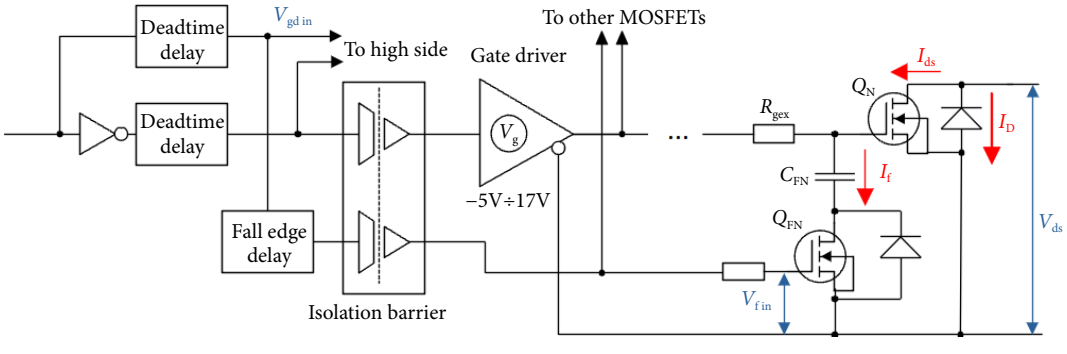

Fig. 15 Structure of proposed gate driver.

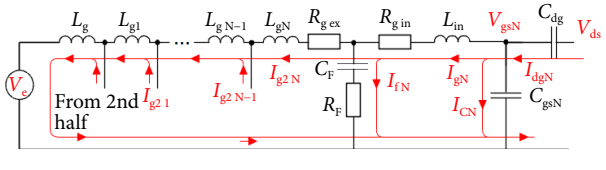

Fig. 16 Equivalent circuit of gate circuit with proposed modification.

The resistance R_f and C_f form a buffer (or short path) for I_{gs}, and their values determine the efficiency of the circuit (see Figure 20). A too small capacitor cannot absorb the current pulse without a noticeable increase in voltage, and too high on-state MOSFET's resistance merely reduces shunt capabilities. Although there are no principal disadvantages of high capacitance or low resistance, high values of capacitance require larger dimensions of the capacitor, and charge current could damage body diode during initial charging.

Figure 21 shows the simulation waveforms of V_{gs} from Figure 14 and PGD for comparison. It is clear that proposed circuit reduces amplitude and duration of generated voltage pulse.

Additional elements increase the overall power consumption of the gate circuit. The power losses include recharging of additional MOSFET's output and reverse capacitances and recharging of its gate capacitance.

$$P = F_{sw}(V_{gmax} - V_e)^2 (C_{DSat} + C_{rssat}) + F_{sw} V_{fin}{}^2 C_{gat} \qquad (14)$$

replaced with its on-state resistance R_F. Meanwhile, the ransistor Q_N has inner gate resistance R_{gin} and inductance L_{in} that are connected in serial with shunt circuit; therefore, they reduce the efficiency of suppression.

For each MOSFET's gate circuit, a system of differential equations is obtained as follows:

$$\begin{cases} V_{fk} = R_{gex} I_{g2k} - R_f I_{fk} + \sum_{i=1}^{k} \left[L_{gi} \sum_{j=i}^{N} \dfrac{dI_{g2j}}{dt} \right] + 2L_g \sum_{j=1}^{N} \dfrac{dI_{g2j}}{dt} - V_e \\ V_{gs\,k} = L_{in} \dfrac{dI_{gk}}{dt} + R_{gin} I_{gk} + V_{fk} + R_f I_{fk} \\ C_{dg}(V_{ds}) \dfrac{dV_{dg}}{dt} = I_{gk} + C_{gs} \dfrac{dV_{gs\,k}}{dt} \\ I_{gk} = I_{fk} + I_{g2k} \\ V_{gs\,k}(0) = V_{fk}(0) = -V_e; I_{gk}(0) = I_{g2k}(0) = 0; \end{cases} \qquad (13)$$

The numerical solution of the system is performed by Simulink/MATLAB using the same voltage generator for $V_{ds}(t)$ based on the integration of I_{gHS}. Figure 17 shows a comparison between proposed and conventional drivers. The proposed driver reduces the crosstalk amplitude significantly, even with high values of trace inductance. Moreover, the duration of a peak of the generated pulse is much shorter with the proposed gate driver (PGD). There are no differences in the pulse's shape for all parallel MOSFETs due to local short paths for injected current (see Figure 18).

PGD helps to maintain V_{gs} below the threshold level with a reasonable level of negative voltage shift, even though it cannot completely eliminate the crosstalk. Comparing Figures 19 and 10 one could easily notice that V_{gs} has almost 2 V margin toward the threshold with auxiliary circuit, although V_{gs} exceeds that level in the previous configuration.

3 Experiment results

To test the proposed method, four gate driver circuits are modified according to Figure 15 with the second capacitor and MOSFET AO3442 (maximum V_{ds} = 100 V, $R_{DS(on)}$ = 0.5 Ohm). One gate circuit is not modified to have a control sample. The modified circuits are shown in Figure 22. In order to reduce additional con-

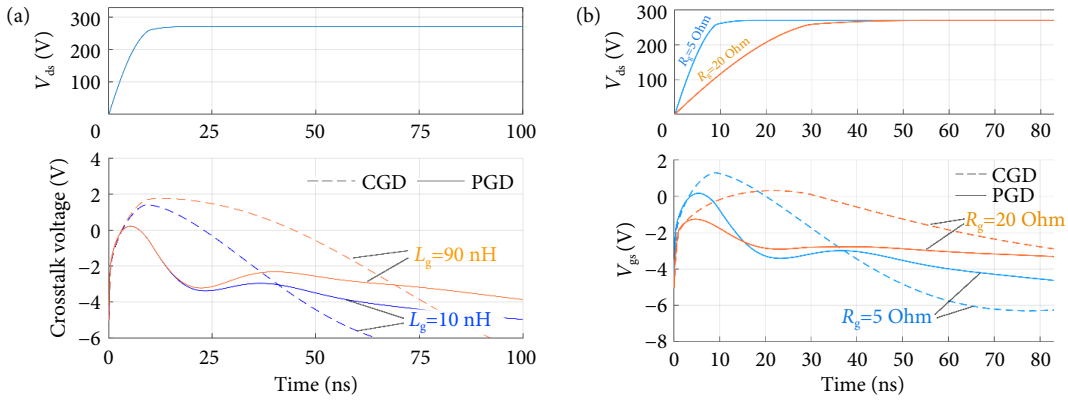

Fig. 17 Comparison of proposed gate driver (PGD) with conventional driver (CGD). (a) Different gate parasitic inductance L_g and **(b)** different gate resistance R_g.

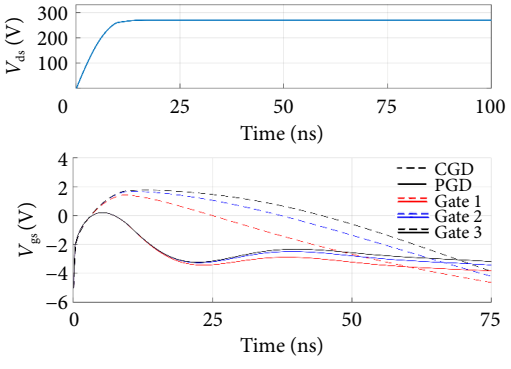

Fig. 18 Gate voltage of different gates with CGD and PGD (L_g = 90 nH).

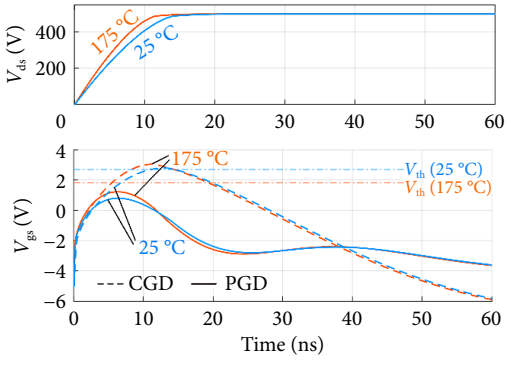

Fig. 19 Simulated crosstalk waveforms of CGD and PGD with different junction temperatures.

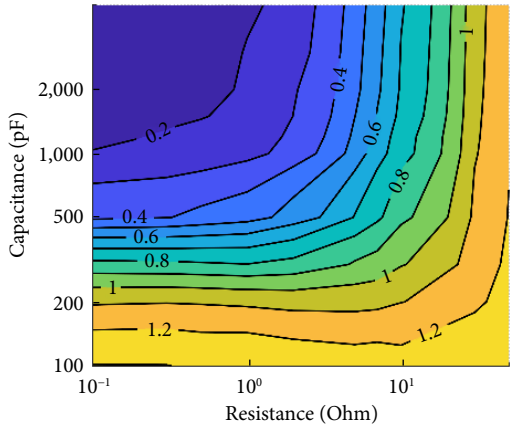

Fig. 20 Amplitude of crosstalk (in volts) with different R_f and C_f values (R_g = 5 Ohm, V_{ds} = 270 V, T_{amb} = 25 °C)

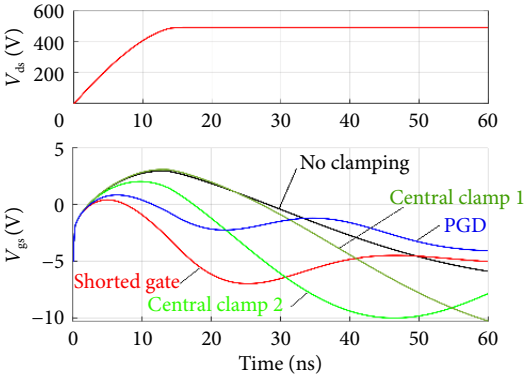

Fig. 21 Comparison of different suppression techniques and PGD.

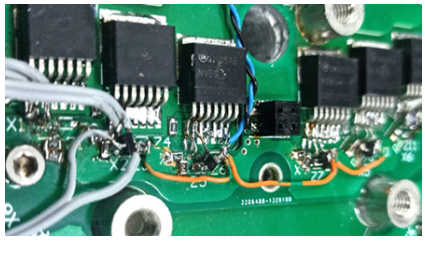

Fig. 22 Modified gate circuit (additional MOSFETs with capacitors).

sumption, the supply voltage for the modified circuit is reduced to +15 V, and it is generated from a +17 V DC–DC converter of the main GD with a zener diode. The second digital isolator is used to transfer the control signal of the auxiliary circuit.

The results are presented in Figure 23. It shows a reduction in the amplitude of gate voltage during the crosstalk. The difference in gate voltage between the modified and unmodified circuits is approximately 1 V, and it remains the same with V_{ds} in a range of 75 to 275 V. The generated gate voltage also decreases faster with modified GD; therefore, the probable length of the shoot-through event is shorter.

Experimental results demonstrate a good correlation with simulation (see Figure 24). So the model can be used to predict the behavior of gate voltage during the crosstalk event and evaluate required values for components of the suppression circuit.

Additional power consumption due to recharging of MOSFET's capacitances is calculated using Eq. (15):

$$P = 4 \times \left(50\ \text{kHz} \times (17\ \text{V} + 4.5\ \text{V})^2\,(10\ \text{pF} + 10\ \text{pF}) + 50\ \text{kHz} \times (15\ \text{V})^2 \times 100\ \text{pF}\right) = 6.3\ \text{mW} \quad (15)$$

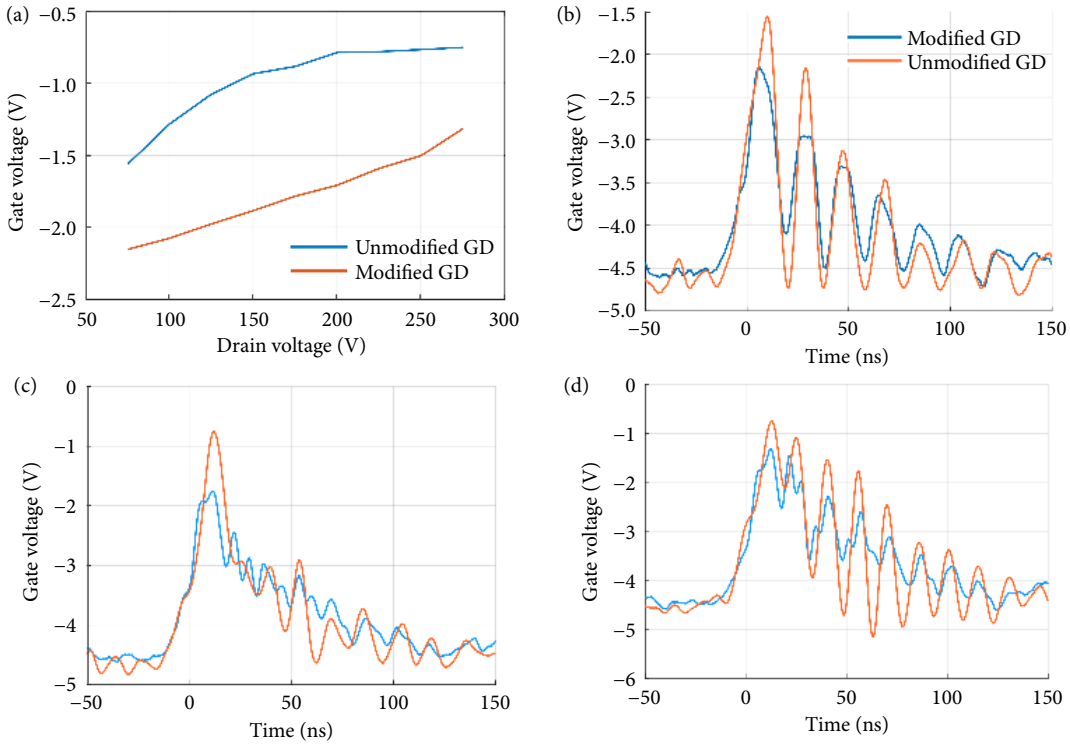

Fig. 23 Comparison of the maximums of gate voltages during crosstalk and waveforms with CGD and PGD. (a) Amplitude's comparison, **(b)** $V_{DC} = 75$ V, **(c)** $V_{DC} = 175$ V and **(d)** $V_{DC} = 275$ V.

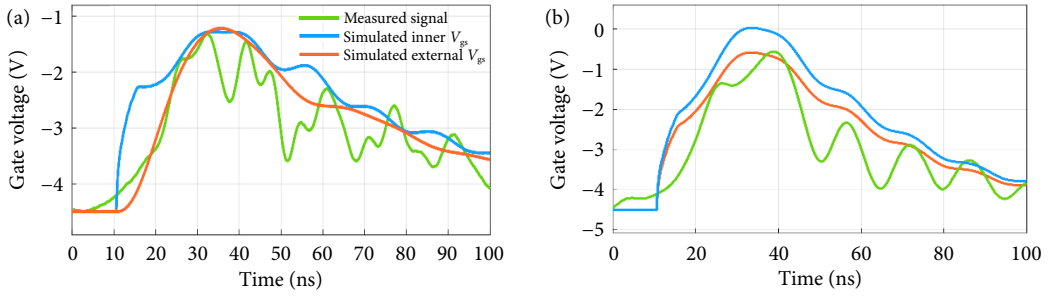

Fig. 24 Comparison of experimental results and simulated results. (a) PGD and **(b)** CGD.

4 Conclusions

This paper proposes a model for evaluating the disturbance of gate voltage during the crosstalk event for parallel connection of power MOSFETs. The proposed model uses logarithmic and linear approximations to calculate an accurate value of C_{rss} and includes a system of differential equations to calculate the gate voltage. Two methods of V_{ds} simulation are described. The limitation of the clamp technique caused by the inner nonzero impedance is explained using the proposed model. An enhanced version of the gate driver is presented, which is suitable for suppressing the crosstalk influence for parallel MOSFET connections without changing switching times. The simulation model is also presented for the modified gate driver to determine the size values of the components and predict the efficiency of the modified circuit.

Experiments are performed to demonstrate the reduction of gate disturbance. The experimental results show that this solution can suppress the effect of high dV/dt during the switching process. The proposed gate driver has a lower crosstalk influence than the previous version. Although suppression cannot eliminate the generated voltage due to natural restrictions, the schematic may be useful in special cases to reduce the negative consequences of parasitic interactions.

Appendix

CGD – conventional gate driver
EMI – electromagnetic interference
GD – gate driver
PCB – printed circuit board
PGD – proposed gate driver
C_{dg} – gate-drain capacitance of a MOSFET (equal to C_{rss})
C_{DSat} – output capacitance of clamping switch
C_{gs} – gate-source capacitance of MOSFET
C_{gat} – gate capacitance of clamping switch
C_{oss} – output capacitance of a MOSFET
C_{rss} – reverse transfer capacitance of a MOSFET (equal to C_{dg})
C_{rssat} – reverse transfer capacitance of clamping switch
F_{sw} – switching frequency of the inverter
I_c –current through MOSFET's gate capacitance
I_{dg} –current between the gate and the drain of MOSFET going through the C_{rss}
I_{ds} – drain-source current of MOSFET

I_d – body diode current of MOSFET
I_f – current of clamping switch
I_g – current through gate pin of a MOSFET
I_{g2} – current through external gate resistor (with clamping circuit)
i_{gHS} – gate current of high-side MOSFET during the transition of V_{ds}
I_{max} – maximum drain current of the MOSFET
g – forward transconductance
$g_{app25°C}$ – approximated forward transconductance at 25 °C
L_g –inductance of the trace between the gate driver and connection of gate circuit's branches
L_{gx} – inductance of the trace between 2 adjacent gates resistors (X – gate number)
L_{in} –combined inductance of MOSFET's gate conductors and the trace between the gate and external gate resistor
R_g – total gate resistance ($R_g = R_{dex} + R_{gin}$)
R_{gex} – external gate resistance
R_{gin} – inner gate resistance
t_{start} – moment of the beginning of the drain-source voltage change
t_1 – moment when is fully charged by gate current
Q_{dgsat} – drain-gate charge of a MOSFET
V_{DC} – inverter's input DC voltage
V_{dg} – drain-gate voltage of a MOSFET
V_{dgHS}, V_{dgLS} – drain-gate voltage of high-side and low-side MOSFETs, respectively
V_{ds} – drain-source voltage of a MOSFET
V_{dsmin} – drain-source voltage of a MOSFET at the beginning of saturation region
V_{dsmax} – maximum steady-state drain-source voltage of a MOSFET
V_{dsHS}, V_{dsLS} – drain-source voltage of high-side and low-side MOSFETs, respectively
$V_{dsHSinit}$ – drain-source voltage of high-side at t_{start}
V_{fin} –gate voltage of clamping switch
V_{gdin} – gate driver input voltage
V_{gs} – gate-source voltage of a MOSFET
V_{gsHS}, V_{gsLS} – gate-source voltage of high-side and low-side MOSFETs, respectively
V_{gsX} – gate-source voltage of X MOSFET
V_g – gate driver output voltage
V_{gmax} – maximum gate driver output voltage
V_e – amplitude of negatively biased gate power supply
V_{miller} – Miller plateau's gate voltage
$V_{miller25°C}$ – Miller plateau's gate voltage at 25°C
V_{th} – MOSFET's threshold voltage
$V_{th25°C}$ – MOSFET's threshold voltage at 25°C

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Additional information

Declaration of competing interest

The authors have no competing interests to declare that are relevant to the content of this article.

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