Anomalous GIDL Effect With Back Bias in FinFET: Physical Insights and Compact Modeling

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***Abstract*— In this work, we report a detailed study and modeling of bulk current in the low forward bias region. In the forward bias region, the bulk current shows a gate-induced drain leakage (GIDL) such as strong modulation with gate voltage although from the band alignment one would not expect any tunneling current. We propose physics-based modeling of this effect and derive a compact model for circuit simulators as state-of-the-art compact models are not suitable to capture this effect. The proposed model has been validated with measurement from Intel's bulk FinFET device.**

***Index Terms*— Band-to-band tunneling (BTBT), compact model, FinFET, gate-induced drain leakage (GIDL), leakage current, MOSFET, trap-assisted tunneling (TAT), tunneling.**

I. Introduction

LOW-POWER CMOS technology demands low leakage current, and it is the major concern for the advanced sub-20-nm FinFET technology nodes [1]–[4]. In addition to subthreshold leakage, gate leakage, and junction leakage, gate-induced drain leakage (GIDL) is also detrimental to sub-20-nm technology node, due to the presence of high electric field in gate–drain overlap region [5], [6]. Although GIDL has been extensively studied in the literature for long-channel Bulk MOSFET and advanced FinFET devices [7]–[19], the physical understanding of bulk voltage dependence of GIDL has not received much attention in the literature and none of the works have addressed the gate bias dependence of bulk current in the forward bias region.

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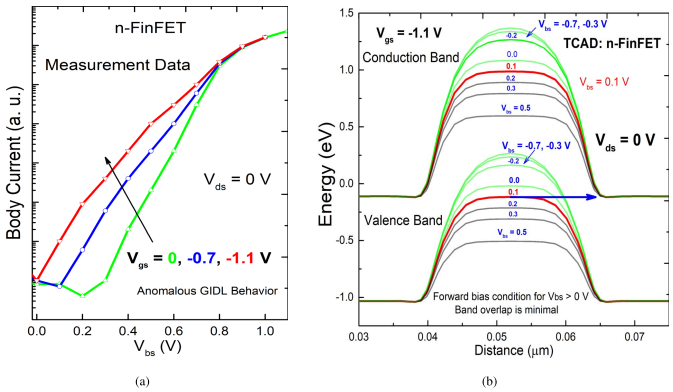

Fig. 1. (a) Measured data of anomalous body current versus back bias in low-field gate–drain overlap region. Measurement data reported in this work are of Intel's state-of-the-art bulk-FinFET devices. (b) Band diagram shows minimal overlapping tunneling states between VB and CB for $V_{bs} = 0.1$ V and more, i.e., forward bias condition.

Fig. 1(a) shows the GIDL current behavior in a bulk FinFET for forward bias region. The current shows a strong conventional GIDL such as V_{gs} dependence. However, the band diagram from TCAD simulation in Fig. 1(b) shows that the band overlap in forward bias is minimal to explain the trend using a conventional GIDL-type band-to-band tunneling (BTBT) model. It is interesting to note that industry-standard models, such as BSIM4 [20], Berkeley short-channel IGFET model-common multi-gate (BSIM-CMG) [21], and Penn State Philips (PSP) [22], consider only the BTBT mechanism to model the GIDL effect from [7], and therefore those models cannot physically explain this anomalous V_{gs} dependence for forward bias bulk current. In this work, we investigate the physical phenomenon responsible for the observed anomalous forward bias body current and present a compact model for the same.

This article is organized as follows. Physical investigation of the anomalous GIDL for low forward bias using calibrated TCAD simulation is presented in Section II. A compact model of back bias-dependent GIDL is proposed in Section III. Anomalous GIDL dependence on temperature is explained in Section IV. Discussion and validation of the proposed unified compact model are presented in Section V. The conclusion is given in Section VI.

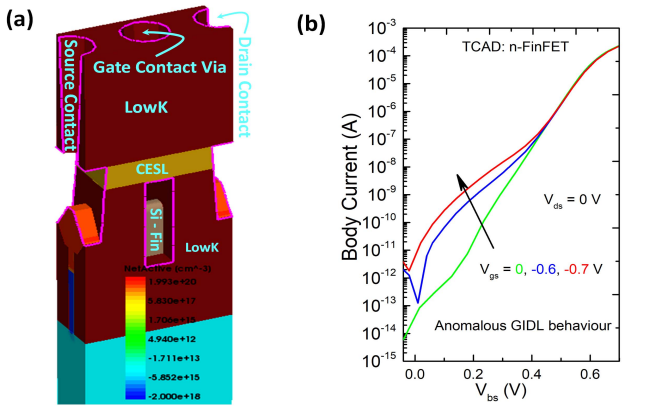

Fig. 2. (a) FinFET structure used for simulations with the dimensions as reported in [23] and [24]. (b) Calibrated TCAD simulated GIDL current, indicating anomalous GIDL trends.

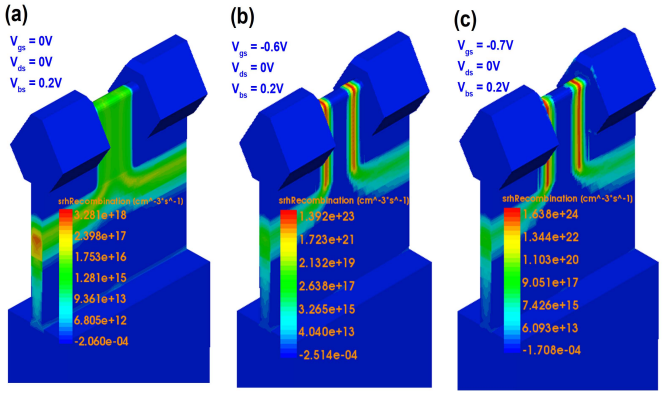

Fig. 3. SRH recombination rate in gate–drain overlap region: calibrated FinFET structure at $V_{bs} = 0.2$ V and (a)–(c) $V_{gs} = 0$, -0.6, and -0.7 V. Increase in gate bias at fixed back-gate bias results in increased SRH recombination rate.

II. TCAD Simulations and Anomalous GIDL Effect at Low Gate–Drain Overlap Field

A. TCAD Device Calibration

In this work, we use the TCAD simulations to reproduce the measurement trends and investigate the physical reason behind the anomalous body current behavior with back bias. The device architectures shown in Fig. 2(a) are generated by performing 3-D process and device TCAD simulations. The calibrated structure used in this work is the same as in [23]. The calibrated structure uses the field-dependent Shockley–Read–Hall (SRH) recombination and tunneling model to capture the effect of gate–drain overlap field on GIDL.

B. Physical Phenomenon Responsible for Anomalous GIDL Effect

In our previous work [11], we identified that two physical phenomena, BTBT and trap-assisted tunneling (TAT), were responsible for gate voltage dependence in reverse bias. To understand the origin of the anomalous behavior, we use TCAD to see how they change in the forward bias.

Fig. 2(b) shows that TCAD produces the similar trend observed in measurement data. As we have seen tunneling in this region is negligible, we investigate trapping contribution

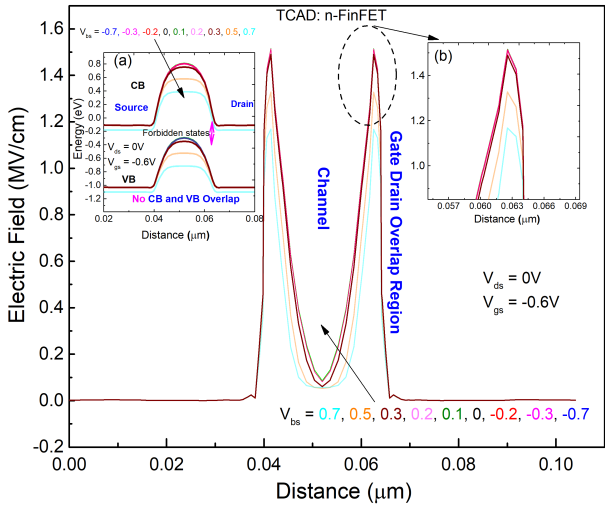

Fig. 4. Band diagram with cutline in the *yz* plane in low-field gate–drain overlap region. Inset (a): no overlapping states between VB and CB, which implies the absence of direct tunneling component. Inset (b): field variation with change in back-gate bias is negligible except for very large positive back bias value, which makes p-n junction forward biased.

in low forward bias. Fig. 3(a)–(c) shows the increase in SRH recombination rate with increase in V_{gs}. This increased SRH recombination rate due to increased field leads to current modulation in low forward bias case [25]. Fig. 4 shows the gate–drain overlap region field versus distance plot in the lateral direction along the channel length, at $V_{gs} = -0.6$ V and $V_{ds} = 0$ V, and for different back bias values. Inset (a) in Fig. 4 indicates that no overlapping states are available for tunneling between the valence band (VB) and conduction band (CB) for the given back bias values. Unavailability of overlapping states forces electrons to go first to midgap trap state from VB and then tunnel to CB, which is the well-known TAT phenomenon in the low gate–drain overlap field case. In addition, inset (b) in Fig. 4 shows that the peak field variation in the gate–drain overlap region is negligibly small for the given back bias value. At very high back bias ($V_{bs} > 0.5$ V), the current is dominated by diode current, as shown in Fig. 2(b).

III. Compact Model for TAT-GIDL and BTBT-GIDL Including Back Bias Effect

A. TAT-GIDL at Low Gate–Drain Overlap Field

The compact model of TAT-GIDL for reverse bias junction condition, at low-field effect, is presented in [11] and is the special case of the generalized model, which will be presented in this article. Trap generation/recombination current is given by Dabhi *et al.* [11]

$$I_{\text{TAT-GIDL}} = \int_0^{x_n} \Gamma(x) \cdot G_{\text{SRH}}(x) \cdot dx. \tag{1}$$

The function $\Gamma(x) \cdot G_{\text{SRH}}(x)$ has a maxima at the Si–SiO_2 interface in the overlap region, and depending on the bias condition, its width is determined by either $\Gamma(x)$ or $G_{\text{SRH}}(x)$, where x is the vertical direction in the gate–drain overlap region, starting from Si–SiO_2 interface. Hence, we approximate I_{TAT} as

$$I_{\text{TAT-GIDL}} = \Gamma_{\max} \cdot G_{\text{SRH,max}} \cdot W_{\text{TAT}} \tag{2}$$

where W_{TAT} is given by Dabhi *et al.* [11]

$$W_{\mathrm{TAT}} = \frac{W_\Gamma \cdot W_{\mathrm{SRH}}}{W_\Gamma + W_{\mathrm{SRH}}} \tag{3}$$

and W_Γ is given as

$$W_\Gamma = W_{\mathrm{dep}} \cdot \left(D_{\mathrm{TAT}} \cdot h_{\mathrm{max}}^{\frac{3}{2}} \cdot +1\right)^{-1}. \tag{4}$$

Here

$$\begin{aligned} D_{\mathrm{TAT}} &= \frac{F_{\mathrm{nor}}}{F_{\mathrm{max}}} \\ F_{\mathrm{nor}} &= \frac{4}{3} \cdot \frac{\sqrt{2 \cdot m^* \cdot \Delta E^3}}{q \cdot \hbar} \\ \Delta E &= \frac{E_g}{2} \end{aligned} \tag{5}$$

where F_{max} is the maximum field approximation. The transition from low- to high-field regime for TAT is taken care by h_{max} [11]. The integration of $\Gamma(x)$ has already been performed using the above method and maximum field approximation in [11]. From Fig. 4, it is evident that the effect of back bias on gate–drain overlap field is negligible, except for the very high back bias, where the drain-side diode becomes forward biased, and hence, the dependence of F_{max} on back bias is neglected. F_{max} and Γ_{max} are the same as in [11] and also reproduced as follows:

$$F_{\mathrm{max}} = \frac{\epsilon_{\mathrm{ox}}}{\epsilon_{\mathrm{si}}} \cdot \frac{\alpha \cdot {V_{\mathrm{dg}}}^2 - \beta \cdot V_{\mathrm{dg}} - \gamma}{T_{\mathrm{ox}}} \tag{6}$$

where α, β, and γ are the temperature-independent parameters

$$\Gamma_{\mathrm{max}} = \frac{E_{\mathrm{TAT}} \cdot \exp(R_{\mathrm{TAT}}) \cdot \mathrm{erfc}[P_{\mathrm{TAT}} \cdot (Q_{\mathrm{TAT}} - 1)] \cdot \sqrt{\pi}}{2 \cdot P_{\mathrm{TAT}}} \tag{7}$$

where

$$\begin{aligned} E_{\mathrm{TAT}} &= \frac{\Delta E}{K_B T} \\ P_{\mathrm{TAT}} &= \sqrt{\frac{3}{8} \cdot D_{\mathrm{TAT}} \cdot h_{\mathrm{max}}^{-\frac{1}{2}}} \\ Q_{\mathrm{TAT}} &= \frac{4}{3} \cdot \frac{E_{\mathrm{TAT}}}{D_{\mathrm{TAT}}} \cdot h_{\mathrm{max}}^{\frac{1}{2}} - h_{\mathrm{max}} \\ R_{\mathrm{TAT}} &= \frac{2}{3} \cdot \frac{E_{\mathrm{TAT}}^2}{D_{\mathrm{TAT}}} \cdot h_{\mathrm{max}}^{\frac{1}{2}} - E_{\mathrm{TAT}} \cdot h_{\mathrm{max}} \\ &\quad + \frac{D_{\mathrm{TAT}}}{2} \cdot h_{\mathrm{max}}^{\frac{3}{2}}. \end{aligned}$$

As back bias becomes positive, the SRH generation/recombination rate is influenced by drain-side junction diode, and the generalized expression for G_{SRH} is given by Sze [26]

$$G_{\mathrm{SRH}} = \sigma \cdot V_{\mathrm{th}} \cdot N_t \cdot n_i(T) \left[\exp\left(\frac{V_{\mathrm{bd}}}{V_t}\right) - 1\right] r(x) \tag{8}$$

where $r(x)$ is given as

$$r(x) = [n + p + 2]^{-1} \tag{9}$$

where n and p are the electron and the hole concentration in the depletion region inside the gate–drain overlap region, respectively. We assume midgap trap, equal lifetimes of electrons and holes, Boltzmann statistics, and constant quasi-Fermi levels of electrons and holes throughout the depletion region. G_{SRH} attains its maximum value when $r(x)$ becomes maximum. The function $r(x)$ peaks up only when the equal concentration of electron and hole is attained, that is

$$n = p = \exp\left(\frac{V_{\mathrm{bd}}}{2 \cdot V_t}\right) \tag{10}$$

and the maximum value of $r(x)$ is given by

$$\max[r(x)] = \frac{1}{2} \cdot \left[\exp\left(\frac{V_{\mathrm{bd}}}{2 \cdot V_t}\right) + 1\right]^{-1}. \tag{11}$$

Substituting (11) into (8), G_{SRH} is given by

$$G_{\mathrm{SRH,max}} = A_{\mathrm{TAT}} \cdot n_i(T) \left[\exp\left(\frac{V_{\mathrm{bd}}}{2 \cdot V_t}\right) - 1\right] \tag{12}$$

where A_{TAT} is $(1/2) \cdot \sigma \cdot V_{\mathrm{th}} \cdot N_t$. Using (3), (7), and (12), the final expression of TAT-GIDL is given as

$$I_{\mathrm{TAT-GIDL}} = A_{\mathrm{TAT}} \cdot n_i(T) \cdot W_{\mathrm{TAT}} \cdot \Gamma_{\mathrm{max}} \times \left[\exp\left(\frac{V_{\mathrm{bd}}}{2 \cdot V_t}\right) - 1\right]. \tag{13}$$

Equation (13) captures the anomalous GIDL (discussed in detail later in Section V), in low forward back-gate bias case, caused by an increasing negative gate bias value and takes care of zero current at zero bias condition. For a specified reverse bias condition, (13) reduces to TAT-GIDL expression in [11].

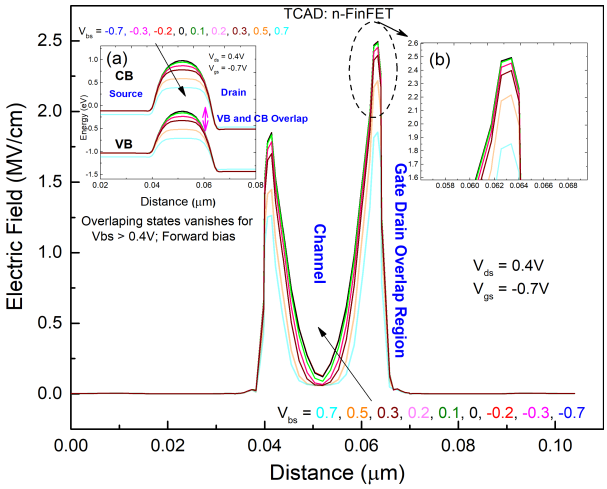

Fig. 5. Band diagram with cutline in the *yz* plane in high-field gate–drain overlap region. Inset (a): large overlapping band states available between VB and CB, charge carriers tunnel to CB from VB through overlapping band states. Inset (b): field variation with change in back-gate bias is negligible except for the very large positive back bias, which makes p-n junction forward biased.

B. BTBT-GIDL at High Gate–Drain Overlap Field

At high gate–drain overlap field, band-to-band tunneling current contributes to the GIDL [11]. Previous works on BTBT-GIDL [7], [11], [20]–[22] use an empirical approach to force the GIDL current to zero, at zero V_{bd}. Body bias dependence of the GIDL current can be physically modeled by the D function [27]–[29]. However, it is worth noting that the expression presented in [29] cannot be extended directly to forward bias as it does not account for band alignment effect shown in Fig. 5 [inset (a)].

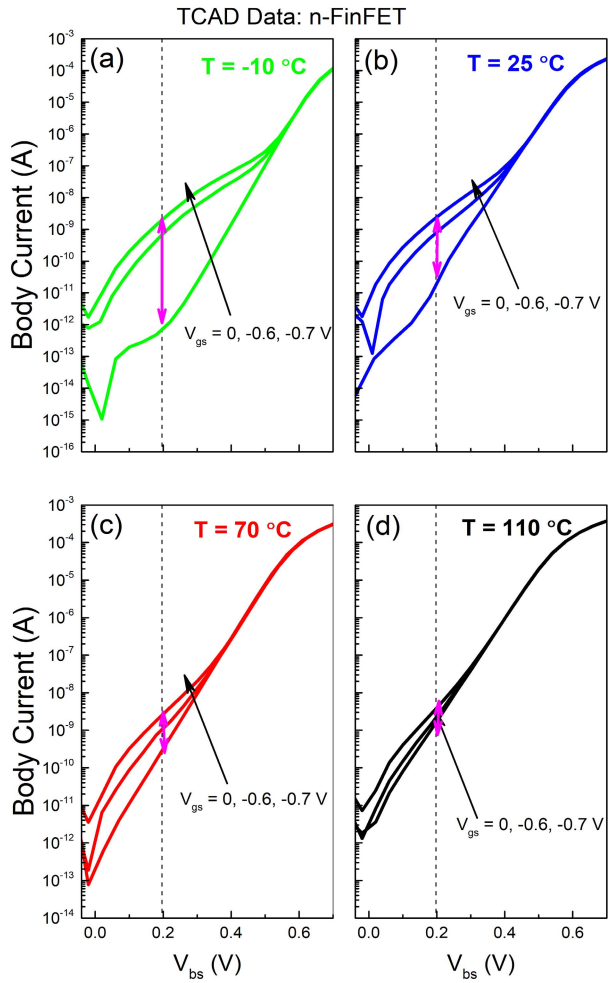

Fig. 6. Anomalous body current dependence on temperature, simulated using bulk n-FinFET. As the temperature increases, the absolute increase in current (at fixed back bias with increasing V_{gs} from 0 to −0.7 V) modulation decreases. (a)–(d) FinFET simulation plots at different temperatures. These plots confirm the reduction in bias-dependent current modulation with increasing temperature. Plots are at $V_{ds} = 0$ V.

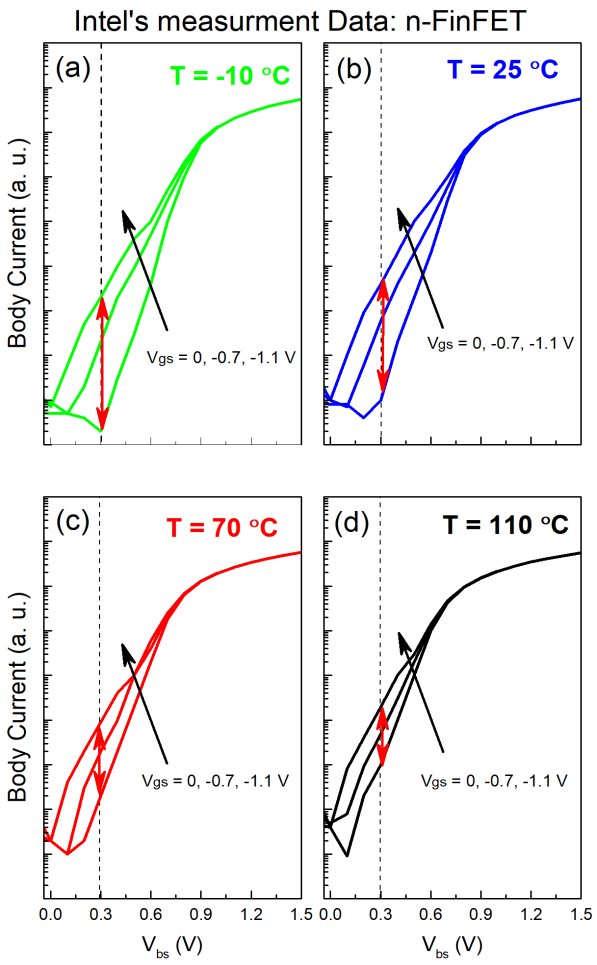

Fig. 7. Measured data of Intel's state-of-the-art bulk-nFinFET for anomalous body current dependence on temperature. As the temperature increases, the absolute increase in current (at fixed back bias with increasing V_{gs} from 0 to −1.1 V) modulation decreases. (a)–(d) FinFET measurement plots at different temperatures. These measurement data confirm the reduction in bias-dependent current modulation with increasing temperature shown in this figure. Plots are at $V_{ds} = 0$ V.

It can be seen in TCAD results of Fig. 5 that the change in gate–drain overlap field with back bias value is negligible, except for the back bias values, for which drain-side diode becomes forward biased (for $V_{bs} > 0.4$ V, since $V_{ds} = 0.4$ V, in Fig. 5). Inset (a) of Fig. 5 shows that for high gate–drain overlap field, the significant band states overlap between VB and CB and, hence, contribute to the band-to-band tunneling. For back bias more than 0.4 V [Fig. 5, inset (a)], the drain-side p-n diode becomes forward biased and results in nonoverlapping of band states between VB and CB. The vanishing overlap between VB and CB for forward bias results in zero BTBT tunneling contribution to the GIDL current. The BTBT-GIDL current is given as [11]

$$I_{\mathrm{BTBT-GIDL}} = W \cdot D \cdot \frac{A}{B} \cdot F_{\max}^2 \cdot \exp\left(-\frac{B}{F_{\max}}\right). \quad (14)$$

The D function in (12) can be deduced as follows [27], [29]:

$$D = \left[\exp\left(\frac{V_{\mathrm{bd}}}{V_t}\right) - 1\right] \cdot D_{\mathrm{fun}}(x) \quad (15)$$

where D_{fun} is given by

$$D_{\mathrm{fun}}(x) = [\mathrm{n} + \mathrm{p} + \mathrm{np} + 1]^{-1} \quad (16)$$

where n and p are the electron and the hole concentrations in the depletion region inside the gate–drain overlap region, respectively. Here, we also assume the midgap trap, equal lifetimes of electrons and holes, Boltzmann statistics, and constant quasi-Fermi levels of electrons and holes throughout the depletion region. D_{fun} is evaluated as its maximum value times its effective width. In (16), the function, $(n + p + (np + 1))$, has a constant factor of $(np + 1)$ and, hence, D_{fun} becomes maximum when the condition $n = p$ is attained, which results in peak BTBT generation rate, and the maximum value of D_{fun} is given by

$$\max[D_{\mathrm{fun}}(x)] = \left[2 \cdot \exp\left(\frac{V_{\mathrm{bd}}}{2V_t}\right) + \exp\left(\frac{V_{\mathrm{bd}}}{V_t}\right) + 1\right]^{-1}. \quad (17)$$

Taking W_{Dfun} as the effective width of the D_{fun} function, the compact equation of BTBT-GIDL, including the back bias

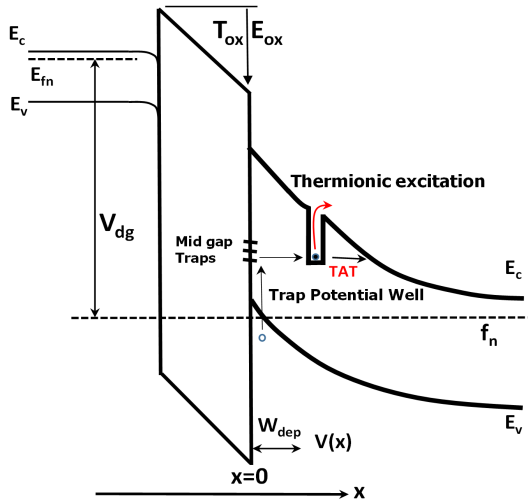

Fig. 8. Simplified energy-band diagram in low-field gate–drain overlap region. The nonavailability of overlapping states between VB and CB pushes the electron to go to the CB via the midgap trap. However, at the higher temperature, the electron that is trapped to the trap potential is likely to escape to the CB rather than tunneling to the CB from trap potential well and, hence, TAT is masked by thermionic excitation, and the bias dependence on anomalous body current is diminished in forward biased.

effect, is given by

$$I_{\mathrm{BTBT-GIDL}} = W \cdot \frac{A}{B} \cdot F_{\max}^2 \cdot \exp\left(-\frac{B}{F_{\max}}\right) \cdot W_{\mathrm{Dfun}} \times \cdot \frac{\left[\exp\left(\frac{V_{\mathrm{bd}}}{V_t}\right) - 1\right]}{\left[2 \cdot \exp\left(\frac{V_{\mathrm{bd}}}{2V_t}\right) + exp\left(\frac{V_{\mathrm{bd}}}{V_t}\right) + 1\right]}. \quad (18)$$

The vanishing tunneling probability for BTBT-GIDL, for forward bias drain-side p-n junction case, is assured by using the following smoothing function:

$$I_{\mathrm{BTBT-GIDL_{smooth}}} = \frac{1}{2}[(a+b) - \sqrt{(a-b)^2 + \Delta^2}] - \frac{1}{2}[b - \sqrt{(b^2 + \Delta)}] \quad (19)$$

where $a = I_{\mathrm{BTBT-GIDL}}$, b is the small positive value to which function is clamped, and Δ is the smoothing parameter. The proposed physics-based BTBT-GIDL model takes care of BTBT contribution to GIDL in reverse bias junction condition and gives smooth transition to vanishing tunneling regime for forward bias junction. Zero BTBT-GIDL current is inherently captured by physical formulation of state occupancy factor D.

IV. Temperature Dependence of Anomalous GIDL Effect

Gate bias dependence on anomalous forward bias body current for different temperatures is shown in Figs. 6 and 7, for TCAD simulation and the measurement data, respectively. Interestingly, TCAD and measurement data show that the bias dependence of body current decreases with an increase in temperature. The physical reason for this reduced bias dependence is evident from Fig. 8. It indicates that for low-temperature operation, the electron trapped in the potential well of the trap is likely to tunnel to the CB, and as the gate bias increases,

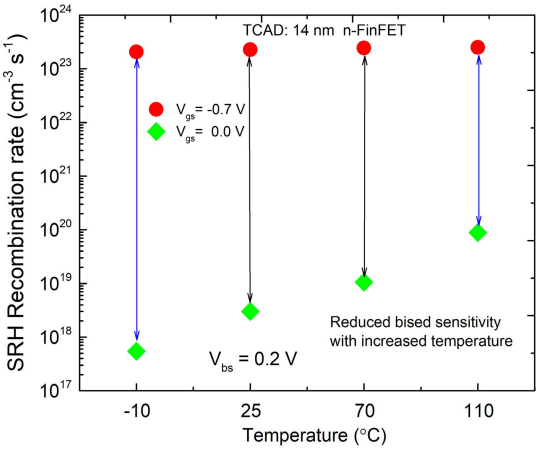

Fig. 9. Peak SRH recombination rate in gate–drain overlap region corresponding to the body current simulation shown in Fig. 7(a)–(d) at different temperatures and constant back bias of 0.2 V. An absolute reduction in SRH recombination rate (with increasing gate bias from 0 and −0.7 V) with the increase in temperature explains the reduction in gate bias dependence on current modulation with increased temperature.

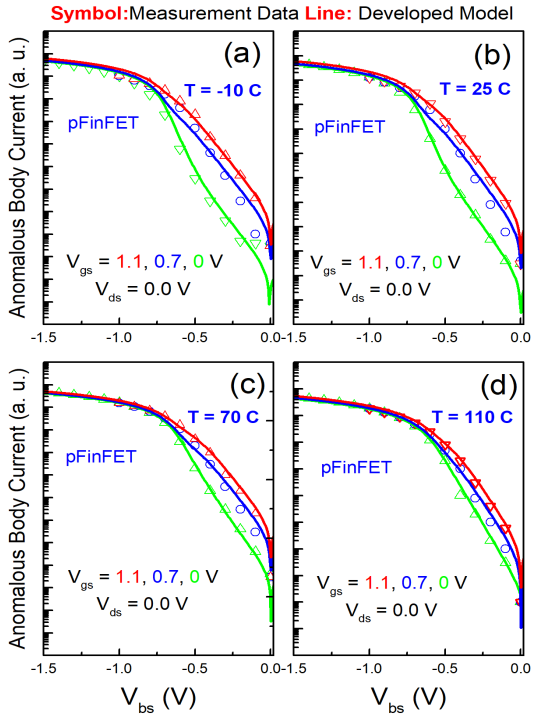

Fig. 10. Validation of developed TAT-GIDL model with the measured data of Intel's state-of-the-art bulk-pFinFET at (a) −10 °C, (b) 25 °C, (c) 70 °C, and (d) 110 °C.

the resultant increased field gives rise to an elevated SRH recombination rate and, hence, increased anomalous body current. However, at high temperatures, the trapped electron is more likely to escape from the trap to the CB due to thermionic excitation rather than tunneling into the CB. For this reason, the temperature dependence of TAT is too weak [19], [27]. For elevated temperature operation, the presence of thermionic excitation masks the TAT phenomena, and as a result, the bias sensitivity to the TAT reduces [19].

Fig. 9 confirms this hypothesis using TCAD by showing that as the temperature increases, the absolute increase in

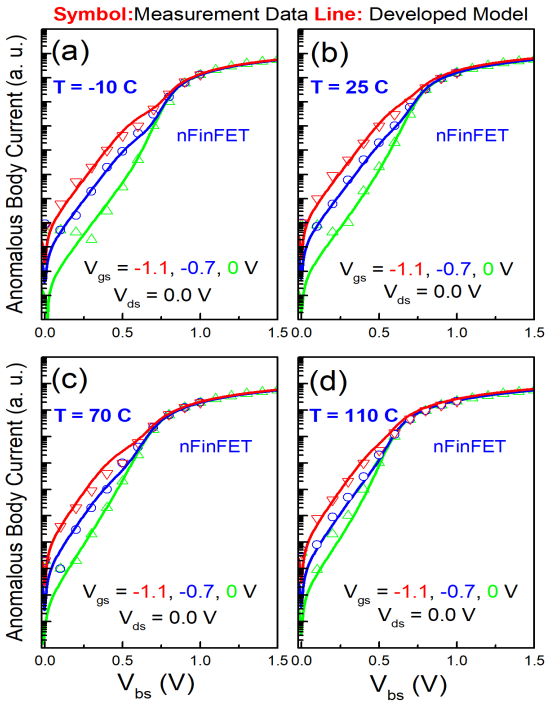

Fig. 11. Validation of developed TAT-GIDL model with the measured data of Intel's state-of-the-art bulk-nFinFET at (a) −10 °C, (b) 25 °C, (c) 70 °C, and (d) 110 °C.

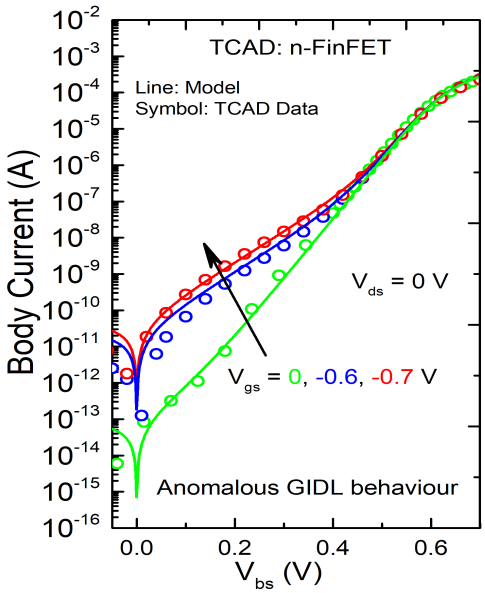

Fig. 12. Validation of the developed TAT-GIDL model with the calibrated TCAD simulations of GIDL current, indicating anomalous GIDL trends in bulk-nFinFET at 25 °C. Line: model. Symbol: TCAD data. The model parameters are extracted at 25 °C, but for the other temperatures, the developed model captures the temperature dependence without any additional parameter. Extracted values of parameters: $A_{TAT} = (1/2)\sigma V_t N_t = 1.5 \times 10^6$ S^{-1}, $\tau = (2/(\sigma V_t N_t))$ = carrier lifetime = 0.6×10^{-6} S. Maximum field approximation related parameters: $\alpha = 0.5$ V^{-1}, $\beta = -0.97$, and $\gamma = -1.019$ V.

SRH recombination rate (with increasing gate bias from 0 and −0.7 V) decreases. As a result, the gate bias sensitivity is decreasing with an increase in temperature.

V. Compact Model Validation and Discussion

The developed model is validated with the measurement data of bulk-FinFET devices fabricated by Intel. Figs. 10 and 11 show the model predictions for p-type and n-type FinFETs, respectively. The measured data in these figures show that the sensitivity of current modulation with increasing V_{gs} for both nFinFET and pFinFET is reducing with increasing temperature, and the proposed model captures this physical behavior accurately. Fig. 12 shows the model validation with the TCAD simulation, where it can be seen that the developed model captures the TCAD simulations accurately. Instead of using an empirical approach like used in state-of-the-art compact models, the physics-based model developed in this work provides a smooth transition from tunneling regime in reverse and zero bias junction to vanishing tunneling regime in the forward bias junction condition and ensures zero current at zero V_{bd} value.

VI. Conclusion

In the low forward bias region, one would expect reduced tunneling current from band alignment, but measurement shows a strong gate bias dependence in low forward bias region. Industry-standard models either have problematic behavior in this region or do not recognize the band alignment aspect in low forward bias region. We showed that TAT successfully explains this anomalous behavior through the gate voltage dependence of peak electric field. Using this insight, we propose a compact model that accurately captures the behavior observed in measurements and improves the state of the art of forward bias bulk current modeling.

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