A 16-bit Carry-Lookahead Adder Using Reversible Energy Recovery Logic for Ultra-Low-Energy Systems

Joonho Lim, Dong-Gyu Kim, and Soo-Ik Chae

***Abstract*—In this paper, we describe an energy-efficient carry-lookahead adder using reversible energy recovery logic (RERL), which is a new dual-rail reversible adiabatic logic. We also describe an eight-phase, clocked power generator that requires an off-chip inductor. For the energy-efficient design of reversible logic, we explain how to control the overhead of reversibility with a self-energy-recovery circuit. A test chip was implemented with a 0.8-μm CMOS technology, which included two 16-bit carry-lookahead adders to allow fair comparison: an RERL one and a static CMOS one. Experimental results showed that the RERL adder had substantial advantages in energy consumption over the static CMOS one at low operating frequencies. We also confirmed that we could minimize the energy consumption in the RERL circuit by reducing the operating frequency until adiabatic and leakage losses were equal.**

***Index Terms*–Adiabatic circuit, carry-lookahead adder, clocked power generator, reversible energy recovery logic, self-energy-recovery circuit.**

I. Introduction

MANY adiabatic logic circuits using a clocked power supply have been proposed [1]–[7]. There are three kinds of energy consumption in adiabatic circuits: adiabatic, nonadiabatic, and leakage losses. When a switch in an adiabatic circuit is on, the adiabatic loss of the switch per each transition of the clocked power is inversely proportional to its transition time T if the time constant of the circuit, which is the product of the turn-on resistance of the switch and its load capacitance, is much smaller than T [5], [6]. Note that this adiabatic loss is reduced to zero if the transition time goes to infinity, which is attractive for the applications that require not high performance but low energy consumption. Leakage loss per cycle in a MOS transistor is proportional to the clock period, which is negligible in the static CMOS circuit. In the adiabatic circuit without nonadiabatic loss, however, leakage loss becomes comparable to adiabatic loss when the operating frequency is low, and we can obtain the minimal energy consumption if the operating frequency is reduced until adiabatic and leakage losses are equal.

In contrast, nonadiabatic loss is not dependent on the operating frequency of the circuit but proportional to the square of the voltage difference between the terminals of a switch when the switch is turned on. Any nonadiabatic loss that exists in the adiabatic circuit can be larger than adiabatic loss during low-speed operation. Therefore, the adiabatic circuits with nonadiabatic loss [1]–[3] are not suitable for the ultra-low-energy systems.

Although adiabatic and leakage losses are unavoidable in adiabatic circuits, nonadiabatic loss can be eliminated by using the concept of reversible logic. Although the logic in [4] eliminates nonadiabatic loss completely, its throughput is inversely proportional to the number of cascaded logic stages, which is referred to as the "retractile cascades" problem because the inputs of a stage must be valid while the energy of its outputs are supplied and recovered. Split-level charge recovery logic (SCRL) in [5] resolved this problem by using reversible logic. However, SCRL requires too many clock rails, up to 24, although it is a simpler single-rail logic. The eight-phase dual-rail logic in [6] efficiently solved the "retractile cascades" problem with reversible logic, but it does not succeed in eliminating all nonadiabatic loss [7], [8]. Recently, we proposed reversible energy recovery logic (RERL), which eliminates nonadiabatic loss completely [7], although it appears to be similar to the logic in [6]. Because these fully reversible adiabatic circuits have large circuit overhead due to reversible logic, it is necessary to control this reversibility overhead in designing ultra-low-energy systems with reversible logic circuits [5], [6].

This paper describes an energy-efficient design of the 16-bit carry-lookahead adder using RERL. In Section II, we describe the operation of RERL briefly. We then introduce a self-energy-recovery circuit (SERC) and describe how to reduce the reversibility overhead. We describe a 16-bit RERL carry-lookahead adder with SERC's and an eight-phase, clocked power generator in Section III. In Section IV, we present experimental results for the test chip. Our conclusions are in Section V.

II. RERL and SERC

A. RERL Operation

A basic RERL gate, which is either a buffer or an inverter, is shown in Fig. 1(a), and its reversible pipeline connection is shown in Fig. 1(b). The transmission gates T1 and T2 (T3 and T4) implement dual-rail forward (backward) logic functions, which determine the charging (discharging) paths of the output nodes. T5 and T6 (T7 and T8) are forward (backward) isolation switches, which isolate the charging (discharging) paths. The clamp transistors M1 and M2 make the undriven output node grounded. Unlike the logic in [6], the charging and discharging clocks of a logic stage are different in RERL, as shown in Fig. 1, which is also true in SCRL and is necessary in order to

Manuscript received April 10, 1998; revised January 6, 1999. This work was supported through the Inter-University Semiconductor Research Center by the Korea Research Foundation and through Seoul National University Nanoelectronics Institute by LG Semicon Co.

The authors are with the School of Electrical Engineering, Seoul National University, Kwanak-gu, Seoul 151-742 Korea.

Publisher Item Identifier S 0018-9200(99)04188-8.

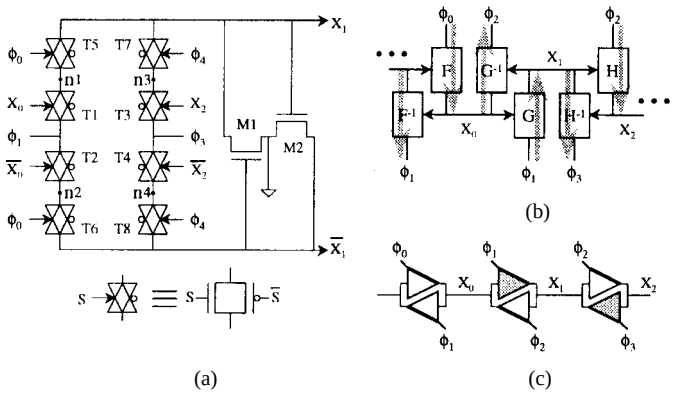


Fig. 1. RERL: (a) buffer, (b) reversible pipeline connection, and (c) symbol for a buffer chain. A shaded arrow in (b) indicates the direction and path of energy charging or discharging. F, G, and H are forward functions of each logic stage, and F^{-1}, G^{-1}, and H^{-1} are their reverse functions, respectively. A thick solid line in the buffer symbol of (c) indicates the energy flow. The buffer in (a) corresponds to the shaded parts in (c).

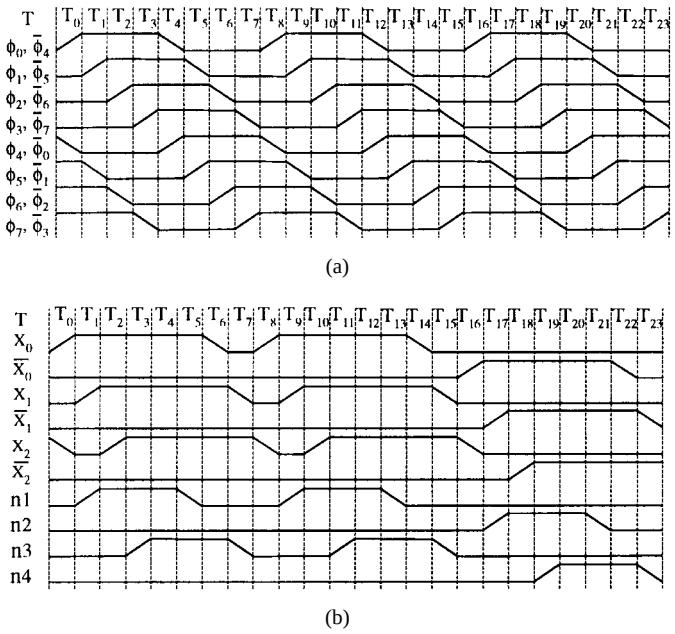


Fig. 2. Waveforms of (a) the eight-phase clock and (b) all the nodes in an RERL buffer.

eliminate nonadiabatic loss [5], [7], [8]. For example, when ϕ_1 is rising, the energy is supplied to node X_1, which is recovered when ϕ_3 is falling. The subindex of each signal X indicates its corresponding clock phase, which supplies the energy to the signal. RERL uses an eight-phase clock, shown in Fig. 2(a). The waveforms of all the nodes in an RERL buffer are shown in Fig. 2(b), as an example, for an input sequence of "110." Here, X_0 is an input signal, X_1 is its pipelined output signal, and X_2 is the output signal of the next stage, whose input is X_1. X_2 is also used as the input to the backward function used to recover the energy of X_1.

The operation of an RERL buffer gate is as follows. During the time interval T_0, the input X_0 goes high and the forward isolation switches T5 and T6 are turned on. During T_1, both X_1 and n1 go high via T1 and T5 by the rising ϕ_1 slowly, but both $\overline{X_1}$ and n2 stay at ground because they are driven

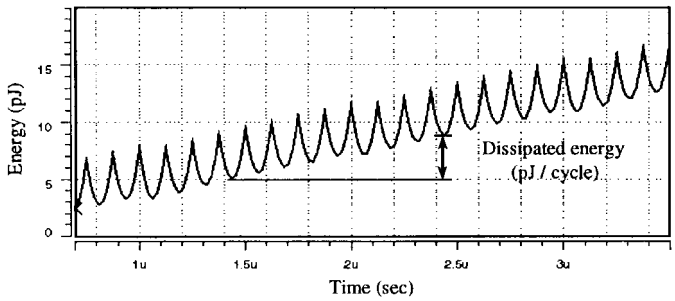


Fig. 3. Energy dissipation curve of the 16-stage RERL buffer chain. The dissipated energy per cycle is 3.6 pJ when the operating frequency is 1 MHz and the peak voltage of the clocked power is 5 V.

by the clamp devices and T2 is off. During T_2, X_2 goes high and $\overline{X_2}$ stays low. During T_3, n3 goes high via T3, and n4 is still at ground because T4 is off. During T_4, the forward isolation switches T5 and T6 are turned off and the backward ones T7 and T8 are turned on. During T_5, the falling ϕ_1 discharges n1 without nonadiabatic loss because T1 is still on due to high X_0. During T_6, the falling ϕ_2 in the previous stage discharges X_0. During T_7, the falling ϕ_3 discharges both X_1 and n3 because both T3 and T7 are still on due to X_2 and ϕ_4, respectively. During T_8, both T7 and T8 are turned off, which restarts a cycle of eight steps. Because the voltage difference between the two terminals of any switch is always zero when it is turned on, there is no abrupt charging or discharging at any node including the internal nodes (n1–n4), as shown in Fig. 2(b). Consequently, there is no nonadiabatic loss. We obtained the energy dissipation curve for a 16-stage buffer chain with SPICE simulations, as shown in Fig. 3. Note that energy is supplied and recovered during the uphill and downhill of the curve, respectively.

Although the buffer (or inverter) shown in Fig. 1 is basically reversible, most of the Boolean gates are not reversible. Note that the mapping from the input to the output must be always one-to-one in a reversible logic gate. Because an irreversible Boolean function requires "garbage" information to make it reversible [9], this reversibility increases the circuit complexity. As an example, the circuit diagram of a two-input RERL XOR gate and its symbols are illustrated in Fig. 4. For reversibility, the output contains a delayed copy A^* of the input signal A, which is "garbage" information.

B. Self-Energy-Recovery Circuit

There are two kinds of overhead in reversible logic: 1) circuit overhead due to reversibility and 2) energy overhead due to the irreversible output node of the last pipeline stage. In [5], tapered buffers were used to reduce energy dissipation in the output node of the last pipeline stage. However, the energy dissipation of the last buffer stage in a tapered buffer chain is still large if the nonadiabatic loss due to a supply-voltage drop exists in the last buffer stage.

We propose to use the SERC, which is shown in Fig. 5(a), to break the logic reversibility if a partially reversible logic consumes less energy than a fully reversible logic. We can break the reversibility of the circuit by using an irreversible function and use an SERC to recover the energy supplied

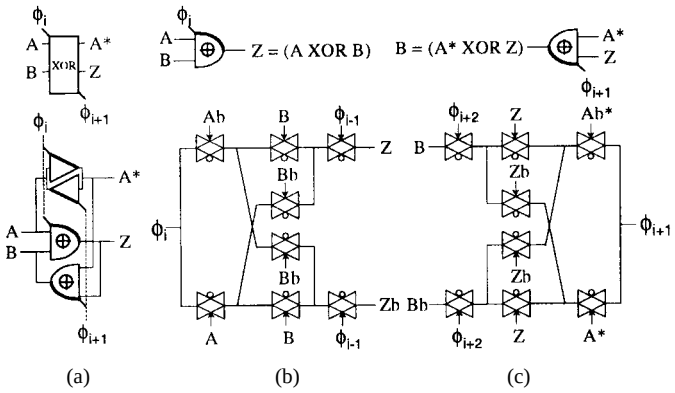


Fig. 4. Two-input XOR RERL gate: (a) symbol and schematic, (b) forward logic part, and (c) backward logic part. A^* is the delayed copy of signal A. The clamp devices are omitted. ϕ_i supplies energy to the output node, and ϕ_{i+1} recovers the energy of the input node.

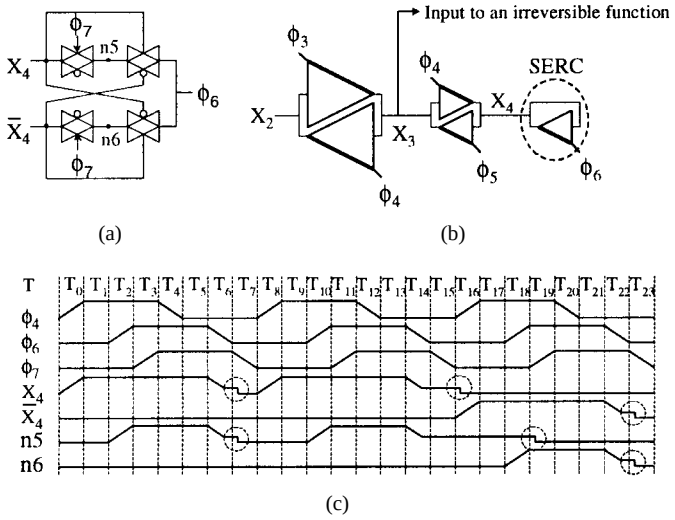


Fig. 5. (a) Schematic of an SERC and (b) tapering buffer: scaling down stage sizes before breaking reversibility with an SERC. (c) Its waveform for an input sequence "110."

to its input node. The circuit overhead due to the "garbage" information can be reduced substantially when SERC's are used properly. SERC's can also be used to minimize the energy dissipation of the output node in the last pipeline stage. Because the energy of an output node with large capacitance must be recovered, we can use tapered buffers before breaking the reversibility with an SERC, as shown in Fig. 5(b).

Although an SERC can recover most of the energy supplied to its input, it has nonadiabatic loss, which is about $(1/2)C_{\rm in}V_{\rm th}^2$, where $C_{\rm in}$ is the capacitance of the input node of the SERC. The waveforms of all the nodes in an SERC are illustrated in Fig. 5(c). Here, the dashed circles indicate the nonadiabatic loss due to abrupt voltage drops from $V_{\rm th}$ to GND. Note that we can reduce the energy consumption of a reversible adiabatic logic circuit if the nonadiabatic loss in SERC's is less than the energy saved by reducing the circuit overhead with SERC's.

III. Carry-Lookahead Adder

RERL, as well as other adiabatic logics, computes only one logic level per phase due to its inherent micropipelining. Therefore, a logic circuit is implemented with a relatively long pipelined stage in RERL, and its circuit overhead due to reversibility and its latency tend to be large. In the reversible ripple carry adder shown in [6], both the critical-path delay and the circuit overhead are large. In this paper, therefore, we selected a carry-lookahead adder (CLA) to show the usefulness of RERL because the number of required pipeline stages is $O(\log N)$ for an N-bit CLA. The schematic of a 16-bit RERL CLA using SERC's is shown in Fig. 6. The basic gates such as AND or OR are implemented in a similar way to the XOR gate shown in Fig. 4. This 16-bit adder can execute an addition for every cycle of eight phases, and it requires six pipeline stages. Its latency before obtaining the first result is 6/8 of a cycle. For a 64-bit RERL adder, the number of pipeline stages is eight and the latency is exactly a cycle.

If a 16-bit RERL CLA is implemented in a fully reversible manner, its complexity is about 32 times that of a static CMOS one. In a partially reversible RERL CLA using SERC's, as shown in Fig. 6(a), we replaced four to six RERL buffers with an SERC to reduce both energy dissipation and area overhead. Consequently, its complexity is reduced to 1/4 that of the fully reversible CLA. We broke the reversibility and inserted SERC's at the nodes of the delayed copies of input operands and the intermediate carries, as illustrated in Fig. 6. Except for the nodes connected to SERC's, the energy of all the internal nodes of the RERL CLA is recovered by using reversible logic. In the last pipeline stage, the energy of the garbage and signal outputs is partially recovered with the falling ϕ_1 with SERC's. Note that we did not use tapered buffers for the outputs to reduce the area overhead.

We generated the eight-phase clocked power in Fig. 2(a) with a small control-logic circuit and an off-chip inductor. To make the clocked power generator (CPG) efficient in energy consumption, we change the connection of the inductor terminals only when the inductor current is zero. Fig. 7(a) illustrates how we connect the inductor terminals to a pair of the clock rails, which is repeated every eight steps. Each unconnected clock rail is clamped to its own state. The block diagram of the CPG is shown in Fig. 7(b). If the frequency of the eight-phase clock is f, then that of the reference clock must be $8f$. The control signals for the driver of the clock rail ϕ_0 are also shown in Fig. 7(b), which can be generated from the outputs of a 3-bit counter.

IV. Experimental Result

A test chip, which includes a 16-bit RERL CLA with a CPG, was fabricated with 0.8-μm n-well double-metal CMOS technology, in which the threshold voltages of nMOS and pMOS are 0.7 and -0.9 V, respectively. Note that the RERL circuit requires no extra pipeline registers for synchronous operation because of its inherent pipelining characteristics. We included selection switches that made it possible to measure the energy dissipation in the RERL CLA and the CPG separately. A 16-bit static CMOS CLA with a synchronous output is also included in the test chip to allow fair comparison. In the static CMOS CLA, we inserted a register at the output stage, which is required for synchronous operation. The energies dissipated

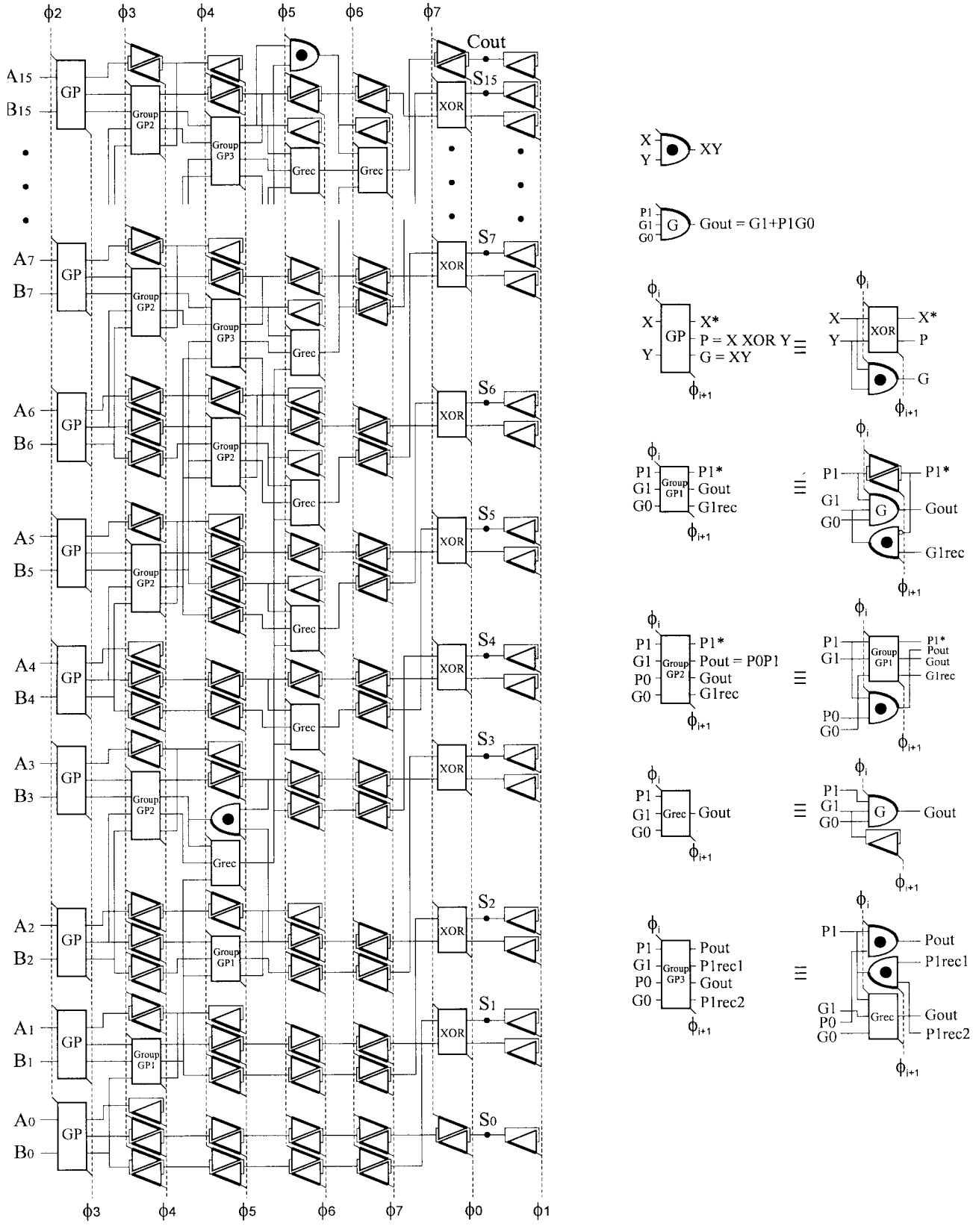
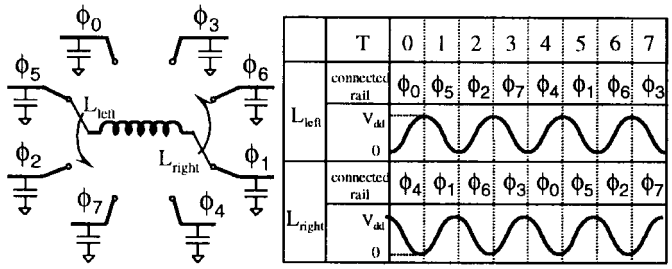
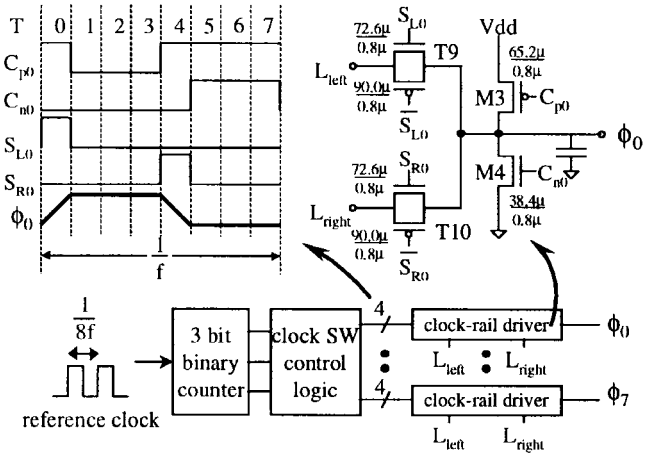


Fig. 6. Schematics of (a) a 16-bit RERL carry-lookahead adder and (b) subcircuits corresponding to the symbols used in (a). The dashed lines in the adder are clock rails: the clocks in the upper part are energy-supplying rails and those in the bottom part are energy-recovering rails. G is the generated carry, and P is the propagated carry.



(a)



(b)

Fig. 7. Clocked power generator: (a) switching order that indicates how the two terminals of the off-chip inductor are connected to two out of eight clock rails and (b) block diagram and timing of its control signals.

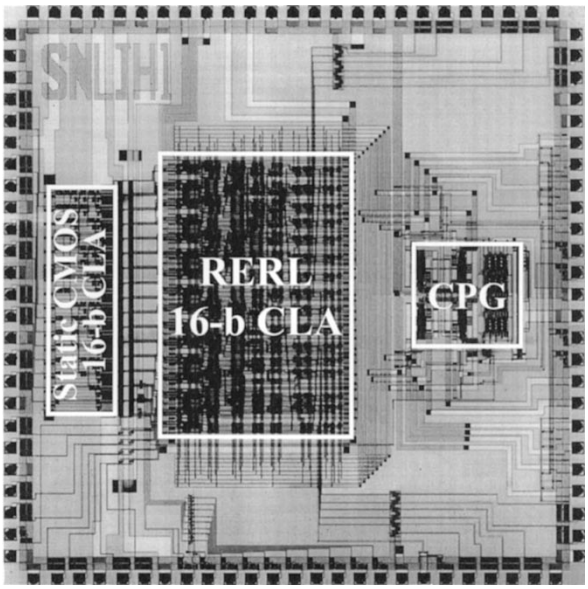


Fig. 8. Photomicrograph of the test chip.

in the static CMOS CLA and the pipeline registers can be measured separately. We used only minimum-sized transistors of $W/L = 2.4\ \mu$m$/0.8\ \mu$m for both nMOS's and pMOS's in all circuits, except for some transistors in the CPG, as shown in Fig. 7(b). Fig. 8 shows a photomicrograph of the test chip. The sizes of the RERL CLA, the CPG, and the static CMOS CLA are 2.3×1.4 mm^2, 0.96×0.74 mm^2 and

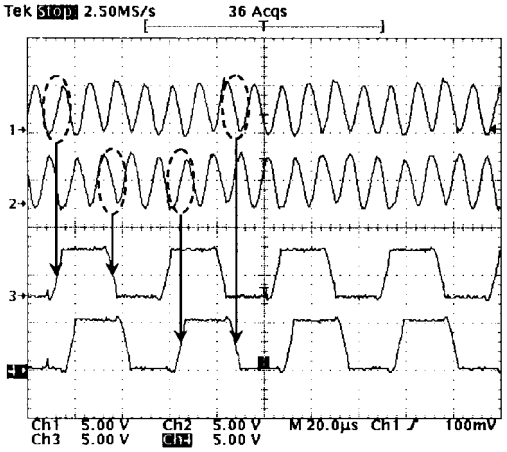


Fig. 9. Clock signal waveforms: Ch1: $L_{\rm right}$; Ch2: $L_{\rm left}$; Ch3: ϕ_1; and Ch4: ϕ_2. The edges of ϕ_1 and ϕ_2 are obtained from the sinusoidal pulses at the off-chip inductor and are designated with circles and arrows.

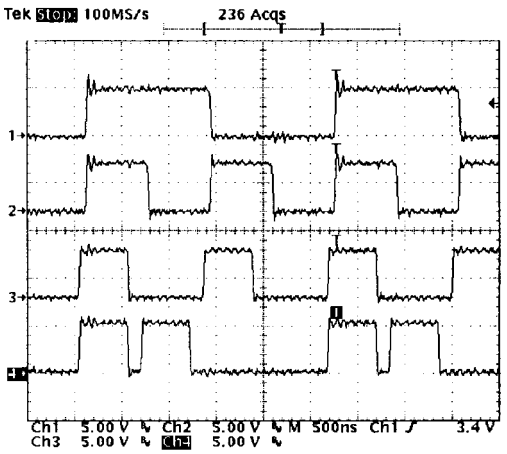


Fig. 10. Waveforms of RERL CLA: Ch1: test input signal A1; Ch2: test input signal A0; Ch3: buffered output signal S0; and Ch4: buffered output signal S1 when B0 and B1 are both high. $f = 1.51$ MHz, $L = 50\ \mu$H, $V_{\rm dd} = 5$ V, and latency $= 578$ ns. The latency from the test-pattern generator to the input of CLA is 1/8 cycle, and that of CLA is 6/8 cycle. Note that the adiabatic waveform corresponding to "high" is a return-to-zero rectangular pulse, which is measured through a static CMOS output driver.

1.8×0.3 mm^2, respectively. The area overhead of the RERL CLA is approximately six times that for the CLA, excluding the area of the CPG.

The measured waveforms of the clocks generated with the CPG are shown in Fig. 9. We confirmed that the CPG operated correctly up to 4 MHz with its corresponding reference clock of 32 MHz ($=8*4$ MHz), which was the maximum frequency of the signal generator available to us. In the SPICE simulation, the maximum operating frequency of CPG was 25 MHz with its corresponding reference clock of 200 MHz. The operation of the RERL CLA was also confirmed with the measured signal waveforms shown in Fig. 10.

Fig. 11 shows the results of the energy dissipation measured for the 16-bit RERL CLA, including the CPG, and that for the 16-bit static CMOS CLA, including the pipeline registers. Note that in the measurements, we excluded the energy consumption of the output drivers in both the static CMOS and RERL circuits. The input patterns to the adder were generated

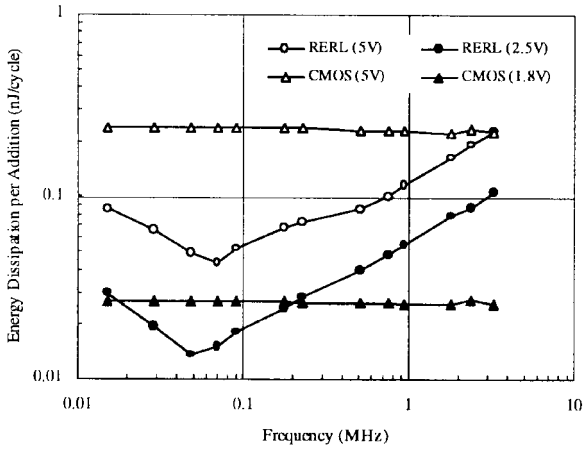


Fig. 11. Energy dissipation of the 16-bit RERL CLA with its clocked power generator and the 16-bit static CMOS CLA with synchronous output registers. Measured 1) at $V_{\rm dd} = 5$ V for both circuits and 2) at the supply voltage that minimizes the energy-delay product: 2.5 V for RERL and 1.8 V ($=2 * |-0.9\ \text{V}| = 2V_{\rm th}$ in [10]) for the static CMOS.

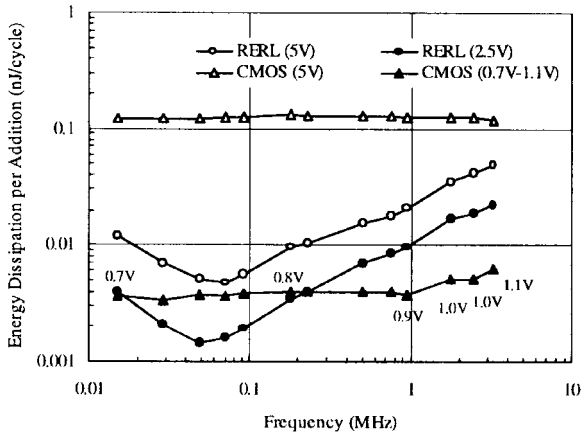


Fig. 12. Energy dissipation of the 16-bit RERL CLA and the 16-bit static CMOS CLA. Measured 1) at $V_{\rm dd} = 5$ V for both circuits and 2) at the supply voltage that minimizes the energy dissipation of each logic circuit: 2.5 V for RERL and near 0.9 V ($=|V_{\rm tp}|$) for the static CMOS.

randomly. The energy consumption of the RERL circuit was minimized when adiabatic and leakage losses were about equal in the operating frequency range between 50 and 70 kHz. At very low operating frequencies, however, slower than about 50 kHz, the consumed energy increased because the leakage loss became dominant to the adiabatic loss.

Fig. 12 shows the results of the energy dissipation measured for the RERL CLA, excluding the CPG, and that for the static CMOS CLA, excluding the pipeline registers. We measured them at the scaled supply voltage that minimized the energy dissipation of each logic circuit. Even when $V_{\rm dd} = 2.5$ V, the RERL circuit consumed much less energy than the theoretical lower limit of the static CMOS circuit at operating frequencies less than 200 kHz.

The energy dissipated in the CPG was about five to ten times larger than that of the RERL CLA, which depends on the operating frequency. The ratio of the energy dissipation of the CPG to that of the RERL CLA became higher during low-speed operation because the nonadiabatic loss of the CPG, which was consumed in the conventional static CMOS logic part in the CPG, dominated the adiabatic loss of the RERL CLA. However, this ratio can be reduced substantially if the circuit complexity of RERL is higher. Therefore, we must optimize the CPG carefully based on the complexity of RERL logic circuits.

V. Conclusion

The reversibility overhead must be controlled in the design of reversible logic for ultra-low-energy systems. Therefore, we addressed the design tradeoff between a fully reversible logic and a partially reversible logic, and proposed to use SERC to reduce the reversibility overhead. We tested a 16-bit RERL CLA using SERC's and an eight-phase, clocked power generator, which were fabricated with a 0.8-μm CMOS technology. Experimental results showed that RERL had a substantial advantage in energy consumption over static CMOS logic during low-speed operation, especially at the operating frequency, when adiabatic and leakage losses are equal. Currently, we are trying to reduce the circuit overhead of RERL. Further study on how to implement a complex RERL circuit and how to control its reversibility overhead is required.

References

[1] A. Kramer, J. S. Denker, B. Flower, and J. Moroney, "2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits," in *Proc. Int. Symp. Low Power Design*, 1995, pp. 191–196.
[2] D. Maksimovic and V. G. Oklobdzija, "Clocked CMOS adiabatic logic with single AC power supply," in *Proc. 21st Eur. Solid State Circuits Conf. (ESSCIRC'95)*, Lille, France, Sept. 1995, pp. 370–373.
[3] Y. Moon and D.-K. Jeong, "An efficient charge recovery logic circuit," *IEEE J. Solid-State Circuits*, vol. 31, pp. 514–522, 1996.
[4] R. Merkle, "Reversible electronic logic using switches," *Nanotechnology*, vol. 4, pp. 21–40, 1993.
[5] S. Younis, "Asymptotically zero energy computing using split-level charge recovery logic," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, June 1994.
[6] W. C. Athas, L. Svensson, J. G. Koller, N. Tzartzanis, and E. Y. Chou, "Low-power digital systems based on adiabatic-switching principles," *IEEE Trans. VLSI Syst.*, vol. 2, pp. 398–407, Dec. 1994.
[7] J. Lim, K. Kwon, and S.-I. Chae, "Reversible energy recovery logic circuit without nonadiabatic energy loss," *Electron. Lett.*, vol. 34, no. 4, pp. 344–346, Feb. 1998.
[8] P. Patra, "Approaches to design of circuits for low-power computation," Ph.D. dissertation, The University of Texas at Austin, Aug. 1995.
[9] C. H. Bennett, "The thermodynamics of computation—A review," *Int. J. Theor. Phys.*, vol. 21, no. 12, pp. 905–940, 1982.
[10] J. M. Rabaey and M. Pedram, *Low Power Design Methodologies*. Norwell, MA: Kluwer Academic, 1996.