

Received 12 January 2022; revised 1 May 2022; accepted 26 September 2022; date of publication 29 September 2022; date of current version 19 October 2022.

Digital Object Identifier 10.1109/TQE.2022.3210705

The Optimization and Application of 3-Bit Hermitian Gates and Multiple Control Toffoli Gates

HAI-SHENG LI[®] (Member, IEEE)

College of Electronic Engineering, Guangxi Normal University, Guilin 541004, China (e-mail: lhs1974@mailbox.gxnu.edu.cn)

This work was supported in part by the Science and Technology Project of Guangxi under Grant 2020GXNSFDA238023 and in part by the National Natural Science Foundation of China under Grant 61762012.

ABSTRACT The well-known 3-bit Hermitian gate (a Toffoli gate) has been implemented using Clifford+T circuits. Compared with the Peres gate, its implementation circuit requires more controlled-NOT (CNOT) gates. However, the Peres gate is not Hermitian. This article reports four 3-bit Hermitian gates named LI gates, whose realized circuits have the same T-count, T-depth, and CNOT-count as the Peres gate. Furthermore, two decomposition methods of a multiple-control Toffoli (MCT) gate are proposed for different primary optimization goals. Then, we design the equality, less-than, and full comparators with the minimum circuit width using proposed Hermitian gates and optimized MCT gates. A fault-tolerant circuit is required for robust quantum computing. Clifford+T circuits are accepted solutions for fault-tolerant implementation. Considering T-count, T-depth, CNOT-count, and circuit width as the primary optimization goals, we design the optimized Clifford+T circuits of three comparators using LI gates and optimized MCT gates. Comparison and analysis show that the proposed comparators have better overall performances for T-count, T-depth, CNOT-count, and circuit width than the best-known comparators without quantum measurements.

INDEX TERMS Multiple control Toffoli (MCT) gate, quantum algorithm, quantum circuit, quantum comparator, quantum optimizing method.

I. INTRODUCTION

Quantum computing enables fast quantum algorithms for factorization [1] and database search [2]. However, one of the most significant challenges in quantum computing is the realization of quantum computers [3]. As a convenient and realistic model of quantum computers, the circuit model [4] promotes the efficient implementation of quantum algorithms, such as quantum Fourier transform [5], [6], quantum wavelet transform [7], [8], and quantum image representation [9], [10], [11], [12], [13], [14], which have demonstrated quantum algorithm power in striking contrast to classical counterpart.

An efficient multiple control gate decomposition in the circuit model is crucial for using less executing time and producing fewer errors [15]. Barenco et al. [16] proposed the well-known multiple control Toffoli (MCT) decomposition, i.e., using one-qubit and two-qubit controlled-NOT (CNOT) gates to construct an MCT gate. Liu and Long [15] gave two analytic expressions for building general *n*-qubit controlled unitary gates.

The fault-tolerant implementation of quantum gates is needed for robust quantum computing in the presence of noise [17]. Clifford+T circuits are widely accepted solutions for fault-tolerant implementation [18], [19]. The T gates are more expensive than other gates in terms of space and time cost due to their increased tolerance to noise errors [20], [21], [22]. But neglecting the cost of the CNOT gates may lead to a significant underestimate [23]. Therefore, the number of T gates (T-count), the maximum number of T gates in any circuit path (T-depth), and the number of CNOT gates (CNOT-count) are the main performance indicators of Clifford+T circuits.

The multiple control gates, such as Toffoli, Peres, Fredkin, TR [24], and MCT gates, are the staple of quantum arithmetic circuits [25]. Quantum circuits without ancillae for Toffoli gates proposed in [22], [26], and [27] have T-count 7 and T-depth 3. The T-depth one representation of the Toffoli gate is presented with four ancillae [22], [28]. Jones utilized quantum measurement and an ancilla to implement the Toffoli gate with T-depth 1 [29]. There are different

decomposition methods of the MCT gate [22], [23], [25], [29], [30]. Amy et al. [22] proposed a T-par algorithm to reduce T-count significantly. However, the T-par algorithm does not effectively reduce the CNOT-count. Compared with the T-par algorithm, an automated optimization algorithm reduces the CNOT-count and has the same T-count [23]. Maslov [25] replaced suitable pairs of the MCT gates with their relative phase implementations and obtained the smaller T-count and CNOT-count than the Tpar algorithm and automated optimization algorithm. But, Maslov's approach does not involve the optimization of Tdepth. Two *n*-qubit MCT decompositions presented in [29] and [30] can obtain the smallest T-count using n quantum measurements. A few alternative works for the MCT/Toffoli gate decomposition have been carried out in the recent past. For instance, Philipp et al. [31] explored the mapping of reversible MCT circuits to IBM quantum computers. Gokhale et al. [32] used three-level qutrits to optimize quantum circuits.

A quantum comparator is an essential arithmetic operator to realize quantum image translation [33], bilinear interpolation [34], image binarization [21], [35], image segmentation [36], and quantum database search [37]. Orts et al. [21] proposed two efficient operators. Compared with the existing comparators [27], [33], [34], [35], [36], [37], Orts's first comparator has the smallest T-count, i.e., T-count 4n, and the second comparator's T-depth is $O(\log n)$. However, the two n-bit comparators need n auxiliary qubits and n quantum measurements, at least. On the other hand, comparators presented in [27] and [38] have an important feature: it only requires a single ancillary qubit.

Quantum algorithms may likely be implemented in these noisy intermediate-scale quantum (NISQ) devices, such as quantum chemistry [39]. Excessive ancillary qubits cause circuit width (the qubit number of circuits) to become too big. As a result, it blocks algorithms applied to NISQ devices. Therefore, in this work, we consider T-count, T-depth, circuit width, and CNOT-count as the main optimization goals for comparators based on Clifford+T circuits. First, we present four 3-bit Hermitian gates named LI gates. Next, two MCT decomposition methods based on LI gates are proposed with different optimization goals. Then, the equality, less-than, and full comparators are designed by proposed Hermitian gates and (n + 1)-b MCT gates. Finally, the optimized Clifford+T circuits of three comparators are presented. The contributions of this article can be summarized as follows.

- This article presents two decompositions of the MCT gate with lower T-depth and T-count against the bestknown optimization methods without quantum measurements. The significant advantage of the proposed MCT gates is that it is convenient for implementing full comparators (see Table 8).
- 2) This article proposes the equality, less-than, and full comparators with the minimum circuit width.

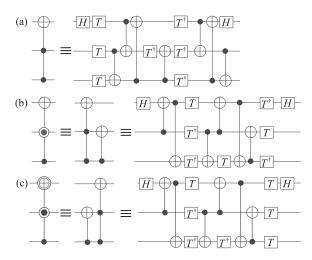


FIGURE 1. Clifford+T circuits for (a) Toffoli gate, (b) Peres gate, and (c) inverse-Peres gate named TR gate in [24]. The Clifford+T circuit of the TR gate is renamed TR1 in [27].

 Considering T-count, T-depth, circuit width, and CNOTcount, this article gives optimized Clifford+T circuits of the proposed comparators.

The rest of this article is organized as follows. Section II introduces background knowledge. Section III presents four LI gates. In Section IV, we implement and optimize the MCT gate. Section V describes the design of three comparators. Comparison and analysis are given in Section VI, and conclusions are drawn in Section VI-A.

II. BACKGROUND

The Pauli matrices I, X, and Z, the Hadamard gate H, the phase gate S, the gate CNOT, and the non-Clifford gate T are elements in the Clifford+T set where I, X, Z, H, S, and T are defined by

$$I = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix},$$
$$H = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, S = \begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix}, T = \begin{bmatrix} 1 & 0 \\ 0 & e^{i\pi/4} \end{bmatrix}.$$

The gate set $\{H, S, S^{\dagger}, \text{CNOT}, T, T^{\dagger}\}$ is universal for quantum computation [26]. Clifford+T circuits for the Toffoli, Peres, and inverse-Peres gates are presented in Fig. 1 [26], [27]. An MCT gate with n qubits can be implemented by 4(n-3) Toffoli gates [16], whose 6-qubit example is given in Fig. 2.

III. 3-BIT HERMITIAN GATES

The TR2 gate presented in Fig. 3 is a previous work [27]. It is considered a variant of the TR gate in [27]. We discover

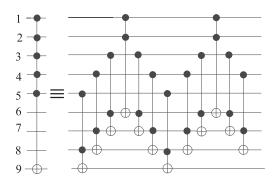


FIGURE 2. The 6-qubit MCT gate with three ancillary qubits.

FIGURE 3. Clifford+T circuit for the TR2 gate in [27].

that the matrix form of the TR2 gate is

whose adjoint is equal to itself. That is, the inverse of the TR2 gate is not the Peres gate or Peres gate's variant. Therefore, the TR2 gate is fundamentally different from the TR gate because the TR gate is the inverse of the Peres gate. Thus, the TR2 gate should not be seen as a variant of the TR gate. Through the above analysis, we revise the symbol and name of the TR2 gate in Fig. 4(b).

The other three Hermitian gates are discovered and designed in Fig. 4(a), (c), and (d). Equation (1) and Fig. 5 show that the proposed 3-b gates are Hermitian.

The proposed four 3-b gates in Fig. 4 can implement

$$\begin{cases} LI1: |C\rangle |B\rangle |A\rangle \rightarrow |\overline{A}.B \oplus C\rangle |A \oplus B\rangle |A\rangle, \\ LI2: |C\rangle |B\rangle |A\rangle \rightarrow |A.\overline{B} \oplus C\rangle |B\rangle |A \oplus B\rangle, \\ LI3: |C\rangle |B\rangle |A\rangle \rightarrow |\overline{A}.\overline{B} \oplus C\rangle |B\rangle |A \oplus B\rangle, \\ LI4: |C\rangle |B\rangle |A\rangle \rightarrow |\overline{A}.\overline{B} \oplus C\rangle |A \oplus B\rangle |A\rangle \end{cases}$$
(2)

where the symbols "." and " \oplus " are multiplication and exclusive-OR operators, respectively. \overline{A} and \overline{B} are equal to (1-A) and (1-B).

Analyzing the circuits in Figs. 1 and 4, we give parameters for Toffoli, Peres, TR, and LI gates in Table 1. Compared with the Toffoli gate, the proposed LI gates reduce a CNOT gate. Therefore, the proposed LI gates have an improvement for some applications. For instance, two 2-b less-than comparators realized by Toffoli gates and LI2 gates in Fig. 6 show

TABLE 1. Parameters of Toffoli, Peres, TR, and LI Gates

Gates	T-count	CNOT-count	Total count	T-depth	Hermitian
Toffoli	7	7	16	3	Yes
Peres	7	6	15	3	No
TR	7	6	15	3	No
LI	7	6	15	3	Yes

TABLE 2. Optimization Results of Rules 1-9

Rules	Preoptimization			Postoptimization			
Kuics	T-count	T-depth	CNOT-count	T-count	T-depth	CNOT-count	
Rule 1	14	6	12	8	4	8	
Rule 2	14	6	12	8	4	10	
Rule 3	14	6	12	8	4	10	
Rule 4	28	12	24	12	6	14	
Rule 5	28	12	24	8	4	12	
Rule 6	42	16	36	16	8	22	
Rule 7	56	20	48	16	8	24	
Rule 8	70	24	60	24	12	34	
Rule 9	42	16	36	16	8	18	

that their CNOT-counts are 28 and 22, respectively. That is, the latter uses six fewer CNOT gates than the former.

On the other hand, since the TR gate is not Hermitian, its inverse (i.e., the Peres gate) needs to be added to implement a less-than comparator [27]. Therefore, the proposed LI gates provide an alternative method to design comparators. For instance, we only use LI2 and CNOT gates to realize a less-than comparator in Fig. 14. Furthermore, due to the symmetry of the Hermitian gates, the proposed LI gates are convenient for the implementation of full comparators (see Fig. 18 and Table 8).

IV. IMPLEMENTATION AND OPTIMIZATION OF THE MCT

A. IMPLEMENTATION OF THE MCT GATE

An MCT gate is labeled TOF_{Not}^n in Fig. 7(a). Then, inspired by the method in Fig. 2 [16], we present the implementation of TOF_{Not}^n in Fig. 7(b) by 4(n-3) LI gates where the (n-3)-qubit unknown state $|xx...x\rangle$ is adopted as ancillae. Finally, for clarity, we give the implementation of TOF_{Not}^6 in Fig. 8 as an example.

B. OPTIMIZATION OF THE MCT GATE

In this section, two optimization methods of the MCT gate are proposed. The first method preferentially reduces T-count and T-depth. The primary purpose of the second method is to optimize T-count and CNOT-count. For clarity, optimization rules 1–9 for the first method are presented in Appendix A-A. The optimization results of these rules are summarized in Table 2.

The optimized circuits for TOF_{Not}^4 and TOF_{Not}^5 are presented in Fig. 9 using the above rules. Fig. 9 illustrates that TOF_{Not}^4 and TOF_{Not}^5 both employ an ancillary qubit $|x\rangle$. We infer that TOF_{Not}^4 has T-count 16, T-depth 8, and CNOT-count 17. TOF_{Not}^5 can be realized with T-count 24, T-depth 12, and CNOT-count 28.

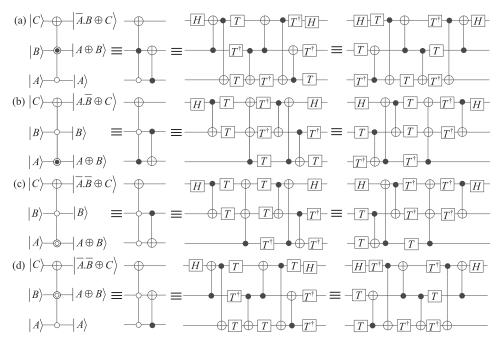


FIGURE 4. Clifford+T circuits for LI gates including (a) LI1 gate, (b) LI2 gate, (c) LI3 gate, and (d) LI4 gate.

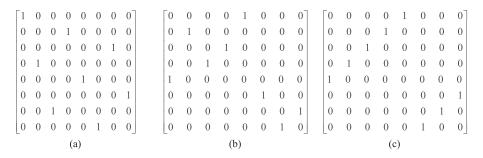


FIGURE 5. Matrix forms of the three Hermitian gates including (a) LI1 gate, (b) LI3 gate, and (c) LI4 gate.

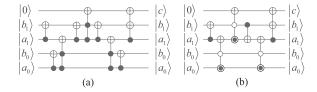


FIGURE 6. Two 2-b less-than comparators realized by (a) Toffoli gates and (b) LI2 gates.

For an even number n with n > 5, one rule 6, (n/2 - 3) times of rule 7, and one rule 9 are used to optimize ${\rm TOF}^n_{\rm Not}$. Therefore, the number of ancillary qubits is 1 + (n/2 - 1) + 1 = n/2 - 1. For instance, the optimized circuit for ${\rm TOF}^6_{\rm Not}$ in Fig. 10 uses one rule 6 and one rule 9 with two ancillary qubits. From Table 2, T-count, T-depth, and CNOT-count are calculated by 16 + 16(n/2 - 3) + 16 = 8n - 16, 8 + 8(n/2 - 3) + 8 = 4n - 8, and 22 + 24(n/2 - 3) + 18 = 12n - 32.

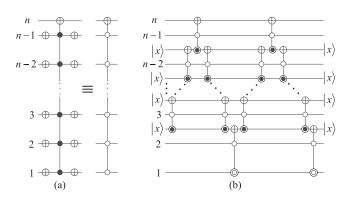


FIGURE 7. Implementation of the MCT gate with n qubits showing (a) TOF_{Not}^n , and (b) implementation circuit of TOF_{Not}^n .

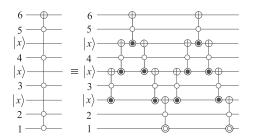


FIGURE 8. Implementation of TOF_{Not}.

TABLE 3. Optimization Results of Rules n1-n9

Rules		Preoptimization]	Postoptimization				
Kules	T-count	CNOT-count	T-depth	T-count	CNOT-count	T-depth			
Rule n1	14	12	6	8	6	8			
Rule n2	14	12	6	8	8	8			
Rule n3	14	12	6	8	8	8			
Rule n4	28	24	12	12	10	12			
Rule n5	28	24	12	8	8	8			
Rule n6	42	36	16	16	16	16			
Rule n7	56	48	20	16	16	16			
Rule n8	70	60	24	24	24	24			
Rule n9	42	36	16	16	12	16			

3)/2. Similarly, we calculate T-count with 16(n-7)/2 + 24 + 16 = 8n - 16, T-depth with 8(n-7)/2 + 12 + 8 = 4n - 8, and CNOT-count with 24(n-7)/2 + 34 + 18 = 12n - 32.

Optimization rules n1–n9 for the second method are presented in Appendix A-B. In addition, the optimization results of these rules are summarized in Table 3.

We obtain the alternative optimized circuits for TOF_{Not}^n using rule ni instead of rule i ($i \in \{5, 6, 7, 8, 9\}$). For instance, the alternative optimized circuits for TOF_{Not}^4 and TOF_{Not}^5 are presented in Figs. 11 and 12 using the rules in Table 3. Results in Tables 2 and 3 show that the T-counts of TOF_{Not}^n (n > 5) for the two methods are both 8n - 16. The T-depth of TOF_{Not}^n is also 8n - 16 for the second method. The CNOT-count of TOF_{Not}^n with an even number n is 16 + 16(n/2 - 3) + 12 = 8n - 20. Meanwhile, the CNOT-count of TOF_{Not}^n with an odd number n is calculated by 16(n - 7)/2 + 24 + 12 = 8n - 20.

For convenience, the optimized circuits for TOF_{Not}^n using the first and second methods are labeled as $^1TOF_{Not}^n$ and $^2TOF_{Not}^n$, respectively. Through the above analysis, we can implement $^1TOF_{Not}^n$ with T-count 8n-16, T-depth 4n-8, and CNOT-count 12n-32, and $^2TOF_{Not}^n$ with T-count 8n-16, T-depth 8n-16, and CNOT-count 8n-20.

V. QUANTUM COMPARATORS

In this section, we design the equality, less-than, and full comparators for the relationships of two integers a and b: a = b or $a \ne b$; a < b or $a \ge b$; a > b, a = b, and a < b.

A. EQUALITY COMPARATOR

We select the MCT gate TOF_{Not}^{n+1} to realize an *n*-bit equality comparator, whose 5-b example is presented in Fig. 13. The

TABLE 4. Optimization Results of Rules for the Less-Than Comparator

Rules		Preoptimiz	ation	Postoptimization			
Kuies	T-count	T-depth	CNOT-count	T-count	T-depth	CNOT-count	
Rule 1	14	6	12	8	4	8	
Rule 10	21	8	19	12	4	12	
Rule 11	28	10	24	16	6	16	
Rule n1	14	6	12	8	8	6	
Rule n10	21	8	19	12	8	9	
Rule n11	28	10	24	16	12	12	

equality comparator gives the results c=0 for $a \neq b$ and c=1 for a=b. Fig. 13 infers that the *n*-bit equality comparator consists of 4(n-2) LI gates and 2n CNOT gates.

Fig. 13 illustrates that $|a_2\rangle$, $|a_3\rangle$, and $|a_4\rangle$ are ancillary qubits implementing TOF $_{\text{Not}}^6$. Using two methods in Section IV-B, we obtain the optimized implementation circuits of TOF $_{\text{Not}}^6$ with two ancillary qubits $|a_3\rangle|a_4\rangle$. Since qubits storing an operand also are used as ancillae, the proposed optimization methods do not increase the width of the equality comparator. Thus, the *n*-bit equality comparator based on ${}^{1}\text{TOF}_{\text{Not}}^{n+1}$ has T-count 8n-8, T-depth 4n-4, circuit width 2n+1, and CNOT-count 14n-20. Compared with the equality comparator based on ${}^{1}\text{TOF}_{\text{Not}}^{n+1}$, the *n*-bit equality comparator based on ${}^{2}\text{TOF}_{\text{Not}}^{n+1}$ keeps the same T-count and circuit width. But its CNOT-count and T-depth are 10n-12 and 8n-8.

B. LESS-THAN COMPARATOR

Modifying the comparator proposed in [27], we only use LI2 and CNOT gates to design the less-than comparator in Fig. 14(a). For example, a 5-b comparator is presented in Fig. 14(b). Here, $|c\rangle$ is the comparison result of two numbers, i.e., if $b \ge a$, $|c\rangle = |0\rangle$; otherwise, $|c\rangle = |1\rangle$. Fig. 14 shows that the less-than comparator consists of 2n-1 LI2 gates and 4(n-1) CNOT gates.

In Appendix B-A, we give rules 10 and 11 with primary optimization goals {T-count, T-depth, width } and rules n10 and n11 with primary optimization goals { T-count, CNOT-count, width}. Their optimization results are summarized in Table 4. For clarity, rules 1 and n1 are also placed in Table 4.

Table 4 shows that rule 11 reduces T-depth of two times of rule 1 in Appendix A-B from 8 to 6. We can infer that each additional rule 1 in the manner provided by rule 11 only increases T-depth 2. The n-bit less-than comparator with primary optimization goals {T-count, T-depth} and $n \geq 3$ is optimized by one rule 10 and (n-2) times of rule 1. For instance, the optimized circuit of the 3-b less-than comparator is given in Fig. 15. The T-count, T-depth, and CNOT-count of the n-bit less-than comparator can be calculated by 12 + 8(n-2) = 8n - 4, 4 + 2(n-2) = 2n, and (4n-5) + 12 + 8(n-2) = 12n - 9, respectively.

Similarly, the n-bit less-than comparator with primary optimization goals {T-count, CNOT-count} can be optimized by one rule n10 and (n-2) times of rule n1. Its optimized circuit with n=3 is presented in Fig. 16. Each additional

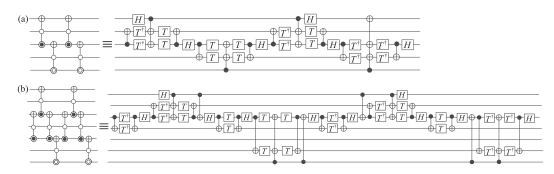


FIGURE 9. Optimized circuits for (a) TOF_{Not} and (b) TOF_{Not}.

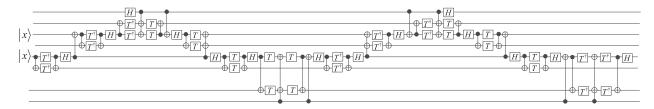


FIGURE 10. Optimized circuit for TOF_{Not}.

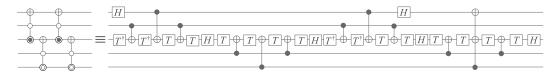


FIGURE 11. Alternative optimized circuit for TOF4_{Not}.

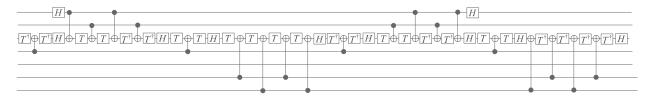


FIGURE 12. Alternative optimized circuit for TOF_{Not}.

rule n1 in the manner provided by rule n11 increases T-depth 4. Thus, the alternative optimized circuit of the *n*-bit less-than comparator has a T-count of 12 + 8(n-2) = 8n - 4, T-depth of 8 + 4(n-2) = 4n, and CNOT-count of (4n-5) + 9 + 6(n-2) = 10n - 8.

Since rules in Table 4 do not use ancillary qubits, two optimized circuit widths of the n-bit less-than comparator are still 2n + 1.

C. FULL COMPARATOR

The equivalent circuits of the equality comparator are presented in Fig. 17. Since the LI2 gate is Hermitian, the circuit in the dashed box in Fig. 17 does not change integers a and b. Therefore, the circuit at the top right is

also for the equality comparator. Applying the LI2 gate on the state $|a_1\rangle|b_0\rangle|a_0\rangle$, we obtain $|a_1\oplus \overline{b_0}a_0\rangle|b_0\rangle|a_0\oplus b_0\rangle$. Thus, eliminating two CNOT gates, we give another equivalent circuit of the equality comparator at the bottom right in Fig. 17.

Substituting the implementation of TOF_{Not}^6 into Fig. 17, we obtain the circuit in the dashed box 2 in Fig. 18, implementing the equality comparator. Comparing the dashed box 1 in Fig. 18 with the circuit in Fig. 14(b), we infer that the state $|c_1\rangle$ stores the result of the less-than comparator. That is, Fig. 18(a) implements a 6-b full comparator. Then, we propose an n-bit full comparator in Fig. 18(b). The results are stored in $|c_1\rangle|c_0\rangle$: $|c_1\rangle|c_0\rangle = |0\rangle|0\rangle$ for b > a, $|c_1\rangle|c_0\rangle = |0\rangle|1\rangle$ for b = a, and $|c_1\rangle|c_0\rangle = |1\rangle|0\rangle$ for b < a. Fig. 18

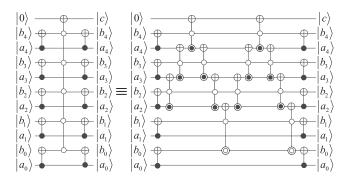


FIGURE 13. Circuit for a 5-b equality comparator.

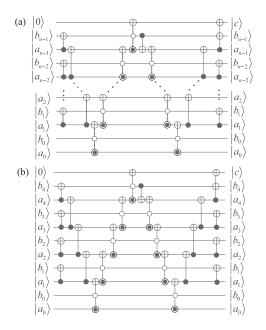


FIGURE 14. Less-than comparator showing (a) *n*-bit comparator, and (b) 5-b comparator.

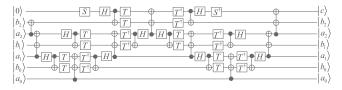


FIGURE 15. Optimized circuit of the 3-b less-than comparator.

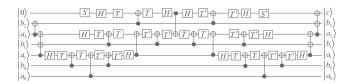


FIGURE 16. Alternative optimized circuit of the 3-b less-than comparator.

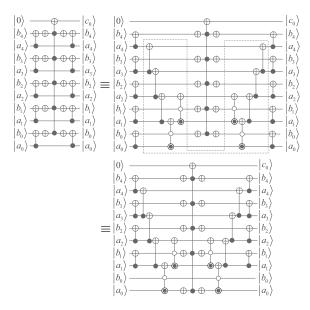


FIGURE 17. Equivalent circuits for the 5-b equality comparator.

TABLE 5. Optimization Results of Rules for the Full Comparator

Rules		Preoptimiz	ation	Postoptimization			
Kules	T-count	T-depth	CNOT-count	T-count	T-depth	CNOT-count	
Rule 4	28	12	24	12	6	14	
Rule 12	14	6	13	12	6	12	
Rule 13	42	16	36	20	8	27	
Rule 14	56	20	48	24	10	28	
Rule n4	28	12	24	12	12	10	
Rule n12	14	6	13	12	8	11	
Rule n13	42	16	36	20	18	20	
Rule n14	56	20	48	24	20	20	

illustrates that the full comparator consists of 4(n-1) LI gates and 4(n-1) CNOT gates.

In Appendix B-B, we present rules 12, 13, and 14 with primary optimization goals {T-count,T-depth}, and rules n12, n13, and n14 with primary optimization goals { T-count,CNOT-count}. The optimization results of these rules are summarized in Table 5. In addition, rules 4 and n4 are placed in Table 5.

We optimize the *n*-bit full comparator with primary optimization goals {T-count, T-depth} and $n \ge 3$ using one rule 12, one rule 13, and (n-3) times of rule 4. The optimized circuit of the 3-b full comparator with T-depth 12 is given in Fig. 19(a). From Table 5, we obtain that each additional rule 4 in the manner provided by rule 14 increases T-depth 4. Therefore, the *n*-bit full comparator has a T-depth of 12 + 4(n-3) = 4n. Its 4-b example is presented in Fig. 19(b). The T-count and CNOT-count for the *n*-bit full comparator are calculated by 12 + 20 + 12(n-3) = 12n - 4 and (4n-5) + 12 + 27 + 14(n-3) = 18n - 8.

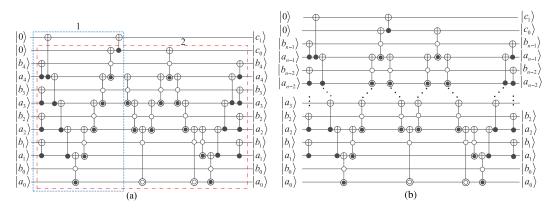


FIGURE 18. Full comparator showing (a) 5-b comparator, and (b) *n*-bit comparator.

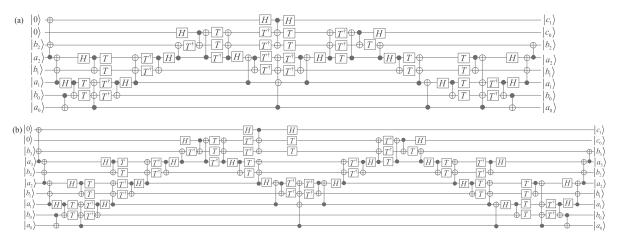


FIGURE 19. Optimized circuit of (a) 3-b full comparator and (b) 4-b full comparator.

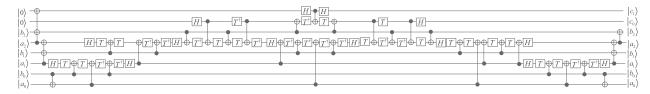


FIGURE 20. Alternative optimized circuit of the 3-b full comparator.

The *n*-bit full comparator with primary optimization goals {T-count, CNOT-count } can be optimized by one rule n12, one rule n13, and (n-3) times of rule n4. A 3-b example with T-depth 26 is presented in Fig. 20. Table 5 shows that each additional rule n4 in the manner provided by rule n14 increases T-depth 8. So, the *n*-bit full comparator with primary optimization goals { T-count, CNOT-count} has the T-depth 26 + 8(n-3) = 8n + 2. From Table 5 and Fig. 18, we calculate the T-count and CNOT-count of the alternative optimized circuit of the *n*-bit full comparator by 12 + 20 + 12(n-3) = 12n - 4 and (4n-5) + 11 + 20 + 10(n-3) = 14n - 4.

VI. COMPARISON ANALYSIS

A. COMPARISON ANALYSIS OF THE MCT GATE DECOMPOSITIONS

The best-known MCT gate TOFⁿ has been realized in [22], [23], [25], [29], and [30]. The gate TOFⁿ_{Not} can be built by a TOFⁿ gate and 2n-2 NOT gates. We summarize the decomposition results of TOFⁿ_{Not} for primary optimization goals {T-count, T-depth} or {T-count, CNOT-count} in Table 6 and compare them against the best known. Table 6 shows that the MCT gates in [29] and [30] have the best T-count of 4n-8. They are realized by n-2 quantum measurements,



TABLE 6. Comparison of the Decomposition Methods for MCT Gates

Gate	Method	Primary optimization goal	T-count	T-depth	CNOT-count	H-count	O-count	Total count	Ancillae	Ancillae type	M-coun
	Proposed	T-count, T-depth	16	8	17	6	0	39	1	$ x\rangle$	0
	$[22]^{1}$	T-count	16	N/A	54	6	6+6	82+6	1	$ x\rangle$	0
	$[29]^2$	T-count, T-depth	8	2	19	10	2+6	39+6	4	$ 0\rangle^{\otimes 4}$	2
TOF_{Not}^4	$[30]^3$	T-count, T-depth	8	8	9	8	14+6	39+6	2	$ 0\rangle^{\otimes 2}$	2
	Proposed	T-count, CNOT-count	16	16	13	6	0	35	1	$ x\rangle$	0
	$[23]^4$	T-count, CNOT-count	16	N/A	18	N/A	N/A	40+6	1	$ x\rangle$	0
	$[25]^5$	T-count, CNOT-count	16	16	14	6	0+6	36+6	1	$ x\rangle$	0
	Proposed	T-count, T-depth	24	12	28	10	0	62	1	$ x\rangle$	0
	$[22]^{1}$	T-count	28	N/A	90	10	0+8	141+8	2	$ x\rangle^{\otimes 2}$	0
	$[29]^2$	T-count, T-depth	12	3	28	15	3+8	58+8	6	$ 0\rangle^{\otimes 6}$	3
TOF_{Not}^{5}	$[30]^3$	T-count, T-depth	12	8	13	12	21+8	58+8	3	$ 0\rangle^{\otimes 3}$	3
	Proposed	T-count, CNOT-count	24	24	20	10	0	54	1	$ x\rangle$	0
	$[23]^4$	T-count, CNOT-count	28	N/A	34	N/A	N/A	72+8	2	$ x\rangle^{\otimes 2}$	0
	$[25]^5$	T-count, CNOT-count	24	24	20	10	0+8	54+8	1	$ x\rangle$	0
	Proposed	T-count, T-depth	32	16	40	14	0	86	2	$ x\rangle^{\otimes 2}$	0
	$[22]^{1}$	T-count	40	N/A	132	14	20+10	206+8	3	$ x\rangle^{\otimes 3}$	0
	$[29]^2$	T-count, T-depth	16	4	37	20	4+10	77+10	8	$ 0\rangle^{\otimes 8}$	4
TOF^6_Not	$[30]^3$	T-count, T-depth	16	12	17	16	28+10	77+10	4	$ 0\rangle^{\otimes 4}$	4
	Proposed	T-count, CNOT-count	32	32	28	14	0	74	2	$ x\rangle^{\otimes 2}$	0
	$[23]^4$	T-count, CNOT-count	40	N/A	50	N/A	N/A	104+10	3	$ x\rangle^{\otimes 3}$	0
	$[25]^5$	T-count, CNOT-count	32	32	28	14	0+10	74+10	2	$ x\rangle^{\otimes 2}$	0
	Proposed	T-count, T-depth	72	36	100	34	0	206	4	$ x\rangle^{\otimes 4}$	0
	$[22]^{1}$	T-count	100	N/A	328	34	55+20	517+20	8	$ x\rangle^{\otimes 8}$	0
	$[29]^2$	T-count, T-depth	36	9	82	45	9+20	172+20	18	$ 0\rangle^{\otimes 18}$	9
TOF_{Not}^{11}	$[30]^3$	T-count, T-depth	36	16	37	36	63+20	172+20	9	$ 0\rangle^{\otimes 9}$	9
	Proposed	T-count, CNOT-count	72	72	68	34	0	174	4	$ x\rangle^{\otimes 4}$	0
	$[23]^4$	T-count, CNOT-count	100	N/A	130	N/A	N/A	264+20	8	$ x\rangle^{\otimes 8}$	0
	$[25]^5$	T-count, CNOT-count	72	72	68	34	0+20	174+20	4	$ x\rangle^{\otimes 4}$	0
	Proposed	T-count, T-depth	8n - 16	4n - 8	12n - 32	4n - 10	0	24n - 58	$\left\lceil \frac{n-3}{2} \right\rceil$	$ xx \dots x\rangle$	0
	[22] ¹	T-count	12n - 32	N/A	N/A	N/A	N/A	N/A	n-3	$ xx \dots x\rangle$	0
	$[29]^2$	T-count, T-depth	4n - 8	n-2	19n - 17	N/A	N/A	N/A	2n - 4	000⟩	n-2
TOF _{Not}	[30] ³	T-count, T-depth	4n - 8	$4\lceil \log(n-1)\rceil$	4n - 7	N/A	N/A	N/A	n-2	000⟩	n-2
(n > 5)	Proposed	T-count, CNOT-count	8n - 16	8n - 16	8n - 20	4n - 10	0	20n - 46	$\left\lceil \frac{n-3}{2} \right\rceil$	$ xx \dots x\rangle$	0
	[23] ⁴	T-count, CNOT-count	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0
	[25] ⁵	T-count, CNOT-count	8n - 16	8n - 16	8n - 20	4n - 10	2n-2	22n - 48	$\left\lceil \frac{n-3}{2} \right\rceil$	$ xx \dots x\rangle$	0

¹ is the optimization algorithm by Amy et al. in 2014 [22];
² is the design by Jones in 2013 [29];
³ is the design (Corollary 2) by He et al. in 2017 [30];

TABLE 7. Comparison Results of the Less-Than Comparators

Less-t	han comparators	Primary optimization goal	T-count	T-depth	CNOT-count	Width	Total count	Total depth	M-count
	Proposed first	T-count, T-depth, Width	8n - 4	2n	12n - 9	2n + 1	24n - 13	10n - 3	0
	Proposed second	T-count, CNOT-count, Width	8n - 4	4n	10n - 8	2n + 1	22n - 12	12n - 5	0
	First [21] 1	T-count, T-depth	4n	2n	12n - 7	3n	21n - 6	14n - 5	n
$n \ge 3$	Second [21] 1	T-depth	$12n - f_1(n)$	$\log(n)$	N/A	$6n - f_2(n)$	N/A	N/A	$\approx 3n$
	[27] 2	T-count, T-depth, Width	14n - 7	6n - 3	16n - 10	2n + 1	34n - 19	16n - 3	0
	[38] 3	T-count, T-depth, Width	8n - 4	2n	14n - 12	2n + 1	26n - 12	14n - 13	0

¹ is the design by Orts et al. in 2021 [21]; ² is the design by Li et al. in 2020 [27];

M-count denotes the number of quantum measurements. $f_1(n)$ and $f_2(n)$ are equal to $8W(n) + 4\log(n)$ and $8W(n) + 2\log(n)$, where W(n) is the number of ones in the binary expansion of n [21].

⁴ is the optimization algorithm (H) by Nam et al. in 2018 [23];

⁵ is the design by Maslov in 2016 [25].

M-count denotes the number of quantum measurements. O-count indicates the total number of S, Z, and NOT gates.

³ is the design by Li et al. in 2022 [38].

TABLE 8.	Comparison	Results	of the	Full	Compara	tors

	Full comparators	Primary optimization goal	T-count	T-depth	CNOT-count	Width	Total count	Total depth
	Proposed	T-count, T-depth, Width	32	12	46	8	92	48
	Proposed	T-count, CNOT-count, Width	32	26	38	8	84	63
n = 3	[36] 1	N/A	84	33	84	11	192	99
n = 0	$[37]^2$	N/A	84	30	84	12	192	90
	Less-than 4 + TOF $_{Not}^4$ [21] 3	N/A	36	22	43	8	103	N/A
	Less-than 5 + TOF $_{\text{Not}}^{n+1}$ [21] 3	N/A	36	28	38	8	98	N/A
	Proposed	T-count, T-depth, Width	68	24	100	14	200	102
	Proposed	T-count, CNOT-count, Width	68	50	80	14	180	129
n = 6	[36] 1	N/A	189	N/A	189	17	432	N/A
n = 0	$[37]^2$	N/A	189	57	189	24	432	171
	Less-than ⁴ + TOF _{Not} [21] ³	N/A	84	52	101	14	239	N/A
	Less-than 5 + TOF $_{\rm Not}^{n+1}$ [21] 3	N/A	84	64	90	14	228	N/A
	Proposed	T-count, T-depth, Width	12n - 4	4n	18n - 8	2n + 2	36n - 16	18n - 6
	Proposed	T-count, CNOT-count, Width	12n - 4	8n + 2	14n - 4	2n + 2	32n - 12	22n - 3
n > 3	[36] ¹	N/A	35n - 21	N/A	35n - 21	2n + 5	80n - 48	N/A
11 / 3	[37] ²	N/A	35n - 21	9n + 3	35n - 21	4n	80n - 48	27n + 9
	Less-than 4 + TOF $_{\rm Not}^{n+1}$ [21] 3	N/A	16n - 12	10n - 8	20n - 19	2n + 2	46n - 37	N/A
	Less-than 5 + TOF $_{\rm Not}^{n+1}$ [21] 3	N/A	16n - 12	12n - 8	18n - 18	2n + 2	44n - 36	N/A

¹ is the design by Yuan et al. in 2020 [36];

⁵ is the less-than comparator proposed in this article with primary optimization goals {T-count, CNOT-count, width}.

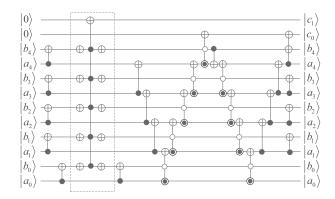


FIGURE 21. Circuit of the 5-b full comparator by a straightforward implementation method. The gate TOF⁶_{Not} in the dashed box is realized by Maslov's method.

which cannot be directly compared with the T-count. In addition, the two MCT gates use n-2 ancillae $|00...0\rangle$ at least. When TOF_{Not}^n is used to implement an equality comparator, the ancillae $|00...0\rangle$ will increase the circuit width. While the ancillae $|xx...x\rangle$ can store an operand, they do not increase the circuit width of the equality comparator (see Fig. 13). It is an advantage for the TOF_{Not}^n using the ancillae $|xx...x\rangle$.

Results presented in Table 6 for n=4,5,6,11 reveal that the proposed methods and Maslov's approach have the advantage over other works without quantum measurements. The proposed ${\rm TOF}_{\rm Not}^n$ for primary optimization goals {T-count, T-depth}, i.e., ${}^1{\rm TOF}_{\rm Not}^{n+1}$, produces 50% T-depth reductions than Maslov's approach. However, Maslov's method uses fewer CNOT gates. The proposed ${}^2{\rm TOF}_{\rm Not}^{n+1}$ for primary optimization goals { T-count, CNOT-count} has the same T-count, CNOT-count, and ancillae as Maslov's work, but

 $^{2}\text{TOF}_{\text{Not}}^{n+1}$ is more suitable for designing a full comparator than Maslov's work (see Table 8).

B. COMPARISON ANALYSIS OF COMPARATORS

Considering {T-count, T-depth, width } and { T-count, CNOTcount, width } as primary optimization goals, we summarize the results of the proposed less-than comparators in Table 7 and compare them with existing works [21], [27], [38]. The proposed less-than comparators keep the minimum width, which is one of the advantages of our previous works [27], [38]. Furthermore, the proposed less-than comparators have less CNOT-count than the comparators presented in [27] and [38]. Specifically, compared with the work in [38], the proposed less-than comparator with primary optimization goals { T-count, CNOT-count, width} reduces approximately the CNOT-count by 28%. Orts's first comparator has a T-count of 4n, a T-depth of 2n, a width of 3n, and an M-count of n, where M-count denotes the number of quantum measurements [21]. Therefore, the proposed comparators reduce the width by 33%. As a result, Orts's first comparator has the best T-count. However, Orts's first comparator uses n quantum measurements. Thus it is not directly comparable with T-count. Similarly, Orts's second comparator has the best option with a T-depth of log(n) and the worst options with a width of $6n - 2W(n) - 2\log(n)$ and an M-count of 3n.

Comparing the proposed full comparator with two n-bit full comparators in [36] and [37], we give results in Table 8. The two full comparators in [36] and [37] consist of 5n-3 Toffoli gates. Therefore, the two n-bit full comparators in [36] and [37] have T-count 35n-21 by the Clifford+T circuit for the Toffoli gate in Fig. 1. Though the detailed circuit of the full comparator was not given in [36],

² is the design by Oliveira et al. in 2007 [37];

³ is the design by Maslov in 2016 [25];

⁴ is the less-than comparator proposed in this article with primary optimization goals {T-count, T-depth, width};

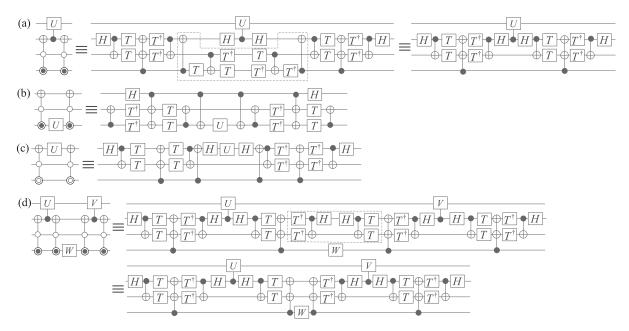


FIGURE 22. Optimization rules for pairs of LI gates showing (a) rule 1, (b) rule 2, (c) rule 3, and (d) rule 4.

we conclude that the T-depth of the n-bit full comparator should be greater than 9n+3 by observing the 3-b full comparator. The results in Table 8 show that the proposed full comparator for primary optimization goals {T-count, T-depth, width} produces approximately 55% T-depth and 66% T-count reductions relative to the existing works in [36] and [37]. Furthermore, compared with the results in [36] and [37], the proposed full comparator for primary optimization goals {T-count, CNOT-count, width} reduces approximately the CNOT-count by 60%.

A straightforward implementation method for a full comparator is the combination of a less-than comparator and an MCT gate. Therefore, a full comparator can be realized by the proposed less-than comparator + TOF_{Not}^{n+1} in [25]. A 5-b example is presented in Fig. 21. Table 8 reveals that the proposed TOF_{Not}^n is convenient for building a full comparator. That is, we only add four LI2 gates and some CNOT gates on the gate TOF_{Not}^{n+1} to create an n-bit full comparator. It results in the proposed full comparators being superior to earlier works in Table 8.

VII. CONCLUSION

This article has proposed four 3-bit Hermitian gates labeled as LI gates, whose implementation circuits have fewer CNOT gates. Then, the equality, less-than, and full comparators are designed by LI gates. These comparators have the minimum circuit width. Two approaches for primary optimization goals {T-count, T-depth} and {T-count, CNOT-count} have been proposed to optimize MCT gates. Furthermore, we have illustrated that the proposed method for primary optimization goals {T-count, T-depth} produces 50% T-depth reductions than the best-known implementation of the MCT

gate without quantum measurements. Selecting {T-count, T-depth, width} and {T-count, CNOT-count, width} as primary optimization goals, we have designed the Clifford+T circuits of the proposed comparators by using the optimized circuits of the MCT gate. Comparison results showed that the proposed comparators have an overall advantage over the known comparators without quantum measurements for T-count, T-depth, CNOT-count, and circuit width.

Some algorithms have been proposed for NISQ devices [40], [41]. For instance, a quantum convolutional neural network (QCNN) on NISQ devices is implemented by multiple control gates [41]. Future works will extend and apply the proposed MCT gate decomposition methods and comparators to realize and optimize QCNN on NISQ devices.

APPENDIX A

TWO OPTIMIZATION METHODS OF THE MCT GATE

Because the T and CNOT gates are more difficult to implement than other Clifford gates [20], [21], [22], two optimization methods of the MCT gate are proposed for different primary optimization goals. Rules of the first optimization method are built by the primary optimization goals {T-count, T-depth}. The second optimization method adopts the primary optimization goals {T-count, CNOT-count}.

A. RULES OF THE FIRST OPTIMIZATION METHOD FOR THE MCT GATE

The optimizing rules for pairs of LI gates are presented in Fig. 22, where U, V, and W are the combination of LI gates and Clifford gates. Then, eliminating the gates in the dashed boxes in Fig. 22(a), we give rules 1 and 2, respectively.

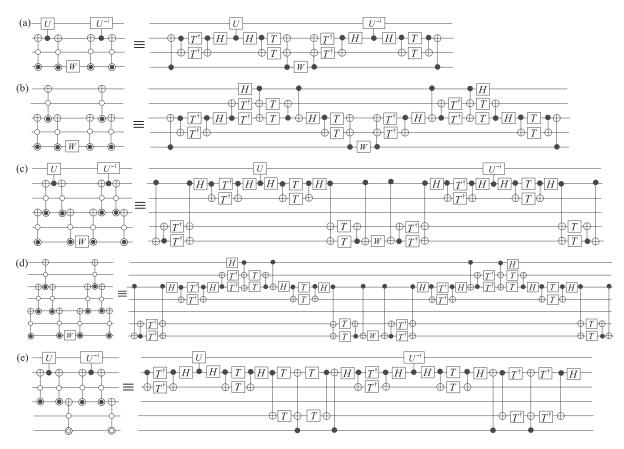


FIGURE 23. Optimization rules for TOF_{Not}^n showing (a) rule 5, (b) rule 6, (c) rule 7, (d) rule 8, and (e) rule 9.

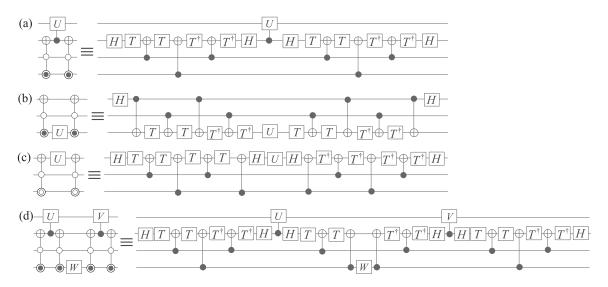


FIGURE 24. Alternative optimization rules for pairs of LI gates showing (a) rule n1, (b) rule n2, (c) rule n3, and (d) rule n4.

When the unitary gate V is the inverse of U, i.e., $V = U^{-1}$, rule 4 can be simplified into rule 5 in Fig. 23(a). Then, combining rules 2, 3, and 4, we present other rules for TOF_{Not}^n in Fig. 23.

B. RULES OF THE SECOND OPTIMIZATION METHOD FOR THE MCT GATE

The primary purpose of the MCT decomposition is to optimize T-count and CNOT-count. Therefore, the optimization

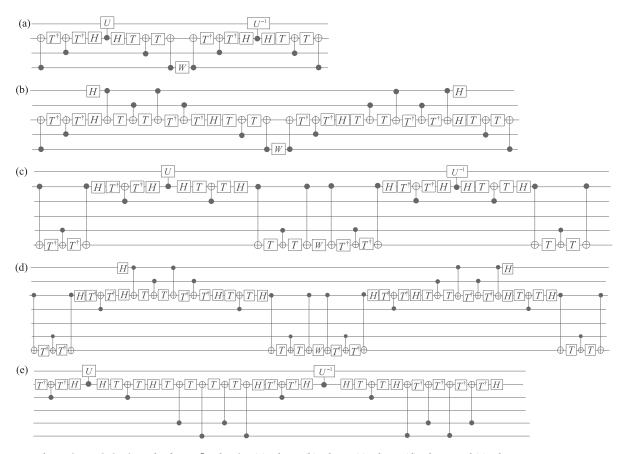


FIGURE 25. Alternative optimization rules for TOF_{Not} showing (a) rule n5, (b) rule n6, (c) rule n7, (d) rule n8, and (e) rule n9.

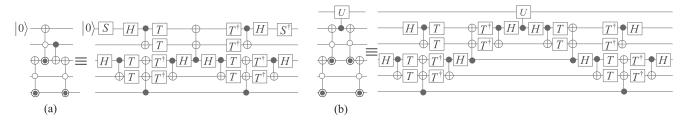


FIGURE 26. Optimization rules for the less-than comparator showing (a) rule 10 and (b) rule 11.

rules in Figs. 22 and 23 are modified into rules in Figs. 24 and 25.

APPENDIX B OPTIMIZATION RULES FOR COMPARATORS

In this section, the optimization rules for comparators are given by primary optimization goals {T-count, T-depth, width} and {T-count, CNOT-count, width}.

A. OPTIMIZATION RULES FOR THE LESS-THAN COMPARATOR

Using rule 1 in Fig. 22 and primary optimization goals {T-count, T-depth, width }, we provide optimization

rules 10 and 11 for the less-than comparator in Fig. 26. When primary optimization goals { T-count, CNOT-count, width} are adopted, optimization rules 10 and 11 are modified into the corresponding rules n10 and n11 in Fig. 27.

B. OPTIMIZATION RULES FOR THE FULL COMPARATOR

Using rules in Fig. 22, we propose rules 12, 13, and 14 for primary optimization goals {T-count, T-depth, width} in Fig. 28. The corresponding rules n12, n13, and n14 for primary optimization goals {T-count, CNOT-count, width} are presented in Fig. 29.

FIGURE 27. Alternative optimization rules for the less-than comparator showing (a) rule n10 and (b) rule n11.

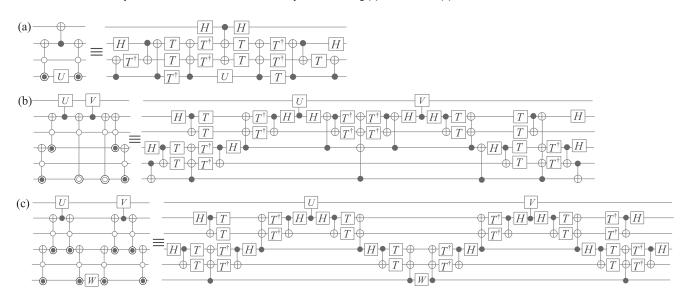


FIGURE 28. Optimization rules for the full comparator showing (a) rule 12, (b) rule 13, and (c) rule 14.

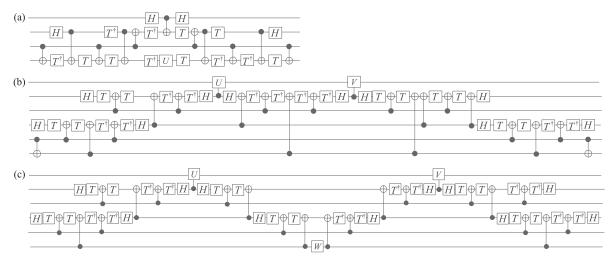


FIGURE 29. Alternative optimization rules for the full comparator showing (a) rule n12, (b) rule n13, and (c) rule n14.

REFERENCES

- [1] P. W. Shor, "Algorithms for quantum computation: Discrete logarithms and factoring," in *Proc. IEEE 35th Annu. Symp. Found. Comput. Sci.*, 1994, pp. 124–134, doi: 10.1109/SFCS.1994.365700.
- [2] L. Grover, "A fast quantum mechanical algorithm for database search," in *Proc. 28th Annu. ACM Symp. Theory Comput.*, 1996, pp. 212–219, doi: 10.1145/237814.237866.
- [3] T. D. Ladd et al., "Quantum computers," *Nature*, vol. 464, pp. 45–53, 2010, doi: 10.1038/nature08812.
- [4] M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information. Cambridge, U.K.: Cambridge Univ. Press, 2000, doi: 10.1017/CBO9780511976667.
- [5] A. Barenco, A. Ekert, K. A. Suominen, and P. Torma, "Approximate quantum fourier transform and decoherence," *Phys. Rev. A*, vol. 5, no. 4, 1996, Art. no. 139, doi: 10.1103/PhysRevA.54.139.
- [6] H. S. Li et al., "The quantum fourier transform based on quantum vision representation," *Quantum Inf. Process.*, vol. 17, no. 12, 2018, Art. no. 333, doi: 10.1007/s11128-018-2096-2.



- [7] M. Terraneo and D. L. Shepelyansky, "Imperfection effects for multiple applications of the quantum wavelet transform," *Phys. Rev. Lett.*, vol. 90, no. 25, 2003, Art. no. 257902, doi: 10.1103/PhysRevLett.90.257902.
- [8] H. S. Li, P. Fan, H. Peng, S. Song, and G.-L. Long, "Multilevel 2-D quantum wavelet transforms," *IEEE Trans. Cybern.*, vol. 52, no. 8, pp. 8467–8480, Aug. 2022, doi: 10.1109/TCYB.2021.3049509.
- [9] P. Q. Le, F. Dong, and K. Hirota, "A flexible representation of quantum images for polynomial preparation, image compression, and processing operations," *Quantum Inf. Process.*, vol. 10, pp. 63–84, 2011, doi: 10.1007/s11128-010-0177-y.
- [10] Y. Zhang, K. Lu, Y. Gao, and M. Wang, "NEQR: A novel enhanced quantum representation of digital images," *Quantum Inf. Process.*, vol. 12, no. 8, pp. 2283–2860, 2013, doi: 10.1007/s11128-013-0567-z.
- [11] H. S. Li et al., "Multidimensional color image storage, retrieval, and compression based on quantum amplitudes and phases," *Inf. Sci.*, vol. 273, pp. 212–232, 2014, doi: 10.1016/j.ins.2014.03.035.
- [12] F. Yan, A. M. Iliyasu, Y. Guo, and H. Yang, "Flexible representation and manipulation of audio signals on quantum computers," *Theor. Comput. Sci.*, vol. 752, pp. 71–85, 2018, doi: 10.1016/j.tcs.2017.12.025.
- [13] H. S. Li, P. Fan, H.-Y. Xia, H. Peng, and S. Song, "Quantum implementation circuits of quantum signal representation and type conversion," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 66, no. 1, pp. 341–354, Jan. 2019, doi: 10.1109/TCSI.2018.2853655.
- [14] B. Hu et al., "A theoretical framework for quantum image representation and data loading scheme," Sci. China. Inf. Sci., vol. 57, 2014, Art. no. 032108, doi: 10.1007/s11432-013-4866-x.
- [15] Y. Liu, G. L. Long, and Y. Sun, "Analytic one-bit and CNOT gate constructions of general N-qubit controlled gates," *Int. J. Quantum Inf.*, vol. 06, no. 3, pp. 447–462, 2008, doi: 10.1142/S0219749908003621.
- [16] A. Barenco et al., "Elementary gates for quantum computation," *Phys. Rev. A*, vol. 52, pp. 3457–3467, 1995, doi: 10.1103/PhysRevA.52.3457.
- [17] X. Zhou, D. W. Leung, and I. L. Chuang, "Methodology for quantum logic gate construction," *Phys. Rev. A*, vol. 62, no. 5, 2000, Art. no. 052316, doi: 10.1103/PhysRevA.62.052316.
- [18] B. Giles and P. Selinger, "Exact synthesis of multiqubit clifford T. circuits," *Phys. Rev. A*, vol. 87, no. 3, 2013, Art. no. 032332, doi: 10.1103/PhysRevA.87.032332.
- [19] V. Kliuchnikov, D. Maslov, and M. Mosca, "Asymptotically optimal approximation of single qubit unitaries by clifford and T. circuits using a constant number of ancillary qubits," *Phys. Rev. Lett.*, vol. 110, no. 19, 2013, Art. no. 190502, doi: 10.1103/PhysRevLett.110.190502.
- [20] E. Munoz-Coreas and H. Thapliyal, "Quantum circuit design of a T-count optimized integer multiplier," *IEEE Trans. Comput.*, vol. 168, no. 5, pp. 729–739, May 2019, doi: 10.1109/TC.2018.2882774.
- [21] F. Orts et al., "Optimal fault-tolerant quantum comparators for image binarization," J. Supercomput., vol. 77, no. 8, pp. 8433–8444, 2021, doi: 10.1007/s11227-020-03576-5.
- [22] M. Amy, D. Maslov, and M. Mosca, "Polynomial-time t-depth optimization of clifford t. circuits via matroid partitioning," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 33, no. 10, pp. 1476–1489, Oct. 2014, doi: 10.1109/TCAD.2014.2341953.
- [23] Y. Nam et al., "Automated optimization of large quantum circuits with continuous parameters," NPJ Quantum Inf., vol. 4, 2018. Art. no. 23, doi: 10.1038/s41534-018-0072-4.
- [24] H. Thapliyal and N. Ranganathan, "Design of efficient reversible binary subtractors based on a new reversible gate," in *Proc. IEEE Comput. Soc. Annu. Symp.*, Tampa, FL, USA, 2009, pp. 229–234, doi: 10.1109/ISVLSI.2009.49.
- [25] D. Maslov, "Advantages of using relative-phase Toffoli gates with an application to multiple control Toffoli optimization," *Phys. Rev. A*, vol. 93, no. 2, 2016, Art. no. 022311, doi: 10.1103/PhysRevA.93.022311.

- [26] M. Amy, D. Maslov, M. Mosca, and M. Roetteler, "A meet-in-the-middle algorithm for fast synthesis of depth-optimal quantum circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 32, no. 6, pp. 818–830, Jun. 2013, doi: 10.1109/TCAD.2013.2244643.
- [27] H. S. Li et al., "Efficient quantum arithmetic operation circuits for quantum image processing," Sci. China-Phys. Mech. Astron., vol. 63, no. 8, 2020. Art. no. 280311, doi: 10.1007/s11433-020-1582-8.
- [28] P. Selinger, "Quantum circuits of T-depth one," Phys. Rev. A, vol. 87, 2013. Art. no. 042302, doi: 10.1103/PhysRevA.87.042302.
- [29] C. Jones, "Low-overhead constructions for the fault-tolerant Toffoli gate," Phys. Rev. A, vol. 87, no. 2, 2013. Art. no. 022328, doi: 10.1103/Phys-RevA.87.022328.
- [30] Y. He et al., "decompositions of N-qubit Toffoli gates with linear circuit complexity," *Int. J. Theor. Phys.*, vol. 56, no. 7, pp. 2350–2361, 2017, doi: 10.1007/s10773-017-3389-4.
- [31] P. Niemann, A. A. A. de Almeida, G. Dueck, and R. Drechsler, "Design space exploration in the mapping of reversible circuits to IBM quantum computers," in *Proc. 23rd Euromicro Conf. Digit. Syst. Des.*, 2020, pp. 401–407, doi: 10.1109/DSD51259.2020.00070.
- [32] P. Gokhale et al., "Asymptotic improvements to quantum circuits via qutrits," in *Proc. 46th Int. Symp. Comput. Architecture*, 2019, pp. 554–566, doi: 10.1145/3307650.3322253.
- [33] J. Wang, N. Jiang, and L. Wang, "Quantum image translation," *Quantum Inf. Process.*, vol. 14, pp. 1589–1604, 2015, doi: 10.1007/s11128-014-0843-6.
- [34] P. Li and X. Liu, "Bilinear interpolation method for quantum images based on quantum Fourier transform," *Int. J. Quantum Inf.*, vol. 6, no. 4, 2018, Art. no. 1850031, doi: 10.1142/S0219749918500314.
- [35] H. Y. Xia et al., "Novel multi-bit quantum comparators and their application in image binarization," *Quantum Inf. Process.*, vol. 18, no. 7, 2019, Art. no. 229, doi: 10.1007/s11128-019-2334-2.
- [36] S. Yuan, C. Wen, B. Hang, and Y. Gong, "The dual-threshold quantum image segmentation algorithm and its simulation," *Quantum Inf. Process.*, vol. 19, 2020, Art. no. 425, doi: 10.1007/s11128-020-02932-x.
- [37] D. S. Oliveira and R. V. Ramos, "Quantum bit string comparator: Circuits and applications," *Quantum Comput. Comput.*, vol. 7, no. 1, pp. 17–26, 2007.
- [38] H. S. Li, P. Fan, H. Xia, and G. L. Long, "The circuit design and optimization of quantum multiplier and divider," Sci. China-Phys. Mech. Astron., vol. 65, no. 6, 2022. Art. no. 260311, doi: 10.1007/s11433-021-1874-2.
- [39] M. H. Yung et al., "From transistor to trapped-ion computers for quantum chemistry," Sci. Rep., vol. 4, 2014, Art. no. 3589, doi: 10.1038/srep03589.
- [40] J. Wen, D. Lv, M. H. Yung, and G. L. Long, "Variational quantum packaged deflation for arbitrary excited states," *Quantum Eng.*, vol. 3, no. 4, 2021, Art. no. e80, doi: 10.1002/que2.80.
- [41] S. Wei, Y. Chen, Z. Zhou, and G. Long, "A quantum convolutional neural network on NISQ devices," *AAPPS Bull.*, vol. 32, 2022, Art. no. 2, doi: 10.1007/s43673-021-00030-3.



Hai-Sheng Li (Member, IEEE) received the M.S. degree in computer science from Chongqing University, Chongqing, China, in 2004 and the Ph.D. degree in computer science from the University of Electronic Science and Technology of China, Chengdu, China, in 2014.

He is currently a Professor with Guangxi Normal University, Guilin, China. His research interests include quantum information processing, quantum neural network, image processing, etc.