Data Sheet
NVIDIA Tegra K1 Series Processors
with Kepler Mobile GPU for Embedded Applications

Description

The NVIDIA® Tegra® K1 series application processor is a revolutionary step in the world of mobile and embedded computing. Tegra K1 processors integrate a power optimized version of the same Kepler GPU architecture that powers the highest performing graphics cards and systems in the world. As a result, Tegra K1 processors are the first to open up features like OpenGL® 4.4, OpenGL ES 3.1 and CUDA® /GPGPU on mobile and embedded devices. A high performance image processing pipeline coupled to the power optimized Kepler GPU and unique Tegra 4-PLUS-1™ CPU complex provides the foundation that enables visual computing and computational solutions on next generation mobile and embedded devices; including autonomous robotic systems, intelligent video analytics, Advanced Driver Assistance Systems (ADAS) and mobile medical imaging.

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Version 02

Description		Tegra K1 Series Processors *			
		CD575M		CD575MI	
		UCM: 1	UCM: 2	UCM: 1	UCM: 2
Use Case Model (UCM)					
% Operating time per day at max frequency		20%	100%	20%	100%
Operating Temperature Range (T_J) ◊		-25°C – 105°C		-40°C – 105°C	
Operating Lifetime		5 years		10 years	
Kepler Mobile GPU					
OpenGL® 4.4 | OpenGL ES 3.1 | CUDA® | GPGPU					
GPU Shader / Compute Performance	GFLOPS	325	308	325	290
CPU Subsystem					
ARM® Cortex® -A15 MPCore Processor with NEON Technology. Operating Frequency per Core (up to)		2.2GHz	1.9GHz	2.1GHz	1.9GHz
L1 Cache: 32KB L1 instruction cache (I-cache) per core; 32KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB					
Companion (Low Power) CPU: single core implementation of the Cortex-A15 CPU, dedicated 512KB L2 cache, 32KB L1 I-cache, 32KB L1 D-cache					
Memory Subsystem					
Dual Channel | Secure External Memory Access Using TrustZone Technology | System MMU					
Memory Type		2 x 32-bit DDR3L			
Maximum Memory Bus Frequency (up to) †		933MHz	800MHz	933MHz	800MHz
Maximum Capacity		4GB			
HD Video & JPEG Decode ‡					
H.264: Baseline, Main, High, Stereo SEI (half-res)		2160p30 1440p60 1080p120	2160p30 1440p50 1080p60	2160p30 1440p60 1080p60	2160p30 1440p50 1080p60
H.264: Multiple stream		4 x 1080p30	4 x 1080p30	4 x 1080p30	4 x 1080p30
WEBM VP8		2160p30 1080p120	2160p30 1080p60	2160p30 1080p120	2160p30 1080p60
VC-1: Simple, Main, Advanced MPEG-4: Simple MPEG-2 JPEG		1080p48 1080p30 1080 60p/120i 120 MP/sec		1080p48 1080p30 1080 60p/120i 120MP/sec	
HD Video & JPEG Encode ‡					
H.264: Baseline, Main, High, Stereo SEI (half-res) WEBM VP8		2160p24 1440p30 1080p60	2160p20 1440p30 1080p60	2160p24 1440p30 1080p60	2160p20 1440p30 1080p60
VC-1: Advanced MPEG-4: Simple H.263: Profile 0 JPEG		720p30 D1 D1 120 MP/sec		720p30 D1 D1 120 MP/sec	
HD Audio Processor					
HD Audio Support | Sample rate conversion and digital mixer | Audio Format HW Support (decode): AAC-LC, ACC, AAC+, eAAC+, MP3, WAVE, AMR-NB, AMR-WB, OGG Vorbis, WMA10, WMA Lossless, WMA Pro LBR 10, MPEG-2, AC3 | Audio Format HW Support (encode): AAC-LC, AMR-WB, AMR-NB					

Description	Tegra K1 Series Processors *			
	CD575M		CD575MI	
	UCM: 1	UCM: 2	UCM: 1	UCM: 2
Display Controller Subsystem				
Two independent display controllers with support for DSI, HDMI, LVDS and eDP				
Captive Panel ‡				
MIPI-DSI (24bpp; 1.5Gbps/lane): Dual DSI link (2x4) Single DSI link (1x4)	 3200x2000 at 60Hz 2560x1440 at 60Hz	 3200x1800 at 60Hz 2560x1440 at 60Hz	 3200x2000 at 60Hz 2560x1440 at 60Hz	 2560x1920 at 60Hz 2560x1440 at 60Hz
eDP 1.4 (24bpp; HBR2, 5.4Gbps per lane): Single link (1x4)	 3200x2000 at 60Hz	 3200x1800 at 60Hz	 3200x2000 at 60Hz	 2560x1920 at 60Hz
LVDS (24bpp; 165MHz): Single channel, 5 lanes (4 data + clock)	 1920x1200 at 60Hz			
External Panel ‡				
HDMI 1.4b	3840x2160 at 30Hz 4096x2160 at 24Hz			
Imaging System				
Up to 14bpp RAW sensor input | Dual ISP up to 1200MP/s | Video capture up to 20MP at 30fps.				
MIPI CSI 2.0	2x4 lane + 1x1 Lane at 1.5Gbps per lane			
Clocks				
System clock: 12 MHz | Sleep clock: 32.768 KHz | Dynamic clock scaling and clock source selection				
Boot Sources				
e.MMC, SPI serial flash, USB (Recovery Mode)				
Security				
Secure memory with video protection region | Hardware cryptographic acceleration for RSA, AES, CMAC, SHA-1, and SHA-256 | 2048-bit RSA HW for PKC secure boot | HW Random number generator (RNG), NIST SP800-90 compliant | TrustZone technology support for DRAM and peripherals				
Storage Interfaces				
4 x SD/MMC controllers (supporting e.MMC 4.51, SD 4.0, SDHOST 4.0 and SDIO 3.0) | SATA				
Peripheral Interfaces				
XHCI host controller with integrated PHY: 2 x USB 3.0 interfaces, 3 x USB 2.0 interfaces, 2 x HSIC | USB 2.0 device controller with integrated PHY | 4 x High-speed UART interfaces | 2 x SPI interfaces | 6 x I^2C controllers | 4 x I2S interfaces: support I^2S, RJM, LJM, PCM, TDM (multi-slot mode), S/PDIF (Sony/Philips Digital Interface) | PWM Controllers (4 channels and up to 8 bits) | 1 x DTV | 5-lane PCIe: x1, x2, x4 configurations | SATA				
Baseband Interfaces				
HSIC, HS-UART, PCM support, SPI (master), USB, SDIO				
Package & Process				
23 x 23 mm (813 Ball) | 0.7mm BP | FCBGA | 1.55mm Max Z-height				
Process: 28nm TSMC | HF and RoHS Compliant				
Applications				
Embedded (Intelligent Video Analytics, Drones, Robotics, etc.), Automotive, Clamshells, Gaming, Internet TV, Tablets, and more				

* Refer to the software release feature list for current software support.

◊ T_J = Die Junction Temperature

† Dependent on board layout; refer to design guide for layout guidelines

‡ Maximum resolution (up to); refer to the software release feature list for current software support.

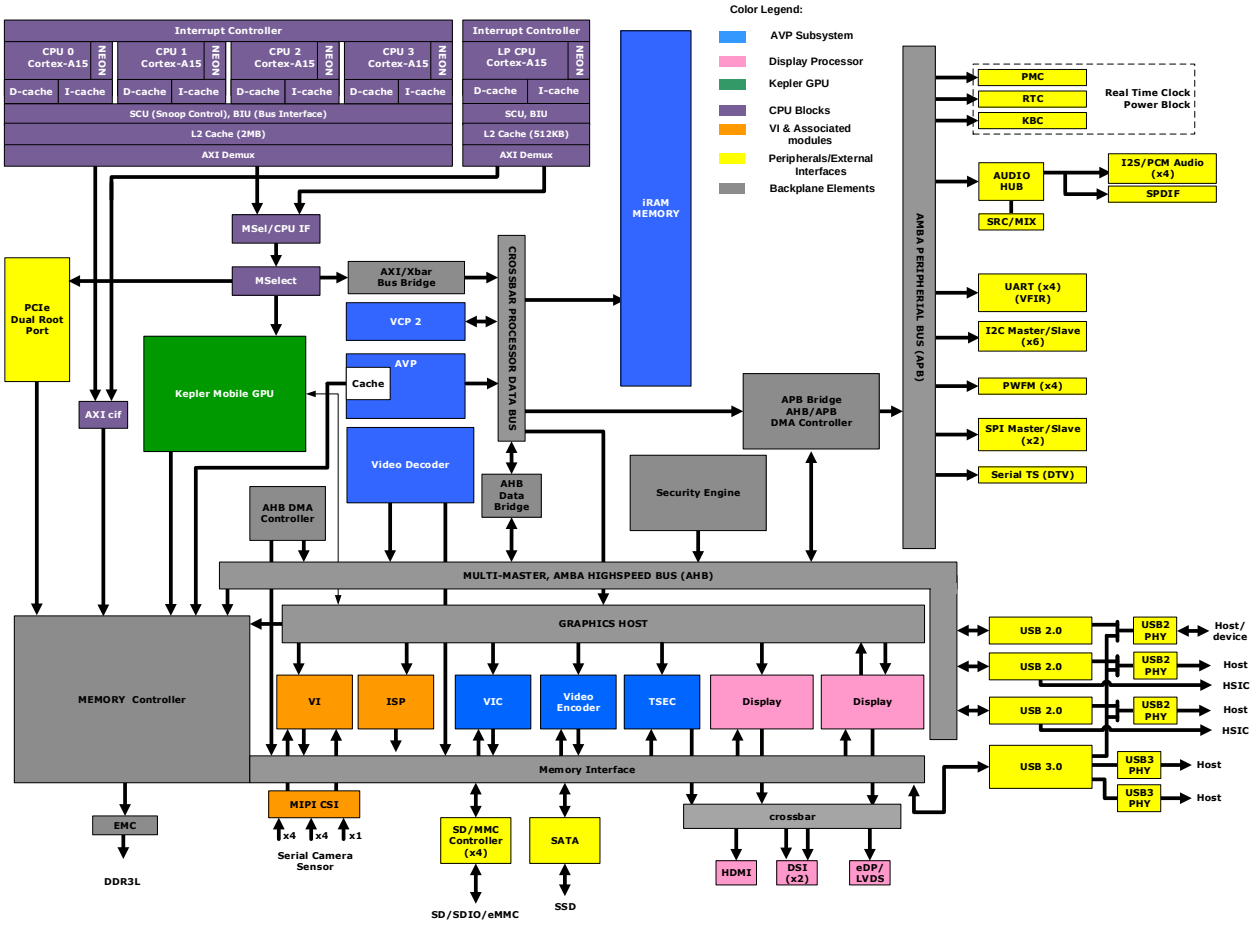
Table of Contents

1.0 Overview

The Tegra K1 series 4-PLUS-1™ quad-core processor is a full-featured applications processor. This section provides a brief overview of the processing blocks listed below. Description of peripheral interfaces can be found in the *Interface and Signal Descriptions* section:

- CPU Complex
- High-Definition Audio-Video Subsystem
- Kepler Mobile GPU
- Image Signal Processor (ISP)
- Display Controller Complex
- Security Controller

Figure 1 Block Diagram



1.1 CPU Complex

The CPU complex is comprised of two CPU clusters used in a mutually exclusive switch-model (only one cluster is active at a time).

- **Cluster0** is a high performance Multi-Core SMP cluster of four Cortex-A15 CPUs with 2MB of L2 cache. It also has an SCU, an interrupt controller (vGIC), timers (including generic timers), and interfaces to the Memory Controller, MSelect and CoreSight.

- **Cluster1** is a low power (low leakage) single core implementation of the Cortex-A15 CPU. It also provides an SCU, 512KB of L2 cache, vGIC, timers (including generic timers), and interfaces to the Memory Controller, MSelect and CoreSight.

The Tegra CPU Complex features:

- ARM® Cortex® -A15 MPCore (Quad-Core) Processor with NEON Technology
  - Triple-Issue pipeline
  - Branch prediction
  - Memory parallelism and prefetch
  - Out-of-order processing
  - Tightly integrated NEON and VFP
  - 15 stage integer pipeline
  - ARM hardware virtualization support
- 2MB L2 cache (16-way) with 4-way address banking
- 32Kbyte I-cache and 32Kbyte D-cache for each core
- CPU complex on a separate, independently controlled, power rail
  - Each CPU core and L2 can be independently power-gated if idle
  - Power to the entire Quad-CPU complex can be removed in low-power use-cases when companion core is used
- Ultra Low Power (ULP) single core CPU operating mode for low compute workloads (Companion Core)
  - 600Mhz crossover to fast quad-core complex
  - Dedicated 512KB companion L2 cache
  - Companion core and companion L2 can be power-gated if no CPU activity is needed

Both CPU clusters interface to the MSelect FIFO via an AXI interface to decouple I/O traffic. MSelect allows an AXI master device to send traffic to the peripheral buses based on transaction address. The AXI/Xbar bridge enables early response on write transfers and full hardware hazard resolution to permit the maximum transaction throughput to MMIO.

1.1.1 Snoop Control Unit and L2 Cache

Each CPU cluster includes an integrated snoop control unit (SCU) and a tightly coupled L2 cache. The L2 cache also provides a 128-bit AXI master interface to access DRAM. L2 cache features include:

- 2MB L2 for cluster0, 512KB for cluster1

  NOTE: L2 cache does not include ECC support
  The L2 cache in each cluster is *not* coherent with the L2 cache of other cluster.
- Fixed line length of 64 bytes
- 16-way set-associative cache structure (cluster0 and cluster1)
- Strictly enforced inclusion property with L1 data caches
- Duplicate copies of the L1 data cache directories for coherency support

1.1.2 Performance Monitoring

The performance monitoring unit (part of MPCore non-CPU logic) provides six counters, each of which can count any of the events in the processor. The unit gathers various statistics on the operation of the processor and memory system during runtime, based on ARM PMUv2 architecture.

1.2 High-Definition Audio-Video Subsystem

The audio-video subsystem off-loads audio and video processing activities from the CPU subsystem resulting in faster, fully concurrent, highly efficient operation.

1.2.1 Audio-Video Processor (AVP)

The Audio-Video Processor (AVP) is used to:

- Manage the initial stages of boot
- Control and assist the hardware audio decoding blocks, BSEA and VCP2
- Control and synchronize the Video Decode Processor (VDE)

It is capable of controlling the system and has access to the entire memory map (except for PCIE and GPU MMIO address aperture, and CPU internal hardware). The AVP has fast access to the IRAM for very low latency and low power code and data accesses. The AVP accesses DRAM either through a 32KB unified cache, or through an un-cached memory aperture.

IRAM and Crossbar Bus

IRAM is configured as four contiguous banks of 64KB of RAM. While the XBAR allows one transaction and one pending transaction at a time for any master or slave; the crossbar bus architecture enables access to each of these banks, so that different crossbar masters could access different banks simultaneously.

The masters on the crossbar bus are:

- AVP
- CPU complex over the AXI bridge
- AHB bus interface

1.2.2 Content Security (TSEC)

A dedicated general purpose hardware accelerator for encryption/decryption operations. Includes on-chip secure memory enabling tamper resistant secure storage and transaction verification.

Features:

- HDCP Link Management
  - HDCP link management without exposing protected content or HDCP keys to SW running on CPU.
  - (Programmable) Ability to disable HDMI output independent of the player if the HDCP status check fails.
- WiFi Alliance Display (WFD) Encryption
  - Requires HDCP 2.0 encryption support
  - Ability to maintain 30 FPS video rate in video pipe
- Blu-Ray/MPEG2-TS playback
  - Decrypt and parse Blu-Ray/MPEG2-TS streams
  - Encrypt video stream using AES and write the encrypted stream to memory.
  - Read/write to the Video Protection Region
- Dedicated Video Protection Region in memory
  - Programmable in the memory controller
  - Extends security controller i-cache and d-cache
  - Only accessible by the Security Controller
  - Minimum size requirements avoid security exposure

1.2.3 Video Decode (VDE)

The video decoder works in conjunction with the AVP to accelerate video decode, supporting low resolution mobile content, and also including Standard Definition (SD), High Definition (HD) and UltraHD (2160p, or “4k” video) profiles. It is also capable of Baseline JPEG decoding and encoding. The video decoder is designed to be extremely power efficient without sacrificing performance.

The video decoder is made up of:

- 6 independent processing modules: Video Bitstream Engine (BSE-V), Syntax Engine (SXE), Transform Engine (TFE), Motion Compensation Engine (MCE), Macroblock Engine (MBE) and the Post-processing Engine (PPE)
- Command Queue and Configuration module
- Video DMA module

The VDE communicates with the memory controller through the video DMA which supports a variety of memory format output options. It also has a fast access to IRAM through the Crossbar interface. For low power operations, the VDE can operate at the lowest possible frequency while maintaining real-time decoding using dynamic frequency scaling techniques; all VDE modules are also capable of active power management and can power down when they are not active.

Video standards supported Include:

- WEBM VP8
- H.264: Main, and High
- H.264: Baseline, Stereo SEI (half-res)
- VC-1: Simple, Main and Advanced
- MPEG-4: Simple
- H.263: Profile 0
- DiVX: 4 / 5 / 6
- XviD Home Theater
- MPEG-2: MP
- JPEG

1.2.4 Multi-Standard Video Encoder

The multi-standard video encoder enables full hardware acceleration of various encoding standards. It performs high quality video encoding operations for mobile applications such as video recording and video conferencing. The encode processor is designed to be extremely power efficient without sacrificing performance.

Video standards supported:

- H.264 Baseline/Main/High Profiles: IDR/I/P/B-frame support
- MVC
- VP8
- MPEG-4 (ME only)
- H.263
- VC1 (ME only): No B frame, no interlaced

Features:

- Support for multi-stream simultaneous encoding, context switch at frame boundary
- Scalable performance (resolution and frame rate) for multi-stream encoding
- Recon Loop (DCT, Q, IDCT, IQ)
- Intra prediction
  - Periodic intra frame insertion (camcorder)
  - Intra mode decision using all sub modes
- De-blocking
- CBR and VBR Rate control
- Entropy coding
- Timestamp for Audio/Video Sync
- Quantization post processing (QPP)

- Error resiliency
  - Bit based / MB based packetization for video telephony
  - Programmable Intra refresh
  - Context save restore
- Video telephony: sequence for eliminating bit rate spikes
- Input surface (90/180/270-degree) rotation and H/V flip
- CABAC and CAVLC conforming to H.264 standard
- MPEG-4 simple profile encoding tools
- MPEG-4 Short video header mode
- Motion estimation (ME) only mode
- Flexible rate control (programmable control processor to do rate control in software)

1.2.5 Video Image Compositor (VIC)

The Video Image Compositor implements various 2D image and video operations in a power-efficient manner. It handles various system UI scaling, blending and rotation operations, video post-processing functions needed during video playback, and advanced de-noising functions used for camera capture.

Features:

- High-quality Deinterlacing
- Inverse Teleciné
- Temporal Noise Reduction
  - High quality video playback
  - Reduces camera sensor noise
- Scaling
- Color Conversion
- Memory Format Conversion
- Blend/Composite
- 2D Bit BLIT operation
- Rotation

1.2.6 Audio Processing

K1 series processors support multiple interfaces to the audio devices in the system: cellular baseband; different audio CODECs; digital audio that is synthesized or decoded by the AVP audio coprocessor or CPU; Bluetooth modules; FM receivers; HDMI audio to a TV or home theater; etc. These applications have different interfaces and requirements for audio signal quality and may use different protocols (e.g., cellular voice is usually at a much lower sample rate than music).

K1 series processors have 3 DAM modules, 4 I2S controllers, a S/PDIF controller, and audio multiplexer (AMX) and de-multiplexer (ADX) blocks. The Audio Hub (AHUB) is a full crossbar switch matrix connecting these modules. Most of AHUB's clients are programmable through APB, while their audio data is exchanged through AHUB. APBIF is the agent for the APB DMA operation, which sends or receives data from/to memory. To process the mixing of audio signals among different audio source, DAMs (Digital Audio Mixers) have been added for audio processing.

1.2.6.1 Vector Coprocessor

Audio processing is centered around the Vector Coprocessor (VCP) audio acceleration module. The VCP module accelerates the inner DSP loops of audio codecs and supports additional audio functionality such as re-sampling, reverberation, FFT computations, and 3D audio. The VCP block incorporates command parsing and DMA control to release the HD AVP from almost any intervention during normal audio playback resulting in highly efficient operation.

Audio formats supported:

- Decode: AAC-LC, ACC, AAC+, eAAC+, WAVE, AMR-WB, AMR-NB, OGG Vorbis, WMA10, WMA Lossless, WMA Pro LBR 10, MP3, MPEG-2, AC3
- Encode: AAC-LC, AMR-WB, AMR-NB

1.2.6.2 Audio Hub

The modules in the audio hub are designed to support various kinds of audio devices that are expected to interface with the application processor such as cellular baseband, different types of audio CODECs, bluetooth modules, A/V receivers, etc. The audio hub is capable of supporting the different interface and signal quality requirements of these devices.

The audio hub (AHUB) is comprised of:

- 5 x I2S controllers and one S/PDIF interface for external peripheral support.
- Audio processing:
  - 3 x Digital Audio Mixers (DAM)
  - 2 x Audio Multiplexers (AMX)
  - 2 x Audio Demultiplexers (ADX)
  - 6 x Audio Flow Controllers (AFC)
- 10 x DMA (APBIF-DMA) channels to communicate with the memory.

1.3 Kepler Mobile GPU

The Kepler Mobile GPU integrated in K1 series processor extends the CUDA™ compute architecture to mobile devices. The Graphics Processing Cluster (GPC) is a dedicated hardware block for rasterization, shading, texturing, and compute; most of the GPU's core graphics functions are performed inside the GPC. Inside the GPC, the Streaming Multiprocessor's (SMX) CUDA cores perform pixel/vertex/geometry shading and physics/compute calculations. Texture units perform texture filtering and load/store units fetch and save data to memory. Special Function Units (SFUs) handle transcendental and graphics interpolation instructions. Finally, the PolyMorph Engine handles vertex fetch, tessellation, viewport transform, attribute setup, and stream output. The SMX geometry and pixel processing performance make it highly suitable for rendering advanced user interfaces and complex gaming applications; the power efficiency of this design enables this performance on mobile devices.

Features:

- OpenGL 4.4, OpenGL ES 3.1 compliant
  - Adaptive Scalable Texture Compression (ATSC)
- DirectX 12 compliant
- CUDA support
- Iterated blend, ROP OpenGL-ES blend modes
- 2D BLIT from 3D class avoids channel switch
- 2D color compression
- Constant color render SM bypass
- 5x MSAA with color and Z compression
- Non-power-of-2 and 3D textures, FP16 texture filtering
- Geometry and Vertex attribute Instancing
- Parallel pixel processing
- Early-z reject: Fast rejection of occluded pixels acts as multiplier on pixel shader and texture performance while saving power and bandwidth
- Video protection region
- Power saving
  - Multiple levels of clock gating for linear scaling of power
  - Automated power throttling

1.4 Image Signal Processor (ISP)

The ISP module takes data from the VI or CSI module in raw Bayer format and processes it to YUV output. The imaging subsystem supports raw (Bayer) image sensors up to 100 million pixels. Advanced image processing is used to convert input to YUV data, and remove artifacts introduced by high-megapixel CMOS sensors, camera-phone lens and color-space conversion.

Features:

- Two dedicated 14bpp RAW to YUV processing engine, up to 600Mpix/s each.
- Flexible post-processing architecture for supporting high speed burst and negative shutter lag
- Spatially varying Noise Reduction, face detection, AOHDR
- Data crossbar with configuration options to suit multiple algorithms
- Per-channel black-level compensation
- High-order lens-shading compensation
- 3x3 color transform
- 16x digital gain for very high ISO support (>ISO 3200)
- Bad pixel correction
- Programmable coefficients for 9x9 de-mosaic with color artifact reduction
  Color Artifact Reduction: a two-level (horizontal and vertical) low-pass filtering scheme that is used to reduce/remove any color artifacts that may result from Bayer signal processing and the effects of sampling an image.
- Enhanced down scaling quality
- Luma enhancement
  Programmable edge filter enables manipulation of edge width, edge strength, low and high limits of the edge value.
- Color and gamma correction
  Enables the ability to manipulate each pixel's data bit at the output of the gamma correction block.
- Color-space conversion (RGB to YUV)
- Image statistics gathering (per-channel)
  - Two 256-bin image histograms
  - Up to 4,096 local region averages
  - Global average, plus count of min. and max. value pixels
  - AC flicker detection (50 Hz and 60 Hz)
  - Focus metric block

1.5 Display Controller Complex

The Tegra Display Controller Complex integrates two independent display controllers. Each display controller is capable of interfacing to an external display device. Each controller supports a cursor and three windows (Window A, B, and C); controller A supports two additional simple windows (Window D,T). The display controller reads rendered graphics or video frame buffers in memory, blends them and sends them to the display.

Features:

- Two independent display controllers
  - Each controller can drive same or different display contents to different resolutions and refresh rates
  - Supports combinations of any two DSI, HDMI or eDP/LVDS
  - Video mirroring
- 90, 180, 270-degree image transformation uses both horizontal and vertical flips (controller A only)
- Byte-swapping options on 16-bit and 32-bit boundary for all color depths
- NVIDIA Pixel Rendering Intensity and Saturation Management™ (PRISM)
- 256x256 cursor size
- Color Management Unit to enhance color accuracy (compensate for the color error specific to the display panel being used)
- Scaling and tiling in HW for lower power operation
- Full color alpha-blending
- Interlaced input/output
- Captive panels
  - Secure window (Win T) for TrustZone
  - Supports cursor and up to four windows (Win A, B, C and D)
  - 2x4-lane MIPI DSI (supports a single Hi-Res panel in 2x4 ganged mode, or 2 separate x4 DSI panels). 2x4 can support left-right, odd-even split configurations.
  - Supports MIPI D-PHY rates up to 1.5Gbps
  - 4-lane (single-link) LVDS
  - 4-lane eDP with AUX channel
  - Independent resolution and pixel clock
  - Supports display rotation and scaling in HW
- External panels
  - Supports cursor and three windows (Window A, B, and C)
  - 1x HDMI supporting resolutions up to 4k x 2k @ 30 Hz or 1080p @ 60 3D
  - HDCP and audio
  - Supports display scaling in HW

1.6 Memory Controller

The Tegra Memory Controller (MC) maximizes memory utilization while providing minimum latency access for critical CPU requests. An arbiter is used to prioritize requests, optimizing memory access efficiency and utilization and minimizing system power consumption. The MC provides access to main memory for all internal devices. It provides an abstract view of memory to its clients via standardized interfaces, allowing the clients to ignore details of the memory hierarchy. It optimizes access to shared memory resources, balancing latency and efficiency to provide best system performance, based on programmable parameters.

Features:

- TrustZone (TZ) Secure and OS-protection regions
- System Memory Management Unit
- Dual CKE signals for dynamic power down per device
- Support for two DRAM ranks of unequal device densities
- Dynamic Entry/Exit from Self -Refresh and Power Down states

The Tegra MC is able to sustain high utilization over a very diverse mix of requests. For example, the MC is prioritized for bandwidth (BW) over latency for all multimedia blocks (the multimedia blocks have been architected to prefetch and pipeline their operations to increase latency tolerance); this enables the MC to optimize performance by coalescing, reordering, and grouping requests to minimize memory power. DRAM also has modes for saving power when it is either not being used, or during periods of specific types of use.

1.7 Security Engine

A dedicated platform security engine supports secure boot using AES or PKC, incorporates an SP800-90 complaint random number generator (RNG) including built in ring oscillator based entropy source used to seed a deterministic random bit generator (DRBG), and a protected memory aperture for video use cases.

Features:

- Streaming memory-to-memory and on-the-fly (OTF) AES decryption
  - Modes: ECB, CBC, OFB, CTR
  - Hash: CMAC
- Secure boot
  - AES: Boot configuration table (BCT) and Boot Loader (BL) are decrypted/authenticated/loaded into memory; Boot ROM locks down security features and clears out state; BL write protects mass storage location of BL and OS
  - PKC: Boot ROM performs 2048-bit RSA signature verification; once the public key stored in mass storage is validated, the key is used to verify the BCT/BL hash.
- Secure memory
  - Secure ROM: regions locked before control given to BL
  - Secure RAM (TZRAM): Security controlled by Secure OS (TZ) Tasks
  - Secure DRAM access
  - Video Protection Region: MC dynamically configures memory region that can only be accessed by video/display HW engines.
- AES key slot protection
  - Protection scheme associated with each key slot defines Read/Write permissions
  - Configure key slots so that they can only be accessed in TZ mode
  - Individual key slots can be set so they can only be used for AES operations by TZ processes
  - Valid AES decryption destination
- TZ Secured Peripheral Bus
- HW Hashing & Authentication: AES CMAC, SHA1, SHA2

2.0 Power and System Management

Tegra processors utilize various means to provide an efficient power management solution for a complex environment:

- **Power Management Controller (PMC)**: Provides an interface to an external power manager IC or PMU. The PMC primarily controls voltage transitions for the Tegra processor as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I2C, RTC, USB attach) which can wake the Tegra processor from a deep sleep state.
- **Power Gating:** Tegra processor aggressively employs power-gating (controlled by PMC) to power-off modules which are idle. CPU cores are on a separate power rail to allow complete removal of power and eliminate leakage. Each CPU can be power gated independently. Software provides context save/restore to/from DRAM.
- **Clock Gating:** Used to further reduce unnecessary power consumption where power gating is not an option.
- **Dynamic Voltage and Frequency Scaling (DVFS):** Raises voltages and clock frequencies when demand requires, Lowers them when less is sufficient, and removes them when none is needed. DVFS is used to change the voltage and frequencies on the following rails: VDD_CPU, VDD_CORE, VDD_GPU and VDD_RTC.
- **Real Time Clock (RTC):** The RTC Always On partition logic of the CPU Complex is not power gated and can wake the system based on either a timer event or an external trigger (e.g., key press).

Figure 2 System Power State Transitions

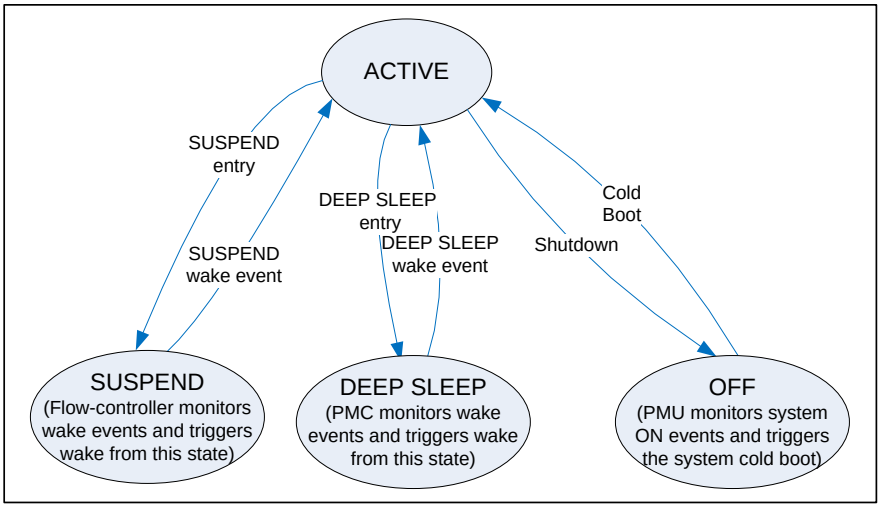


Table 1 System Power States

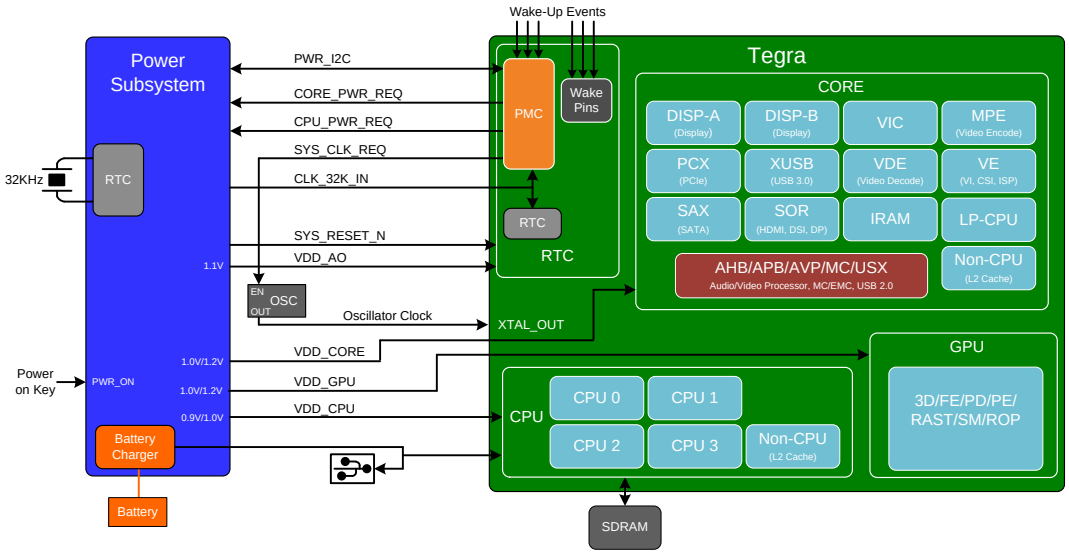
Name	Description
ACTIVE	▪ System is running under DVFS control ▪ CPU, Devices, and System clocks are dynamically scaled and halted ▪ Full functionality available
SUSPEND (LP1)	▪ Inactivity timeout, no CPU process needed, no devices are active ▪ OS is suspended ▪ DRAM is in self-refresh ▪ CPU power rail is OFF. ▪ All power-gate-able blocks under the CORE rail are power-gated (including LP-CPU) ▪ Wake events (incl. interrupts) are possible ▪ Some Tegra devices may be available, but at extremely low performance

Name	Description
DEEP SLEEP (LP0)	▪ Inactivity timeout, no CPU process needed, no devices are active ▪ OS is suspended ▪ DRAM is in self-refresh ▪ CPU, GPU and CORE power rails are OFF ▪ PMC, RTC and KBC functionality available. ▪ Wake events (including key press or USB attach) are possible. ▪ PADs are powered off except for PADs which monitor wake events
OFF	▪ Tegra system (incl. DRAM) is completely powered off. ▪ No state is maintained. ▪ No internal wake events possible.

2.1 Power Domains/Islands

Tegra processors are partitioned into power domains and power islands to optimize mobile device battery life by reducing power consumption for various use cases and limiting leakage current.

Figure 3 Power Domains Diagram



K1 series processors have four power domains (RTC/CORE/GPU/CPU); RTC domain is always on, CORE/CPU/GPU domains can be turned on and off. The CPU and CORE power domains contain power-gated islands which are used to power individual modules (as needed) within each domain. The CORE power domain also has a Non-Power-Gated island (NPG) where modules are clock-gated (off) when not used, to further reduce unnecessary power consumption.

Table 1 Power Domains

Power Domain	Power Island in Domain	Modules in Power Island
RTC (VDD_RTC)	N/A	PMC (Power Management Controller)
		KBC (Keyboard Controller)
		RTC (Real Time Clock)
CORE (VDD_CORE)	NPG (Non-Power-Gated)	AHB, APB Bus, AVP, Memory Controller (MC/EMC), USB 2.0
	LP-CPU	Low Power Companion CPU
	Non-CPU	L2 Cache for Low Power CPU

Power Domain	Power Island in Domain	Modules in Power Island
	SAX	SATA
	VE	ISP (image signal processing), VI (video input), CSI
	MPE	Video Encode
	VDE	Video Decode
	PCX	PCIe
	SOR	HDMI, DSI, DP
	IRAM	IRAM
	DISP-A, DISP-B	Display Controllers A and B
	XUSB	USB 3.0 Host Mode
	VIC	Video Image Compositor
GPU (VDD_GPU)	GPU	3D, FE, PD, PE, RAST, SM, ROP
CPU (VDD_CPU)	CPU 0	CPU 0
	CPU 1	CPU 1
	CPU 2	CPU 2
	CPU 3	CPU 3
	Non-CPU	L2 Cache for Main CPU complex (Cluster 0)

2.2 Clocks

2.2.1 Input Clock

The Tegra processor supports a large number of internal functional blocks and external interfaces. To accommodate all clocking requirements, the clock generation (CLKGEN) block requires two external clock sources as input:

- 32KHz external clock: Required by the Real Time Clock (RTC) and Power Management Controller (PMC), typically provided by the Power Management Unit (PMU).
- Oscillator (OSC) clock: This higher frequency reference clock feeds several integrated PLLs that provide a variety of clocking options for the many core and I/O blocks. Two methods of generating the internal Oscillator clock are supported. Normal Oscillation Mode (on-chip oscillator) with crystal connected to XTAL_IN and XTAL_OUT, and Bypass Mode (external clock source with XTAL_IN tied high).

CLKGEN programs the PLLs and controls the clock source programming and clock dividers.

Table 2 Clock Signal Descriptions

Clock	Description / Typical Use	Power Rail	Type	Source	Pin
32kHz	32.768kHz clock. Used by PMC	VDDIO_SYS2	Input	PMU	CLK_32K_IN
OSC	Oscillator. Main Tegra clock source	AVDD_OSC VDDIO_SYS2	Internal	XTAL or External	XTAL_IN/OUT XTAL_OUT only
PLLA	Used for Audio	AVDD_PLL_APC2C3	Internal	OSC or divided down PLLP	
PLLC2				OSC	
PLLC3					

Clock	Description / Typical Use	Power Rail	Type	Source	Pin
PLLP	Peripheral PLL – Used for various blocks				
PLLC		AVDD_PLL_CG	Internal	OSC	
PLLG	Used for Graphics Engine				
PLLD	Typically used for Display & MIPI (DSI & CSI)	AVDD_PLL_UD2DPD	Internal	OSC	
PLLD2	Typically used for Display (HDMI) & MIPI (DSI & CSI)			OSC, PLLP, or PLL_REFE	
PLLDP	Used for eDP/LVDS				
PLLU	Used for USB			OSC	
PLLM	Typically used for DRAM controller	AVDD_PLL_M	Internal	OSC	
PLLC4		AVDD_PLL_C4	Internal	OSC, PLLP, or PLL_REFE	
PLLX	Used for CPU	AVDD_PLL_X	Internal	OSC	
PLLE	Used for USB3/PEX or as high precision clock source	AVDD_PLL_EREFE	Internal	OSC, PLLP, or PLL_REFE	
PLL_REFE				OSC	
PEX/USB3 PLL	Used for USB3/PEX	AVDD_PEX_PLL	Internal	OSC	
SATA PLL	Used for SATA	AVDD_SATA_PLL	Internal	OSC	
	Optional buffered version of CLK_32K_IN	VDDIO_SYS	Output	32KHz input	CLK_32K_OUT
	Optional requests for clock outputs below	VDDIO_AUDIO VDDIO_SDMMC1 VDDIO_UART	Inputs		DAP_MCLK1_REQ CLK2_REQ CLK3_REQ
VIMCLK	Used for Camera 1 master reference clock.	VDDIO_CAM	Output	Various	CAM_MCLK
VIMCLK2	Used for Camera 2 master reference clock.				GPIO_PBB0
EXTPERIPH1_CLK	Peripheral Clock output #1. Used for Audio MCLK	VDDIO_AUDIO	Output	Various	DAP_MCLK1
EXTPERIPH2_CLK	Peripheral Clock output #2	VDDIO_SDMMC1	Output	Various	CLK2_OUT
EXTPERIPH3_CLK	Peripheral Clock output #3	VDDIO_UART	Output	Various	CLK3_OUT

2.2.1.1 32KHz Clock Input Timing

The 32KHz clock is input on the CLK_32K_IN ball. This is a standard CMOS input on the VDDIO_SYS power rail operating at 1.8V ± 5%.

Figure 4 CLK_32K_IN Clock Input Timing Diagram

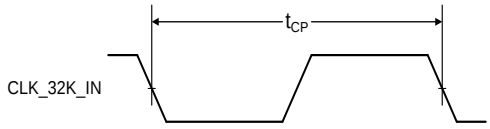


Table 3. CLK_32K_IN Clock Input Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_{CP}	CLK_32K_IN Input period		30.52		us	
	CLK_32_K_IN Input frequency while SYS_RESET_N is asserted	16.384	32.768	65.536	KHz	4
	CLK_32K_IN Input frequency otherwise	32.375	32.768	33.161	KHz	
	CLK_32K_IN duty cycle	40		60	%	
	CLK_32K_IN tolerance Basic functionality Accurate RTC functionality (e.g. time keeping)			 1.2 100	 % ppm	1, 2, 3

1. 100ppm is the absolute maximum and can limit long term accuracy of time; recommend 30 ppm for improved accuracy over time
2. Any requirements from the 32KHz external clock source (i.e., PMU) must also be met.
3. There are no specific requirements for rise/fall times on CLK_32K_IN, but the edges should be increasing (rising) or decreasing (falling) only – There should be no significant glitches on the edges. The input is Schmidt trigger, so some minor noise is allowed.
4. While SYS_RESET_N is asserted, CLK_32K_IN can be anywhere from 16.384kHz to 65.536kHz.

2.2.1.2 External Reference Clock Input Timing

The XTAL_OUT pin can either be used in conjunction with XTAL_IN to support a crystal connection, or XTAL_OUT can be used as an input for an external reference clock. The crystal oscillator block is powered by AVDD_OSC

Figure 5 XTAL_OUT as Input for External Reference Option

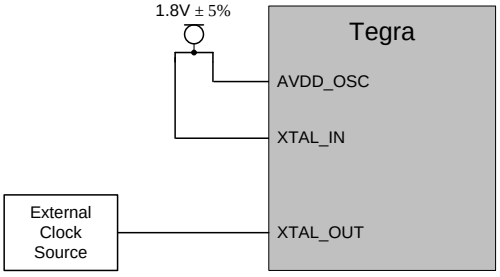


Figure 6 XTAL_OUT External Clock Input Option Timing Diagram

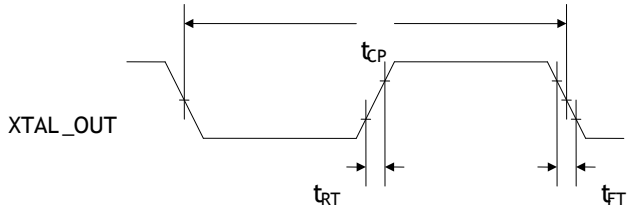


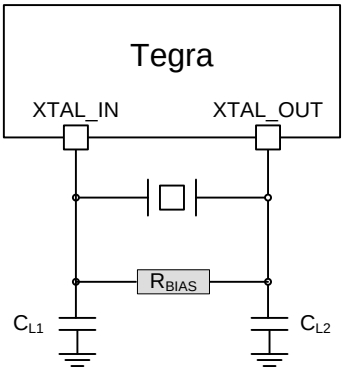
Table 4. XTAL_OUT External Clock Input Option Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CP}	XTAL_OUT Input period (12MHz)		83.33		us
	XTAL_OUT duty cycle	45		55	%
	XTAL_OUT Jitter (RMS)			250	ps
t_{RT}	XTAL_OUT edge rise time	2			ns
t_{FT}	XTAL_OUT edge fall time	2			ns

2.2.2 Crystal Connection and Selection

Tegra processors support the use of an external reference clock input to XTAL_OUT or a crystal connection to XTAL_OUT and XTAL_IN to generate the reference clock internally. The crystal oscillator block is powered by AVDD_OSC. Table 5 contains the requirements for the crystal used, the value of the parallel bias resistor and information to calculate the values of the two external load capacitors (C_{L1} and C_{L2}) shown in the circuit.

Figure 7 Crystal Connection



Note: The R_{BIAS} resistor should only be used in designs that incorporate a Tegra processor in the 23mm x 23mm package configuration.

Table 5. Crystal and Circuit Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_P	Parallel resonance crystal Frequency	12			MHz	1
F_{TOL}	Frequency Tolerance		±50		ppm	1
C_L	Load Capacitance for crystal parallel resonance Typical values used for C_{L1}/C_{L2}	5	7 12	10	pf	1, 3, 4
DL	Crystal Drive Level			300	uW	1, 5
R_{BIAS}	External Bias Resistor		2		MΩ	
ESR	Equivalent Series Resistance			100	Ω	2

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{START}	Start Time (From AVDD_OSC on or SYS_CLK_REQ active coming out of Deep Sleep)		6	10	mS	
T_{BUF_DRV}	Tegra Oscillator Buffer drive strength register value		1			6

1. F_P, F_{TOL}, C_L and DL are found in the Crystal Datasheet
2. ESR = RM * (1 + C0/CL)/2 where: RM = Motional Resistance; C0 =Shunt Capacitance from Crystal datasheet; Datasheets may specify ESR directly – consult manufacturer if unclear whether ESR or RM are specified.
3. C_L = Load capacitance (Crystal datasheet). CPCB is PCB capacitance (trace, via, pad, etc.)
4. Load capacitor values (CLx) can be found with formula: C_L = [(CL1xCL2)/(CL1+CL2)]+CPCB. Or since CL1 and CL2 are typically of equal value, CL = (CLx/2)+CPCB. or CLx = (CL – CPCB) x 2
5. DL = 0.5*ESR*(2π × F_P × CL × V)^2. V = AVDD_OSC = 1.8VPLLs
6. If other drive strength settings are used, XTAL_OUT swing should reach below 200mV and above 1.3V over all conditions

2.3 Power Sequencing

The Vm_pin constraint described in the Absolute Maximum Ratings table applies when a rail is powered off, ramping up, powered on, or ramping down. Violating the V_{M_PIN} constraint can cause leakage back onto the power rail which may permanently damage the Tegra processor or connected components. Do not violate the V_{M_PIN} constraint during Power-Up, Power-Down, Deep Sleep entry, Deep Sleep exit, or at any other time.

Rails sequenced by software can (optionally) be configured to be powered down/up by the external PMIC HW during Boot or Deep Sleep transitions, at a possible power penalty by powering them more often than necessary

Table 6 Power Rails Summary

Logical Group	Rail	Nominal Voltage (V)	Sequenced On	Power-up Stage	Notes
CPU	VDD_CPU	0.75 to 1.3	Hardware	4 (final boot)	Fast CPU Complex logic rail
GPU	VDD_GPU	0.75 to 1.08	Software		Power rail for GPU
AO	VDD_RTC	0.81 to 1.08	Hardware	1 (pre-boot core)	“Always On” rail for RTC, Power Management Controller, and Key Board Controller. This rail is tracked to the VDD_SOC rail by SW within +/- 300 mV except when Tegra is in Deep Sleep.
CORE	VDD_CORE	0.81 to 1.08	Hardware	1 (pre-boot core)	Logic rail for the remainder of the SoC logic
Core Clocks	AVDD_OSC	1.8	Hardware	2 (pre-boot IO)	12 to 48 MHz xtal/oscillator interface, Also CPU VDD sensing mux supply
	AVDD_PLL_APC2C3	1.05	Hardware	2 (pre-boot IO)	General PLL power supply rail
	AVDD_PLL_C4	1.05			ISP/VI
	AVDD_PLL_CG	1.05			General/GPU
	AVDD_PLL_EREFE	1.05			USB3/PCIE
	AVDD_PLL_M	1.05	Hardware	2 (pre-boot IO)	Primarily used for DRAM
	AVDD_PLL_UD2DPD	1.05	Hardware	2 (pre-boot IO)	Primarily used for Display
	AVDD_PLL_UTMIP	1.8	Hardware	2 (pre-boot IO)	USB
	AVDD_PLLX	1.05	Hardware	2 (pre-boot IO)	Primarily used for the Fast CPU Complex
DRAM	VDDIO_DDR	1.20, 1.35	Hardware	3 (boot IO)	

Logical Group	Rail	Nominal Voltage (V)	Sequenced On	Power-up Stage	Notes
	VDDIO_DDR_HS	1.05	Hardware	3 (boot IO)	
	VDDIO_DDR_MCLK	1.20, 1.35			
Display / Camera	AVDD_CSI_DSI	1.2	Software		
	AVDD_HDMI	3.3	Software		
	AVDD_HDMI_PLL	1.05	Software		
	AVDD_LVDS0_IO	1.05			
	AVDD_LVDS0_PLL	1.8, 3.3			1.8V for LVDS, 3.3V eDP
USB 2.0 / HSIC	AVDD_USB	3.3	Hardware	2 (pre-boot IO)	USB 2.0 interface I/O power (3.3V)
	VDDIO_HSIC	1.2	Software		High Speed Inter-Chip interface (1.2V) I/O power.
USB 3.0 / PCIe	AVDDIO_PEX	1.05			USB 3.0 / PCIe interface I/O power (1.05V)
	DVDDIO_PEX	1.05			
	AVDD_PEX_PLL	1.05	Hardware	2 (pre-boot IO)	
	HVDD_PEX	3.3			USB 3.0 / PCIe interface I/O power (3.3V)
	HVDD_PEX_PLL_E	3.3			
	VDDIO_PEX_CTL	3.3			USB 3.0 / PCIe Wake (2.8-3.3V)
Fuse	VPP_FUSE	1.8	Software		Powered only during fuse programming. Rail must be turned off or switched off when NOT programming fuses.
Digital IO	VDDIO_AUDIO	1.8	Software	3 (boot IO), (32-bit NOR only)	
	VDDIO_BB	1.8	Software		
	VDDIO_CAM	1.8, 3.3	Software		CAM I/O partition power. Non-CSI camera interface
	VDDIO_GMI	1.8	Hardware	2 (pre-boot IO)	NAND, NOR, SD, eMMC interface
	VDDIO_HV	1.8	Software		
	VDDIO_SDMMC1	1.8	Software		Typically 1.8 V, typically SD card interface
	VDDIO_SDMMC3	1.8, 2.8 – 3.3	Software		Typically 1.8 V, typically SD card interface
	VDDIO_SDMMC4	1.8	Hardware	3 (boot IO), (eMMC boot)	eMMC interface
	VDDIO_SYS	1.8	Hardware	2 (pre-boot IO)	Powered during Deep Sleep. Includes matrix keyboard, JTAG, etc.
	VDDIO_SYS_2	1.8			
	VDDIO_UART	1.8	Software		

Logical Group	Rail	Nominal Voltage (V)	Sequenced On	Power-up Stage	Notes
SATA	AVDD_SATA_PLL	1.05			
	HVDD_SATA	3.3			
	VDDIO_SATA	1.05			

Table 7 Power Control Signal Descriptions

Name	Type	Description
CLK_32K_IN	Input	32.768kHz Clock: input for 32kHz clock used by RTC & PMC blocks
SYS_RESET_N	Input	System Reset: Reset input for Tegra
RESET_OUT_N	Output	Buffered output based on SYS_RESET_N from the PMU
PWR_I2C_SCL (PMUI2C) PWR_I2C_SDA (PMUI2C)	Output Bidirectional	Power I2C: I2C bus typically used to communicate with PMU, CPU/GPU regulators (if required) & possibly Sub-PMU.
CORE_PWR_REQ	Output	Core Power Request. Used to enable main CORE power rail. Driven high by Tegra when reset is asserted to ensure Core power is on during power-on sequence. Driven low by Tegra for Deep Sleep entry and driven back high up again for Deep Sleep exit. May be used by PMIC to control other rails and resources in Deep Sleep
CPU_PWR_REQ	Output	CPU Power Request. Used to enable CPU power rail. Driven low by Tegra when reset is asserted. Configured to drive high later by Bootloader to power up CPU rail if required. Driven low by Tegra prior to Deep Sleep entry. Driven high by Tegra under SW control during Deep Sleep exit. May be toggled when Tegra is active.
PWR_INT_N	Input	PMU Interrupt. This is typically connected to an output on a PMU (Power Management Unit) and used to wake or otherwise inform the Tegra MWP some critical event has occurred. This could be a low battery alert, a PMU RTC watchdog timer terminating, a new USB Host connection, etc.

2.3.1 Power-up Sequence

The Tegra processor power-up process involves the following high-level steps

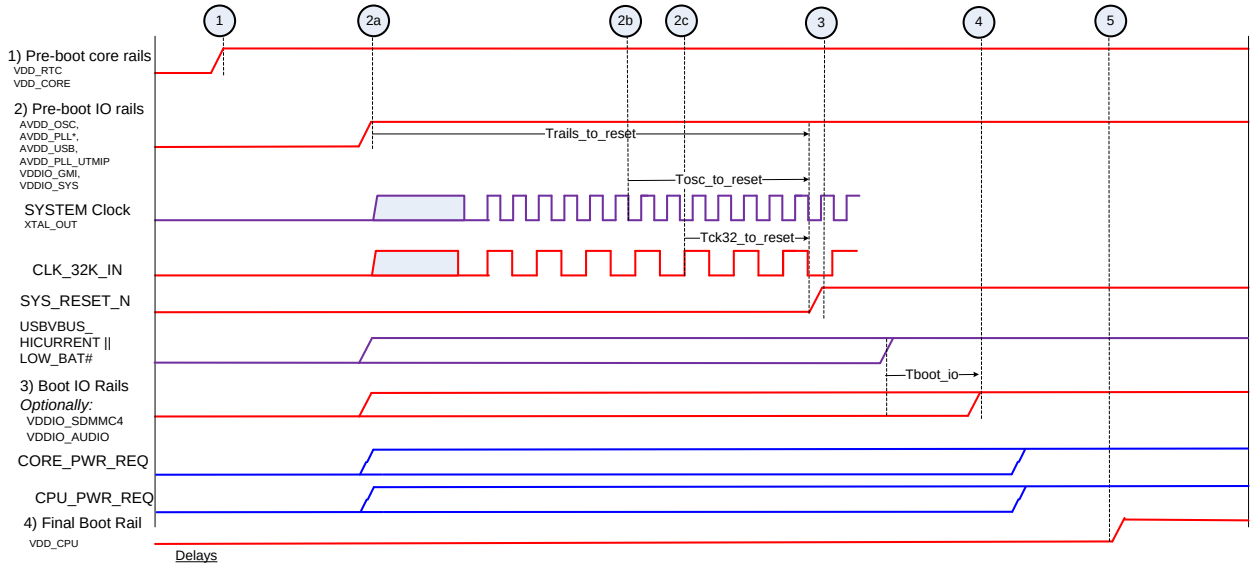
1. Power is off
2. System-level hardware applies power and clocks to the Tegra processor (according to constraints in this section).
3. System-level hardware deasserts the Tegra processor's SYS_RESET_N pin.
4. The Tegra processor's boot ROM executes and eventually passes control to system-dependent software.

2.3.1.1 USB VBUS Power Supported

This sequence depends on the state of two GPIOs specific to this feature:

- LOW_BAT#: input to Tegra signaling that USB VBUS is the only available power source. Initially, the system must consume less than 100mA of current from USB VBUS.
- USBVBUS_HICURRENT: output from Tegra signaling that a USB charger has been detected, and USB VBUS can provide more than 100mA of current.

Figure 8 Power-up Sequence Timing Diagram – USB VBUS Power Supported



Delays
Tck32_to_reset – CLK_32K_IN must have four full cycles before SYS_RESET_N may deassert
Trails_to_reset – SYS_RESET_N must remain asserted for at least 1ms after both all voltage rails have stabilize
Tosc_to_reset – SYS_RESET_N must remain asserted for at least 1ms after the clock at XTAL_OUT is oscillating within spec.
Tboot_io – The Boot IO rails must be up **no later** than 5 ms after (USBVBUS_HICURRENT || LOW_BAT#) becomes true

Timestamps
1) The pre-boot core rails VDD_CORE and VDD_RTC are powered and stable
2a) The pre-boot IO rails are powered and stable.
2b) System clock is oscillating within spec. **When using Tegra's oscillator in oscillation mode, timestamp 2b is 10ms after AVDD_OSC is powered on**
2c) The 32kHz oscillator has provided at least 4 cycles and is oscillating within spec
3) SYS_RESET_N is deasserted and Tegra's boot ROM begins execution
4) Boot IOs are up and platform firmware is fetched from the boot media
5) Via I2C or SPI, software programs CPU regulator to turn on and start using CPU_PWR_REQ

Notes
Timestamps 2a, 2b, and 2c may occur in any order

Power-up Sequence (USB VBUS Power Supported)

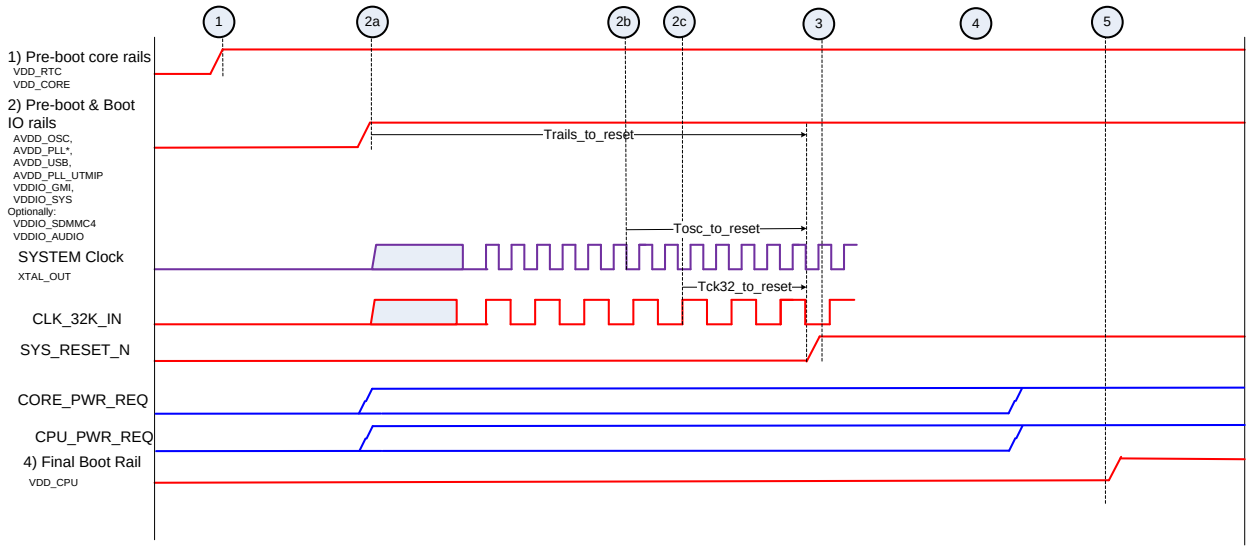
1. All Tegra power rails are off
2. PMIC receives wake event (e.g., ONKEY# assertion)
3. PMIC ramps up VDD_RTC and VDD_CORE (this happens regardless of the currently undriven state of CORE_PWR_REQ)

4. The Tegra processor's SYS_RESET_N input is asserted before ramping up any Tegra power rails other than VDD_RTC and VDD_CORE
   a. Violating this for the Core Clocks rails may unnecessarily increase power dissipation
   b. Violating this for VPP_FUSE, VDDIO_DDR, or other rails may cause permanent damage.
5. PMIC completely ramps up the next group of power rails:
   a. AVDD_OSC
   b. AVDD_PLL*
   c. VDDIO_SYS
      i. PMIC interface
   d. AVDD_USB
   e. AVDD_PLL_UTMIP
      i. USB recovery mode, later USB boot
   f. VDDIO_GMI
      i. straps
6. If either LOW_BAT# isn't asserted or USBVBUS_HICURRENT is asserted, PMIC completely ramps up the remainder of hardware-sequenced power rails excluding VDD_CPU:
   a. If eMMC or NOR is a boot device, VDDIO_SDMMC4
      i. VDDIO_GMI for NAND, NOR, and SPI boot was already previously ramped for strap sensing
   b. If 32-bit NOR is the boot device, VDDIO_AUDIO must be powered
7. The XTAL_OUT to Tegra must have been toggling for at least 1ms
   a. When the internal oscillator is used, this occurs 10ms after AVDD_OSC has ramped up.
   b. The Tegra processor's CLK_32K_IN input must also have toggled for at least 4 complete cycles
8. PMIC deasserts the Tegra processor's SYS_RESET_N input
9. If LOW_BAT# is still asserted, the Tegra processor senses presence of a USB VBUS charger. If present, USBVBUS_HICURRENT is asserted, and the PMIC must ramp up the following rails (just like in step #5):
   a. If eMMC or NOR is a boot device, VDDIO_SDMMC4
      i. VDDIO_GMI for NAND, NOR, and SPI boot was already previously ramped for strap sensing
   b. If 32-bit NOR is the boot device, VDDIO_AUDIO must be powered
   c. VDD*_DDR* if hardware sequenced (i.e., the platform doesn't rely on microboot to turn them on)

   This power ramp must complete within 5ms.
10. If either LOW_BAT# is deasserted, or USBVBUS_HICURRENT is asserted, Tegra begins initial boot, loading boot firmware from the boot interface selected by straps or fuses.
11. Tegra Boot Loader fimware later enables the CPU_VDD power rail via an I2C or SPI access
    Note that CPU_PWR_REQ is not used to control CPU_VDD power sequencing until later enabled via an I2C/SPI register write.
12. Tegra firmware or software drives CPU_PWR_REQ to assert high.
    a. PMIC is still ignoring CPU_PWR_REQ at this time.
13. Tegra software enables CPU_PWR_REQ to control CPU_VDD power sequencing (until the next SYS_RESET_N assertion)
    a. CPU_PWR_REQ is now a direct sideband control for CPU_VDD powering

2.3.1.2 USB VBUS Power Not Supported

Figure 9 Power-up Sequence Timing Diagram – USB VBUS Power Not support



Delays
Tck32_to_reset – CLK_32K_IN must have four full cycles before SYS_RESET_N may deassert
Trails_to_reset – SYS_RESET_N must remain asserted for at least 1ms after both all voltage rails have stabilize
Tosc_to_reset – SYS_RESET_N must remain asserted for at least 1ms after the clock at XTAL_OUT is oscillating within spec.

Timestamps
1) The pre-boot core rails VDD_CORE and VDD_RTC are powered and stable
2a) The pre-boot IO rails are powered and stable.
2b) System clock is oscillating within spec. **When using Tegra's oscillator in oscillation mode, timestamp 2b is 10ms after AVDD_OSC is powered on**
2c) The 32kHz oscillator has provided at least 4 cycles and is oscillating within spec
3) SYS_RESET_N is deasserted and Tegra's boot ROM begins execution
4) Boot IOs are up and platform firmware is fetched from the boot media
5) Via I2C or SPI, software programs CPU regulator to turn on and start using CPU_PWR_REQ

Notes
Timestamps 2a, 2b, and 2c may occur in any order

Power-up Sequence (USB VBUS Power NOT Supported)

1. All Tegra processor power rails are off
2. PMIC receives wake event (e.g., ONKEY# assertion)
3. PMIC ramps up VDD_RTC and VDD_CORE (this happens regardless of the currently undriven state of CORE_PWR_REQ)
4. The Tegra processor's SYS_RESET_N input is asserted before ramping up any Tegra power rails other than VDD_RTC and VDD_CORE.
   Violating this for the Core Clocks rails may unnecessarily increase power dissipation
   Violating this for VPP_FUSE, VDDIO_DDR, or other rails may cause permanent damage.
5. PMIC completely ramps up the next group of power rails:
   a. AVDD_OSC
   b. AVDD_PLL*
   c. VDDIO_SYS
      i. PMIC interface
   d. AVDD_USB
   e. AVDD_PLL_UTMIP
      i. USB recovery mode, later USB boot
   f. VDDIO_GMI
      i. straps
   g. If eMMC or NOR is a boot device, VDDIO_SDMMC4
      i. VDDIO_GMI for NOR, and SPI boot was already previously ramped for strap sensing
   h. If 32-bit NOR is the boot device, VDDIO_AUDIO must be powered
   i. VDD*_DDR* if hardware sequenced (i.e., the platform does not rely on microboot to turn them on)

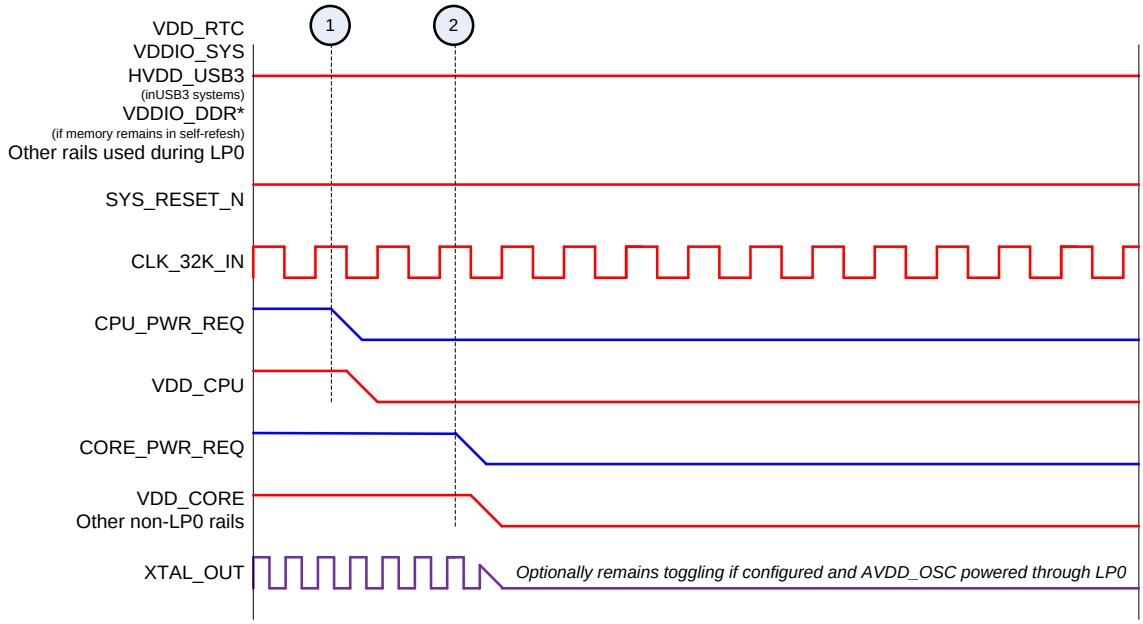
6. The XTAL_OUT to the Tegra processor must have been toggling for at least 1ms
   a. When the internal oscillator is used, this occurs 10ms after AVDD_OSC has ramped up.
   b. The Tegra processor's CLK_32K_IN input must also have toggled for at least 4 complete cycles
7. PMIC deasserts the Tegra processor's SYS_RESET_N input
8. The Tegra processor begins initial boot, loading boot firmware from the boot interface selected by straps or fuses.
9. Tegra Boot Loader fimware later enables the CPU_VDD power rail via an I2C or SPI access
   a. Note that CPU_PWR_REQ is not used to control CPU_VDD power sequencing until later enabled via an I2C/SPI register write.
10. Tegra firmware or software drives CPU_PWR_REQ to assert high.
    a. PMIC is still ignoring CPU_PWR_REQ at this time.
11. Tegra software enables CPU_PWR_REQ to control CPU_VDD power sequencing (until the next SYS_RESET_N assertion)
    a. CPU_PWR_REQ is now a direct sideband control for CPU_VDD powering

2.3.2 Deep Sleep Entry

The Tegra deep sleep (LP0) entry process includes the following basic steps:

1. If powered, the Tegra processor deasserts CPU_PWR_REQ
2. PMIC powers off VDD_CPU
3. The Tegra processor de-asserts CORE_PWR_REQ
4. PMIC powers off all Tegra rails except:
   a. VDD_RTC
   b. VDDIO_SYS
   c. HVDD_USB3 (if the platform supports USB3 wake from LP0)
   d. Any platform-specific digital IO rails (i.e., VDDIO_*) used for wake events
   e. Any platform-specific digital IO rails that must maintain their state during LP0
   f. VDDIO_DDR* if the memory contents are to be kept in self-refresh

Figure 10 Deep Sleep Entry Timing Diagram



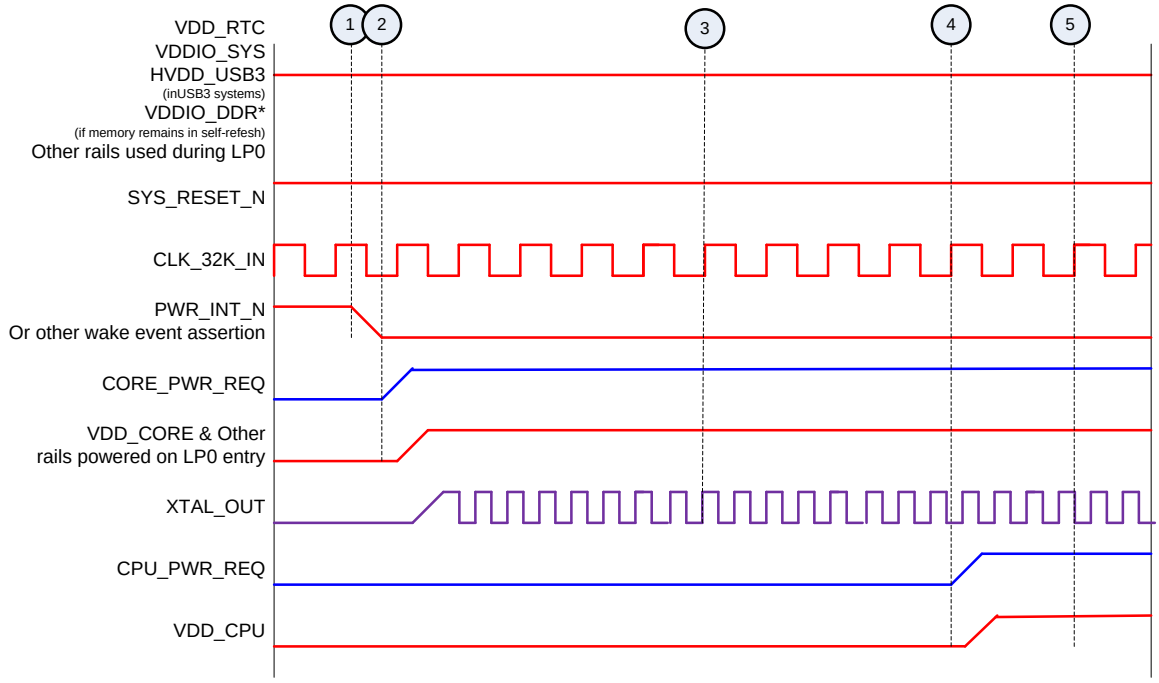
Timestamps
1) Tegra deasserts CPU_PWR_REQ and PMIC powers down VDD_CPU
2) Tegra later deaserts CORE_POWER_REQ and poweres down other non_LP0 rails

2.3.3 Deep Sleep Exit

The Tegra deep sleep (LP0) exit process includes the following basic steps:

1. The Tegra processor receives a wake event
   For example, the PMIC may assert the Tegra processor's PWR_INT_N interrupt input in response to a debounced ONKEY# assertion.
2. The Tegra processor asserts CORE_PWR_REQ
3. The PMIC ramps up VDD_CORE and all rails that were up when CORE_PWR_REQ had deasserted on current deep sleep (LP0) entry. These rails and the oscillator input to the Tegra processor must be in spec within the Tegra processor's programmable power good timer after CORE_PWR_REQ asserts.
   The default power good timer value in APBDEV_PMC_PWRGOOD_TIMER_0 is 3.876 ms, and can range from 30µs to 128ms. Shorter values are preferred to minimize user-visible latencies.
   After VDD_CORE ramps up, the VDD_RTC voltage will change from its fixed LP0 voltage to tracking the VDD_CORE voltage.
4. The Tegra processor may later assert CPU_PWR_REQ to explicitly request that VDD_CPU ramp up. VDD_CPU must remain off until then.

Figure 11. Deep Sleep Exit



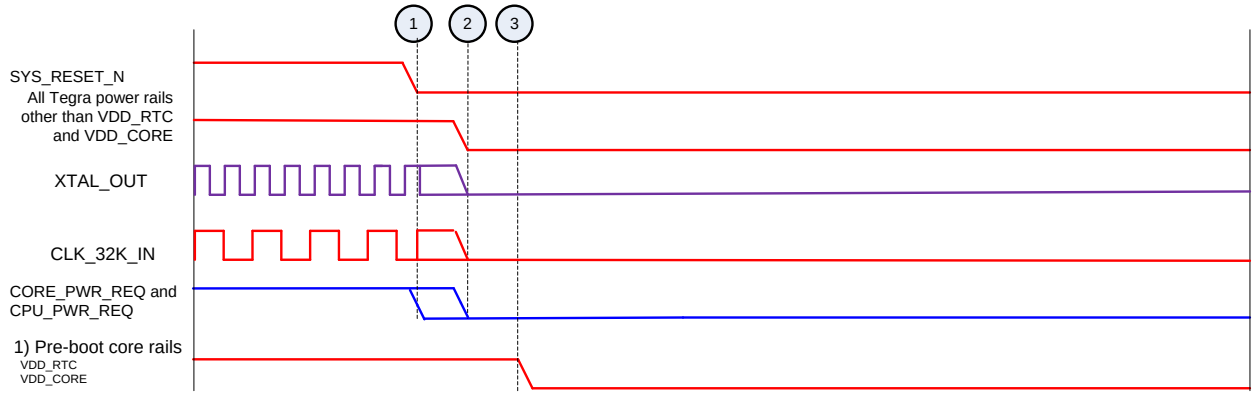
Timestamps
1) PWR_INT_N or other wake event asserts
2) Tegra asserts CORE_PWR_REQ and PMIC ramps up VDD_CORE and other rails powered on LP0 entry
3) Platform-specific "power good" timer expires; Tegra begins booting
4) Tegra later asserts CPU_PWR_REQ and PMIC ramps up VDD_CPU
5) Platform-specific "CPU power good timer expires", fast CPU complex begins execution

2.3.4 Power-Down Sequence

NVIDIA strongly recommends the following power-down sequence. Violating this sequence may cause permanent damage.

1. Assert SYS_RESET_N
   Returns the Tegra processor IOs to safe values and prevents glitches during power-down.
2. Power down all rails except VDD_CORE (if currently powered) and VDD_RTC to at least below 200 mV.
   Keeping CORE logic powered keeps IOs controlled.
3. Power down VDD_CORE (if powered) and VDD_RTC

Figure 12 Power-Down Sequence Timing Diagram



Timestamps
1) SYS_RESET_N deasserted
2) All Tegra power rails other than VDD_RTC and VDD_CORE are ramped down
3) VDD_RTC and VDD_CORE ramp down

Notes
CORE_PWR_REQ and CPU_PWR_REQ are indeterminate as soon as SYS_RESET_N drops below VIH_MIN.

3.0 Pin Definitions

This section details each signal location and multiplexing functions (if applicable). The Tegra processor has pins that are multi-purpose digital I/O pads (MPIO). Each MPIO can be configured to act as a GPIO or it can be assigned for use by a particular I/O controller. Tegra processors include many types of I/O controllers (e.g., I2C, SDMMC, GMI, etc.). For some of these controller types, the Tegra processor includes multiple controller instances. For example, K1 series processors include six I2C controller instances. Each controller instance on the Tegra processor communicates with external devices via a set of external signals. For each controller instance, each signal can be brought out on (at least) one MPIO. For example, each I2C controller has two external signals: CLK and DAT. The CLK signal of the I2C1 controller is available on the MPIO whose ball name is GEN1_I2C_SCL. An MPIO acting as a particular signal for a particular I/O controller is said to be acting as a Special-Function IO (SFIO). Each MPIO has up to four SFIO functions. Each MPIO can also be programmed to act as a GPIO. For example, the pin named UART3_RTS_N can behave in the following ways:

- As a GPIO
- Signal RTS for UART3
- Signal PWM for PM3
- Signal DATA for DTV
- Signal A4 for NOR

Though each MPIO has up to 5 functions (GPIO function and up to 4 SFIO functions), a given MPIO can only act as a single function at a given point in time. The Tegra pinmux controller includes the logic and registers to select a particular function for each MPIO. Some controller instances have a particular signal available on more than one MPIO. For example, the UA3_TXD signal is available on the following MPIO pads (ball names): UART2_RTS_N, KB_ROW9, SDMMC3_DAT1, ULPI_DAT0, SDMMC_DAT2, GPIO_PU0. In a system which brings out the UA3_TXD signal on the SDMMC_DAT2 ball, the pinmux registers for PM3_PWM0 should be programmed to select some other signal. Some controller instances make their entire set of signals available on two or more sets of MPIO pads; these controllers have more than one interface.

NOTE: Before using any controller:
- Make sure that the pinmux registers are programmed to bring each signal out on only ONE MPIO.
- Make sure that the pinmux registers are programmed to bring out the controller's signals on only ONE interface.

Though each MPIO pad shares a similar structure, there are several varieties of such pads. The varieties are designed to minimize the number of on-board components (such as level shifters or pull-up resistors) required in Tegra-based designs.

Tegra processors employ five types of MPIO pads:

- ST (standard) pads are the most common pads on the chip.
- DD (dual-driver) pads are similar to the ST pads with the addition of a 3.3V tolerant true open-drain mode. A DD pad can tolerate its I/O pin being pulled to 3.3V (regardless of supply voltage) as long as the pad's output-driver is set to open-drain mode. There are special power-sequencing considerations when using this functionality.

  NOTE: The output of DD pads cannot be pulled High during deep-power-down (DPD).
- OD (open drain) pads are optimized to tolerate 5V on the I/O pin regardless of the supply voltage. They are similar to ST pads except for an improved I/O voltage tolerance, the absence of a weak pull-up, and the absence of a push-pull output driver.

  NOTE: OD pads do NOT retain their output during DPD. OD pads should NOT be configured as GPIOs in a platform where they are expected to hold a value during DPD.
- CZ (controlled output impedance) pads are optimized for use in applications requiring tightly controlled output impedance. They are similar to ST pads except for changes in the drive strength circuitry and in

the weak pull-ups/-downs. CZ pads are included on the VDDIO_SDMMC1 and VDDIO_SDDMC3 power rails. Each of those rails also includes a pair of CZ_COMP pads. Circuitry within the Tegra processor continually matches the output impedance of the CZ pads to the on-board pull-up/-down resistors attached to the CZ_COMP pads.

- LV (low voltage) pads are optimized for use with a 1.8V supply voltage (and signaling level). The Tegra processor includes LV pads on the VDDIO_SDMMC4 power rail.

Table 8 MPIO Pad Types

MPIO Pad Type	Input Buffer	Output Buffer	I/O Voltage Tolerance	Nominal Pull Strength	Slew Rate Control	Drive Strength Control
CZ	schmitt & CMOS	push-pull	VDDIO	15kΩ	2-bits, up & down	7-bits, up & down.
DD	schmitt & CMOS	push-pull & open-drain	3.3V for open-drain, VDDIO otherwise	50kΩ	2-bits, up & down	5-bits, up & down. LPMD
LV	schmitt & CMOS	push-pull	VDDIO	15kΩ	4-bits, up & down	5-bits, up & down.
OD	CMOS	open-drain	5V	100kΩ (down only)	2-bits, down only	5-bits, down only. LPMD
ST	schmitt & CMOS	push-pull	VDDIO	100kΩ	2-bits, up & down	5-bits, up & down. LPMD

Each MPIO pad consists of:

- An output driver with tristate capability, drive strength controls and push-pull mode, open-drain mode, or both
- An input receiver with either schmitt mode, CMOS mode, or both
- A weak pull-up and a weak pull-down

3.1 Pad Controls

The following controls can be independently configured on a per-pad basis

Table 9 Per-pad Controls

Control	Description
PUPD	Internal Pull-up/down option: Option to enable internal Pull-up, Pull-down resistors or neither
TRISTATE	Tristate (high-z) option: Disables or enables the pad's output driver. This setting overrides any other functional setting and also whether pad is selected for SFIO or GPIO. Can be used especially when the pad direction changes or pad is assigned to different SFIO to avoid glitches.
E_INPUT	Input Receiver (Enable/Disable): Enables or disables input receiver.
OD	Open Drain option: (applies to DD pads only) Selects between open-drain output driver and push-pull driver.

During normal operation, these per-pad controls are driven by the pinmux controller registers. During deep sleep, PMC bypasses and then resets the pinmux controller registers. Software reprograms these registers as necessary after returning from deep sleep.

The following table list available pad signals and their control mechanism.

Table 10 Per-pad Functional Pins

Pin Name	Description	Control/ Mechanism
EN	Active Low. Driver Enable EN=0; Driver tri-state EN=1	Per Pad control via GPIO or Pin Mux SFIO. Overriding control via Pin Mux TRISTATE pin
E_HSM	Active High. Enables High Speed mode for the driver and receiver	PAD Control Group
E_OD (Applicable for DD type pads)	Active High Enable Open Drain Output Driver mode	Per Pad (i.e., via Pin Mux control register). When this bit set then only the DD pads become tolerant I/O level (upto 3.3V) irrespective of I/O power supply otherwise it is limited by I/O supply. Before pulling/driving external I/Os to a value greater than I/O power supply this bit must be set to avoid excessive leakage. Default value recommended for DD pads is 1 to ensure that during power up no excessive leakage is happening irrespective of I/O voltage. For other pads E_OD is driven to Logic0
E_LPBK	Active High. Enables Loopback mode.	Functional Control
E_PULLD	Active High, weak pull-down enable (100KΩ).	Per-Pad (i.e., via Pin Mux control register).
E_PULLU	Active High, weak pull-up enable (100KΩ).	Per-Pad (i.e., via Pin Mux control register).
E_INPUT	Active high, Enables input path IO => ZI / TZI	Per-Pad (i.e., via Pin Mux control register). Default for pins acting as strap: Enabled
E_TZI	Active high, enables TZI path.	Functional Control
E_SCHMT	Active high, Enables Schmitt Trigger on the Inverter/Schmitt input receiver. When low, becomes Inverter type.	PAD Control Group
RCV_SEL (Applicable for OD type pads)	Select between “High VIL/VIH” and ‘Normal VIL/VIH” receivers RCV_SEL=1: “High VIL/VIH” RCV_SEL=0: “Normal VIL/VIH”	Per-Pad (i.e., via Pin Mux control)

The MPIO pads are partitioned into 35 pad control groups. The following controls can be configured independently for each pad control group.

Table 11 Pad Control Group Controls

Control	Description
HSM	High Speed Mode (Enable/Disable)
SCHMT	Schmitt Trigger (Enable/Disable): (Not applicable to LV pads)
DRVDN / UP	Drive Down / Up: Driver Output Pull-Up/Pull-Down drive strength code. Normally 5-bit code and for CZ type pads it has 7-bit control.
SLWR/ SLWF	Slew Falling / Rising: Driver Output Pullup/ Pull-Down slew control code and normally a 2-bit value

The controls are configured via the per pad control group registers. There is one pad control register per pad control group. During deep sleep, all of these pad control registers automatically return to their power-on-reset state. Software reprograms these registers as necessary following deep sleep. Table 14 lists the pad control group for each MPIO (see the pad control group column).

3.2 Power Rail Controls

Per-power-rail controls are included in PMC registers which maintain their state during deep sleep. Software does NOT need to reprogram these register following deep sleep. The following table explains the brief functionality of these signals along with the way how they are controlled by in PMC

Table 12 Power Rail Controls

Pin Name	Description	Control/Grouping Mechanism in PMC
E_33V*	Active high 3.3V mode select. When low selects VDDP 1.8v mode.	Generated based on respective PWR_DET signal and the logic is maintained in PMC (AO Domain). Default: maintained at Logic 1 to ensure safe power up of I/Os that are pulled to 3.3V. The programming sequence: Enabling the Power Detect Wait for specified time Enable control to latch the correct value of Power Detect
E_NO_IOPWR**	Active High, when high prevents leakage when IO power is gone while core power is still on.	Maintained per power rails for 11 power rails. Set during Cold Reset so that I/O rail voltage ramping does not affect the pad. Whenever an I/O power rail is shut off for any specific use case, this bit has to be set to Logic1 before the I/O rails are brought down to avoid excessive leakage to the pad.
DPD_IO_[1..0]*	Core voltage level. Programs IO to Hi/Lo/Tri-state for DPD mode. (2-bits)	Controlled via PMC logic by means of latching the I/O value prior to entering the DPD state and driving the same throughout DPD.
SEL_DPD*	Core voltage level. Selects input source. SEL_DPD=0 selects A. SEL_DPD=1 selects DPD_IO_[1..0].	Generated based “APBDEV_PMC_DPD_ENABLE_0” in PMC with some delayed transition so that E_DPD, DPD_IO are at proper value
E_DPD*	Core voltage level. Active high. Places pad in DPD mode by deactivating bias, clamping settings for DPD mode, and gating-out inputs from core.	Based on“APBDEV_PMC_DPD_ENABLE_0” register in PMC

In addition to pads described in Table 12, 9 other pads are used for Power Detect status on various I/O rails. They are used to sense the I/O rail voltage level (i.e., 3.3V or not). They are reflected through the PWR_DET registers in the PMC.

3.3 POR Behavior

Each MPIO pad has a deterministic POR state. The particular reset state for each pad is chosen to minimize the need of on-board components like pull-up resistors in a Tegra-based system. For example, the on-chip weak pull-ups are enabled during POR for pads which are usually used to drive active-low chip selects.

The following list is a simplified description of the Tegra boot process focusing on those aspects which relate to the MPIO pins.

1. System-level hardware executes the power-up sequence. This sequence ends when system-level hardware releases SYS_RESET_N.
2. The Tegra processor’s boot ROM begins executing and programs the on-chip I/O controllers to access the secondary boot device.
3. The Tegra processor’s boot ROM fetches the Boot Configuration Table (BCT) and boot loader from the secondary boot device.
4. If the BCT and boot loader are fetched successfully, the Tegra processor’s boot ROM yields to the boot loader.
5. Otherwise, the Tegra processor’s boot ROM enters USB recovery mode.

Table 13 POR—Default Reset States

POR Type	Description
High	POR value listed as 1 in MPIO Pads table
Low	POR value listed as 0 in MPIO Pads table
PU	Pulled Up
PD	Pulled Down
Z	High impedance state

3.4 Deep Sleep Behavior

Deep Sleep is an ultra-low-power standby state in which the Tegra processor maintains much of its I/O state while most of the chip is powered off. The following lists offer a simplified description of the deep sleep entry and exit concentrating on those aspects which relate to the MPIO pads. During deep sleep most of the pads are put in a state called Deep Power Down (DPD). The sequence for entering to DPD is same across pads. Specific variations are there in some pads in terms of type of features that are available in DPD.

NOTE: The output of DD pads cannot be pulled High during deep-power-down (DPD).
OD pads do NOT retain their output during DPD. OD pads should NOT be configured as GPIOs in a platform where they are expected to hold a value during DPD.

ALL MPIO pads **do NOT** have identical behavior during deep sleep. They differ with regard to:

- Input buffer behavior during deep sleep
  - Forcibly disabled OR
  - Enabled for use as a “GPIO wake event” OR
  - Enabled for some other purpose (e.g., a “clock request” pin)
- Output buffer behavior during deep sleep
  - Maintain a static programmable (0, 1, or tristate) constant value OR
  - Capable of changing state (i.e., dynamic while the chip is still in deep sleep; e.g., a pin related to the keyboard controller)
- Weak pull-up/pull-down behavior during deep sleep
  - Forcibly disabled OR
  - Can be configured
- Behavior coming out of deep sleep
  - Maintain its deep sleep state until software requests OR
  - PMC forcibly returns the pad to its power-on-reset state before software is running
- Pads that do not enter deep sleep
  - Some of the pads whose outputs are dynamic during deep sleep are of special type and they do not enter deep sleep (e.g., pads that are associated with PMC logic do not enter deep sleep, pads that are associated with JTAG do not enter into deep sleep any time.

3.4.1 Deep Sleep Entry

1. Software programs PMC to enter deep sleep
2. PMC latches much of the Tegra processor’s I/O state, takes control of the I/Os by setting them in SEL_DPD mode, puts the I/Os in a low power state by asserting E_DPD if applicable and resets the I/O controllers
3. PMC de-asserts CORE_PWR_REQ
4. The PMIC powers down VDD_CORE
5. PMC continues driving the I/O state that it has latched

3.4.2 Deep Sleep Exit

1. PMC detects a wake event (e.g., a rising edge on an appropriately configured MPIO)
2. PMC asserts CORE_PWR_REQ
3. The PMIC powers up VDD_CORE

4. PMC resets the logic within VDD_CORE
5. PMC takes the I/Os out of E_DPD but continues to drive them in SEL_DPD mode (the values of I/Os do not change during deep sleep exit until platform specific software takes control of the I/Os).
6. PMC yields control of some of the MPIOs to the I/O controllers
7. The boot ROM executes and wakes up software
8. Software re-initializes the I/O controllers
9. When software requests, PMC yields control of the remaining MPIOs to the I/O controllers.

3.4.3 Entering DPD

Ensure VDD supply is active throughout the DPD cycle.

1. SEL_DPD must be asserted (set to Logic 1) before entering DPD mode.
   Prior to this ensure all the pins related to DPD (E_33V, E_IO_NOPWR, E_PULLD, E_PULLU, DPD_IO) are driven with proper value, this will ensure the transition does not produce glitches.
   a. For DD pads the E_OD also should be driven with proper value while entering into DPD
   b. For DD pads If E_OD is at Logic 1 during DPD the I/Os cannot be pulled High
   c. For OD pads RCV_SEL has to be held in proper state during DPD
   d. E_33V and E_IO_NOPWR may be in correct state while entering DPD
   e. For some of the pads the E_PULLU/E_PULLD are not available during DPD and those pads are marked with PU/PD availability as NO in Table 14
2. Give setup time as per the requirement (see Figure 13)
3. E_DPD must be asserted (set to Logic 1) to enter into DPD state.

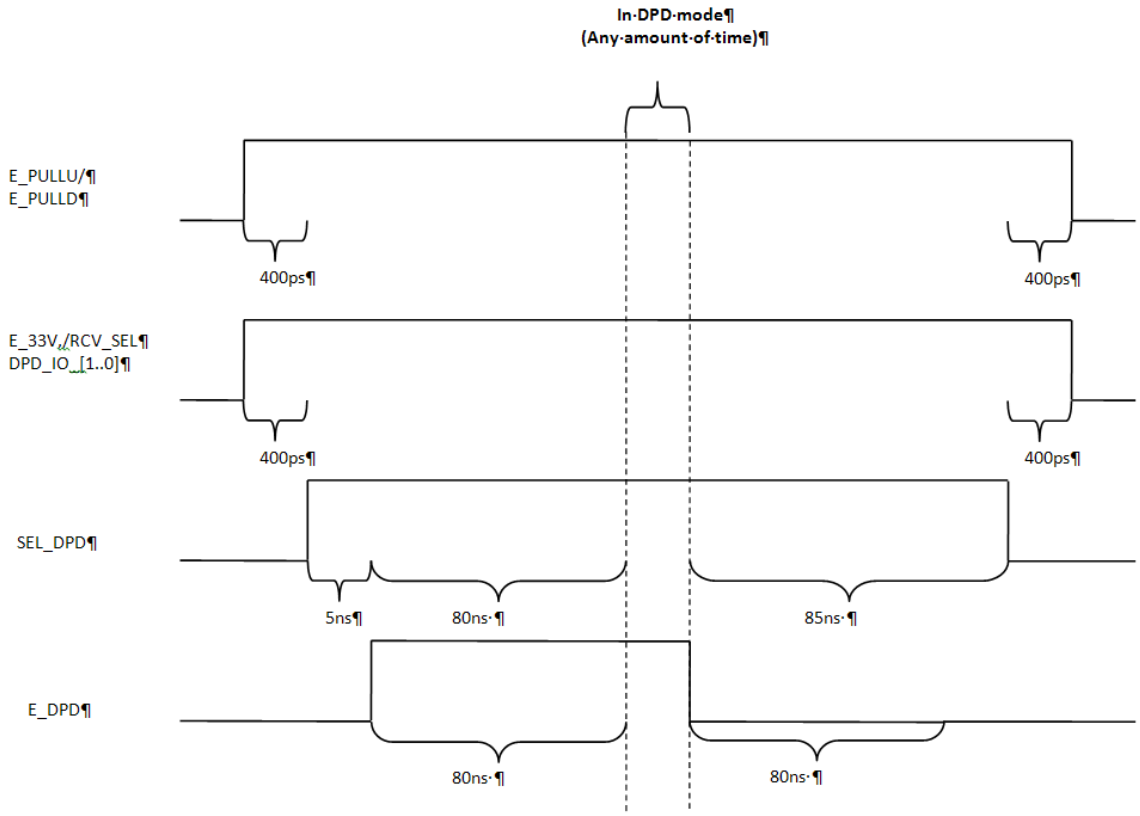
3.4.4 Staying in DPD

1. SEL_DPD must be asserted (set to Logic 1) and E_DPD is at Logic 1
2. DPD related inputs set during DPD entry phase remain unchanged.

3.4.5 Coming Out of DPD

1. E_DPD must be resettled (set to Logic 0)
2. Wait specified time (see Figure 13)
3. SEL_DPD must be resettled (set to Logic 0)
4. Change the control signals related to DPD (E_PULLD, E_PULLU, etc. depending on necessity)

Figure 13 DPD Wait Times

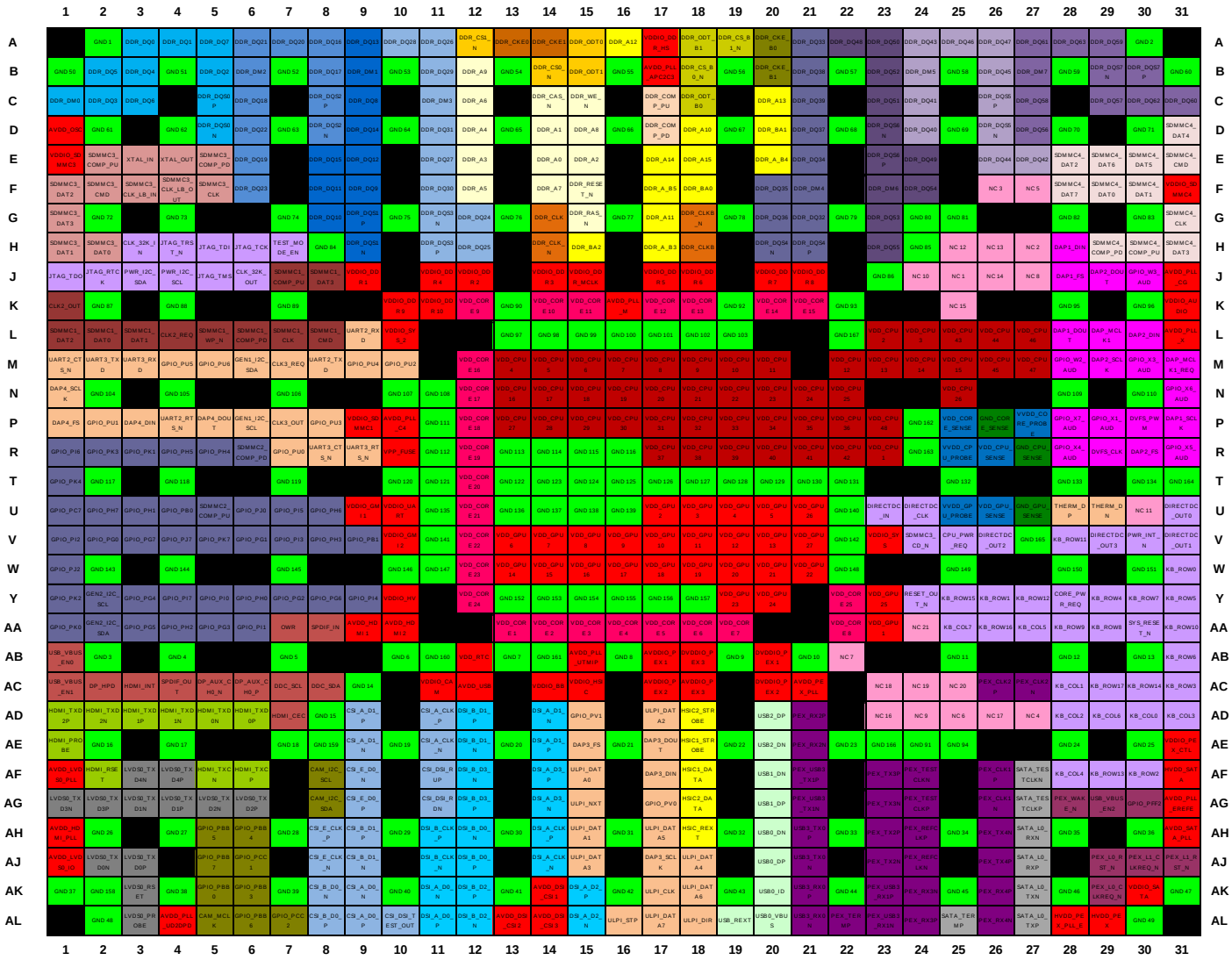


3.5 GPIO Controller

The Tegra processor's GPIO controller provides the tools for configuring each MPIO for use as a software-controlled GPIO. Each GPIO is individually configurable as Output/Input/Interrupt sources with level/edge controls. The GPIO controller is divided into 8 banks. Each bank handles the GPIO functionality for up to 32 MPIOs. Within a bank, GPIOs are arranged as four ports of 8-bits each. The ports are labeled consecutively from A through Z and then AA through FF. Ports A through D are in bank 0. Ports E through H are in bank 1. There are 183 available GPIOs. Table 14 maps each MPIO pad to a particular GPIO port and bit (see the GPIO column).

NOTE: The GPIO banking and numbering conventions show some breaks, this was to maintain backward compatibility with previous generation GPIO register configurations.

3.6 23x23 mm 813 FCBGA Pin Assignments



3.7 Pin Descriptions

In the following table, pads are categorized by functional block. The power rail name is listed in parentheses with the functional block name.

Table 14 Multi-Purpose I/O

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
AUDIO (vddio_audio)											
DAP_MCLK1	L29	GPIO3_PW.04	extperiph1_clk					pd	ST	cdev1cfg	100
DAP_MCLK1_REQ	M31	GPIO3_PEE.02			SATA_DEV_SLP			pd	ST	cdev1cfg	100
DAP1_DIN	H28	GPIO3_PN.01	I2S0_SDATA_IN					pd	ST	dap1cfg	100
DAP1_DOUT	L28	GPIO3_PN.02	I2S0_SDATA_OUT			SATA_LED_ACTIVE	wake30	pd	ST	dap1cfg	100
DAP1_FS	J28	GPIO3_PN.00	I2S0_LRCK					pd	ST	dap1cfg	100
DAP1_SCLK	P31	GPIO3_PN.03	I2S0_SCLK					pd	ST	dap1cfg	100
DAP2_DIN	L30	GPIO3_PA.04	I2S1_SDATA_IN					pd	ST	dap2cfg	100
DAP2_DOUT	J29	GPIO3_PA.05	I2S1_SDATA_OUT					pd	ST	dap2cfg	100
DAP2_FS	R30	GPIO3_PA.02	I2S1_LRCK					pd	ST	dap2cfg	100
DAP2_SCLK	M29	GPIO3_PA.03	I2S1_SCLK					pd	ST	dap2cfg	100
GPIO_X4_AUD	R28	GPIO3_PX.04						pd	ST	spicfg	100
GPIO_X5_AUD	R31	GPIO3_PX.05						pu	ST	spicfg	100
GPIO_X6_AUD	N31	GPIO3_PX.06						pu	ST	spicfg	100
GPIO_X7_AUD	P28	GPIO3_PX.07						pd	ST	spicfg	100
GPIO_W2_AUD	M28	GPIO3_PW.02					wake12	pu	ST	spicfg	100
GPIO_W3_AUD	J30	GPIO3_PW.03					wake11	pu	ST	spicfg	100
DVFS_PWM	P30	GPIO3_PX.00		CLDVFS_PWM				pd	ST	spicfg	100
GPIO_X1_AUD	P29	GPIO3_PX.01						pd	ST	spicfg	100
DVFS_CLK	R29	GPIO3_PX.02		CLDVFS_CLK				pu	ST	spicfg	100
GPIO_X3_AUD	M30	GPIO3_PX.03						pu	ST	spicfg	100
BB (vddio_bb)											
DAP3_DIN	AF17	GPIO3_PP.01	I2S2_SDATA_IN					pd	ST	dap3cfg	100
DAP3_DOUT	AE17	GPIO3_PP.02	I2S2_SDATA_OUT					pd	ST	dap3cfg	100
DAP3_FS	AE15	GPIO3_PP.00	I2S2_LRCK					pd	ST	dap3cfg	100

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
DAP3_SCLK	AJ17	GPIO3_PP.03	I2S2_SCLK					pd	ST	dap3cfg	100
GPIO_PV0	AG17	GPIO3_PV.00					wake24	z	ST	uabcfg	100
GPIO_PV1	AD15	GPIO3_PV.01					wake1	z	ST	uabcfg	100
ULPI_CLK	AK17	GPIO3_PY.00	SPI1A_DOUT					z	ST	udacfg	100
ULPI_DATA0	AF15	GPIO3_PO.01						pu	ST	uaacfg	100
ULPI_DATA1	AH15	GPIO3_PO.02						pu	ST	uaacfg	100
ULPI_DATA2	AD17	GPIO3_PO.03						pu	ST	uaacfg	100
ULPI_DATA3	AJ15	GPIO3_PO.04					wake32	pu	ST	uaacfg	100
ULPI_DATA4	AJ18	GPIO3_PO.05					wake0	pu	ST	uabcfg	100
ULPI_DATA5	AH17	GPIO3_PO.06						pu	ST	uabcfg	100
ULPI_DATA6	AK18	GPIO3_PO.07						pu	ST	uabcfg	100
ULPI_DATA7	AL17	GPIO3_PO.00						pu	ST	uabcfg	100
ULPI_DIR	AL18	GPIO3_PY.01	SPI1A_DIN					z	ST	udacfg	100
ULPI_NXT	AG15	GPIO3_PY.02	SPI1A_SCK					z	ST	udacfg	100
ULPI_STP	AL16	GPIO3_PY.03	SPI1A_CS0					z	ST	udacfg	100
CAM (vddio_cam)											
CAM_I2C_SCL	AF8	GPIO3_PBB.01		I2C3_CLK			wake53	z	DD	gmecfg	50
CAM_I2C_SDA	AG8	GPIO3_PBB.02		I2C3_DAT			wake48	z	DD	gmecfg	50
CAM_MCLK	AL5	GPIO3_PCC.00			vimclk_alt3			pu	ST	gmgcfg	100
GPIO_PBB0	AK5	GPIO3_PBB.00				vimclk2_alt3		pd	ST	gmecfg	100
GPIO_PBB3	AK6	GPIO3_PBB.03	VGP3					pd	ST	gmecfg	100
GPIO_PBB4	AH6	GPIO3_PBB.04	VGP4					pd	ST	gmfcfg	100
GPIO_PBB5	AH5	GPIO3_PBB.05	VGP5					pd	ST	gmfcfg	100
GPIO_PBB6	AL6	GPIO3_PBB.06					wake45	pd	ST	gmfcfg	100
GPIO_PBB7	AJ5	GPIO3_PBB.07						pd	ST	gmfcfg	100
GPIO_PCC1	AJ6	GPIO3_PCC.01						pu	ST	gmhcfg	100
GPIO_PCC2	AL7	GPIO3_PCC.02						pu	ST	gmecfg	100
GMI (vddio_gmi)											
GEN2_I2C_SCL	Y2	GPIO3_PT.05	I2C2_CLK					z	DD	atcfg5	50
GEN2_I2C_SDA	AA2	GPIO3_PT.06	I2C2_DAT				wake47	z	DD	atcfg5	50

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
GPIO_PJ7	V4	GPIO3_PJ.07	UD3_TXD				arm_jtag0	z	CZ	atcfg4	30
GPIO_PB0	U4	GPIO3_PB.00	UD3_RXD					z	CZ	atcfg4	30
GPIO_PB1	V9	GPIO3_PB.01	UD3_CTS					z	CZ	atcfg4	30
GPIO_PK7	V5	GPIO3_PK.07	UD3_RTS				arm_jtag1	z	CZ	atcfg4	30
GPIO_PG0	V2	GPIO3_PG.00					boot_select0	z	CZ	atcfg2	30
GPIO_PG1	V6	GPIO3_PG.01					boot_select1	z	CZ	atcfg2	30
GPIO_PH2	AA4	GPIO3_PH.02	PM3_PWM2					pd	CZ	atcfg1	30
GPIO_PH3	V8	GPIO3_PH.03	PM3_PWM3					pd	CZ	atcfg1	30
GPIO_PH4	R5	GPIO3_PH.04	SDMMC2A_DAT0					pu	CZ	atcfg6	30
GPIO_PH5	R4	GPIO3_PH.05	SDMMC2A_DAT2					pd	CZ	atcfg6	30
GPIO_PH6	U8	GPIO3_PH.06	SDMMC2A_DAT3	tracedata3		DTV_DATA		pu	CZ	atcfg6	30
GPIO_PH7	U2	GPIO3_PH.07	SDMMC2A_CMD	tracedata4		DTV_CLK		pu	CZ	atcfg6	30
GPIO_PG2	Y7	GPIO3_PG.02		tracedata0			boot_select2	z	CZ	atcfg2	30
GPIO_PG3	AA5	GPIO3_PG.03		tracedata1			boot_select3	z	CZ	atcfg2	30
GPIO_PG4	Y3	GPIO3_PG.04				SPI4C_CS3	ram_code0	z	CZ	atcfg2	30
GPIO_PG5	AA3	GPIO3_PG.05				SPI4C_SCK	ram_code1	z	CZ	atcfg2	30
GPIO_PG6	Y8	GPIO3_PG.06				SPI4C_DOUT	ram_code2	z	CZ	atcfg2	30
GPIO_PG7	V3	GPIO3_PG.07				SPI4C_DIN	ram_code3	z	CZ	atcfg2	30
GPIO_PH0	Y6	GPIO3_PH.00	PM3_PWM0	tracedata2		DTV_VALID		pd	CZ	atcfg1	30
GPIO_PH1	U3	GPIO3_PH.01	PM3_PWM1					pd	CZ	atcfg1	30
GPIO_PK0	AA1	GPIO3_PK.00				soc_therm_oc3_n		pu	CZ	atcfg2	30
GPIO_PK1	R3	GPIO3_PK.01	SDMMC2A_CLK	traceclk				pd	CZ	atcfg6	30
GPIO_PJ0	U6	GPIO3_PJ.00					wake33	pu	CZ	atcfg3	30
GPIO_PJ2	W1	GPIO3_PJ.02				soc_therm_oc4_n	wake15	pu	CZ	atcfg4	30
GPIO_PK3	R2	GPIO3_PK.03	SDMMC2A_DAT4	tracectl				pu	CZ	atcfg6	30
GPIO_PK4	T1	GPIO3_PK.04	SDMMC2A_DAT5					pu	CZ	atcfg6	30
GPIO_PK2	Y1	GPIO3_PK.02					wake34	pu	CZ	atcfg2	30
GPIO_PI3	V7	GPIO3_PI.03				SPI4C_CS0		pu	CZ	atcfg2	30
GPIO_PI6	R1	GPIO3_PI.06				SDMMC2A_DAT7	wake35	pu	CZ	atcfg6	30
GPIO_PI2	V1	GPIO3_PI.02	SDMMC2A_DAT6	tracedata5				pu	CZ	atcfg6	30

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
GPIO_PI5	U7	GPIO3_PI.05	SDMMC2A_DAT1				wake23	pu	CZ	atcfg6	30
GPIO_PI1	AA6	GPIO3_PI.01					force_recovery	pu	CZ	atcfg2	30
GPIO_PI4	Y9	GPIO3_PI.04	SPI4C_CS1	tracedata6				pd	CZ	atcfg2	30
GPIO_PI7	Y4	GPIO3_PI.07		tracedata7		DTV_ERR_PSYNC		pu	CZ	atcfg2	30
GPIO_PC7	U1	GPIO3_PC.07					wake8	pu	CZ	atcfg3	30
GPIO_PI0	Y5	GPIO3_PI.00						pu	CZ	atcfg2	30
SDMMC2_COMP_PD	R6		SDMMC2_COMP_PD							sdio2comp	
SDMMC2_COMP_PU	U5		SDMMC2_COMP_PU							sdio2comp	
PCI Express CTRL (vddio_pex_ctl) ◇											
PEX_L0_CLKREQ_N	AK29	GPIO3_PDD.02	pe0_clkreq_l					z	ST	gpvcfg	100
PEX_L0_RST_N	AJ29	GPIO3_PDD.01	pe0_rst_l					z	ST	gpvcfg	100
PEX_L1_CLKREQ_N	AJ30	GPIO3_PDD.06	pe1_clkreq_l					z	ST	gpvcfg	100
PEX_L1_RST_N	AJ31	GPIO3_PDD.05	pe1_rst_l					z	ST	gpvcfg	100
PEX_WAKE_N	AG28	GPIO3_PDD.03	pe_wake_l				wake14	z	ST	gpvcfg	100
USB_VBUS_EN2	AG29	GPIO3_PFF.01	usb_vbus_en2					0	DD	gpvcfg	50
GPIO_PFF2	AG30	GPIO3_PFF.02	SATA_DA				wake59	z	DD	gpvcfg	50
PEX_CLK1P	AF26		PEX_CLK_OUT_1_P					0			
PEX_CLK1N	AG26		PEX_CLK_OUT_1_N					0			
PEX_CLK2P	AC26		PEX_CLK_OUT_2_P					0			
PEX_CLK2N	AC27		PEX_CLK_OUT_2_N					0			
SDMMC1 (vddio_sdmmc1)											
CLK2_OUT	K1	GPIO3_PW.05	extperiph2_clk					pd	ST	cdev2cfg	100
CLK2_REQ	L4	GPIO3_PCC.05						z	ST	cdev2cfg	100
SDMMC1_WP_N	L5	GPIO3_PV.03	SDMMC1_WP_N					pu	ST	sdio4cfg	100
SDMMC1_CLK	L7	GPIO3_PZ.00	SDMMC1_CLK					pd	CZ	sdio1cfg	30
SDMMC1_CMD	L8	GPIO3_PZ.01	SDMMC1_CMD					pu	CZ	sdio1cfg	30
SDMMC1_DAT0	L2	GPIO3_PY.07	SDMMC1_DAT0					pu	CZ	sdio1cfg	30
SDMMC1_DAT1	L3	GPIO3_PY.06	SDMMC1_DAT1				wake13	pu	CZ	sdio1cfg	30
SDMMC1_DAT2	L1	GPIO3_PY.05	SDMMC1_DAT2					pu	CZ	sdio1cfg	30
SDMMC1_DAT3	J8	GPIO3_PY.04	SDMMC1_DAT3					pu	CZ	sdio1cfg	30

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
SDMMC1_COMP_PD	L6		SDMMC1_COMP_PD							sdio1comp	
SDMMC1_COMP_PU	J7		SDMMC1_COMP_PU							sdio1comp	
SDMMC3 (vddio_sdmmc3)											
SDMMC3_CLK	F5	GPIO3_PA.06	SDMMC3_CLK					pd	CZ	sdio3cfg	30
SDMMC3_CMD	F2	GPIO3_PA.07	SDMMC3_CMD					pu	CZ	sdio3cfg	30
SDMMC3_DAT0	H2	GPIO3_PB.07	SDMMC3_DAT0					pu	CZ	sdio3cfg	30
SDMMC3_DAT1	H1	GPIO3_PB.06	SDMMC3_DAT1				wake3	pu	CZ	sdio3cfg	30
SDMMC3_DAT2	F1	GPIO3_PB.05	SDMMC3_DAT2					pu	CZ	sdio3cfg	30
SDMMC3_DAT3	G1	GPIO3_PB.04	SDMMC3_DAT3					pu	CZ	sdio3cfg	30
SDMMC3_CLK_LB_OUT	F4	GPIO3_PEE.04	SDMMC3_CLK_LB_OUT					z	CZ	sdio3cfg	30
SDMMC3_CLK_LB_IN	F3	GPIO3_PEE.05	SDMMC3_CLK_LB_IN					pd	CZ	sdio3cfg	30
SDMMC3_COMP_PD	E5		SDMMC3_COMP_PD							sdio3comp	
SDMMC3_COMP_PU	E2		SDMMC3_COMP_PU							sdio3comp	
SDMMC4 (vddio_sdmmc4)											
SDMMC4_CLK	G31	GPIO3_PCC.04	SDMMC4_CLK					pd	LV	gmacfg	15
SDMMC4_CMD	E31	GPIO3_PT.07	SDMMC4_CMD					pu	LV	gmacfg	15
SDMMC4_DAT0	F29	GPIO3_PAA.00	SDMMC4_DAT0					pu	LV	gmacfg	15
SDMMC4_DAT1	F30	GPIO3_PAA.01	SDMMC4_DAT1				wake10	pu	LV	gmacfg	15
SDMMC4_DAT2	E28	GPIO3_PAA.02	SDMMC4_DAT2					pu	LV	gmacfg	15
SDMMC4_DAT3	H31	GPIO3_PAA.03	SDMMC4_DAT3					pu	LV	gmacfg	15
SDMMC4_DAT4	D31	GPIO3_PAA.04	SDMMC4_DAT4					pu	LV	gmacfg	15
SDMMC4_DAT5	E30	GPIO3_PAA.05	SDMMC4_DAT5					pu	LV	gmacfg	15
SDMMC4_DAT6	E29	GPIO3_PAA.06	SDMMC4_DAT6					pu	LV	gmacfg	15
SDMMC4_DAT7	F28	GPIO3_PAA.07	SDMMC4_DAT7					pu	LV	gmacfg	15
SDMMC4_COMP_PD	H29		SDMMC4_COMP_PD								
SDMMC4_COMP_PU	H30		SDMMC4_COMP_PU								
SYS (vddio_sys, vddio_sys_2)											
KB_COL0	AD30	GPIO3_PQ.00					wake51	pu	ST	aocfg2	100
KB_COL1	AC28	GPIO3_PQ.01						pu	ST	aocfg2	100
KB_COL2	AD28	GPIO3_PQ.02						pu	ST	aocfg2	100

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
KB_COL3	AD31	GPIO3_PQ.03						pu	ST	aocfg2	100
KB_COL4	AF28	GPIO3_PQ.04			SDMMC3_WP_N			pu	ST	aocfg2	100
KB_COL5	AA27	GPIO3_PQ.05					wake54	pu	ST	aocfg2	100
KB_COL6	AD29	GPIO3_PQ.06						pu	ST	aocfg2	100
KB_COL7	AA25	GPIO3_PQ.07						pu	ST	aocfg2	100
KB_ROW0	W31	GPIO3_PR.00						pd	ST	aocfg1	100
KB_ROW1	Y26	GPIO3_PR.01						pd	ST	aocfg1	100
KB_ROW10	AA31	GPIO3_PS.02				UA3_RXD	wake9	pd	ST	aocfg2	100
KB_ROW11	V28	GPIO3_PS.03						pd	ST	aocfg2	100
KB_ROW12	Y27	GPIO3_PS.04					wake25	pd	ST	aocfg2	100
KB_ROW13	AF29	GPIO3_PS.05					wake26	pd	ST	aocfg2	100
KB_ROW14	AC30	GPIO3_PS.06					wake28	pd	ST	aocfg2	100
KB_ROW15	Y25	GPIO3_PS.07		soc_therm_oc1_n			wake29	pd	ST	aocfg2	100
KB_ROW16	AA26	GPIO3_PT.00						pd	ST	aocfg2	100
KB_ROW17	AC29	GPIO3_PT.01						pd	ST	aocfg2	100
KB_ROW2	AF30	GPIO3_PR.02						pd	ST	aocfg1	100
KB_ROW3	AC31	GPIO3_PR.03			SYS_CLK_REQ			1	ST	aocfg1	100
KB_ROW4	Y29	GPIO3_PR.04					wake50	pd	ST	aocfg1	100
KB_ROW5	Y31	GPIO3_PR.05						pd	ST	aocfg1	100
KB_ROW6	AB31	GPIO3_PR.06			DCA_LSPII			pd	ST	aocfg1	100
KB_ROW7	Y30	GPIO3_PR.07					wake49	pd	ST	aocfg1	100
KB_ROW8	AA29	GPIO3_PS.00					wake27	pd	ST	aocfg2	100
KB_ROW9	AA28	GPIO3_PS.01				UA3_TXD		pd	ST	aocfg2	100
SDMMC3_CD_N	V24	GPIO3_PV.02	SDMMC3_CD_N				wake56	pu	ST	aocfg2	100
CLK_32K_OUT	J6	GPIO3_PA.00		soc_therm_oc2_n				pd	ST	aocfg2	100
PWR_I2C_SCL	J4	GPIO3_PZ.06	I2CPMU_CLK					z	ST	aocfg1	50
PWR_I2C_SDA	J3	GPIO3_PZ.07	I2CPMU_DAT				wake46	z	ST	aocfg1	50
JTAG_RTCK	J2		RTCK					pu	ST	aocfg0	50
JTAG_TRST_N	H4		JTAG_TRST_N					pd	ST		50
JTAG_TDO	J1		JTAG_TDO					0	ST	aocfg0	100

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
JTAG_TMS	J5		JTAG_TMS					pu	ST		100
JTAG_TCK	H6		JTAG_TCK						ST		100
JTAG_TDI	H5		JTAG_TDI					pu	ST		100
TEST_MODE_EN	H7		TEST_MODE_						ST		100
SYS_RESET_N	AA30		SYS_RESET_N								
CLK_32K_IN	H3		CLK_32K_IN					z	ST	aocfg2	100
CORE_PWR_REQ	Y28		PWRON					1			
CPU_PWR_REQ	V25		CPU_PWR_REQ					0			
PWR_INT_N	V30		PMICINTR				wake18	z			
RESET_OUT_N	Y24					RESET_OUT_N		0			
UART (vddio_uart)											
CLK3_OUT	P7	GPIO3_PEE.00	extperiph3_clk					z	ST	dev3cfg	100
CLK3_REQ	M7	GPIO3_PEE.01						z	ST	dev3cfg	100
DAP4_DIN	P3	GPIO3_PP.05	I2S3_SDATA_IN					pd	ST	dap4cfg	100
DAP4_DOUT	P5	GPIO3_PP.06	I2S3_SDATA_OUT					pd	ST	dap4cfg	100
DAP4_FS	P1	GPIO3_PP.04	I2S3_LRCK					pd	ST	dap4cfg	100
DAP4_SCLK	N1	GPIO3_PP.07	I2S3_SCLK					pd	ST	dap4cfg	100
GEN1_I2C_SCL	P6	GPIO3_PC.04	I2C1_CLK					z	DD	dbgcfg	50
GEN1_I2C_SDA	M6	GPIO3_PC.05	I2C1_DAT				wake44	z	DD	dbgcfg	50
GPIO_PU0	R7	GPIO3_PU.00		UA3_TXD				z	ST	dbgcfg	100
GPIO_PU1	P2	GPIO3_PU.01		UA3_RXD				z	ST	dbgcfg	100
GPIO_PU2	M10	GPIO3_PU.02		UA3_CTS				z	ST	dbgcfg	100
GPIO_PU3	P8	GPIO3_PU.03		UA3_RTS				z	ST	dbgcfg	100
GPIO_PU4	M9	GPIO3_PU.04						z	ST	dbgcfg	100
GPIO_PU5	M4	GPIO3_PU.05					wake6	z	ST	dbgcfg	100
GPIO_PU6	M5	GPIO3_PU.06					wake7	z	ST	dbgcfg	100
UART2_CTS_N	M1	GPIO3_PJ.05		UB3_CTS				pu	ST	uart2cfg	100
UART2_RTS_N	P4	GPIO3_PJ.06		UB3_RTS				pu	ST	uart2cfg	100
UART2_RXD	L9	GPIO3_PC.03	IR3_RXD					pu	ST	uart2cfg	100
UART2_TXD	M8	GPIO3_PC.02	IR3_TXD					pu	ST	uart2cfg	100

Ball Name	Location	Pin Muxing					General				
		GPIO	SFIO0	SFIO1	SFIO2	SFIO3	Wake Capable	POR	Pad Type	Pad Control Group	Pull Strength (kΩ)
UART3_CTS_N	R8	GPIO3_PA.01	UC3_CTS				wake55	pu	ST	uart3cfg	100
UART3_RTS_N	R9	GPIO3_PC.00	UC3_RTS					pu	ST	uart3cfg	100
UART3_RXD	M3	GPIO3_PW.07	UC3_RXD					pu	ST	uart3cfg	100
UART3_TXD	M2	GPIO3_PW.06	UC3_TXD					pu	ST	uart3cfg	100
HV (vddio_hv) †											
OWR	AA7		OWR					z	OD	owrcfg	100
HDMI_CEC	AD7	GPIO3_PEE.03	CEC				wake52	z	DD	ceccfg	50
HDMI_INT	AC3	GPIO3_PN.07					wake4	pd	OD	hvcfg0	100
DDC_SCL	AC7	GPIO3_PV.04	I2C4_CLK					z	OD	ddccfg	100
DDC_SDA	AC8	GPIO3_PV.05	I2C4_DAT					z	OD	ddccfg	100
SPDIF_OUT	AC4	GPIO3_PK.05	SPDIF_OUT					pu	ST	dap5cfg	100
SPDIF_IN	AA8	GPIO3_PK.06	SPDIF_IN				wake57	pd	ST	dap5cfg	100
USB_VBUS_EN0	AB1	GPIO3_PN.04	usb_vbus_en0					0	DD	usb_vbus_en_cfg	50
USB_VBUS_EN1	AC1	GPIO3_PN.05	usb_vbus_en1					0	DD	usb_vbus_en_cfg	50
DP_AUX_CH0_P	AC6		I2C6_CLK					z		ddccfg	N/A
DP_AUX_CH0_N	AC5		I2C6_DAT					z		ddccfg	N/A
DP_HPD	AC2	GPIO3_PFF.00	DP_HPD					z	ST	dap5cfg	100

† When VDDIO_HV is operated at 1.8V, only I2C4 SFIO supported. GPIOs supported on other GPIO capable pins.

◇ If VDDIO_PEX_CTL is operated below 3.3V, only GPIO functionality supported on the pins

Table 15 Single Function I/O

Ball Name	Location
DDR	
DDR_A0	E14
DDR_A1	D14
DDR_A2	E15
DDR_A3	E12
DDR_A4	D12
DDR_A5	F12
DDR_A6	C12
DDR_A7	F14
DDR_A8	D15
DDR_A9	B12
DDR_A10	D18
DDR_A11	G17
DDR_A12	A16
DDR_A13	C20
DDR_A14	E17
DDR_A15	E18
DDR_BA0	F18
DDR_BA1	D20
DDR_BA2	H15
DDR_CAS_N	C14
DDR_CKE0	A13
DDR_CKE1	A14
DDR_CLK	G14
DDR_CLK_N	H14
DDR_CLKB	H18
DDR_CLKB_N	G18
DDR_CS0_N	B14
DDR_CS1_N	A12
DDR_DM0	C1
DDR_DQS0N	D5
DDR_DQS0P	C5
DDR_DQ0	A3
DDR_DQ1	A4
DDR_DQ2	B5
DDR_DQ3	C2
DDR_DQ4	B3
DDR_DQ5	B2
DDR_DQ6	C3
DDR_DQ7	A5
DDR_DM1	B9
DDR_DQS1N	H9
DDR_DQS1P	G9
DDR_DQ8	C9
DDR_DQ9	F9
DDR_DQ10	G8
DDR_DQ11	F8
DDR_DQ12	E9
DDR_DQ13	A9
DDR_DQ14	D9
DDR_DQ15	E8
DDR_DM2	B6
DDR_DQS2N	D8
DDR_DQS2P	C8
DDR_DQ16	A8
DDR_DQ17	B8
DDR_DQ18	C6
DDR_DQ19	E6
DDR_DQ20	A7
DDR_DQ21	A6
DDR_DQ22	D6
DDR_DQ23	F6
DDR_DM3	C11
DDR_DQS3N	G11
DDR_DQS3P	H11
DDR_DQ24	G12
DDR_DQ25	H12
DDR_DQ26	A11
DDR_DQ27	E11
DDR_DQ28	A10
DDR_DQ29	B11
DDR_DQ30	F11
DDR_DQ31	D11
DDR_DM4	F21
DDR_DQS4N	H20
DDR_DQS4P	H21
DDR_DQ32	G21
DDR_DQ33	A21
DDR_DQ34	E21
DDR_DQ35	F20
DDR_DQ36	G20
DDR_DQ37	D21
DDR_DQ38	B21
DDR_DQ39	C21
DDR_DM5	B24
DDR_DQS5N	D26
DDR_DQS5P	C26
DDR_DQ40	D24
DDR_DQ41	C24
DDR_DQ42	E27
DDR_DQ43	A24
DDR_DQ44	E26

Ball Name	Location
DDR_DQ45	B26
DDR_DQ46	A25
DDR_DQ47	A26
DDR_DM6	F23
DDR_DQS6N	D23
DDR_DQS6P	E23
DDR_DQ48	A22
DDR_DQ49	E24
DDR_DQ50	A23
DDR_DQ51	C23
DDR_DQ52	B23
DDR_DQ53	G23
DDR_DQ54	F24
DDR_DQ55	H23
DDR_DM7	B27
DDR_DQS7N	B29
DDR_DQS7P	B30
DDR_DQ56	D27
DDR_DQ57	C29
DDR_DQ58	C27
DDR_DQ59	A29
DDR_DQ60	C31
DDR_DQ61	A27
DDR_DQ62	C30
DDR_DQ63	A28
DDR_ODT0	A15
DDR_ODT1	B15
DDR_RAS_N	G15
DDR_RESET_N	F15
DDR_WE_N	C15
DDR_ODT_B0	C18
DDR_ODT_B1	A18

Ball Name	Location
DDR_CS_B0_N	B18
DDR_CS_B1_N	A19
DDR_CKE_B0	A20
DDR_CKE_B1	B20
DDR_A_B3	H17
DDR_A_B4	E20
DDR_A_B5	F17
DDR_COMP_PU	C17
DDR_COMP_PD	D17
DSI_CSI	
CSI_A_CLK_N	AE11
CSI_A_CLK_P	AD11
CSI_A_D0_N	AK9
CSI_A_D0_P	AL9
CSI_A_D1_N	AE9
CSI_A_D1_P	AD9
CSI_B_D0_N	AK8
CSI_B_D0_P	AL8
CSI_B_D1_N	AJ9
CSI_B_D1_P	AH9
CSI_E_CLK_N	AJ8
CSI_E_CLK_P	AH8
CSI_E_D0_N	AF9
CSI_E_D0_P	AG9
DSI_A_CLK_N	AJ14
DSI_A_CLK_P	AH14
DSI_A_D0_N	AK11
DSI_A_D0_P	AL11
DSI_A_D1_N	AD14
DSI_A_D1_P	AE14
DSI_A_D2_N	AL15
DSI_A_D2_P	AK15

Ball Name	Location
DSI_A_D3_N	AG14
DSI_A_D3_P	AF14
DSI_B_CLK_N	AJ11
DSI_B_CLK_P	AH11
DSI_B_D0_N	AH12
DSI_B_D0_P	AJ12
DSI_B_D1_N	AE12
DSI_B_D1_P	AD12
DSI_B_D2_N	AL12
DSI_B_D2_P	AK12
DSI_B_D3_N	AF12
DSI_B_D3_P	AG12
CSI_DSI_RUP	AF11
CSI_DSI_RDN	AG11
LVDS / eDP	
LVDS0_TXD0N	AJ2
LVDS0_TXD0P	AJ3
LVDS0_TXD1N	AG3
LVDS0_TXD1P	AG4
LVDS0_TXD2N	AG5
LVDS0_TXD2P	AG6
LVDS0_TXD3N	AG1
LVDS0_TXD3P	AG2
LVDS0_TXD4N	AF3
LVDS0_TXD4P	AF4
LVDS0_RSET	AK3
LVDS0_PROBE	AL3
HDMI	
HDMI_TXCN	AF5
HDMI_TXCP	AF6
HDMI_TXD0N	AD5

Ball Name	Location
HDMI_TXD0P	AD6
HDMI_TXD1N	AD4
HDMI_TXD1P	AD3
HDMI_TXD2N	AD2
HDMI_TXD2P	AD1
HDMI_RSET	AF2
HDMI_PROBE	AE1
HSIC	
HSIC1_DATA	AF18
HSIC1_STROBE	AE18
HSIC2_DATA	AG18
HSIC2_STROBE	AD18
HSIC_REXT	AH18
USB 2.0	
USB0_ID	AK20
USB0_VBUS	AL20
USB0_DN	AH20
USB0_DP	AJ20
USB1_DN	AF20
USB1_DP	AG20
USB2_DN	AE20

Ball Name	Location
USB2_DP	AD20
USB_REXT	AL19
USB 3.0 + PEX	
USB3_RX0N	AL21
USB3_RX0P	AK21
USB3_TX0N	AJ21
USB3_TX0P	AH21
PEX_USB3_RX1N	AL23
PEX_USB3_RX1P	AK23
PEX_USB3_TX1N	AG21
PEX_USB3_TX1P	AF21
PEX_RX2N	AE21
PEX_RX2P	AD21
PEX_TX2N	AJ23
PEX_TX2P	AH23
PEX_RX3N	AK24
PEX_RX3P	AL24
PEX_TX3N	AG23
PEX_TX3P	AF23
PEX_RX4N	AL26
PEX_RX4P	AK26
PEX_TX4N	AH26

Ball Name	Location
PEX_TX4P	AJ26
PEX_REFCLKN	AJ24
PEX_REFCLKP	AH24
PEX_TESTCLKN	AF24
PEX_TESTCLKP	AG24
PEX_TERMP	AL22
SATA	
SATA_L0_RXP	AJ27
SATA_L0_RXN	AH27
SATA_L0_TXP	AL27
SATA_L0_TXN	AK27
SATA_TESTCLKP	AG27
SATA_TESTCLKN	AF27
SATA_TERMP	AL25
THERM	
THERM_DP	U28
THERM_DN	U29
XTAL	
XTAL_IN	E3
XTAL_OUT	E4

Table 16 Power

Ball Name	Location
AO	
VDD_RTC	AB12
CORE CLOCKS	
AVDD_OSC	D1
AVDD_PLL_APC2C3	B17
AVDD_PLL_C4	P10
AVDD_PLL_CG	J31
AVDD_PLL_EREFE	AG31
AVDD_PLL_M	K16
AVDD_PLL_UD2DPD	AL4
AVDD_PLL_UTMIP	AB15
AVDD_PLL_X	L31
DIGITAL I/O	
VDDIO_AUDIO	K31
VDDIO_BB	AC14
VDDIO_CAM	AC11
VDDIO_GMI	U9, V10
VDDIO_HV	Y10
VDDIO_SDMMC1	P9
VDDIO_SDMMC3	E1
VDDIO_SDMMC4	F31
VDDIO_SYS	V23
VDDIO_SYS_2	L10
VDDIO_UART	U10
DISPLAY / CAMERA	
AVDD_CSI_DSI	AK14, AL13, AL14

Ball Name	Location
AVDD_HDMI	AA9, AA10
AVDD_HDMI_PLL	AH1
AVDD_LVDS0_IO	AJ1
AVDD_LVDS0_PLL	AF1
USB 2.0 / HSIC	
AVDD_USB	AC12
VDDIO_HSIC	AC15
USB 3.0 + PCIe	
AVDDIO_PEX	AB17, AC17, AC18
DVDDIO_PEX	AB20, AC20, AB18
AVDD_PEX_PLL	AC21
HVDD_PEX	AL29
HVDD_PEX_PLL_E	AL28
VDDIO_PEX_CTL	AE31
SATA	
VDDIO_SATA	AK30
HVDD_SATA	AF31
AVDD_SATA_PLL	AH31
FUSE	
VPP_FUSE	R10
DRAM	
VDDIO_DDR_HS	A17
VDDIO_DDR_MCLK	J15
VDDIO_DDR	J9, K11, J12, J14, J11, J17, J18, J20, J21, K10
GPU	
VDD_GPU	AA23, V17, V18, V19, V20, W13, W14, W15,

Ball Name	Location
	W16, W17, W18, U17, W19, W20, W21, Y19, Y20, Y23, U21, V21, U18, U19, U20, V13, V14, V15, V16
CPU	
VDD_CPU	R23, M19, M20, M22, M23, M24, M25, N13, N14, N15, N16, L23, N17, N18, N19, N20, N21, N22, N25, P13, P14, P15, L24, P16, P17, P18, P19, P20, P21, P22, R17, R18, R19, M13, R20, R21, R22, L25, L26, M26, L27, M27, P23, M14, M15, M16, M17, M18
CORE	
VDD_CORE	AA13, K14, K15, K17, K18, K20, K21, M12, N12, P12, R12, AA14, T12, U12, V12, W12, Y12, Y22, AA15, AA16, AA17, AA18, AA19, AA22, K12

Table 17 Power Controls

Ball Name	Location
CLK_32K_IN	H3
SYS_RESET_N	AA30
RESET_OUT_N	Y24
PWR_I2C_SCL (PMUI2C)	J4
PWR_I2C_SDA (PMUI2C)	J3
CORE_PWR_REQ	Y28
CPU_PWR_REQ	V25
PWR_INT_N	V30

Table 18 Sense

Ball Name	Location
VDD_CORE_SENSE	P25
VDD_CPU_SENSE	R26
VDD_GPU_SENSE	U26
GND_CORE_SENSE	P26
GND_CPU_SENSE	R27
GND_GPU_SENSE	U27
VVDD_CORE_PROBE	P27
VVDD_CPU_PROBE	R25
VVDD_GPU_PROBE	U25

Table 19 GND

Ball Name	Location
GND	A2, AB21, L16, L17, L18, L19, N2, N4, N7, N10, N11, N28, AB25, N30, P11, R11, R13, R14, R15, R16, T2, T4, T7, AB28, T10, T11, T13, T14, T15, T16, T17, T18, T19, T20, AB30, T21, T22, T25, T28, T30, U11, U13, U14, U15, U16, AC9, U22, V11, V22, W2, W4, W7, W10, W11, W22, W25, AD8, W28, W30, Y13, Y14, Y15, Y16, Y17, Y18, AK2, AE8, AE2, AB11, AB14, P24, R24, T31, V27, AE23, L22, AE4, AE7, AE10, A30, AE13, AE16, AE19, AE22, AE28, AE30, AH2, AH4, AH7, AH10, AB2, AH13, AH16, AH19, AH22, AH25, AH28, AH30, AK1, AK4, AK7, AB4, AK10, AK13, AK16, AK19, AK22, AK25, AK28, AK31, AL2, AL30, AB7, B1, B4, B7, B10, B13, B16, B19, B22, B25, B28, AB10, B31, D2, D4, D7, D10, D13, D16, D19, D22, D25, AB13, D28, D30, G2, G4, G7, G10, G13, G16, G19, G22, AB16, G24, G25, G28, G30, H8, H24, J23, K2, K4, K7, AB19, K13, AE24, K19, K22, AE25, K28, K30, L13, L14, L15

4.0 Interface and Signal Descriptions

This section describes device signals. Additional alternate use signals are described in the *Tegra K1 Series Processor Technical Reference Manual*. Signals are arranged in functional groups according to their associated interface.

4.1 External Memory Controller (EMC)

The EMC supports multiple devices with data widths of 8, 16, or 32 bits, where a 16-bit or 32-bit wide device may also be formed from two 8-bit or 16-bit devices respectively, all identical to form a single rank of either 32 or 64 bits. Up to 2 ranks are supported. Each rank can have different sizes constructed using different devices with the restriction that both ranks should have the same width and the size of the first rank is larger than or equal to the second rank.

Features:

- Single channel 64-bit data bus
  - 4 chip selects
  - 4 individually-controllable clock-enable
  - 4 individually-controllable ODT (DDR3L)
  - Operates in either single x32 or single x64 configuration
    - x32 configuration
      - 1 chip-select, clock control, and ODT for each rank
      - Supports 512MB, 1GB, 2GB, or 4GB attached DRAM
    - x64 configuration as two x32 sub-partitions
      - 1 chip-select, clock control, and ODT for each sub-partition of each rank
      - Supports 1GB, 2GB, 4GB, attached DRAM
  - Supports per-byte data masks
- x32 sub-partitions support for x64 configuration: additional address bits allow targeting different columns of each sub-partitions
- Each rank may support different sizes and geometries
  - Size of Rank 0 must be larger than or equal to Rank 1
  - Bank bits: 3
  - Row width: 12 to 16
  - Column width: 9 to 12
- BL8 support
- Low Latency Path and Fast Read/Response Path Support for the CPU Complex Cluster
- Support for low-power modes:
  - Software controllable entry/exit from: self-refresh, power down, deep power down
  - Hardware dynamic entry/exit from: power down, self-refresh
  - Support for intermittent or disabled DLL
  - Disable unused address/command taps based on mode
  - Pads use DPD-mode during idle periods
- Support for x32, x16, or x8 chips attached to the channel
  - DQ/DQS swizzling: MRR_BYTESEL need to match byte swizzling.
- Set/adjust trims per-byte and per-chip-select. Use PVT-compensated value and either add a PVT/freq-compensated adjustment to it (1/16, 1/8, 3/16 of a cycle) or a non-PVT- offset to it.
- Calibration logic is pad loading aware across different cmd mappings.

Table 20 DDR3L Signal Descriptions

Name	Type	Description
DDR_COMP_PD	Analog	DDR3L: connected to 34 ohm, 1% (closest 1% value) resistor to GND.

Name	Type	Description
DDR_COMP_PU	Analog	DDR3L: connected to 34 ohm, 1% (closest 1% value) resistor to same rail as VDDIO_DDR (1.35V for DDR3L)
DDR_RESET_N	Output	
DDR_DM[7:0]	Output	DRAM I/F Data Masks. Mask signals for write data. Data out when DM sampled high in same period with data being sent.
DDR_DQ[63:0]	Bidirectional	DRAM I/F 64-bit Data Bus
DDR_DQS[7:0]N	Bidirectional	DRAM I/F Data Strobes. Negative half of Differential pair of data strobes. Output for writes where data is edge aligned. Input for reads where data transition is centered.
DDR_DQS[7:0]P	Bidirectional	DRAM I/F Data Strobes. Positive half of Differential pair of data strobes. Output for writes where data is edge aligned. Input for reads where data transition is centered.
DDR_RAS_N	Output	DRAM I/F Row Add Select.
DDR_WE_N	Output	DRAM I/F Write Enable.
DDR_A[15:0] DDR_B_A[15:0]	Output	DRAM I/F DDR3L Address lines.
DDR_BA[2:0]	Output	DRAM I/F Bank Select.
DDR_CAS_N	Output	DRAM I/F Column Add Select.
DDR_CKE[1:0] DDR_CKE_B[1:0]	Output	DRAM I/F Clock Enable. When high, activates DDR internal clocks. Low deactivates the clocks.
DDR_CLK DDR_CLKB	Output	DRAM I/F Clock +
DDR_CLK_N DDR_CLKB_N	Output	DRAM I/F Clock –
DDR_CS[1:0]_N DDR_CS_B[1:0]_N	Output	DRAM I/F Chip Selects. Active low select lines, considered part of the command code. If single rank configuration, DDR_CS1_N can be used as A15 instead to support larger memories.
DDR_ODT[1:0] DDR_ODT_B[1:0]	Output	DRAM I/F DRAM on die terminator control.

4.2 SD/eMMC Controller

The SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is capable of interfacing to SD/eSD, SDIO cards, and eMMC devices. It has a direct memory interface and is capable of initiating data transfers between memory and external card. The SD/eMMC controller supports 2 different bus protocols: SD and eMMC bus protocol for eMMC. It has an APB Slave interface to access configuration registers. To access the iRAM for Micro Boot, the SD/eMMC controller relies on the AHB redirection arbiter in the Memory Controller.

Features:

- Adheres to SD Host Controller Standard Specification Version 4.0
- Supports eMMC Specification version 4.51
- Supports SD Physical Layer Specification Version 4.0
- Supports SDIO Physical Layer Specification Version 4.0 (up to UHS1, not UHS2)
- Supports of 8-bit data interface for eMMC/eSD cards
- Supports 4-bit data interface for SD cards

- Allows card to interrupt host in 1-bit, 4-bit, 8-bit SD modes.
- Supports Read wait Control, Suspend/Resume operation for SDIO cards
- Supports FIFO overrun and underrun condition by stopping SD clock
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TB.
- Supports eMMC 4.5.1 features including HS200 at 200MHz.

K1 series processors support four instances of this controller. These controllers can be routed to multiple physical locations on the device. The SD/SDIO controllers support Default and High Speed modes as well as the High and Low voltage ranges.

Table 21 SD/MMC Controller I/O Capabilities

Controller	Muxing Options	eMMC 4.51 Support	Supported Voltages (V)	I/O bus clock (MHz)	Maximum Bandwidth (MBps)	Notes
SDMMC1	SDMMC1	No	3.3, 1.8	208	104	SD/SDIO
SDMMC2	GMI	Yes	1.8	208	104	
SDMMC3	SDMMC3	No	3.3, 1.8	208	104	SD/SDIO
SDMMC4	SDMMC4	Yes	1.8	200	200	Bootable eMMC

Table 22 SDMMC4 (eMMC) Signal Descriptions

Signal Name	Type	Description
SDMMC4_CLK	Output	eMMC Clock: Connect to CLK pin of device
SDMMC4_CMD	Bidirectional	eMMC Command: Connect to CMD pin of device
SDMMC4_DAT[7:0]	Bidirectional	eMMC Data: Connect to Data pins of device
SDMMC4_COMP_PD	Analog	SDMMC Compensation Pull-down input. Connect to 1% resistor to GND. See Design Guide for correct resistor value(s)
SDMMC4_COMP_PU	Analog	SDMMC Compensation Pull-up input. Connect to 1% resistor to same rail powering the associated interface. See Design Guide for correct resistor value(s)

Table 23 SDMMC[3:1] Signal Descriptions

Signal Name	Type	Description
SDMMC[3,1]_CLK SDMMC2A_CLK	Output	SD/SDIO/MMC Clock
SDMMC[3,1]_CMD SDMMC2A_CMD	Bidirectional	SD/SDIO/MMC Command
SDMMC[3,1]_DAT[3:0] SDMMC2A_DAT[7:0]	Bidirectional	SD/SDIO/MMC Data bus
SDMMC3_CD_N	Input	SD Card Detect. No dedicated pin; driven by UART3_CTS_N or KB_COL5
SDMMC[3,1]_WP_N	Output	SD Write Protect. No dedicated pin; driven by HDMI_CEC or KB_COL4
SDMMC[3:1]_COMP_PD	Analog	SDMMC Compensation Pull-down input. Connect to 1% resistor to GND. See Design Guide for correct resistor value(s)
SDMMC[3:1]_COMP_PU	Analog	SDMMC Compensation Pull-up input. Connect to 1% resistor to same rail powering the associated interface. See Design Guide for correct resistor value(s)

Signal Name	Type	Description
SDMMC3_CLK_LB_IN SDMMC3_CLK_LB_OUT	Input Output	Clock Loop Back input/output – [Optional; internal delay available] SDMMC3_CLK_LB_IN connects to SDMMC_CLK_LB_OUT. Total trace length is the length of a round trip, from Tegra to connector and back.

4.3 Serial ATA (SATA) Controller

The SATA controller enables a control path from the Tegra processor to an external SATA device. A SSD / HDD / ODD drive can be connected. Controller can support the maximum throughput of a Gen 2 drive.

Features:

- SATA specification rev 3.1 and AHCI specification rev 1.3.1 compliant
  - Including all errata, ENC, and TP, except DHU (direct head unload)
- Device sleep feature support
  - Software initiated device sleep from slumber state only
  - Software initiated device sleep from any link states (active, partial, slumber)
  - Hardware initiated aggressive device sleep management
- Port multiplier with command based switching (CBS)support
- Supported Cables and connectors
  - Standard internal connector
  - Internal micro connector
  - Internal slimline connector
  - mSATA connector
  - BGA SSD interface
  - Not supported: External connector (eSATA), USM, Internal LIF-SATA

Table 24 SATA Signal Descriptions

Signal Name	Type	Description
SATA_TERMP		SATA Termination Compensation SATA pad termination compensation I/O. Optionally used by the SATA pads to calibrate their internal termination resistance.
SATA_REFCLKP SATA_REFCLKN	Input	SATA Reference Clocks These signals are a differential reference clock pair. They may be mapped to be associated with any of the PCI Express controllers via software configuration.
SATA_TESTCLKP SATA_TESTCLKN	Input	Test clock
SATA_L0_RXP SATA_L0_RXN	Input	Receive data, differential analog input
SATA_L0_TXP SATA_L0_TXN	Output	Transmit data, differential analog output

4.4 Display Interfaces

The Tegra Display Controller Complex integrates two independent display controllers. Each display controller is capable of providing an interface to external devices.

4.4.1 MIPI Display Serial Interface (DSI)

The Display Serial Interface (DSI) is a serial bit-stream replacement for the parallel MIPI DPI and DBI display interface standards. DSI reduces package pin-count and I/O power consumption. DSI support enables both display controllers to connect to an external display(s) with a MIPI DSI receiver. The DSI transfers pixel data from the internal display controller to an external third-party LCD module.

Features:

- PHY Layer
  - Start / End of Transmission. Other out-of-band signaling
  - Per DSI interface: 1 Clock Lane; up to 4 Data Lanes
  - Supports Link configuration – 1x4, 2x4
  - Supports Dual link operation in 2x4 configurations for asymmetrical/symmetrical split in both left-right side or odd-even group split schemes.
  - Maximum link rate 1.5Gbps as per MIPI D-PHY 1.1v version
  - Maximum 10MHz LP receive rate
- Lane Management Layer with Distributor
- Protocol Layer with Packet Constructor
- Supports MIPI DSI 1.0.1v version mandatory features
- Command Mode (One-shot) with Host and/or display controller as master
- Clocks
  - Bit Clock : Serial data stream bit-rate clock
  - Byte Clock : Lane Management Layer Byte-rate clock
  - Application Clock: Protocol Layer Byte-rate clock.
- Error Detection / Correction
  - ECC generation for packet Headers
  - Checksum generation for Long Packets
- Error recovery
- High Speed Transmit timer
- Low Power Receive timer
- Turnaround Acknowledge Timeout

Table 25 DSI Signal Descriptions

Name	Type	Description
DSI_[A:B]_CLK_N	Output	Output Clock Negative for interfaces A & B
DSI_[A:B]_CLK_P	Output	Output Clock Positive for interfaces A & B
DSI_[A:B]_D[3:0]_N	Bidirectional	Bidirectional Data Lanes [3,2,1,0] Negative for interfaces A & B
DSI_[A:B]_D[3:0]_P	Bidirectional	Bidirectional Data Lanes [3,2,1,0] Positive for interfaces A & B

1. The CSI_DSI_* signals are also available to the CSI signals and appear in the CSI Signal table.

4.4.2 High-Definition Multimedia Interface (HDMI)

HDMI support provides a unified method of transferring both audio and video data over a TMDS-compatible physical link to an audio/visual device.

Features:

- High-Definition Multimedia Interface (HDMI) Specification, version 1.4b
- High-bandwidth Digital Content Protection (HDCP) System Specification, version 1.4
- On-chip HDCP key storage, no external SecureROM required
- TMDS (Transition Minimized Differential Signaling) Phy I/F

Table 26 HDMI Signal Descriptions

Signal Name	Type	Description
HDMI_CEC	Bidirectional	Consumer Electronics Control (CEC) one-wire serial bus. CEC support requires 3rd party libraries be made available. Refer to the software release feature list for current software support.
DDC_SCL (I2C4)	Output	See I2C section. Serial Clock. Interface used for DDC for HDMI. As the pin only needs to drive low, and is 5V tolerant. This line must be pulled up to 5V to communicate correctly with an HDMI display.
DDC_SDA (I2C4)	Bidirectional	See I2C section. Serial Data. See DDC_SCL description.
HDMI_INT	Input	Interrupt. Used for Hot Plug detection.
HDMI_PROBE	Analog	Test only signal. Leave NC
HDMI_RSET	Analog	Reference Set. For current set resistor. Must be connected to external 1KΩ, 1% resistor to Ground
HDMI_TXCN	Output	Transmit Clock Negative
HDMI_TXCP	Output	Transmit Clock Positive
HDMI_TXD[2:0]N	Output	Data Lanes 0, 1 & 2 Negative
HDMI_TXD[2:0]P	Output	Data Lanes 0, 1 & 2 Positive

4.4.3 eDP / LVDS Interface

eDP / LVDS is a mixed-signal interface consisting of 5 differential serial I/O lanes and 1 PLL. This PLL is used to generate a high frequency bit-clock from an input pixel clock enabling the ability to handle 7-bit / 10-bit parallel data per lane at the pixel rate for the desired mode.

- LVDS mode: interface will take input pixel clock and handle 7-bit parallel data per lane at the pixel rate for LVDS mode. The pixel clock rate is guaranteed from 25MHz up to 165MHz.
- Embedded DisplayPort (eDP) mode: interface will take in a clock frequency of 270 MHz. (i.e. it will generate a 6x, 10x, and 20x high frequency clock (1.6GHz for RBR, 2.7GHz for HBR, and 5.4GHz for HBR2).

eDP mode has been tested according to the DP1.2b PHY Compliance Test Specification (CTS) even though eDP v1.4 supports lower swing voltages and additional intermediate bit rates. This means the following nominal voltage levels (400mV, 600mV, 800mV, 1200mV) and data rates (RBR, HBR, HBR2) are tested. This interface can be tuned to drive lower voltage swings below 400mV and can be programmed to other intermediate bit rates as per the requirements of the panel.

Table 27 eDP / LVDS Signal Descriptions

Signal Name	Type	Description
LVDS0_TXD[4:0]N LVDS0_TXD[4:0]P	Output	Differential transmitter outputs for lanes 0-4
LVDS0_RSET	Input	Reference Set. For current set resistor. Must be connected to external 1KΩ, 1% resistor to Ground
LVDS0_PROBE	Output	Test only signal. Leave NC

4.5 Audio Interfaces

4.5.1 I2S, PCM and TDM

K1 series processors support up-to five I2S interfaces. The I2S Controller transports streaming audio data between system memory and an audio codec. The controller supports I^2S format, Left-justified Mode format, Right-justified Mode format, and DSP mode format, as defined in the Philips inter-IC-sound (I^2S) bus specification. The timing in the following sections applies to any of these interfaces depending on whether they are configured for I2S/PCM or TDM mode.

The I2S and PCM (master and slave modes) interfaces support clock rates up to 24.5760MHz.

The I2S controller supports point-to-point serial interfaces for the I^2S digital audio streams. I^2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors, and those with digital TV sound may be directly connected to the I^2S controller. The controller also supports the PCM and telephony mode of data-transfer. Pulse-Code-Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. The Telephony mode is used to transmit and receive data to and from an external mono CODEC in a slot-based scheme of time-division multiplexing. The I2S controller supports bidirectional audio streams and can operate in half-duplex or full-duplex mode.

Features:

- Basic I2S modes to be supported (I2S, RJM, LJM and DSP) in both Master and Slave modes.
- PCM mode with short (one-bit-clock wide) and long-fsync (two bit-clocks wide) in both master and slave modes.
- NW-mode with independent slot-selection for both Tx and Rx
- TDM mode with flexibility in number of slots and slot(s) selection.
- Capability to drive-out a High-z outside the prescribed slot for transmission
- Flow control for the external input/output stream.
- Support for u-Law and A-Law compression/decompression

Table 28 I2S Signal Descriptions

Signal Name	Type	Description
I2S[3:0]_LRCK	Bidirectional	Frame Sync/Word Select. DAP pins support I2S/PCM audio. Interface can be master or slave
I2S[3:0]_SCLK	Bidirectional	Serial Clock/Bit Clock. DAP pins support I2S/PCM audio. Interface can be master or slave
I2S[3:0]_SDATA_IN	Input	Data In. DAP pins support I2S/PCM audio. Interface can be master or slave.
I2S[3:0]_SDATA_OUT	Output	Data Out. DAP pins support I2S/PCM audio. Interface can be master or slave.

4.5.2 Sony/Philips Digital Interface Format (S/PDIF)

The S/PDIF interface supports both professional and consumer applications. When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programs, at a 48 kHz sampling frequency and with a resolution of up to 24-bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz. When used in a consumer application, the interface primarily carries stereophonic programs with a resolution of up to 20-bits per sample.

The interface normally carries audio data coded as other than linear PCM-coded audio samples. The interface may also carry data related to computer software or signals coded using non-linear PCM.

Features:

- Five data formats: 16-bit, 20-bit, 24-bit, Raw, 16-bit packed
- Supported sample rates: 32, 44.1, 48, 88.2, 96, 176.4 and 192 kHz
- Flexible clock divisor for use to generate different "spdifout" data rate
- SPDIFOUT (Tx)
  - 16-word data FIFO for storage of outgoing audio data
  - 4-word user FIFO for storage of outgoing user data
  - 6-word page buffer for storage of outgoing channel status

Table 29 S/PDIF Signal Descriptions

Signal Name	Type	Description
SPDIF_IN	Input	Data In
SPDIF_OUT	Output	Data Out

4.6 USB and Baseband Interfaces

The K1 USB complex provides a mechanism to communicate with a PC and/or USB 2.0 peripherals, such as keyboard, mouse, and card readers; USB 3.0 peripherals, such as camera and storage devices, as a host using regular USB 3.0 ports; and to an on-board baseband controller using either USB HSIC or HSI interfaces. The USB complex consists of a single USB 3.0 controller and three USB 2.0 controllers. The USB 3.0 controller supports up to 2 regular USB 3.0 ports and their companion regular USB 2.0 ports. The USB 2.0 controllers support up to: 2x regular USB ports, 2x HSIC interfaces.

Tegra USB interfaces are compliant with the following USB specifications:

- *Universal Serial Bus Specification Revision 3.0*
- *Universal Serial Bus Specification Revision 2.0*, plus the following:
  - *USB Battery Charging Specification, version 1.0;* including Data Contact Detect protocol
  - Modes: Host and Device
  - Speeds: Low, Full, and High
- *Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0*

Refer to the appropriate specification for related interface timing details.

HSIC is only one of the interfaces available for the baseband. Other interfaces, such as SPI (Serial Peripheral Interface) and UART are described in the Peripheral Interfaces section. K1 series processors support multiple interfaces for baseband interconnections:

- USB HSIC
- HS-UART
- PCM to Baseband
- SDIO
- SPI (master)
- USB

USB 3.0 Controller

The USB 3.0 controller (XUSB) — USB 3.0 ports only operate in USB 3.0 Super Speed (SS) mode. All USB 3.0 ports share one Super Speed Bus Instance (5Gb/s bandwidth is distributed across these ports). The XUSB controller supports:

- xHCI programming model for scheduling transactions and interface management as a host that natively support USB 3.0, USB 2.0, and USB 1.1 transactions through USB 3.0 and USB 2.0 interfaces.
- Remote wakeup, wake on connect, wake on disconnect, and wake on overcurrent in all Tegra power states, including deep sleep mode.

USB 2.0 Controllers

All USB 2.0 controllers support:

- USB host controller registers and data structures are compliant to Intel ™ EHCI specification. The max packet size supported on any endpoint is 1024 bytes in high-speed mode, for both device and host modes.
- USB legacy (USB 1.1) Full and Low speed devices without a companion USB 1.1 host controller or host controller driver software using EHCI standard data structures.

USB 2.0 Controller #1 — Supports both USB 2.0 device and USB 2.0 host operations. USB recovery is supported only with USB 2.0 port 0 (USB0). USB controller #1 only connects to USB 2.0 port 0, which is the primary USB 2.0 port on Tegra devices. This controller shares the same USB 2.0 port 0 pins with the XUSB controller.

USB 2.0 Controller #2 — Can be configured to use regular USB 2.0 port 1 (USB1) or can be configured to use an HSIC interface that allows connection of an on-board peripheral supporting an HSIC interface to the Tegra processor. This controller shares the same USB 2.0 port 1 pins with the XUSB controller.

USB 2.0 Controller #3 — Can be configured to use regular USB 2.0 port 2 (USB2) or can be configured to use an HSIC interface that allows connection of an on-board peripheral supporting an HSIC interface to the Tegra processor. This controller shares the same USB 2.0 port 2 pins with the XUSB controller.

Figure 14 USB Controllers and Interface

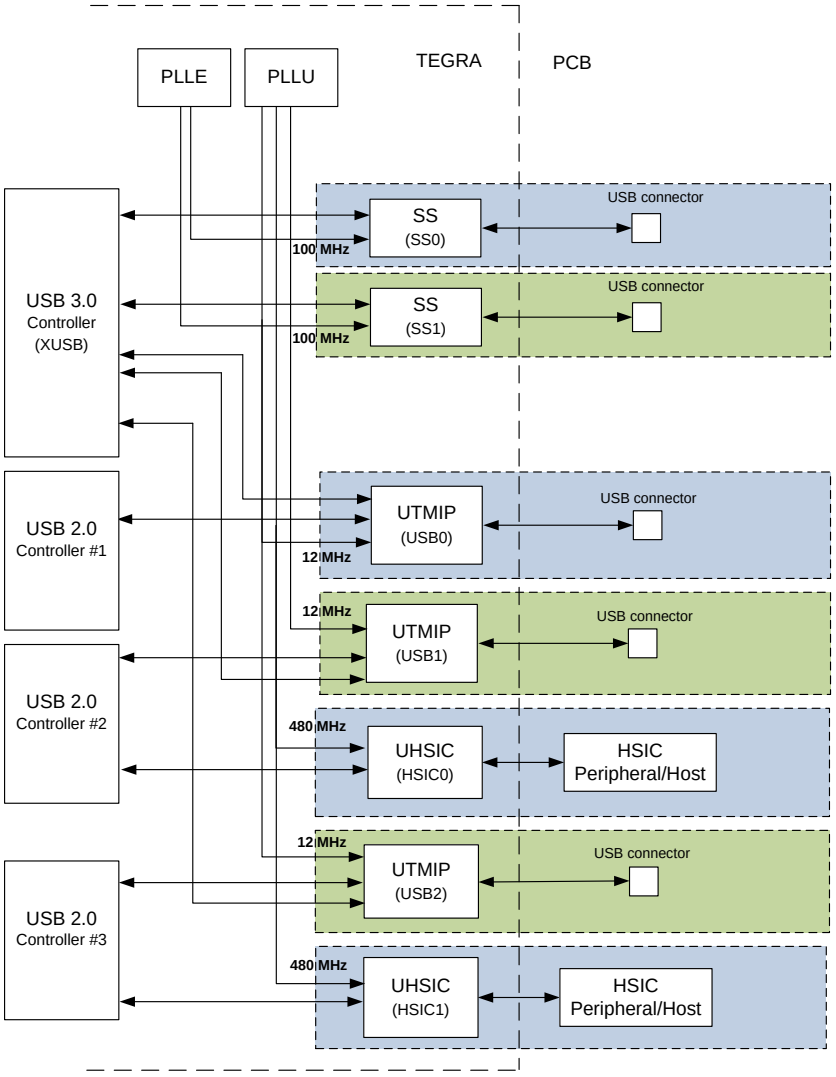


Table 30 USB Signals

Signal Name	Type	Description
USB_REXT	Analog	Reference External. Generates an accurate bias current. Has an external precision biasing PD resistor of 1 KΩ ± 1%.
USB[2:0]_DN	Analog	USB Data Negative
USB[2:0]_DP	Analog	USB Data Positive
USB0_ID	Analog	Indicates a device connection. If device detection is based on cable-ID, then the USB0_ID pin goes low whenever a USB device is connected
USB0_VBUS	Analog	When the USB interface is used in a mobile product as a Device, typically the USB interface is powered down, so the presence of USB_VBUS from a Host is

Signal Name	Type	Description
		detected by a PMU (Power Management Unit) which sends an interrupt or VBUS can be connected indirectly to a wake capable pin to wake the mobile device
USB3_REFCLKN	Input	Reference Clock Negative. Not used - Connect to GND
USB3_REFCLKP	Input	Reference Clock Positive. Not used - Connect to GND
USB3_RX0N	Input	Receive Data Negative input
USB3_RX0P	Input	Receive Data Positive input
USB3_TESTCLKN	Output	Test Clock Negative. Not used - Leave NC
USB3_TESTCLKP	Output	Test Clock Positive. Not used - Leave NC
USB3_TX0N	Output	Transmit Data Negative output
USB3_TX0P	Output	Transmit Data Positive output
PEX_TERMP		Termination. Connect to 2.5K, 1% (closest 1% value) resistor to GND

Table 31 USB High Speed Inter-Chip Interface (HSIC)

Signal Name	Type	Description
HSIC[2:1]_DATA	Bidirectional	Serial Data. Data is transferred when STROBE and DATA transition from IDLE to END-OF-IDLE which is defined by STROBE switching from high to low while data is low. Data is transferred for the next strobe transition and all subsequent transitions of STROBE until IDLE is again signaled.
HSIC[2:1]_STROBE	Bidirectional	Strobe. See Serial Data description
HSIC_REXT	Analog	Reference External. Generates an accurate bias current. Has an external precision biasing PD resistor of 1.0 KΩ ± 1%.

4.7 PCI Express (PCIe) Interface

Standard	Notes
PCI Express Base Specification Revision 2.0	Tegra processors meet the timing requirements for the Gen2 (5.0 GT/s) data rates. Refer to specification for complete interface timing details. Although NVIDIA validates K1 design complies with PCIe specification, PCIe software support may be limited. Specific PCIe use cases should be discussed with your NVIDIA representative.

K1 series processors integrate a x4 lane PCIe bridge to enable a control path from the Tegra chip to external PCIe devices. Two PCIe Gen2 controllers (one with a maximum width of x4 and the other with a maximum width of x1) support connections to one or two endpoints.

Table 32 PCIe Signal Descriptions

Signal Name	Type	Description
PEX_CLK[2:1]P PEX_CLK[2:1]N	Output	Clock
PEX_USB3_RX1P PEX_RX[4:2]P PEX_USB3_RX1N PEX_RX[4:2]N	Input	Receive data, differential analog input for each lane
PEX_USB3_TX1P PEX_TX[4:2]P PEX_USB3_TX1N PEX_TX[4:2]N	Output	Transmit data, differential analog output for each lane
PEX_REFCLKP PEX_REFCLKN	Output	PCI Express Reference Clocks These signals are a differential reference clock pair. They may be mapped to be associated with any of the PCI Express controllers via software configuration.
PEX_TESTCLKP PEX_TESTCLKN	Output	Test clock
PEX_L[1:0]_CLKREQ_N	Input	PCI Express Reference Clock Request This signal is used by a PCI Express device to indicate it needs the PEX_REFCLKP and PEX_REFCLKN to actively drive reference clock. It may be mapped to any of the PCI Express controllers via software configuration
PEX_WAKE_N	Input	PCI Express Wake This signal is used as the PCI Express defined WAKE# signal. When asserted by a PCI Express device, it is a request that system power be restored. No interrupt or other consequences result from the assertion of this signal.
PEX_L[1:0]_RST_N	Output	PCI Express Reset This signal provides a reset signal to all the PCI Express links. It must be asserted 100 ms after the power to the PCI Express slots has stabilized.
PEX_TERMP		PCI Express Termination Compensation PCI Express pad termination compensation I/O. Optionally used by the PCI Express pads to calibrate their internal termination resistance.

4.8 Serial Peripheral Interface

The SPI controller supports both master (up to 65Mhz) and slave (up to 45MHz) operation. It allows a duplex, synchronous, serial communication between the controller and external peripheral devices. It consists of 4 signals, SS_N (Chip select), SCK (clock), MOSI (Master data out and Slave data in) and MISO (Slave data out and master data in). The data is transferred on MOSI or MISO based on the data transfer direction on every SCK edge. The receiver always receives the data on the other edge of SCK.

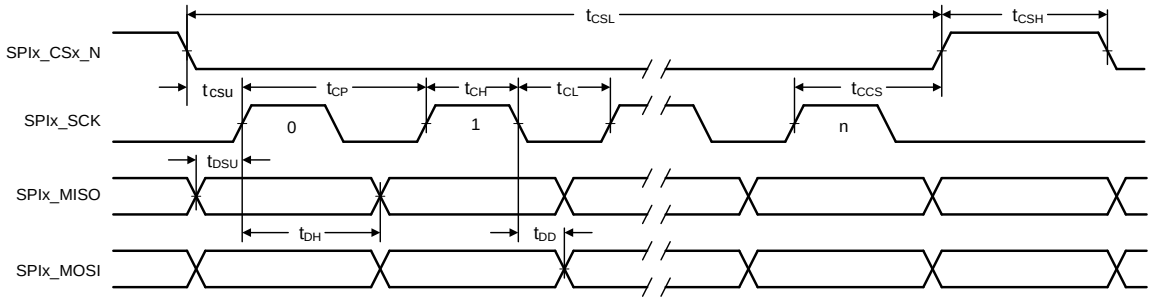
Features:

- Independent RX FIFO and TX FIFO.
- Software controlled bit-length supports packet sizes of 1 to 32 bits.
- Packed mode support for bit-length of 7 (8-bit packet size) and 15 (16-bit packet size).
- SS_N can be selected to be controlled by software, or it can be generated automatically by the hardware on packet boundaries.
- Receive compare mode (controller listens for a specified pattern on the incoming data before receiving the data in the FIFO).
- Simultaneous receive and transmit supported.
- Supports Master and Slave modes of operation

Table 33 SPI Signal Descriptions

Signal Name	Type	Description
SPI1A_CS0_N SPI4C_CS[3,1:0]_N	Bidirectional	Chip Select options for SPI[6:1]: Depending on pin multiplexing, there may be one or more chip select options for each SPI interface. Multiple available chip selects can be used to differentiate between two or more SPI slave devices
SPI1A_DIN SPI4C_DIN	Bidirectional	Master In: the Tegra MWP receives data (input) on this pin.
SPI1A_DOUT SPI4C_DOUT	Bidirectional	Master Out: the Tegra MWP drives data (output) onto this pin.
SPI1A_SCK SPI4C_SCK	Bidirectional	Serial Clock: clock phase and polarity is programmable.

Figure 15 SPI Master Timing Diagram



Note: CSx_N can be driven by Software or Hardware. When driven by Hardware, the polarity is programmable. Active low Hardware driven CSx_N is shown in the diagrams

Table 34 SPI Master Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CP}	SPIx_SCK period			20	ns
	SPIx_SCK duty cycle	45		55	%
t_{CH}	SPIx_SCK high time	9			ns
t_{CL}	SPIx_SCK low time	9			ns
t_{DSU}	SPIx_MISO setup to SPIx_SCK rising edge	3			ns
t_{DH}	SPIx_MISO hold from SPIx_SCK rising edge	2			ns
t_{DD}	SPIx_MOSI delay from SPIx_SCK falling edge	0		4	ns
t_{CSU}	SPIx_CSx_N setup time		0.5		t_{CP}
t_{CSL}	SPIx_CSx_N low time		$t_{CSU} + t_{CCS} + n$[1]		t_{CP}
t_{CSH}	SPIx_CSx_N high time		(INT_SIZE[2] + 1) / 4		t_{CP}
t_{CCS}	SPIx_SCK rising edge to SPIx_CSx_N rising edge		1		t_{CP}

1. n is the number of bits in the Bit Length of the transfer
2. INT_SIZE is the register bit field for selecting the idle time between transfers.

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

Note: SPIx_CSx_N can be driven by Software or Hardware. When driven by Hardware, the polarity is programmable. Active low Hardware driven. SPIx_CSx_N is shown in the diagrams.

Figure 16 SPI Slave Timing Diagram

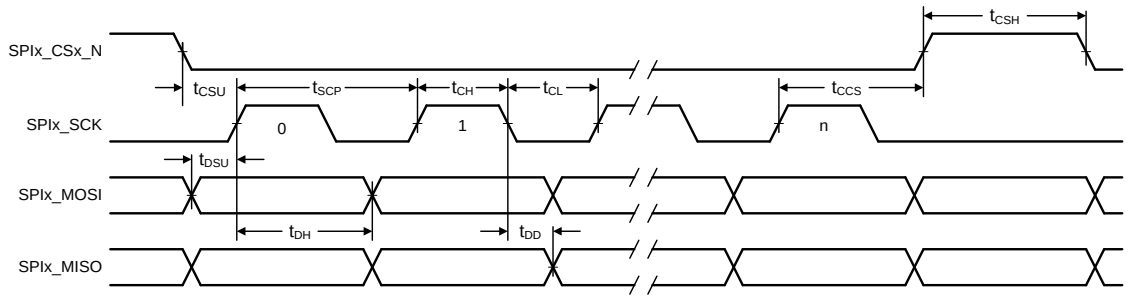


Table 35 SPI Slave Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCP}	SPIx_SCK period	$2*(t_{SDD}+ t_{MSU}$[1]$)$			ns
t_{SCH}	SPIx_SCK high time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCL}	SPIx_SCK low time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCSU}	SPIx_CSx_n setup time	1			t_{SCP}
t_{SCSH}	SPIx_CSx_n high time	1			t_{SCP}
t_{SCCS}	SPIx_SCK rising edge to SPIx_CSx_n rising edge	1		1	t_{SCP}
t_{SDSU}	SPIx_MOSI setup to SPIx_SCK rising edge	4			ns
t_{SDH}	SPIx_MOSI hold from SPIx_SCK rising edge	2			ns

Symbol	Parameter	Min	Typ	Max	Unit
t_{SDD}	SPIx_MISO delay from SPIx_SCK falling edge (Primary[2])	2.5		11	ns
t_{SDD}	SPIx_DIN delay from SPIx_SCLK falling edge (ALT1[2])	3.5		16	ns
t_{SDD}	SPIx_DIN delay from SPIx_SCLK falling edge (ALT2[2])	3		13	ns
t_{SDD}	SPIx_DIN delay from SPIx_SCLK falling edge (ALT3[2])	4		17	ns

1. t_{MSU} is the setup time required by the external master
2. Primary, ALT1/2/3 refers to the position of the SPI pins in the Signal Pinout Multiplexing tables in Section 3.1, *Signal List and Multiplexing Functions*.

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

4.9 Inter-Chip Communication (I2C) Controller

Standard	Notes
NXP inter-IC-bus (I^2C) specification	

The I2C controller implements an I^2C-bus specification compliant I2C master and a slave controller. The I2C controller supports multiple masters and slaves in: Standard-mode (up to 100Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1Mbit/s) and High-speed mode (up to 3.4Mbit/s) of operations. A general purpose I2C controller allows system expansion for I2C-based devices, such as AM/FM radio, remote LCD display, serial ADC/DAC, and serial EPROMs, as defined in the NXP inter-IC-bus (I^2C) specification. The I2C bus supports serial device communications to multiple devices. The I2C controller handles bus mastership with arbitration, clock source negotiation, speed negotiation for standard and fast devices, and 7-bit and 10-bit slave address support according to the I2C protocol and supports master and slave mode of operation.

Table 36 I2C Signal Descriptions

Signal Name	Type	Description
I2C[6,4:1]_CLK, I2CPMU_CLK	Bidirectional	Serial Clock for I2C interfaces 1 through 4, 6 and I2CPMU
I2C[6,4:1]_DAT, I2CPMU_DAT	Bidirectional	Serial Data for I2C interfaces 1 through 4, 6 and I2CPMU

4.10 UART Controller

UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

Features:

- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock upto 200MHz, baudrate of 12.5Mbits/second
- Data integrity by attaching parity bit to the data character
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs

- DMA capability for both TX and RX
- 8-bit x 36 deep TX FIFO
- 11-bit x 36 deep RX FIFO. 3 bits of 11 bits per entry will log the RX errors in FIFO mode (break, framing and parity errors as bits 10,9,8 of fifo entry)
- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped
- Priority interrupts mechanism
- Flow control support on RTS and CTS
- Internal loopback
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

Table 37 UART Signal Descriptions

Function	Type	Description
U[D:A]3_TXD	Output	UART[4:1]_TXD Transmit
U[D:A]3_RXD	Input	UART[4:1]_RXD Receive
U[D:A]3_CTS_N	Input	UART[4:1]_CTS_N Clear-to-send
U[D:A]3_RTS_N	Output	UART[4:1]_RTS_N Request-to-send

1. UB3_TXD/RXD supports IR functionality.

4.11 Video Input Interfaces

4.11.1 MIPI Camera Serial Interface (CSI)

Standard	Notes
MIPI CSI 2.0 Receiver specification	

The Camera Serial Interface (CSI) is based on MIPI CSI 2.0 standard specification and implements the CSI receiver which receives data from an external camera module with a CSI transmitter. It consists of two CSI receiver interfaces so it can receive serial transmission from two cameras.

Features:

- MIPI CSI 2.0 receiver
- Support for 3 camera sensors (any 2 can be active at the same time)
  - 1 x4 (single camera with 4 lane sensor)
  - 1 x4 + 1 x1 (one high resolution camera and another front facing low resolution camera)
  - 2 x4 (dual cameras for stereo with 4 lanes for each camera)
- Supported input data formats:
  - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
  - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b, YUV444-8b
  - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - DPCM: user defined
  - User defined: JPEG8
  - Embedded: Embedded control information
- Supports single-shot mode
- D-PHY Modes of Operation
  - High Speed Mode – High speed differential signaling up to 1.5Gbps; burst transmission for low power
  - Low Power Control – Single-ended 1.2V CMOS level. Low speed signaling for handshaking.
  - Low Power Escape –Low speed signaling for data, used for escape command entry only. 20Mbps

The two streams can come from any one or two of the three possible sources. If the two streams come from a single source, then the streams are separated using a filter indexed on different virtual channel numbers or data types. In case of separation using data types, the normal data type is separated from the embedded data type. Since there are only two pixel parsers, virtual channel and embedded data capability cannot be used at the same time.

Table 38 CSI Signal Descriptions

Signal Name	Type	Description
CSI_[A,E]_CLK_N	Input	CSI Clock Negative
CSI_[A,E]_CLK_P	Input	CSI Clock Positive
CSI_[A,B]_D[1:0]_N CSI_E_D0_N	Bidirectional	CSI Data Negative
CSI_[A,B]_D[1:0]_P CSI_E_D0_P	Bidirectional	CSI Data Positive
CSI_DSI_RDN	Analog	Reference Down. Provides a ground voltage reference point for the MIPI switching. A 50Ω , 1% (closest 1% value) resistor to GND is required.
CSI_DSI_RUP	Analog	Reference Up. Provides a source voltage reference point for the MIPI switching. A 450Ω, 1% (closest 1% value) resistor to the AVDD_CSI_DSI power rail is required.

4.11.2 Camera / VI (Video Input)

The Video Input (VI) is the cross bar unit for camera processing. It receives video from CSI and directs that data to either main memory or ISP.

Table 39 Camera and VI Signal Descriptions

Signal Name	Type	Description
CAM_I2C_SCL (I2C3)	Bidirectional	See I2C section
CAM_I2C_SDA (I2C3)	Bidirectional	See I2C section
VGP[5:3]	Bidirectional	Video Input General Purpose I/Os
VIMCLK_ALT3	Output	Video Input Master clock alternate output option 3

4.12 Miscellaneous Interfaces

4.12.1 Debug

K1 series processors have an optional JTAG interface that can be used for SCAN testing or for communicating with either integrated CPU. The JTAG interface is located on the SYS interface and powered by VDDIO_SYS.

Table 40 Debug Signal Descriptions

Signal Name	Type	Description
JTAG_RTCK	Input	Return Test Clock
JTAG_TCK	Input	Test Clock
JTAG_TDI	Input	Test Data In

Signal Name	Type	Description
JTAG_TDO	Output	Test Data Out
JTAG_TMS	Input	Test Mode Select
JTAG_TRST_N	Input	Test Reset
TRACECLK		
TRACEDATA[7:0]		

4.12.2 Pulse Width/Frequency Modulation (PWFM)

The Pulse Width Frequency Modulator (PWFM) is a frequency divider with a varying pulse width. The PWFM runs off a device clock programmed in the Clock and Reset controller, and can be any frequency up to the device clock maximum speed of 48MHz. The PWFM gets divided by 256 before being subdivided based on a programmable value. The PWFM has 4 pulse width frequency generators. An APB interface transports the PWFM register logic to the APB bus.

PWM signals are useful for LCD contrast and brightness control, VCO-generated clocks and other analog voltage references where high precision is not required.

Table 41 PWFM Signal Descriptions

Signal Name	Type	Description
PM3_PWM[3:0]	Output	Pulse Width Frequency Modulation. These are four outputs from the four pulse width frequency modulators. They output a frequency divided down from the device clock source and output a pulse of programmed width.

4.12.3 Serial Transport Stream (TS) Controller

Tegra processors incorporate a DTV interface to support compatible DTV, DVB-T & ISDB-T tuners. The serial TS controller converts the serially incoming DATA / forward error correction (FEC) packets to parallel packets, stores them to make visible to software and updates status registers for different error conditions (if any).

Features

- SLAVE support for serial TS interface for different mobile TV protocols.
- Frequency of operation 2-75MHz dtv_clk.
- Programmable polarity for valid/ packet sync and error signals.
- Programmable clock edge and clock mode (continuous/discontinuous).
- Bit swizzling and Byte swizzling capabilites.
- Capture of Reed-Solomon data.
- Statistics counters.
- DMA mastering capability.
- Error detection capability in any given packet.

Table 42 DTV Signal Descriptions

Signal Name	Type	Description
DTV_CLK	Input	DTV Clock.: Connect to Tuner CLK pin
DTV_DATA	Input	DTV Serial Data input: Connect to Tuner DATA pin
DTV_VALID	Input	DTV Valid input: Connect to Peripheral Tuner VALID pin
DTV_ERR_PSYNC	Input	DTV Error packet indicator or packet sync input: Connect to Tuner ERROR or PSYNC pin

5.0 Electrical Specification

5.1 Absolute Maximum Ratings

The absolute maximum ratings describe stress conditions. These parameters do not set minimum and maximum operating conditions that will be tolerated over extended periods of time. If the device is exposed to these parameters for extended periods of time, no guarantee is made and device reliability may be affected. It is not recommended to operate Tegra K1 series processors under these conditions, recommended operating conditions are provided in the following section

WARNING: Exceeding the listed conditions may damage and/or affect long-term reliability of the part. Tegra K1 series processors should never be subjected to conditions exceeding absolute maximum ratings.

Table 43. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
VDD_{MAX}	VDD_CPU	-0.5	1.36	V	
	VDD_CORE VDD_RTC VDD_GPU	-0.5	1.35	V	
	AVDDIO_PEX AVDD_PEX_PLL AVDD_HDMI_PLL AVDD_LVDS0_IO AVDD_PLL_APC2C4 AVDD_PLL_C4 AVDD_PLL_GX AVDD_PLL_EREFE AVDD_PLL_M AVDD_PLL_UD2DPD AVDD_PLL_X AVDD_SATA_PLL DVDDIO_PEX VDDIO_DDR_HS VDDIO_SATA	-0.5	1.1025	V	
	AVDD_CSI_DSI VDDIO_HSIC	-0.5	1.32	V	
	VDDIO_DDR VDDIO_DDR_MCLK	-0.5	1.32	V	Applicable when ▪ The power sequencing specification is violated OR ▪ VDD_RTC voltage is outside operating spec OR ▪ VDD_RTC is powered within spec AND software has configured this rail for 1.2V
			1.65	V	Applicable otherwise
	VDDIO_SDMMC3	-0.5	1.98	V	Applicable when ▪ The power sequencing specification is violated OR ▪ VDD_RTC voltage is outside operating spec OR ▪ VDD_RTC is powered within spec AND software has configured this rail for 1.2V
			3.63	V	Applicable otherwise

Symbol	Parameter	Min	Max	Unit	Notes
	VDDIO_BB VDDIO_UART VDDIO_AUDIO VDDIO_CAM VDDIO_SYS VDDIO_SYS_2 AVDD_OSC AVDD_PLL_UTMIP VDDIO_SDMMC1 VDDIO_SDMMC4 VDDIO_GMI	-0.5	1.98	V	
	AVDD_LVDS0_PLL VDDIO_PEX_CTL AVDD_HDMI AVDD_USB HVDD_PEX HVDD_PEX_PLL_E HVDD_SATA VDDIO_HV	-0.5	3.63	V	
	VDD_FUSE	-0.5	1.98	V	
V_{M_PIN}	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	1
V_{M_VBUS}	USB Supply voltage	-0.5 -0.5	6.0 0.5	V V	USB_VBUS enabled USB_VBUS not enabled
V_{ESD}	Electrostatic Discharge Voltage Human Body Model (HBM)		2000	V	
	Electrostatic Discharge Voltage Charge Device Model (CDM)		225	V	
T_J	Operating temperature as sensed from Thermal Diode	-25 -40	105 105	°C	CD575M CD575MI
T_{stg}	Storage temperature	-40	125	°C	

1. All power rails are with respect to GND. VDD = Common name for powered voltage rail under consideration
2. VBUS (V_{M_VBUS}) is an exception to the stated V_{M_PIN} specification and has its own absolute maximum specification.
3. T_J = Die Junction Temperature; Thermal Design Power at T_J (max) is the power dissipation for use in thermal design considering high-compute applications. Thermal Design Power (TDP) is not the theoretical maximum power the device can generate.

5.2 Recommended Operating Conditions

The parameters listed in following table are specific to a temperature range and operating voltage. Operating the Tegra processor beyond these parameters is not recommended. Exceeding these conditions for extended periods may adversely affect device reliability.

Table 44. Recommended Operating Conditions (Voltage Measured at Tegra Ball)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
VDD_{DC}	VDD_CPU CD570M (UCM #1) CD570M (UCM #2) CD570MI (UCM #1) CD575MI (UCM #2)	0.75	0.90	 1.26 1.12 1.21 1.1	V	DVFS setpoints (selected at runtime by software) Step size: 10mV
	VDD_GPU CD570M (UCM #1) CD570M (UCM #2) CD570MI (UCM #1) CD575MI (UCM #2)	0.75	0.90	 1.23 1.09 1.2 1.07	V	DVFS setpoints (selected at runtime by software) Step size: 10mV
	VDD_CORE / VDD_RTC CD570M (UCM #1) CD570M (UCM #2) CD570MI (UCM #1) CD575MI (UCM #2)	0.80	0.90	 1.15 1.01 1.13 1.0	V	DVFS setpoints (selected at runtime by software) Step size: 10mV
	AVDDIO_PEX AVDD_PEX_PLL AVDD_HDMI_PLL AVDD_LVDS0_IO AVDD_PLL_APC2C3 AVDD_PLL_C4 AVDD_PLL_CG AVDD_PLL_EREFE AVDD_PLL_M AVDD_PLL_UD2DPD AVDD_PLL_X AVDD_SATA_PLL DVDDIO_PEX VDDIO_DDR_HS VDDIO_SATA	0.9975	1.05	1.1025	V	
	AVDD_CSI_DSI VDDIO_HSIC	1.14	1.20	1.26	V	
	VDDIO_DDR VDDIO_DDR_MCLK	1.31	1.35	1.45	V	DDR3L

Symbol	Parameter	Min	Nom	Max	Unit	Notes
	VDDIO_BB VDDIO_UART VDDIO_AUDIO VDDIO_CAM VDDIO_SYS VDDIO_SYS_2 AVDD_PLL_UTMIP AVDD_OSC VDDIO_GMI VDDIO_SDMMC1 VDDIO_SDMMC4	1.71	1.80	1.89	V	
	AVDD_LVDS0_PLL VDDIO_SDMMC3	1.71	1.80, 3.30	3.465	V	LVDS (1.8V) and eDP (3.3V) modes
	VDDIO_HV VDDIO_PEX_CTL	1.71 2.60	1.80 2.8 – 3.3	1.89 3.465	V	When VDDIO_HV is operated at 1.8V, only I2C4 SFIO supported. GPIOs supported on other GPIO capable pins. If VDDIO_PEX_CTL is operated below 3.3V, only GPIO functionality supported on the pins
	AVDD_HDMI AVDD_USB HVDD_PEX HVDD_PEX_PLL_E HVDD_SATA	3.23	3.40	3.57	V	Recommended: AVDD_HDMI should not be tied to any other 3.3V rail to prevent leakage
	VDD_FUSE	1.71	1.80	1.89	V	

1. These voltage rails are intended to operate over the range defined by the Dynamic Voltage and Frequency Scaling (DVFS) mechanism.
2. Minimum core voltage may be updated at the end of the characterization.
3. At power on, VDD_CORE and VDD_RTC must run at 0.9V and VDD_CPU must be off. After power on with software enabled voltages can vary to accommodate different operating conditions.
4. Do not tie VDD_CORE and VDD_CPU voltage regulators together.
5. Min and Max values are absolute worst case DC specs for the voltage rail under any combination of workloads, silicon corners, temperature conditions, voltage regulator DC variance, and board level IR drops.

5.3 Digital Logic Characteristics

Voltages less than the minimum stated value can be interpreted as an undefined state or logic level low which may result in unreliable operation. Voltages exceeding the maximum value can damage and/or adversely affect device reliability.

Table 45. Digital I/O Characteristics

Pad Type	Symbol	Parameter	Min	Max	Unit	Notes
	V_{IL-XO}	Input Low Voltage	-0.5	0.1 x VDD	V	XTAL_OUT pin when used as input for external clock.
	V_{IH-XO}	Input High Voltage	0.9 x VDD	0.5 + VDD	V	XTAL_OUT when used as input for external clock.

Pad Type	Symbol	Parameter	Min	Max	Unit	Notes
ST	V_{IL} V_{IH} V_{OL} V_{OH}	Input Low Voltage Input High Voltage Output Low Voltage (I_{OL} = 1mA) Output High Voltage (I_{OH} - -1mA)	-0.5 0.75 x VDD 0.85 x VDD	0.25 x VDD 0.5 + VDD 0.15 x VDD	V	Weak PU Strength: 50 kΩ Weak PD Strength: 50 kΩ
DD	V_{IL} V_{IH} V_{OL} V_{OH}	Input Low Voltage Input High Voltage Output Low Voltage (I_{OL} = 1mA) Output High Voltage (I_{OH} - -1mA)	-0.5 0.75 x VDD 0.85 x VDD	0.25 x VDD 3.63 0.15 x VDD	V	3.3V tolerant pad Weak PU Strength: 50 kΩ Weak PD Strength: 50 kΩ
LV	V_{IL} V_{IH} V_{OL} V_{OH}	Input Low Voltage Input High Voltage Output Low Voltage (I_{OL} = 1mA) Output High Voltage (I_{OH} - -1mA)	-0.5 0.75 x VDD 0.85 x VDD	0.25 x VDD 0.5 + VDD 0.15 x VDD	V	Weak PU Strength: 15 kΩ Weak PD Strength: 15 kΩ
OD	V_{IL} V_{IH} V_{OL} V_{OH}	Input Low Voltage Input High Voltage Output Low Voltage (I_{OL} = 1mA) Output High Voltage	-0.5 0.75 x VDD NA	0.25 x VDD 5.3 0.15 x VDD	V	5V tolerant pad Weak PD Strength: 100 kΩ
CZ	V_{IL} V_{IH} V_{OL} V_{OH}	Input Low Voltage Input High Voltage Output Low Voltage (I_{OL} = 1mA) Output High Voltage (I_{OH} - -1mA)	-0.5 0.75 x VDD 0.85 x VDD	0.25 x VDD 0.5 + VDD 0.15 x VDD	V	Weak PU Strength: 15 kΩ Weak PD Strength: 15 kΩ
	$V_{IL\text{-}VBUS}$	VBUS Detect Input Low Voltage	-0.5	0.8	V	USB VBUS input.
	$V_{IH\text{-}VBUS}$	VBUS Detect Input High Voltage	3.35	5.25	V	USB VBUS input.
	C_{IN}	Pin Capacitance			pf	

5.4 DC Characteristics

The maximum operating currents are specified as the worst-case average current consumed by Tegra over any 6µs interval on worst-case silicon at worst-case temperature with nominal I/O loads and with power rails at maximum recommended operational voltages. These maximums do not apply to systems that fail to implement on-board decoupling and filtering networks specified by NVIDIA. The maximums have not been verified by characterization and are not guaranteed.

Power supply designs should reserve the specified current sourcing capability for Tegra. Additional current sourcing capability is required to drive other system-level components (including DRAM).

Table 46 Maximum Operating Currents

Logical Group	Rail	Maximum Current		Notes
CPU	VDD_CPU	(peak)	(sustained)	Peak measurement was taken over 6µs interval; sustained was collected over 1s.
	CD575M (UCM #1)	15.5 A	15.5 A	
	CD575M (UCM #2)	11.2 A	11.2 A	
	CD575MI (UCM #1)	13.2 A	13.2 A	
	CD575MI (UCM #2)	11.2 A	11.2 A	
GPU	VDD_GPU	(peak)	(sustained)	Peak measurement was taken over 6µs interval; sustained was collected over 1s.
	CD575M (UCM #1)	12 A	6.37 A	
	CD575M (UCM #2)	11 A	5.64 A	
	CD575MI (UCM #1)	11.4 A	5.64 A	

Logical Group	Rail	Maximum Current		Notes
	CD575MI (UCM #2)	10 A	5.19 A	
CORE	VDD_CORE	(peak) 3.7 A	(sustained) 2.5 A	Peak measurement was taken over 6µs interval; sustained was collected over 1s.
IO with DRAM	DDR3L			
	VDDIO_DDR	550 mA		Reads
		990 mA		Writes
	VDDIO_DDR_MCLK	35/40 mA		Reads/Writes
IO with Display / Camera	AVDD_CSI_DSI	146 mA		Assumption 2 DSI panels connected, Max resolution camera sensor.
	1080p Panel on HDMI			
	AVDD_HDMI_PLL	23 mA		
	AVDD_HDMI	48 mA		Connected TV
		90 mA		Disconnected TV
	2160p Panel on HDMI			
	AVDD_HDMI_PLL	35 mA		
	AVDD_HDMI	68 mA		Connected TV
		140 mA		Disconnected TV
	2560x1440			
	AVDD_LVDS0_IO	25 mA		
	AVDD_LVDS0_PLL	45 mA		
	3200x1800			
	AVDD_LVDS0_IO	35 mA		
	AVDD_LVDS0_PLL	66 mA		
Digital IO	VDDIO_AUDIO	16 mA		Based on 40pF load limit and 25/50 (DVFS) DAP/SPI frequencies
	VDDIO_CAM	5 mA		Based on 40pF load limit and 3.48/40.8/12.3 (DVFS) i2c/cam1_mclk/cam2_mclk frequencies
	VDDIO_HSIC	10 mA		UPM estimate +10%
	AVDD_OSC	3 mA		Measured on 12Mhz OSC
	VDDIO_SDMMC1	58 mA		Based on 30pF load, 200 MHz HS200 mode estimate, scaled by 1.8x correlation factor + 10% margin
	VDDIO_SDMMC3	58 mA		Based on 30pF load, 200 MHz HS200 mode estimate, scaled by 1.8x correlation factor + 10% margin
	VDDIO_SDMMC4	57 mA		Based on 30pF load, 200 MHz HS200 mode estimate + 10% margin
	VDDIO_SYS	15 mA		Based on 40pF load limit and 150 MHz BCL
	VDDIO_UART	51 mA		Based on 40pF load limit and 6.43/50 (DVFS) UART/SPI frequencies
USB	AVDD_USB	47 mA		Based on UPM estimates scaled to silicon +10%
	AVDD_PLL_UTMIP	11 mA		Based on UPM estimates scaled to silicon +10%

Logical Group	Rail	Maximum Current	Notes
USB 3.0	AVDD_1V05_A_PEX	148 mA	
	VDD_1V05_D_PEX	43 mA	
	AVDD_1V05_PEX_PLL	70 mA	
	AVDD_3V3_PEX	18 mA	
	AVDD_3V3_PEX_PLL_E	26 mA	

VDD_CPU current on the Tegra processor varies with workload. Typical workloads consume far less than stress and benchmark tests used to measure CPU and GPU performance. For example, executing a CPU stress test designed to maximize current consumption consumes approximately 30% more dynamic current than Dhrystone. Dhrystone is a traditional CPU benchmark. VDD_CPU current also varies with temperature and operating frequency. Software running on Tegra can limit the maximum VDD_CPU operating current by throttling CPU frequency as a function of temperature.

The following tables show the operating current limits at various temperatures for the maximum CPU frequency. Measurements were based on VDD_CPU peak current consumption (averaged over 6µs interval) as Tegra executes four instances of a CPU stress test designed to maximize current consumption. The measurements were taken on worst-case silicon at the specified temperature at voltage set by DVFS.

Tables list the CPU frequencies that silicon is capable of supporting at different levels of power delivery capacity. CPU frequency and voltage are actively managed by Tegra Power and Thermal Management Software and influenced by workload. Frequency may be throttled at higher temperatures (over 70C) resulting in a behavior that reduces CPU operating frequency. Observed chip-to-chip variance is due to NVIDIA ability to maximize performance (DVFS) on a per-chip basis, within available power budget.

NOTE: VDD_CPU current limits are preliminary and subject to change. Refer to the *K1 Interface Design Guide* for Feedback and Sense connections from the Tegra processor to the PMU and guidelines on trace impedance for both CORE and CPU rails.

Table 47 CD575M (UCM #1) CPU Maximum Current Limits

VDD_CPU Maximum Operating Current Limit (A)	Guaranteed CPU Operating Frequency			
	Tj <= 50C	Tj <= 70C	Tj <= 90C	Tj <= 105C
Quad-Core CPU Operation				
8.0	2.0GHz	1.88GHz	1.73GHz	1.53GHz
9.0	2.1GHz	2.0GHz	1.83GHz	1.63GHz
10.0	2.2GHz	2.1GHz	1.91GHz	1.81GHz
11.0	2.2GHz	2.2GHz	2.0GHz	1.88GHz
Dual-Core CPU Operation				
8.0 – 11.0	2.2GHz	2.2GHz	2.1GHz	2.1GHz
Single-Core CPU Operation				
8.0 – 11.0	2.2GHz	2.2GHz	2.1GHz	2.1GHz

NOTES: Some parts may exceed listed operating frequencies (up to a 2.2GHz) at lower temperatures.
UCM #1 – Operating time per day at max frequency: 20%

Table 48 CD575MI (UCM #1) CPU Maximum Current Limits

VDD_CPU Maximum Operating Current Limit (A)	Guaranteed CPU Operating Frequency			
	Tj <= 50C	Tj <= 70C	Tj <= 90C	Tj <= 105C
Quad-Core CPU Operation				
8.0	2.0GHz	1.88GHz	1.73GHz	1.53GHz
9.0	2.1GHz	2.0GHz	1.83GHz	1.63GHz
10.0	2.1GHz	2.1GHz	1.91GHz	1.81GHz
11.0	2.1GHz	2.1GHz	2.0GHz	1.88GHz
Dual-Core CPU Operation				
8.0 – 11.0	2.1GHz	2.1GHz	2.1GHz	2.1GHz
Single-Core CPU Operation				
8.0 – 11.0	2.1GHz	2.1GHz	2.1GHz	2.1GHz

NOTES: Some parts may exceed listed operating frequencies (up to a 2.1GHz) at lower temperatures.
UCM #1 – Operating time per day at max frequency: 20%

Table 49 CD575M, CD575MI (UCM #2) CPU Maximum Current Limits

VDD_CPU Maximum Operating Current Limit (A)	Guaranteed CPU Operating Frequency			
	Tj <= 50C	Tj <= 70C	Tj <= 90C	Tj <= 105C
Quad-Core CPU Operation				
8.0	1.91GHz	1.88GHz	1.73GHz	1.53GHz
9.0	1.91GHz	1.91GHz	1.83GHz	1.63GHz
10.0	1.91GHz	1.91GHz	1.91GHz	1.81GHz
11.0	1.91GHz	1.91GHz	1.91GHz	1.88GHz
Dual-Core CPU Operation				
8.0 – 11.0	1.91GHz	1.91GHz	1.91GHz	1.91GHz
Single-Core CPU Operation				
8.0 – 11.0	1.91GHz	1.91GHz	1.91GHz	1.91GHz

NOTES: Some parts may exceed listed operating frequencies (up to a 1.9GHz) at lower temperatures.
UCM #2 – Operating time per day at max frequency: 100%

6.0 Package and Thermal Specification

RoHS Compliance

Tegra processor packages are RoHS compliant. All Tegra series parts are lead free unless marked with "E" for Eutectic part number.

The Tegra product family meets the RoHS guidelines for electronic components, and hardware set forth in the European Union's Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Hazardous Substance (RoHS).

Storage and Handling

Refer to the packing label shipped with your order for specific storage, handling and expiration instructions.

Table 50. Typical Handling and Storage Environment

Symbol	Description	Relative Humidity (RH)	Minimum Temperature	Maximum Temperature
T_{STG}	Storage temperature (shelf life in sealed bag): 1 year	Less than 90 %	NA	40ºC
T_A	Floor Life: JEDEC MSL 3 (up to 168 hours after breaking the vacuum seal on the bag containing the device)[1]	Less than 60%	NA	30ºC

1. Compliant with IPC/JEDEC Moisture Sensitivity Level J-STD-020 MSL 4.

6.1 Thermal Characteristics

Table 51 provides package thermal characteristics under the following conditions:

- 0m/s air velocity surrounding the package
- Ambient operating temperature: 55ºC
- No thermal underfill epoxy present
- Board type defined by JEDEC Standard JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Table 51. Package Thermal Characteristics

Package	Θ_{JA} (˚C/W)	Θ_{JB} (˚C/W)	Θ_{JC} (˚C/W)	Ψ_{JB} (˚C/W)	Ψ_{JC} (˚C/W)
23 x 23 mm | 813 Ball FCBGA | 0.7 mm pitch	12.3	4.9 – 5.4	0.08	4.7 – 5.1	0.02

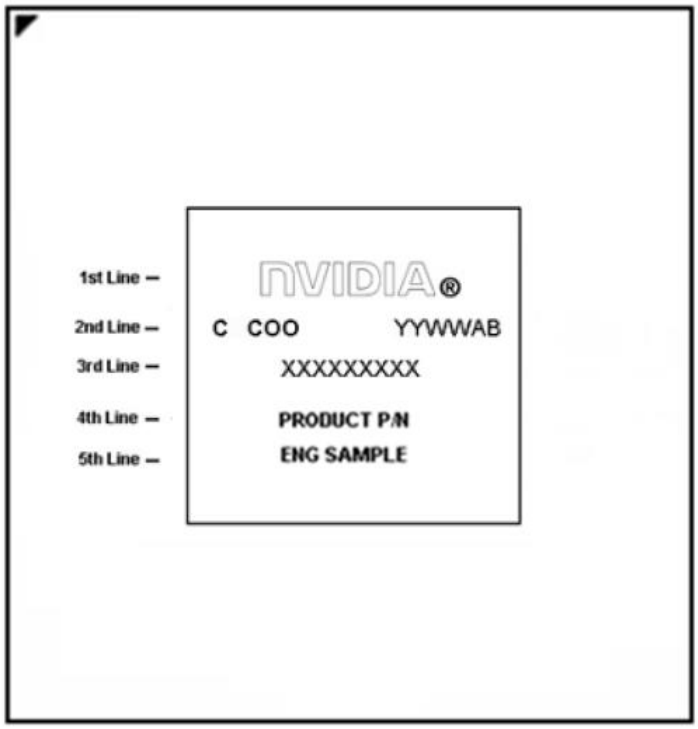
Notes:

- Θ_{JA} – Junction to Air thermal resistance (˚C/W)
- Θ_{JB} – Junction to Board thermal resistance (˚C/W)
- $\Theta_{JC} = \Theta_{JT}$ – Junction to Case (or top) thermal resistance (˚C/W)
- ψ_{JB} – Junction to Board thermal characterization parameter (˚C/W)
- ψ_{JT} – Junction to Top (case) thermal characterization parameter (˚C/W)
- Results are based on simulation results for JEDEC 4 Layer High K PCB. Actual values for Θ_{JA}, Θ_{JB}, and Θ_{JC} may differ in your system
- Ranges on ψ_{JB} and Θ_{JB} are based on temperature measured at the edge of the package or 1 mm from the package (as per JEDEC spec)

6.2 Package Marking

Complete product marking is done during assembly. All marking in each line is center justified within the marking area. All character font style is “Arial” or equivalent except in the company and logo area.

Figure 17 Package Marking Example



Pin 1 Location of Pin 1: upper left

1st Line NVIDIA Company Name

2nd Line C – Vendor ID
COO – Country of Origin
YYWW – Date Code
AB – Die Revision

3rd Line XXXXXXXXX – Assembly Lot Number up to 10 characters.

4th Line Product P/N*

5th Line Engineering Lots: ENG SAMPLE*
Qualification Lots: QUAL SAMPLE*
Production – blank

* Laser or ink

Table 52. Product Part Numbers & Package Marking

Product	Part Number		4th Line (Product P/N)	Package
	Tray	Tape & Reel		
CD575M	CD575M-A1	CD575M-R-A1	CD575M-A1	813 Ball FCBGA | 23x23mm
CD575MI	CD575MI-A1	CD575MI-R-A1	CD575MI-A1	813 Ball FCBGA | 23x23mm

6.3 Package Drawing & Dimensions

Figure 18 23 x 23 mm 6L 0.7mm 813 Ball FCBGA Package Drawing – Top View

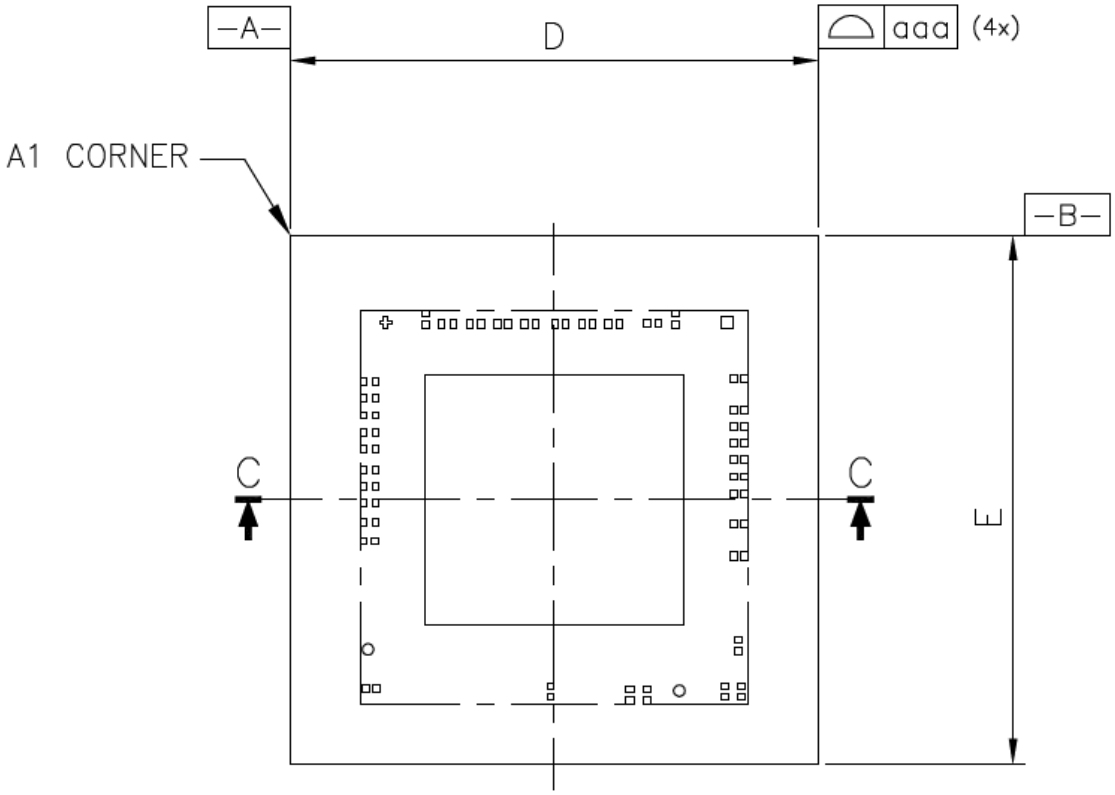


Figure 19 23 x 23 mm 6L 0.7mm 813 Ball FCBGA Package Drawing – Section C-C

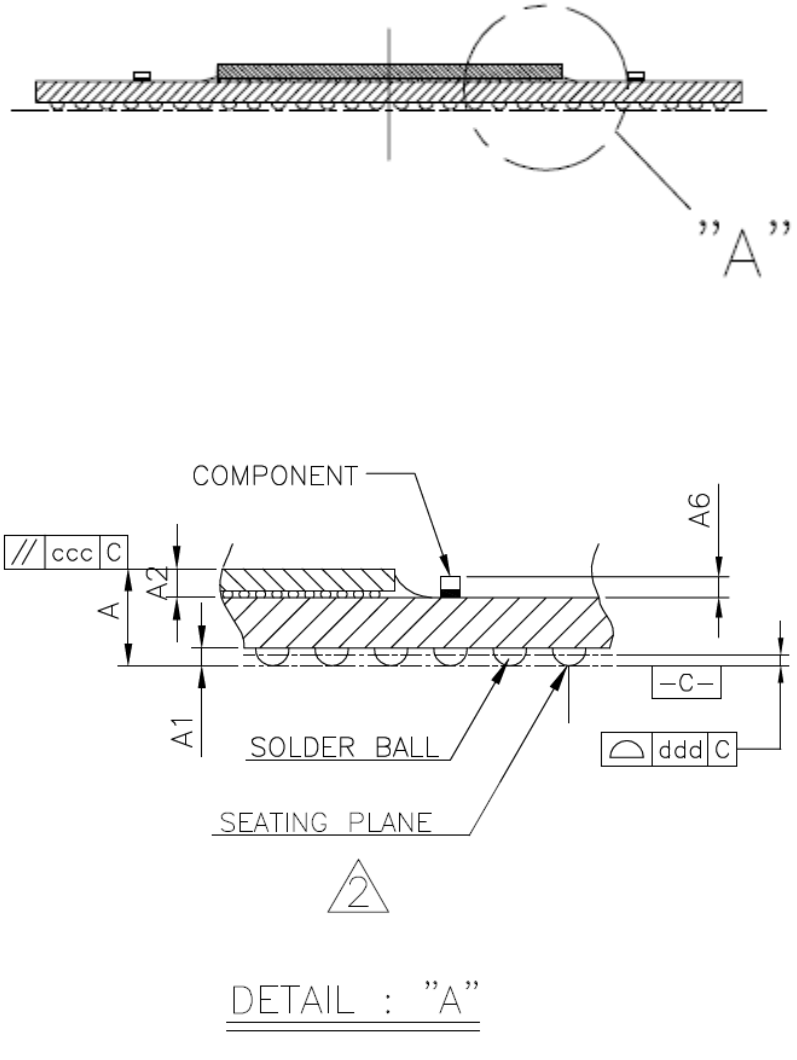


Figure 20 23 x 23 mm 6L 0.7mm 813 Ball FCBGA Package Drawing – Bottom View

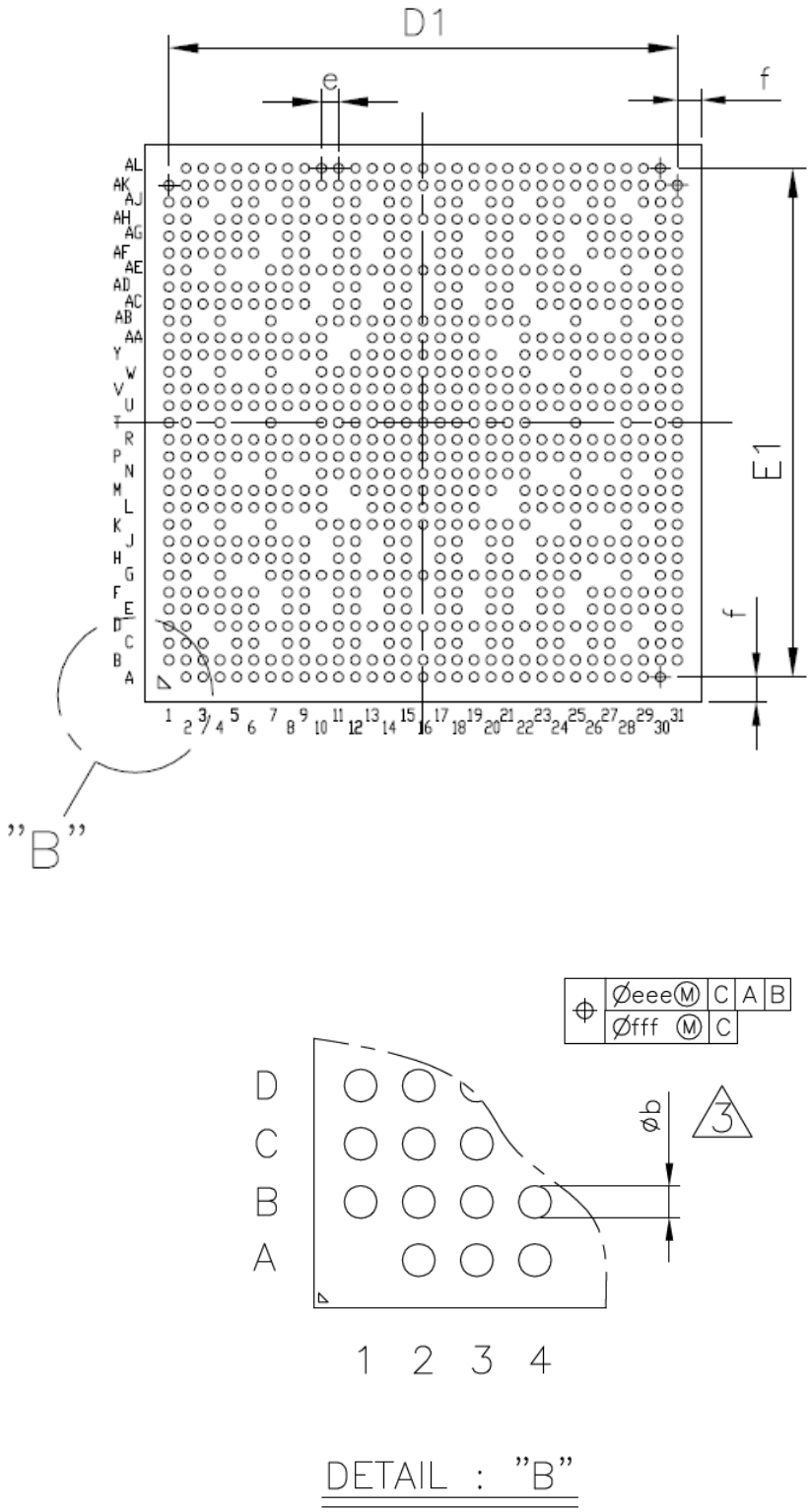


Table 53. 23 x 23 mm 6L 0.7mm 813 Ball FCBGA Package Drawing Dimensions and Notes

Symbol	Dimension in mm			Description
	Min	Nom	Max	
A	1.35	1.45	1.55	Total package height (Pre-SMT)
A1	0.17	0.22	0.27	Package stand-off
A2	0.50	0.53	0.56	Die height (top of substrate to top of die)
A6	0.28	0.31	0.34	0201 chip cap height
D/E	23.00 BASIC			Package body outline size
D1/E1	21.00 BASIC			Distance between centerlines of the two outermost rows of balls parallel to the D and E axis of the package.
e	0.70 BASIC			Solder ball pitch (outside array)
f	1.00 BASIC			Distance from centerline of the outermost row of balls to substrate edge (reference only)
b	0.35	0.40	0.45	Reflowed solder ball diameter
aaa	0.15			Package outline tolerance
ccc	0.20			Parallelism of top of die relative to seating plane defined by datum C
ddd	0.20			Co-planarity, with respect to datum C
eee	0.15			Solder ball pattern true position tolerance with respect to datum's A and B and perpendicular to datum C
fff	0.08			Tolerance of Solder Ball position within the ball pattern matrix with respect to each other, and perpendicular to datum C.
Number of Balls	813			Solder ball count within ball pattern

NOTES

1. Controlling Dimension: Millimeter.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. The pattern of pin 1 fiducial is for reference only.
5. Drawing not to scale.
6. All passive locations shown, some or all locations may not be populated.
7. Compliant to JEDEC publication 95, page 4.5-1/E to 4.5-19/E, with exception of dimension ddd.

Terms and Definitions

Term	Definition
A/D	Analog-to-Digital
AAC	Advanced Audio Coding
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
AVP	Audio-video Processor
BIST	Built-in Self test
BSE	Bit Stream Engine
CODEC	Coder-Decoder
D/A	Digital-to-Analog
DAP	Digital Audio Port
DDR	Double Data Rate
DMA	Direct Memory Access
DVFS	Dynamic Voltage and Frequency Scaling
EMC	External Memory Controller
eMMC	Embedded MMC (embedded storage solution with MMC interface, and flash memory and controller)
GPIO	General Purpose Input/Output
GPU	Graphics Processor Unit
HD AVP	High-Definition Audio-video Processor
HDMI	High-Definition Multimedia Interface
HS-MMC	High-Speed Multimedia Card
HSYNC	Horizontal Sync Pulse
I^2C	NXP Inter-IC multimaster bus
I^2S	NXP Inter-IC sound bus
iRAM	Internal Random Access Memory
ISDB-T	Integrated Services Digital Broadcasting-Terrestrial, the Japanese format for digital TV broadcast.
JTAG	Joint Test Action Group
MC	Memory Controller
MCE	Motion Compensation Engine
MLC	Multiple Level Cell
MMC	Multimedia Card
MSelect	Memory Select
MPIO	Multi-Purpose IO

Term	Definition
NB	Narrow Band
NTSC	National Television System Committee, defines a television standard used in the USA and elsewhere.
PCM	Pulse-code Modulation
PD	Pull-down
PHY	Physical Layer
PIO	Programmed Input Output
PLL	Phase-lock Loop
PMU	Power Management Unit
POR	Power-on Reset
PU	Pull-up
RTC	Real Time Clock
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SFIO	Special Function I/O
SLC	Single Level Cell
SMT	Surface Mount Technology
SoC	System on a Chip
S/PDIF	SONY/Philips Digital Interconnect Format
SPI	Serial Peripheral Interface
TFE	Transform Function Engine
ULP	Ultra-low Power
USB	Universal Serial Bus
VCP	Vector Coprocessor
VI	Video Input
VSYNC	Vertical Sync Pulse
XBAR	Cross Bar
XMB	External Memory Bus
XTAL	Crystal

Revision History

Version	Date	Description
v01	DEC, 2014	Initial Release for Embedded Applications
v02	FEB, 2015	Full Data Sheet Release for Embedded Applications

