Reg. No.: 21BPS1364

Name : Mubin Chinchwalkar

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Continuous Assessment Test II – October 2022

Programme	:	**B.Tech (CSE, AI/ML, CPS, AIR)**	Semester	:	**Fall 2022-23**
Course Code	:	**BCSE 205L**	Class Number	:	**CH2022231001507, CH2022231001510, CH2022231001511, CH2022231001512, CH2022231001513, CH2022231001514, CH2022231001515**
Course Title	:	**Computer Architecture and Organization**	Slot	:	**B2+TB2**
Faculty	:	**Dr.Rama Prabha , Dr. Aswiga, Prof.Nivedita, Dr. Bhanu Chander Balusa, Dr.Anushiya Rachel, Dr. Sambasivarao, Dr A.K. Ilavarasi**			
Time	:	**1½ Hours**	Max. Marks	:	**50**

Answer ALL Questions

Q. No.	Question Text	Marks
1.	For a 64-bit machine describe how the processor fetches the instruction Add R1, R2 from the memory location 2044 (which is represented in hexadecimal) and executes it. Explain the role of different registers and buses involved during the instruction fetch and execution cycle and write down the values of MAR, MDR, IR and PC while the instruction is being fetched and executed considering each instruction is 64-bit long. Also draw the architectural diagram for the above scenario.	**10**
2.	Consider the following expression below and write the assembly language code by listing out all the possible sequence using 2 - address, 1-address and 0 -address instruction formats. $$Y = \frac{A + (B \times C)}{D - E + F}$$	**10**
3.	i) In order to implement the instruction given below, you are asked to design a single bus data path architecture and describe the sequence of steps needed to perform the operation. Also indicate the control signals required for the micro operations at each timing signal or clock cycle for the given instruction. (Note: 2000 is the effective address of the operand.)(5 Marks) Instruction : SUB R1, 2000	**10**

	ii) In order to implement the instruction given below, you are asked to design a Multi bus data path architecture and describe the sequence of steps needed to perform the operation. Also indicate the control signals required for the micro operations at each timing signal or clock cycle for the given instruction. (5 Marks) Instruction : DIV R1, (R2)	
4.	The series of address references given as addresses are 6, 2, 2, 6, 8, 8, 2, 4, 2, 4, 6, 8, 6, and 4. Label each reference in the list as a hit or a miss and show the final contents of the cache for a. A direct mapped cache that is initially empty (3 Marks) b. Fully associative cache that is initially empty. (4 Marks) c. Four way set associative cache that is initially empty. (3 Marks) Assume that all these cache memories have eight one-word cache lines	**10**
5.	Assume that processor in your PC generates a 32 bit address for each request. The capacity of the cache memory is 8KB of data and the block size is of 8 words. Assume one word is equal to 4 bytes. a) Find the number of bits required to represent cache line index and tag for the given 32-bit address using directed mapping. (3 Marks) b) Find the number of bits required to represent tag for the given 32-bit address using fully associative mapping. (4 Marks) c) Find the number of bits required to represent tag for the given 32-bit address using 2 way set associative mapping.(3 Marks)	**10**

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Continuous Assessment Test 2 – October 2022

Programme	: B.Tech (ECE/ECM)	Semester	:	FS 2022-23	
Course	: Computer Organization and Architecture	Code	:	ECE3004	
		Class Nbr	:	CH2022231000032 CH2022231001961	
Faculty	: Dr. E. Sathish, Dr. J. Florence Gnana Poovathy	Slot	:	D2+TD2	
Time	: 90 Minutes	Max. Marks	:	50	

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		Consider that a program has 60% simple instructions and 40% complex instructions. The cycle time is 100 ns. The total number of instructions is 7,00,000. Following table gives you the number of machine cycles for simple and complex instructions. a) Calculate the time taken to execute the whole program in both RISC and CISC architectures and compare the both. (7 Marks) b) Give a suggestion on which architecture is the best. Give reasons (3 Marks)	10

Type of Architecture	No. of Machine cycles for simple instructions	No. of machine cycle for complex instructions
RISC	1	12
CISC	4	8

2.		Imagine that you are going to perform any ALU operation with 8086 between on two operands 60 and 40 in the address of memory 6000 and 6009 respectively. These two operands are stored in the main memory/RAM. Make suitable assumptions and elaborate with neat diagrams, how this can be done using the following addressing modes. • Immediate (1 marks) • Register (1 marks) • Direct (1 marks) • Register Indirect (1 marks) • Register Relative Indirect (2 marks) • Base Indexed Indirect (2 marks) • Base Relative Indirect (2 marks)	10
3.		You have purchased a new microprocessor with 8KB cache memory and 16GB of main memory and it follows fully associate mapping for address translation. You have an option to convert it to two way or four way set associative mapping. Compare the mapping techniques with number of blocks, tag size, no of searches and hit ratio and select a mapping technique which has minimum tag size for your application. Assume block size of 32 bytes.	10

4. A system architecture allows 4GB virtual address space for processes and 8GB of main memory The size of pages and physical frames is 4KB. The system can allow a maximum of 1K processes to run concurrently. If the Operating System uses hierarchical paging, calculate the maximum memory space for required to store both outer and inner page tables of all processes in the system. Assume that each page table entry requires an additional 10 bits to store various flags. Elaborate with neat diagrams. 10

5. Consider the data 0856 to be communicated from Register 1 (R1) to Register 2 (R2) using a small micro instruction which is stored in the code segment of the processor. State whether programmed or Interrupt initiated I/O control will be suitable and explain both with neat diagrams. 10

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Continuous Assessment Test II – June 2023

Programme	: B. Tech. (ECM)	Semester	:	Fall Inter 2022-23
Course	: Computer Architecture and Organization	Code	:	BCSE205L
		Slot	:	A1+TA1
Faculty	: Dr. Sindhuja M Mr. Srinivasan R Mr. Prasanna Kumaar S	Class Nbr.	:	CH2022232500330 CH2022232500333 CH2022232500335
Time	: 90 Minutes	Max. Marks	:	50

Answer ALL the questions.

Q. No.	Sub. Sec.	Questions	Marks
1.		Assume that in 1000 memory references, there are 40 misses in the first-level cache and 20 misses in the second level cache. What are the various miss rates? The miss penalty from L2 cache to memory is 200 clock cycles, the hit time of L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 memory references per instruction. What is the average memory access time and average stall cycles per instructions?	10
2.	(a)	To construct a 2 KB x 8 RAM using 1 KB x 4 chip, find the no. of chips required and the no. of address lines for each chip. Also draw the organization of memory module. [5 marks]	10
	(b)	In a 4-way set associate mapped cache of size 64 KB with block size 512 bytes. The size of main memory is 1MB. Find the no. of bits in tag and the tag directory size. [5 marks]	
3.	(a)	Consider a fully associative cache with a total of 8 cache blocks (0-7). The main memory block requests are as follows: 5, 4, 26, 9, 19, 6, 26, 9, 16, 35, 42, 23, 9, 4, 16, 26, 7, 10 If LRU replacement policy is used, which cache block will have memory block-10. Calculate hit ratio and miss ratio. [5 marks]	10
	(b)	If FIFO replacement policy is used, which cache block will have memory block-7. Calculate hit ratio and miss ratio. [5 marks]	
4.	(a)	A processor executes 50,000 cycles in one second. A printer device is sent 8 bytes in programmed I/O mode. The printer can print 500 characters per second and does not have a print-buffer. (i) How much time will be taken to acknowledge the character status? (ii) How many processor cycles are used in transferring just 8 bytes? [2+3=5 marks]	10

(b) In virtually all computers having DMA modules, DMA access to main memory is given higher priority than CPU access to main memory. Why?

[5 marks]

5. Suppose a system has following specifications:

- 400 ns memory cycle time for read/write
- 3 microsec for execution of an instruction on average
- interrupt service routine (ISR) consists of seven instructions
- each byte transfer requires 4 cycles (instructions)
- 50% of the cycles use memory bus

Determine the peak data transfer rate for

(a) programmed I/O (b) interrupt I/O, and (c) DMA

10

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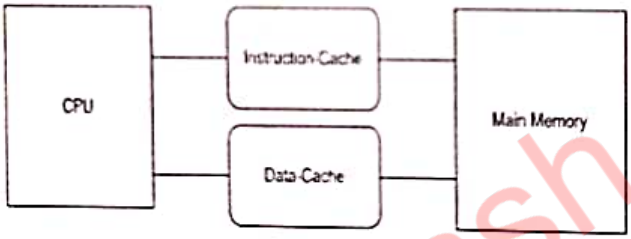
Continuous Assessment Test II – June 2023

Programme	:	B.Tech (ECM)	Semester	:	Fall Inter 2022-23
Course	:	Computer Architecture and Organization	Code	:	BCSE205L
			Slot	:	A2+TA2
Faculty	:	Dr. Sindhuja M Dr. Sunil Kumar Pradhan Dr. Balakrishnan R Mr. Ajeyprasaath Kb	Class Nbr.	:	CH2022232500336 CH2022232500337 CH2022232500338 CH2022232500340
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		Consider a 2-level memory hierarchy with separate instruction and data caches in level 1, and main memory in level 2. Figure 1 for the reference.  **Figure 1** The following parameters are given: a) The clock cycle time is 2ns b) The miss penalty is 12 clock cycles (for both read and write) c) 2% of instructions are not found in instruction cache d) 5% of data references are not found in data cache e) 25% of the total memory accesses are for data f) Cache access time (including hit detection) is 1 clock cycle Find average access time.	10
2.		How many 256 x 4 RAM chips are needed to construct a memory chip of 2048x8? Show the corresponding interconnection diagram.	10

3. Consider a direct mapped cache of size 4 KB with block size 1024 bytes. The size of main memory is 1MB. Find- 10

1. Number of Bits in Physical Address [2 marks]
2. Number of Bits in Block Offset [2 marks]
3. Number of bits in tag [3 marks]
4. Tag directory size [3 marks]

4. (a) On a non-pipelined sequential processor, the following program segment, that is part of the Interrupt Service Routine (ISR), is given to transfer 500 bytes from an I/O device to memory. 10

Initialize the memory address register

Initialize word count register to 500

Loop: Load a byte from device

Store in memory at address given by address register

Increment the memory address register

Decrement the word count register

If count != 0 goto Loop

Assume that each statement in the program is equivalent to a machine instruction that takes 1 clock cycle to execute if it is a non LOAD/STORE instruction. The LOAD/STORE instructions take 2 clock cycles to execute. The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes 2 clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speedup when the DMA controller-based design is used in place of the interrupt driven approach? [8 marks]

(b) Suppose that a disk is rotating at a speed of 10,000 rpm, and there are 120 Kbytes of data recorded in every track. Once the disk head reaches the desired track, what is the sustained data transfer rate in Mbytes/sec? [2 marks]

5. (a) The size of the word count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 Kbytes from disk to main memory. The memory is byte addressable. What is the minimum number of times the DMA controller needs to get control of the system bus from the processor to transfer the file from disk to main memory? [5 marks] 10

Assume1 kb = 1024 bytes.

(b) A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 4800 characters per second. The CPU is fetching and executing instructions at an average rate of one million instructions per second. By how much % will the CPU be slowed down because of the DMA transfer? [5 marks]

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Continuous Assessment Test II - October, 2023

Programme	:	B. Tech. CSE	Semester	:	Fall 2023-24
Course	:	Computer Architecture and Organization	Code	:	BCSE205L
Faculty	:	Dr. A. K Ilavarasi Dr. Vaidehi Vijayakumar Dr. B V A N S S Prabhakar Rao	Class Nbr(s)	:	CH2023240101204 CH2023240100884 CH2023240100883
			Slot(s)	:	F2+TF2
Time	:	1½ Hours	Max. Marks	:	50

Answer ALL the Questions

Q. No	Question Text	Mar
1.	i) Consider a one addressed machine with the following memory address of the word and its corresponding accumulator value. (5 marks)	1

Address	Content
20	70
30	60
40	50
50	40
60	30
70	20

What values do the following instructions load into the accumulator after execution?

a. Load IMMEDIATE 30
b. Load DIRECT 20
c. Load INDIRECT 20
d. Load IMMEDIATE 40
e. Load INDIRECT 30

ii) Write the sequence of control signals required for executing any two of the above instructions based on your choice in single bus organization. (5 marks)

2	Given the expression R1 + =20 i. Write the instruction to implement the given expression and give the control sequence for single cycle and multi cycle data path. (7 marks) ii. How many clock cycles are reduced with multi cycle data path and justify your answer. (3 marks)	10
3.	A computer has to be interfaced with a memory module that consists of a 1 M x 32 RAM. i. Construct this memory module using 512 K x 8 RAM chips. Discuss with appropriate diagram. (6 marks) ii. How will the address bits be decoded for each memory module of this organization? (4 marks)	10

4.	Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. i. How is a 16-bit memory address divided into tag, line number, and byte number? (3 marks) ii. Into what line would bytes with each of the following addresses be stored? (4 marks) 0001 0001 0001 1011 1100 0011 0011 0100 1101 0000 0001 1101 1010 1010 1010 1010 iii. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it? (2 marks) iv. Calculate the total bytes of memory that can be stored in the cache? (1 mark)	10
5.	The following steps represent an algorithm: Step 1: In this step, the corresponding registers will be initialized, i.e., register A contains value 0, register M has the Divisor, register Q has the Dividend, and N is used to specify the number of bits in dividend. Step 2: In this step, register A and register Q will be treated as a single unit, and the value of both the registers will be shifted left. Step 3: After that, the value of register M will be subtracted from register A. The result of subtraction will be stored in register A. Step 4: Now, check the most significant bit of register A. If this bit of register A is 0, then the least significant bit of register Q will be set with a value 1. If the most significant bit of A is 1, then the least significant bit of register Q will be set to with value 0, and restore the value of A that means it will restore the value of register A before subtraction with M. Step 5: After that, the value of N will be decremented. Here n is used as a counter. Step 6: Now, if the value of N is 0, we will break the loop. Otherwise, we have to again go to step 2. Step 7: This is the last step. In this step, the quotient is contained in the register Q, and the remainder is contained in register A. Use the knowledge of Computer Instruction Sets and try to develop a precise of assemble language program code as per the requirement pertaining to each and every step represented above. Also justify the need for each of the instruction.	10

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Continuous Assessment Test II – October 2023

Programme	:	**B.Tech CSE & B.Tech CSE with all Specializations**	Semester	:	**Fall Semester 2023-24**
Course	:	**Computer Architecture and Organization**	Code	:	**BCSE205L**
			ClassNbr		**CH2023240100674** **CH2023240100675** **CH2023240100676** **CH2023240100677**
Faculty	:	**Dr. Ancy Micheal A** **Prof. Sukanya G** **Dr. Shruti Mishra** **Dr. Pavithra S**	Slot(s)	:	**G2+TG2**
Time	:	**90 Minutes**	Max. Marks	:	**50**

Answer ALL the Questions

1	a)	List out the possible control sequence for implementing the instruction as given below, **MOV ACC, R1** **MUL R1, R2** on the processor in single bus organization of data path. This instruction multiplies the contents of the registers R1 and R2 and stores the result in R1. Higher order bits in the product, if any are discarded.	[5]
	b)	Write down the micro-instructions for the above control sequences.	[5]
2		Two different compilers are used for executing the same program. The table below shows the execution time of the two different compiled programs.	[10]

	Compiler A		Compiler B	
	# instructions	Execution Time	# instructions	Execution Time
Program 1	1.00 E+09	1s	1.20 E+09	1.4s
Program 2	1.00 E+09	0.8s	1.20 E+09	0.7s

a) Find the average CPI for each program, given that the processor has a clock cycle time of 1ns.

b) Assume the average CPIs found in part (a), but that the compiled programs run on

		two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code? c) A new compiler is developed that uses only 600 million instructions and has an average CPI of 1.1. What is the speed-up of using this new compiler versus using Compiler A or B on the original processor of part (a)?	
3		Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. a. How is a 16-bit memory address divided into tag, line number, and byte number? b. Into what line would bytes with each of the following addresses be stored? 0001 0001 0001 1011 1100 0011 0011 0100 1101 0000 0001 1101 1010 1010 1010 1010 c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it? d. How many total bytes of memory can be stored in the cache? e. Why is the tag also stored in the cache?	[15]
4		Consider an Intel P4 microprocessor with a 16 KB unified L1 cache. The miss rate for this cache is 3% and the hit time is 2 Clock Cycles (CCs). The processor also has an 8 MB, on-chip L2 cache. 95% of the time, data requests to the L2 cache are found. If data is not found in the L2 cache, a request is made to a 4 GB main memory. The time to service a memory request is 100,000 CCs. On average, it takes 3.5 CCs to process a memory request. How often is data found in main memory?	[7]
5		A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a 2-way set-associative cache that uses the LRU replacement algorithm with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176 All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.	[8]