Reg. No.:

Name :

VIT

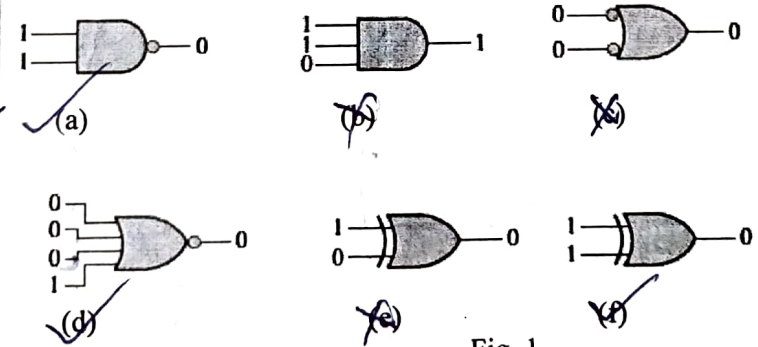
Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test I – September 2022

Programme	:	B.Tech (CSE, CSE(AIR), CSE(CPS), CSE(AI&ML))	Semester	:	FS 2022-23
Course	:	DIGITAL SYSTEM DESIGN	Code	:	BECE102L
			Class Nbr	:	CH2022231001870
Faculty	:	Dr. SELVENDRAN S	Slot	:	E2+TE2
Time	:	90 Minutes	Max. Marks	:	50

Answer Any 5 questions

Q. No.	Sub. Sec.	Questions	Marks
1.	a)	Simplify the expression using Boolean laws **AB + (AC)'+AB'C(AB+C)**	[5]
	b)	Implement the following expression using the CMOS structure and explain the operation of the circuit using any one input combination. **Y = (ABC+DE)'**	[5]
2.	a)	Reduce the following function using K-map technique. F (A, B, C, D) = ∏ M(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6). Implement the function using only NOR gates.	[7]
	b)	Examine the input, output conditions of the gates given in Fig.1 and identify the faulty gates.  Fig. 1	[3]
3.		Design a combinational logic circuit using Verilog HDL in data flow modelling which is used to instruct a Floor cleaning robot to recharge (R=1) itself only when a specific set of following conditions are met. (i). When its battery is low (B = 1) *or* (ii). When the working time is over (T=1) *or* (iii). When vacuuming is complete (V=1), *and* when waxing is complete (W=1).	[10]

4.		Find all the errors (syntax and logical) in the following Verilog declarations. ***module*** *Exmpl-3(A, B, C, D, F)* // Line 1 ***inputs*** *A, b, C, Output D, F,* // Line 2 ***output*** *B;* // Line 3 ***and*** *(A, B, D);* // Line 4 ***and g1(y,A,B);*** // Line 5 ***not g2****(D, A, C);* // Line 6 ***OR*** *(F, B; C);* // Line 7 ***endmodule;*** // Line 8	[10]
5.		Design a full-subtractor circuit with three inputs x , y , B_{in} and two outputs *Diff* and B_{out} . The circuit subtracts $x - y - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and *Diff* is the difference.	[10]
6.	a)	Implement the function f (w_1, w_2, w_3) = $\sum$m (1, 3, 5, 7) by using a 3-to-8 binary decoder and an OR gate.	[5]
	b)	Implement a full adder combinational circuit using two half adders.	[5]

⇔⇔⇔