Reg. No.:

Name :

VIT

Vellore Institute of Technology

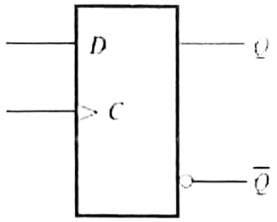
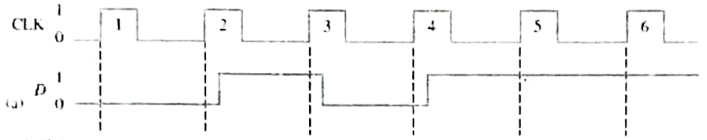
(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test - II – OCT 2022

Programme	:	**B.Tech.(ECE/ECM)**	Semester	:	**FALL 2022-23**
Course	:	**DIGITAL SYSTEM DESIGN**	Code	:	**BECE102L**
			Class Nbr	:	**CH2022231001870**
Faculty	:	**Dr. SELVENDRAN S**	Slot	:	**E2+TE2**
Time	:	**90 Minutes**	Max. Marks	:	**50**

Answer ALL the questions

Q. No.	Sub. Sec.	Question Description	Marks
1		Design a combinational circuit whose input is 4-bit binary data (A, B, C, D) and output is X. The output X is produced based on the following conditions. (a) X : detects the numbers that are divisible by 3 OR (b) X : detects the numbers which are prime **(i)** Write the truth table for the above design **(ii)** Write the output function X in terms of Min term. **(iii)**Implement the output function X using 8 × 1 Multiplexer **(iv)** Write a data flow Verilog code for the output expression.	**15**
2	a)	Design an adder–subtractor circuit which has the following values for mode input M and data inputs A and B. Explain the concept and determine the output for the given cases. *M* *A* *B* (a) 0 0111 0110 (b) 1 1100 1000	**5**
	b)	Design a combinational circuit which accepts input S_i and R_i and produces output at three conditions of R_i equal to S_i, R_i less than S_i and R_i greater than Si where i = 0,1,2.	**5**
3		Use a suitable algorithm for performing signed multiplication of 12 × (-9). (a) Find the register size used for the calculation using specific algorithm (1 mark) (b) Elaborate each step of calculation using the algorithm selected, for the required number of steps or count. Show step wise algorithmic variables used, as a tabulation and obtain the final result (7 marks) (c) Why you have selected the specific algorithm and mention any two advantages (2 marks)	**10**

4	a)	Determine the Q and Q' output waveforms of the flip-flop in Figure 1(a) for the D and CLK inputs in Figure 1(b). Assume that the positive edge-triggered flip-flop is initially RESET.  Fig.1(a)  Fig.1(b) Draw Q and Q' for the above clk and D values.	2
	b)	Write the Verilog code and test bench for D flip flop.	3
5		In the packaging department of a cricket ball manufacturing company, the balls roll down a conveyor and get filled into the empty boxes for shipment. Capacity of each box is 6 balls. Each ball is allowed to pass through IR scanner, which generates a one clock pulse for every ball that crosses the scanner. Design an appropriate counter using T-Flipflop to count the clock pulse generated from scanner to indicate whether the box is full or not, so that next empty box can be moved into the position.	10
		Total	**50**

⇔⇔⇔