Reg. No.:

Name :

DIVYANSH 21BLC1488

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Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act 1956)

Continuous Assessment Test I – May 2023

Programme	:	B.Tech (ECM)	Semester	:	Fall Inter 2022-23
Course	:	Computer Architecture and Organization	Code	:	BCSE205L
			Slot	:	A2+TA2
Faculty	:	Dr. Sindhuja M	Class Nbr.	:	CH2022232500336
		Dr. Sunil Kumar Pradhan			CH2022232500337
		Dr. Balakrishnan R			CH2022232500338
		Mr. Ajeyprasaath Kb			CH2022232500340
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.	(a)	Explain the internal structure of an IAS computer using a neat diagram.	5
	(b)	Suppose for an implementation of a **RISC ISA** there are 4 instruction types, with their frequency of occurrence and CPI as shown	5

Type	Frequency	CPI
LOAD	20%	4
STORE	8%	3
ALU	60%	1
BRANCH	12%	2

Calculate average CPI.

2.	(a)	Tabulate the difference between RISC and CISC Architectures.	5
	(b)	Draw the block diagram of the Harvard architecture and explain why is Harvard architecture faster than Von Neumann?	5

(a) Draw the flow chart of booth's algorithm.

(b) Show the steps of multiplication performed by using booth's algorithm of (-12) x (4)

3. (c) Draw the flow chart of restoring division algorithm **10**

(d) Divide the following binary format positive numbers using the restoring division algorithm: A= 10101, B= 000011, and verify your answer by converting A and B and your result (A / B) to decimal.

4. What are the advantages of hardwired control unit? Describe the design of hardwired control unit of CPU, with diagram. **10**

Let's consider three different processors P1, P2 and P3 and they execute the same instruction set. P1 processor has 3GHz clock rate and a CPI (Cycles Per Instructions) of 1.5, P2 processor has a clock rate of 2.5 GHz and a CPI of 1.0 and P3 processor has 4.0 GHz clock rate and has a CPI of 2.2.

(a) Which processor has the highest performance expressed in instructions per second?

5.

(b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions? **10**

(c) Let's consider a situation, where the execution time is reduced by 30%, which result an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

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Continuous Assessment Test I – September 2022

Programme	:	B.Tech. CSE	Semester	:	FALL 2022-23
Course	:	Computer Architecture and Organization	Code	:	BCSE205L
			Slot	:	B2
Faculty	:	Dr.Rama Prabha , Dr. Aswiga, Prof.Nivedita, Dr. Bhanu Chander Balusa, Dr.Anushiya Rachel, Dr. Sambasivarao, Dr A.K. Havarasi	Class Nbr	:	CH2022231001507 CH2022231001510 CH2022231001511 CH2022231001512 CH2022231001513 CH2022231001514 CH2022231001515
Time	:	1½ Hours	Max. Marks	:	50

Answer ALL the questions

Q.No.	Questions	Marks
	i) Suppose you are an architect at Zion Computers and you are assigned the task of designing a processor that stores both data and instructions in the same memory and always accesses a pair of instructions at a time. Identify the suitable architecture for the given scenario and explain its structure with a neat diagram. (5 Marks)	10
	ii) Explain how the following assembly language program would be stored in the memory and executed by the processor. (5 Marks) 1001 Load A, LOC1 1002 Add A, LOC2 1003 JNC 1005 1004 Sub A, LOC3 1005 Store LOC4, A 1006 HLT	
2.	Assume that you want to multiply two numbers, which are stored in the memory locations 2:2 and 3:3 as shown in the following figure.	10

Memory	1	2	3
1			
2		2	
3			3

Two possible set of instructions to carry out the above process are as follows:

A) Instruction set

Mul 2:2, 3:3

B) Instruction Set

Load A, 2:2
Load B, 3:3
Mul A,B
Store 3:2, A

Identify the processor corresponding to the instruction set A and B and elaborate on the same. Also discuss the merits and demerits of these processors.

3. Multiply $(-7)_{10} \times (8)_{10}$ using modified Booth's Algorithm.

   i. State how the modified booth is more efficient when dealing with operands of large value. Comment whether the multiplier yields best case/worst case /ordinary case outcome. 4

   ii. Determine the final product of multiplicand and bit-pair recoded multiplier in binary format. 6

4. A coin-change dispensing machine provides an appropriate number of Rs.5 coins in exchange for a note inserted into it. If the machine makes use of non-restoring division algorithm to calculate the number of coins dispensed, illustrate the steps involved in calculating the number of Rs.5 coins to be dispensed in exchange for a Rs.20 note. 10

5. Perform the following Floating point operation on the numbers $(251.529)_{10}$ and $(142.758)_{10}$

   i. Convert the above decimal numbers to normalized notation of binary format. 4

   ii. Perform subtraction for the given numbers and write the normalized result in IEEE single precision format. 6

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Continuous Assessment Test I – May 2023

Programme	: B.Tech (ECM)	Semester	:	Fall Inter 2022-23
Course	: Computer Architecture and Organization	Code	:	BCSE205L
		Slot	:	A1+TA1
Faculty	: Dr. Sindhuja M Mr. Srinivasan R Mr. Prasanna Kumaar S	Class Nbr.	:	CH2022232500330 CH2022232500333 CH2022232500335
Time	: 90 Minutes	Max. Marks	:	50

Answer ALL the questions.

Q.No.	Sub. Sec.	Questions	Marks
1.	(a)	Describe the concept of interconnection of components and its importance in the functioning of a computer system. (5 marks)	10
	(b)	Explain the different types of registers commonly found in a processor, such as general-purpose registers, control registers, and status registers. (5 marks)	
	(c)	Draw the block diagram of the von Neumann architecture and explain its key components. (5 marks)	
2.		Explain the multiplication of -0.75_{10} and 0.3125_{10} using IEEE 754 floating point representation. (5 marks)	10
3.		Using Booth's non-restoring binary division algorithm, calculate the result of 14÷4.	10
4.	(a)	What is addressing mode? Explain register indirect, auto increment and relative addressing modes with example. (6 marks)	10
	(b)	What are the general attributes of vertical and horizontal micro-instructions? (4 marks)	
5.		A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:	10

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

Reg. No.: 20BLC1079

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Continuous Assessment Test I – August 2022

Programme	:	B.Tech (ECE/ECM)	Semester	:	FS 2022-23
Course	:	Computer Organization and Architecture	Code	:	ECE3004
			Class Nbr	:	CH2022231000032 CH2022231001961
Faculty	:	Dr. E. Sathish, Dr. J. Florence Gnana Poovathy	Slot	:	D2+TD2
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.	a	Explain in brief about interconnection of components in a computer for communicating data, address and control information. (5 Marks)	10
	b	Discuss in detail about control signals used for communications in a processor. (5 Marks)	
2.	a	If the number of transistors in Intel's i7 core processor is ~4 billion, according to Moore's law, what would be the number of transistors of the new model released by 2030? Explain the same in brief. (5 Marks)	10
	b	Discuss in details about various functions and structure of a computing system. (5 Marks)	
3.		Discuss in detail about signed number representation in computers. Perform the essential bit calculations of representation for the following values. a) -14.125 b) 2AB3	10
4.		Perform Booth's Algorithm for the following numbers: Multiplicand = 16, Multiplier = -5. Mention the advantage of Booth's algorithm over traditional binary multiplication	10
5.		Find the quotient and remainder of 6/3 using restoring division along with a flowchart or an algorithm.	10

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School of Computer Science and Engineering
Continuous Assessment Test I – August – 2018

B.Tech Computer Science and Engineering- III Semester

CSE2001 –Computer Architecture and Organization

PART - A Answer all the questions (5 x10 = 50Marks)

1. a) Identify the instruction type (Data transfer, Arithmetic, Logical and Program Control) for the following instructions
   a. Exchange – swap contents of source and destination
   b. Negate – Change sign of the operand
   c. Test –Test specified conditions;(set flags based on outcome)
   d. Halt – Stop program Execution
   e. Skip – increment PC to skip next instruction

   b) Identify the addressing mode for the following specification:
   An instruction is stored at location 2000 with its address field at location 2001. The address field has the value 800. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate (c) relative (d) register (e) index with R1 as the index register.

2. Explain the expanded structure of IAS Architecture in detail with the help of diagram.

3. a) A benchmark program is on a 40 MHz processor. The executed program consist of 1,100 instruction executions with the following instruction mix and clock cycle count.

Instruction Type	Instruction Count	Cycles Per Instruction
Integer Arithmetic	300	1
Data transfer	200	2
Floating point	100	2
Control transfer	500	2

Determine the effective CPI. MIPS rate, and execution time for this program

b) Perform Booth's multiplication on the given data of 6 * (-3).

4. Compute Memory traffic, total memory for encoding and storing code that implements the expression evaluation for the following code. Assume that the opcode occupy one byte, addresses occupy two bytes, and data values also occupy two bytes and 1 byte world length for 3-, 2-, 1-, 0- address machines.

3 addr	2-addr	1-addr	0-addr
MUL A,B,C	MUL B,C	LOAD D	PUSH B
DIV D,D,E	DIV D,E	DIV E	PUSH C
SUB A,A,D	SUB B,D	STOR D	MUL
	STOR A,B	LOAD B	PUSH D
		MUL C	PUSH E
		SUB D	DIV
		STOR A	SUB
			POP A

5. Draw the flowchart for restoring division and perform the same for 12 by 3.

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School of Computer Science and Engineering

Continuous Assessment Test I – August – 2018
B.Tech Computer Science and Engineering- III Semester

CSE2001 –Computer Architecture and Organization

Answer all the questions **(5 x10 = 50Marks)**

1.(a) Compare and Contrast Von-Neumann and Harvard architecture. [3]

1.(b) If the last operation performed on a computer with an 8-bit word was an addition in which the two operands were binary 2 and 9, what would be the value of the following status flags: carry, zero, overflow, sign, and even parity? [2]

1. (c) Match the following columns: [5]

instruction	Operation
Shift left	SUBTRACT
Compare	DIVISION
Exclusive-or of same register	AND
Shift right	CLEAR
TEST instruction	MULTIPLICATION

2. Comment on the Booth's algorithm and its efficiency for multiplication representing the steps as a flow chart. Demonstrate step by step multiplication of (-9) × (-15) using Booth's algorithm. [10]

3. With divisor as 2 and dividend as 9, perform step by step restoring binary division. [10]

4.(a) Explain the big-endian and little-endian memory storage formats. Illustrate with an example for a 4 byte value. [5]

4 (b) Discuss in detail various stages of instruction execution cycle with a neat sketch. [5]

5. Given a mathematical operation "a = b + c", where a, b and c are memory locations. CPU has 128 different instructions, If word length of memory is given to be 2 bytes and the address length to store the data is given as 16 bits. calculate [10]

(i) Memory to encode these instructions
(ii) Memory traffic for these instructions

for following instruction formats:

(a) 3 Address instruction format
(b) 2 Address instruction format
(c) 1 Address instruction format
(d) 0 Address instruction format

Mention assumptions if made any.

**** All the best ****

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Continuous Assessment Test I - September, 2023

Programme	:	B. Tech. Computer Science and Engineering	Semester	:	Fall 2023-24
Course	:	Computer Architecture and Organization	Code	:	BCSE205L
Faculty	:	Dr. A. K Ilavarasi Dr. Vaidehi Vijayakumar Dr. B V A N S S Prabhakar Rao	Class Nbr(s)	:	CH2023240101204 CH2023240100884 CH2023240100883
			Slot(s)	:	F2+TF2
Time	:	1½ Hours	Max. Marks	:	50

Answer ALL the Questions

Q. No.	Sub-division	Question Text	Marks
1.	i)	Identify the type of processor that uses instruction buffer register to hold temporarily the instruction from a word in memory. Justify the use of instruction buffer register in processor with neat labeled structure. **(5 marks)**	15
	ii)	The above processor is used to perform a task Y= A * B and the operands are present in the main memory location 3000 and 4000 respectively. Assume each instruction is 20 bits long and each address location is 40 bits long.	

Address	Mnemonics	*Comment*
500	LDA 3000	*Load accumulator with the content of memory location 3000*
	MOV B, 4000	*Copy content of the memory location 4000 to register B*
501	MUL B	*Multiply the content of accumulator with register B and store it in accumulator*
	STA 5000	*Store content of accumulator to memory location 5000*

Trace the contents of the Program Counter, Memory Address Register, Memory Buffer Register, Instruction Register, Instruction Buffer Register and Accumulator for the given code. **(10 marks)**

2		Discuss the features of CISC and RISC processors as per the modern computational requirements. **(5 marks)**	5
3.		A 9 litres jar filled with kerosene was poured to a big keg for 15 times. A part of a processor module uses the Booth's algorithm to perform this operation. With respect to this algorithm, answer the following	10
	i)	Show the step-by-step process used in this algorithm. **(7 Marks)**	
	ii)	Validate the correctness of the result in both binary and decimal format. **(3 Marks)**	

4.		As per the Gregorian Calendar the average (mean) length of a year is 365.2425 days.	10
	i)	Represent the given floating-point number in IEEE 754 standard single precision format. **(5 Marks)**	
	ii)	After adding 180.75 days to 365.2425 days, present the result in IEEE double precision format. **(5 Marks)**	
5.		A company wants to manufacture a Spherical Jar which has different diameters at the top and the bottom and requires a program that calculates the sum of the volume of both the spheres. Assume, the radius of the bigger sphere A is R and the smaller sphere B is S. **Hint**: $Volume\ of\ \ sphere\ A = \frac{4}{3}\pi R^3\ and\ Volume\ of\ a\ sphere\ B = \frac{4}{3}\pi S^3$ Represent the task clearly and device an assembly code using 0-address, 1-address and 2-address instruction format that does this task. Explain each instruction clearly to achieve the final result. **(10 marks)**	10

Reg. No.:

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Continuous Assessment Test I - September 2023

Programme	:	B. Tech (CSE)	Semester	:	**Fall 2023-24**
Course	:	Computer Architecture and Organization	Code	:	BCSE205L
Faculty	:	Dr. Anusha K Dr. Vaidehi Vijayakumar Dr. Rathna R Dr. Dhanalakshmi R	Class Nbr(s)	:	CH2023240100879 CH2023240100882 CH2023240100877 CH2023240100878
			Slot(s)	:	**F1 + TF1**
Time	:	**1½ Hours**	Max. Marks	:	**50**

Answer ALL the Questions

Q. No.	Question Text	Marks
1.	Interpret how the processor manipulates the results for the given numbers using IEEE 754 – 32-bit floating point format. 24.735 - 12.25	10

2	Consider the following three instructions stored in memory in consecutive memory locations.
	ADD R1, R2
	SUB R3, R1
	XOR R3, R2.
	The first instruction is stored at memory location 10000(in hexadecimal). R1, R2 and R3 are all 8-bit registers. R1 = 30 (in hexadecimal), R2 = 47 (in hexadecimal), and R3 = 80 (in hexadecimal).
	
	i) What will be the value of R1, R3, IR, AC and PC after executing all the three instructions? (3 marks)
	ii) Assume that all instructions are 32 bits in size. Elaborate the sequence flow with the help of the internal structure of IAS computer. (7 marks)
		10

3.	You are selected as an assembly language programmer at TWR info systems. Your manager has given an instruction K= (G * (Z+(F+T*W))) asking you to code the instruction by considering the below constraints. i) Using zero address format (5 Marks) ii) Using two operand instruction set architecture (5 Marks)	10

4. Mr. Kelvin has been assigned a project to design an algorithm for restoring Division. Help Mr. Kelvin in designing an algorithm by sketching the flowchart and also check the working of it with the following numbers: 10

i) $(10000)_2$ by $(100)_2$. (5 Marks)
ii) How many numbers of cycles are required to get the correct division result for the above? (2 Marks).
iii) After performing the following operations - left shift operation on A, Q and A=A-M, if MSB of A is 1, What will be the next set of actions? (3 Marks)

5. Estimate the effective address and the operand values in each of the following instructions. Assume that the initial values of the registers are R1= 4100, R2=3000, PC=4500. The memory address and values are given in the diagram below. 10

i) LDA #4000
ii) LDA 4100
iii) LDA (4200)
iv) MOV R1, 50[PC]
v) LDA (R1)

Address	Value
4000	1000
	•
4100	1100
	•
4200	4000
4220	2500
	•
4250	4500
4300	3000
	•
	•
4500	4200
4550	4300
	•
4600	4220