Reg. No.:

Name :

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test (CAT-2) – May 2023

Programme	:	B.Tech (CSE)	Semester	:	Winter 2022-2023
			Code	:	BECE102L
Course	:	Digital System Design	Class Nbr	:	CH2022232300522 CH2022232300543 CH2022232300532 CH2022232300556 CH2022232300195 CH2022232300524
Faculty	:	Dr.Nithya Venkatesan, Dr.B.Sri Revathi, Dr.G.Kanimozhi, Dr.S.Angalaeswari, Dr.Ravi Tiwari, Prof. Mohammed Aneesh	Slot	:	B2+TB2
Time	:	90 minutes	Max. Marks	:	50

Answer **ALL** the Questions

S.No.	Question Description	Marks
1.	Perform multiplication of (20) x (-19) using Booth's Multiplication algorithm. Also find out the number of additions, number of subtractions and number of arithmetic shifts required.	[10]
2.	Perform multiplication of $(1010)_2$ x $(101)_2$ using unsigned array multiplier and draw equivalent logic diagram of 4 x 3 Multiplier.	[10]
3.	Consider a simple human counter system for an elevator overload indication in which the number of persons entering the elevator is detected by an IR sensor. By default, it must display value '0' and increment the number on the display by one each time a human enters the elevator. Assume the maximum capacity of the elevator is 9 persons and if it exceeds the count of 9, there will be an alarm sound to indicate the overload condition and reset the counter. Draw state diagram and design an appropriate control circuit which performs increment operation using T-Flip flop and explain each state in detail.	[10]
4.	Design a synchronous counter which can count the random state sequence as 001,100,011,101,111,110,010,001... using JK flip flops. a) Draw the state diagram. (2 marks) b) Draw the state table and excitation table. (2 marks) c) Draw the required K Maps and find the expression. (4 marks) d) Draw the logic diagram of the given counter. (2 marks)	[10]

5. A sequential circuit has three D flip-flops with outputs as A, B, and C and one input, x. It is described by the following flip-flop input functions:

$$D_A = (BC' + B'C)x + (BC + B'C')x'$$

$$D_B = A$$

$$D_C = B$$

[10]

(a) Draw the logic diagram of the above function. (3 marks)

(b) Derive the state table for the circuit. (3 marks)

(c) Draw two state diagrams: one for $x = 0$ and the other for $x = 1$. (4 marks)

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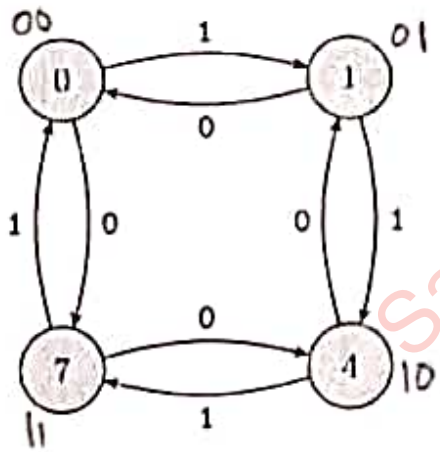
Continuous Assessment Test II - May 2023

Programme	:	B.Tech CSE	Semester	:	Winter 2022-23
Course	:	Digital System Design	Code	:	BECE102L
Faculty	:	G. Angeline Ezhilarasi	Slot	:	B2+TB2
			Class Number	:	CH2022232300528
Time	:	$1\frac{1}{2}$ Hours	Max. Marks	:	50

Answer ALL Questions

1. Design a synchronous sequential circuit to realize the state diagram shown below.
   (a) Obtain the state table for design using JK flip flop. (6)
   (b) Find combinational circuit required for the design using k-maps. (6)
   (c) Draw the sequential circuit. (3)



2. Design a asynchronous sequential circuit using a positive edge triggered D Flip Flop to generate a 4 KHz timing signal from a 16kHz clock frequency signal.
   (a) How many flip flops are required for the design? Verify the output with a timing diagram. (6)
   (b) How will the operation of the circuit change if all the flip flops in the design are triggered simultaneously with the same clock signal. Validate your answer with the output. (4)

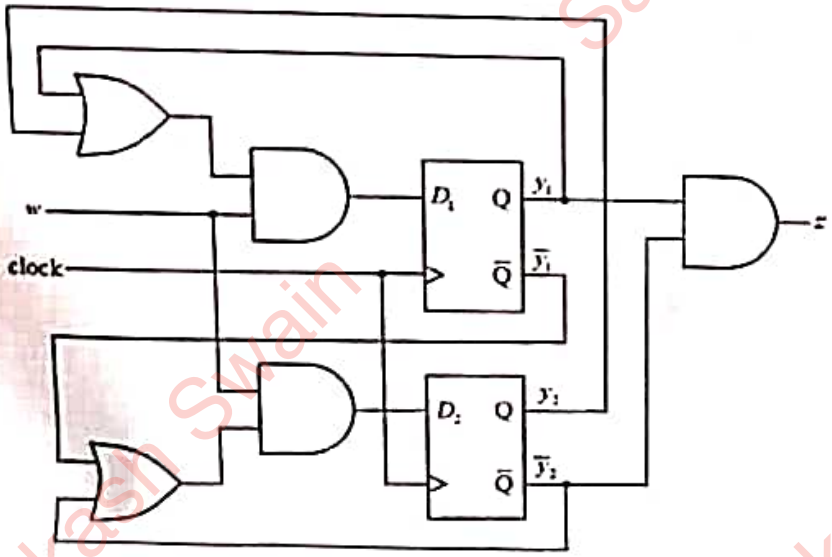
3. A Finite State Machine (FSM) is required to detect the sequence 10101 in a serial input. Draw the state diagram for
   (a) Mealy FSM with overlapping bit pattern. (5)
   (b) Moore FSM with non-overlapping bit pattern. (5)

4. Observe the sequential circuit shown below, where w is the input and z is the output.

(a) Write the necessary input and output equations. (6)

(b) Obtain the state table and draw the state diagram. (6)

(c) Identify if it is Mealy FSM or Moore FSM. Justify your answer. (3)



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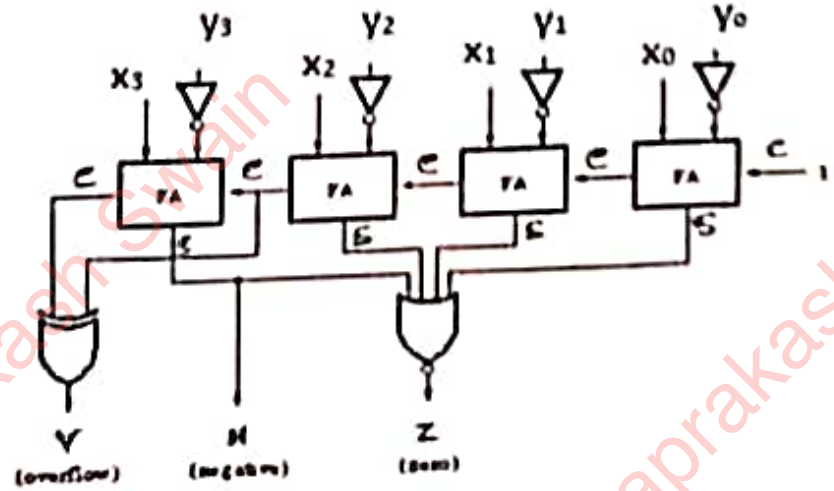
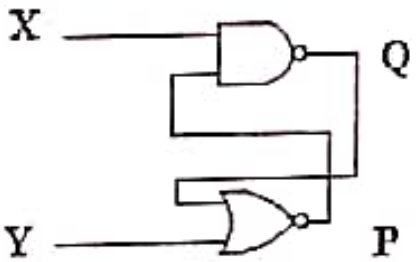
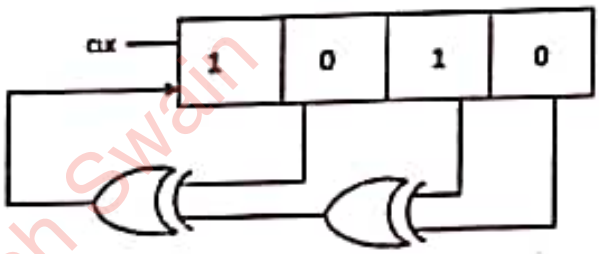
Continuous Assessment Test - II (CAT 2) – May 2023

Programme	:	B. Tech CSE & Spins	Semester	:	Winter 22-23
Course	:	Digital Systems Design	Code	:	BECE102L
			Slot	:	B1+TB1
Faculty	:	Dr. Ashok Mondal Dr. Deepa T Prof. Deepa M Dr. Meera P S. Dr. Sriramalakshmi P Dr. Subbulekshmi D	Class Nbr	:	CH2022232300193 CH2022232300530 CH2022232300191 CH2022232300559 CH2022232300535 CH2022232300526
Time	:	1.5 hours	Max. Marks	:	50

Answer ALL Questions

Q.No.	Question Description	Marks
1.	Compute the output of a 5 bit booth multiplier taking A = 11 as the multiplicand and B = - 13 as the multiplier.	10
2.	a) In computer computations it is often necessary to compare numbers. Two four-bit signed numbers, $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$, can be compared using the subtractor circuit shown in Figure, which performs the operation X – Y . The three outputs denote the following: • Z = 1 if the result is 0; otherwise Z = 0 • N = 1 if the result is negative; otherwise N = 0 • V = 1 if arithmetic overflow occurs; otherwise V = 0 Show how Z, N, and V can be used to determine the cases X = Y , X <Y, X ≤ Y , X > Y, and X ≥ Y with the help of an example . (5 marks)	10



	b) Draw the logic diagram of a 4 bit cascaded full adder/subtractor. Perform the addition of two unsigned numbers 11 and 14 using the above circuit and mark the inputs and outputs correctly in the diagram. (5 marks)	
3.	Design a synchronous modulo 8 up/down counter using D flip flops.	10
4.	A carry look ahead (CLA) adder is designed to add two 4-bit numbers. The circuit of CLA adder is made up of full adders, half adders and logical AND gates. The input bits for CLA adder are $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ respectively. a) Draw the circuit diagram of the 4-bit carry look ahead adder. b) Determine the number of full adders, half adders and logical AND gates. c) Find the expressions of 3rd and 4th stage output signals.	10
5.	a) What is the function table for the feedback circuit shown in Figure ? Can it work as a flip-flop or not? Give reasons. (5 marks)  b) The shift register shown in Figure is initially loaded with 1010. If clock is applied continuously, after how many clock pulses the content of the shift register becomes 1010 again ? (5 marks) 	10

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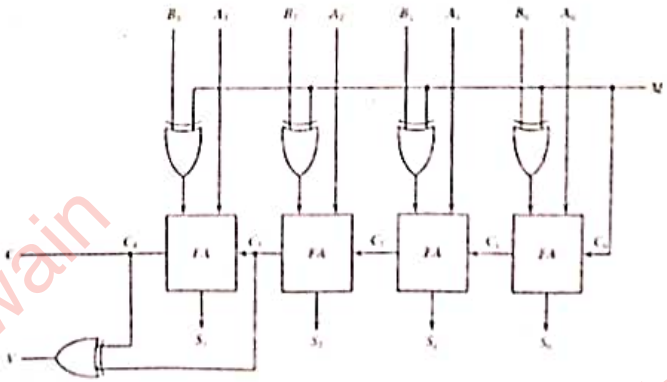
Continuous Assessment Test II – May 2023

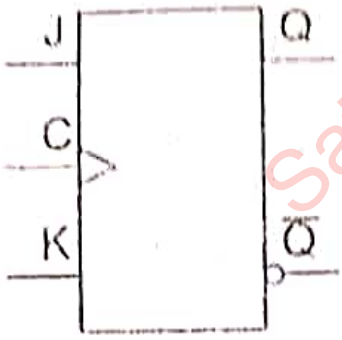
Programme	:	B.Tech	Semester	:		WS 2022-23
Course	:	Digital System Design	Code	:		BECE102L
			Class Nbr	:		CH2022232300125
Faculty	:	Prof.K.Srivatsan	Slot	:		D1
Time	:	90 Minutes	Max. Marks	:		50

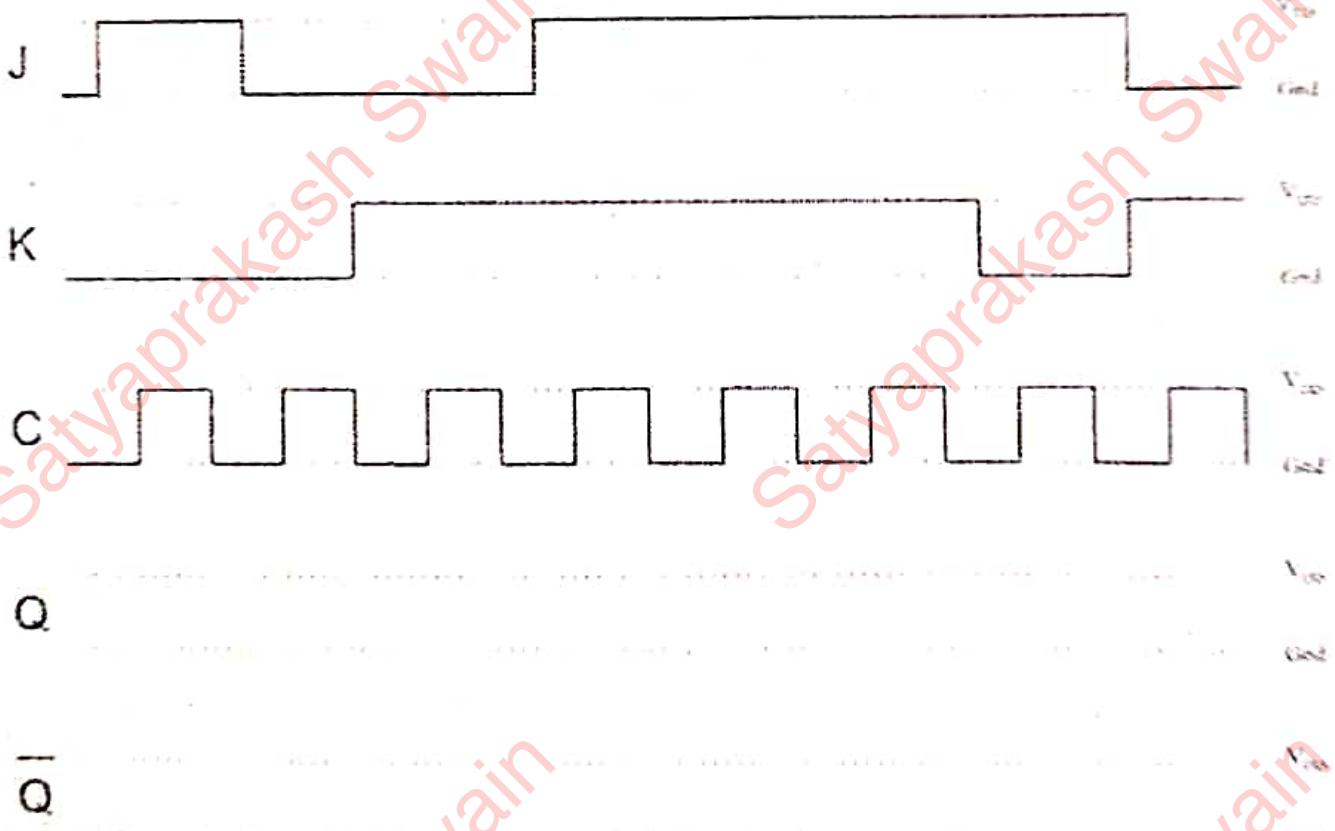
Answer ALL the questions

Q.No.	Sub-division	Question Text	Marks
1.		Indicate the input, output and clock pattern as waveforms in every clock cycle for Serial In Serial Out Register for the following input pattern "1110". Initially assume the output of every flip-flop as zero.	[5]
2.	a)	Implement the Boolean function F(A, B, C) = Σ(3, 5, 6, 7) with a 4:1 multiplexer.	[10]
	b)	Write a Verilog code for the above design	
3.		Generate a parity bit for the binary code "0110" to be in even parity. Include the generated parity bit to determine the binary code "0100" at the receiver side is error free. Draw the logic circuit for the same.	[10]
4.		Determine the product of the following integers (14 x -8) using appropriate multiplication algorithm that uses addition and shift operation.	[10]
5.		Write a Verilog code for the given circuit using adder instantiations	[10]



6.		Determine the output states for this J-K flip-flop, given the pulse inputs shown:	[5]





Reg. No.:

Name :

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(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II – October 2023

Programme	:	B.Tech (ECE/ECM)	Semester	:	WS 2022-23
Course	:	Digital System Design	Code	:	BECE102L
			Class Nbr	:	CH2023240100388 CH2023240100550 CH2023240100549 CH2023240100406 CH2023240100387 CH2023240100553
Faculty	:	Dr. Kaustab Ghosh,Dr.S.Umadevi,Dr.V.Prakash, Dr.Chandramauleshwar Roy, Dr. Jeans Jenifer, Ms. Hemavathy	Slot	:	B2+TB2
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q. No.	Sub. Sec.	Questions	Marks	Module No.	Level	Hot?	CO's
1.		Consider that you need to design an Arithmetic and Logic Unit (ALU) circuit in your lab which will perform either addition or subtraction operation depending upon a single one-bit binary input as 0 or 1. However, your lab has only full adder IC chips along with all chips of all other logic gates. Explain how you would design this ALU with the minimum facilities available in your lab. The ALU should be designed by considering arithmetic operations upto 5 bits of binary numbers. Explain the design and working of the ALU by taking 21 and 26 as two the numbers. The circuit should add this numbers or subtract 21 from 26 and produce the output.	[10]	4	D	Y	3
2.		Perform multiplication of (-25) x (-15) using Booth's Multiplication algorithm. Also list out the number of additions, number of subtractions and number of arithmetic shifts required.	[10]	4	D	Y	3
3.		Assume a control unit designed for a rice packing machine with the purpose of making rice packs, each weighing precisely 5 kilograms. The machine measures the weight of the pack and represent it as a 3-bit binary number. This measured weight is then compared to a reference value of 5 kilograms. If the rice pack weighs less or more than 5 kilograms, a control signal is generated to either add or remove excess rice from the pack. If the rice pack's weight is exactly 5 kilograms, a control signal is generated to seal the pack. For the given requirement perform the following. (i) Design an appropriate control circuit for this comparison operation using basic logic gates. [6 marks] (ii) Write a Verilog HDL code in dataflow modelling for the same.	[10]	4	E	Y	3

[4 marks]

4. In general, Microcontrollers process data in parallel formats like nibbles (4 bits), bytes (8 bits), or words (16 bits, 32 bits). However, many external interfacing devices such as sensors, display devices prefer to operate on serial format. [10] 5 E Y 4

(i). Design a sequential logic circuit using appropriate flip-flops which converts the incoming data from sensor into data that can be handled by the microcontroller as shown in Figure-1. [4 Marks]

(ii). Illustrate with a neat table, how serial input 1010 (D3D2D1D0) of sensor is get transferred to microcontroller. [3 marks]

(iii). Write a Verilog HDL code for the same in behavioural modelling [3 marks]

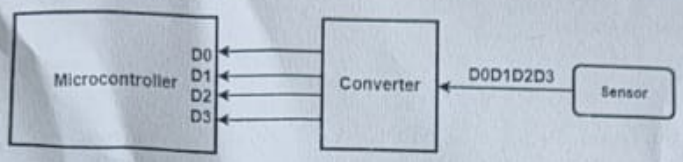

Figure-1

5. For the logic diagram shown in Figure-2, assume output of a D flip-flop is HIGH and output of the JK flip-flop LOW. Formulate a table as shown below representing the sequence of outputs produced from J-K flip flop for the next 5 clock pulses. [10] 5 C Y 4

CLK	D	Q_D	Q_{D+1}	J	K	Q_{JK}	Q_{JK+1}
1							
2							
3							
4							
5							

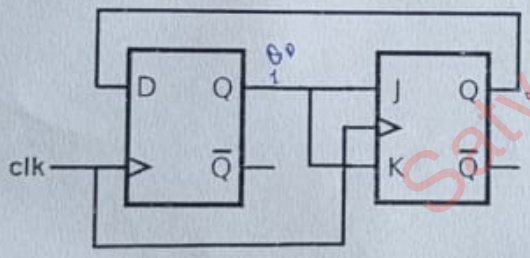

Figure-2

Reg. No.:

Name :

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CHENNAI
Vellore Institute of Technology

Continuous Assessment Test II – March 2024

Programme	: B. Tech. (CSE-AIM), B. Tech. (CSE), B. Tech. (CSE-CPS) & B. Tech. (CSE-AIR)	Semester	:	WS 2023-24
		Code	:	BECE102L
Course	: DIGITAL SYSTEMS DESIGN	Class Nbr.	:	CH2023240502074, CH2023240502114, CH2023240502132, CH2023240502083, CH2023240502148, CH2023240502122, CH2023240502499, CH2023240503428, CH2023240502062, CH2023240502095
Faculty	: Dr. Shoba S, Dr. Kiruthika V, Dr.Sukriti , Dr. Ranjeet Kumar, Dr. K. Srivatsan, Dr. Girija Shankar Sahoo, Dr. V.Sumathi, Dr. A. Bharathi Sankar, Dr. Ravi Tiwari, Dr. Dheeren Ku Mahapatra	Slot	:	A2+TA2
Time	: 90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q. No.	Sub. Sec.	Questions	Marks
1.	(i)	Construct the truth table of 4-bit parity generator for odd parity and implement its Boolean function using 4:1 multiplexer. [8 Marks]	8+7=15
	(ii)	Write a Verilog HDL program for designing 1 × 8 De-multiplexer using 1 × 2 De-multiplexer. [7 Marks]	
2.		Use a suitable algorithm, perform multiplication of **(14) x (-24).** **(i)** Find the register size used for the calculation using specific algorithm [1 mark] **(ii)** Elaborate each step of calculation using the algorithm selected, for the required number of steps or count. Show step wise algorithmic variables used, as a tabulation and obtain the final result [7 marks] **(iii)** Why you have selected the specific algorithm and mention any two advantages [2 marks]	10
3.		Design an adder circuit that reduces the propagation delay with inputs A= '1101' and B = '1000'. Explain the concept and determine the output for each stage. [7 Marks] Comment on the performance of the circuit compared to 4-bit parallel adder. [3 Marks]	10
4.	(i)	Build a holding circuit using data flip-flops, which creates a reel projector that displays the inputs on their respective output simultaneously until all the 5 pieces of inputs '11010' are filled. Design and write the Verilog HDL for the same. [8 Marks]	7+8=15
	(ii)	Imagine you are designing a security access control system for a high-security facility. The system requires a countdown timer that starts from 13 and decrements by one every second. When the countdown reaches 0, an alarm is triggered, indicating the end of a secure time window. Design a sequential circuit and sketch the timing diagram for the outputs.[7 Marks]	

Course Faculty

Reg. No.: 23BAI1038

Name : Adithyaa.D

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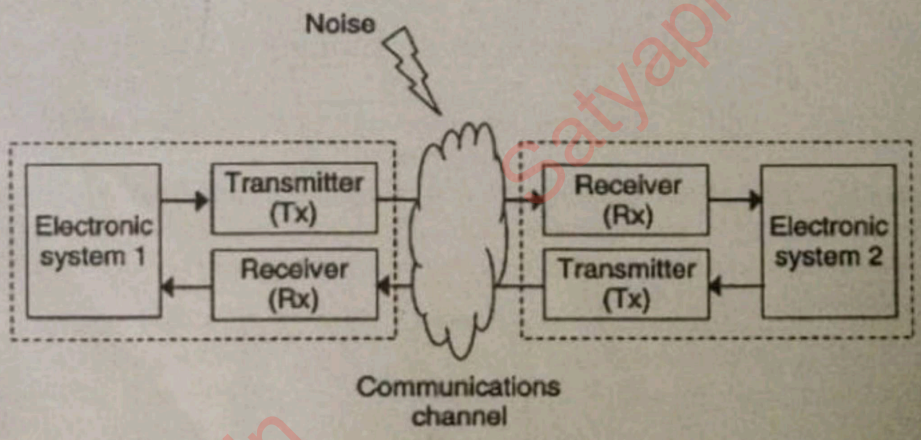
(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II – March 2024

Programme	:	B.Tech. (CSE – All Programme)	Semester	:	WS 2023-24
Course	:	Digital System Design	Code	:	BECE102L
			Slot	:	A1 + TA1
Faculty	:	RANJEET KUMAR	Class Nbr	:	CH2023240502023
		G LAKSHMI PRIYA			CH2023240502025
		DHEEREN KU MAHAPATRA			CH2023240502027
		KIRUTHIKA			CH2023240502029
		GIRIJA SHANKAR			CH2023240502033
		SUKRITI			CH2023240502045
		JEAN JENIFER NESAM J			CH2023240502054
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		 **Figure.1** Errors may arise during the data transmission process depicted in Figure 1 when noise is introduced into the signal. These errors occur particularly when the level of noise surpasses a threshold significant enough to disrupt the transmitted data. To ensure data transmissions between communication nodes are accurate, design an even parity checker with data inputs A, B, and C. Also implement the circuit using suitable multiplexer and write the Verilog HDL code for the same.	10
2.		Identify and implement the algorithm that involves 2's complement, addition, subtraction and shifting operations, to perform multiplication of two numbers 15 and -12. Elaborate on the step-by-step procedure involved using a flowchart.	10
3.		(a)Can JK flip-flop be considered as a universal flip-flop? If yes, then justify by comparing and contrasting with the help of its truth table and other flip-flops. (6 marks)	10

(b) Complete the timing diagram shown in Figure 2 for two types of D flip-flop devices: (i) an active HIGH enabled latch and (ii) a positive edge-triggered D flip-flop. (4 marks)

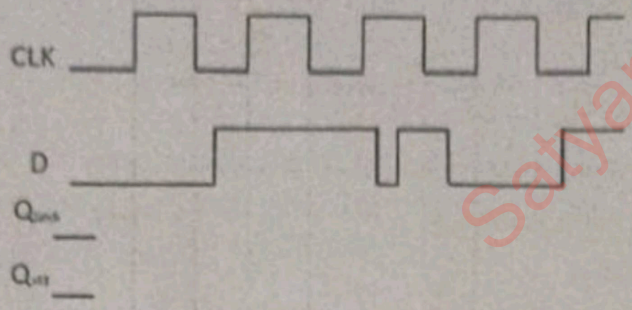


Figure.2

4. Consider a control unit for a wheat packing machine to pack wheat of 6kg each. Present weight of the pack is measured and then it is compared with the reference value (6kg). If the wheat pack is less/greater than 6kg control signal generated to add/remove excess wheat into/from the wheat pack. If the wheat pack weight is exactly 6kg then control signal is generated to make a pack. Design an appropriate control circuit for the above mentioned comparison operation using basic logic gates. Also write a Verilog HDL code in dataflow modelling for the same. 10

5. (a) Draw the logic diagram of a 4-bit register incorporating D flip-flop and a 4 × 1 multiplexer with mode selection inputs S_1 and S_0. The register functions according to the following Table 1: (5 Marks) 10

S_1	S_0	Register Operation
0	0	No change
0	1	Complement the output
1	0	Clear register to 0
1	1	Load Data

Table. 1

(b) For the circuit shown in figure 3, two 4-bit parallel-in serial-out shift registers loaded with the data shown are used to feed the data to a Full Subtractor (FS). Initially, all the flip-flops are in clear state. After applying two clock pulses, identify the outputs of the Full Subtractor (FS). (5 Marks)

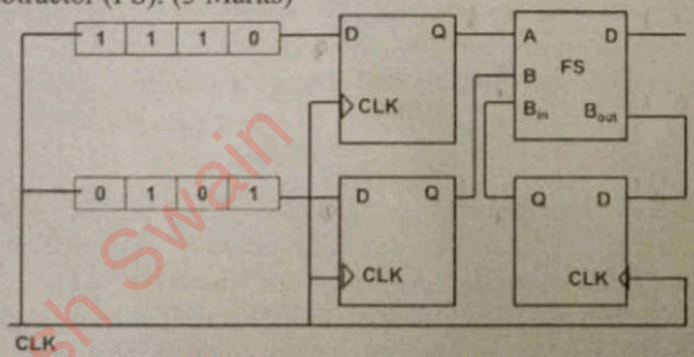


Figure.3