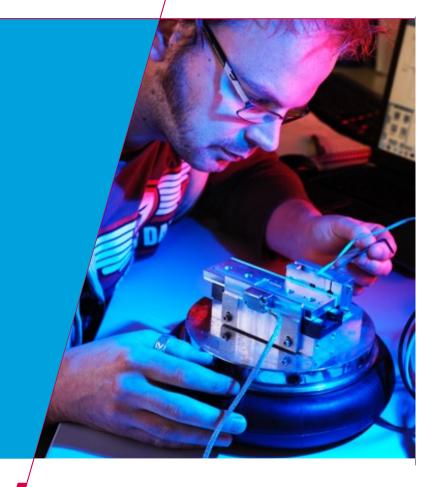
2IC30: Computer systems Optimizing circuits Karnaugh maps

Jan Friso Groote

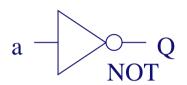


Technische Universiteit
Eindhoven
University of Technology

Where innovation starts

Logical gates I

Logical gates:



$$Q = \neg a$$

$$Q = a'$$

$$Q = \overline{a}$$

$$Q = a \wedge b$$

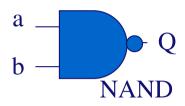
$$Q = a \cdot b$$

$$Q = aVb$$

$$Q = a+b$$



Logical gates II



$$Q = \neg(a \land b)$$

$$Q = (a \cdot b)$$

$$Q = \neg(aVb)$$

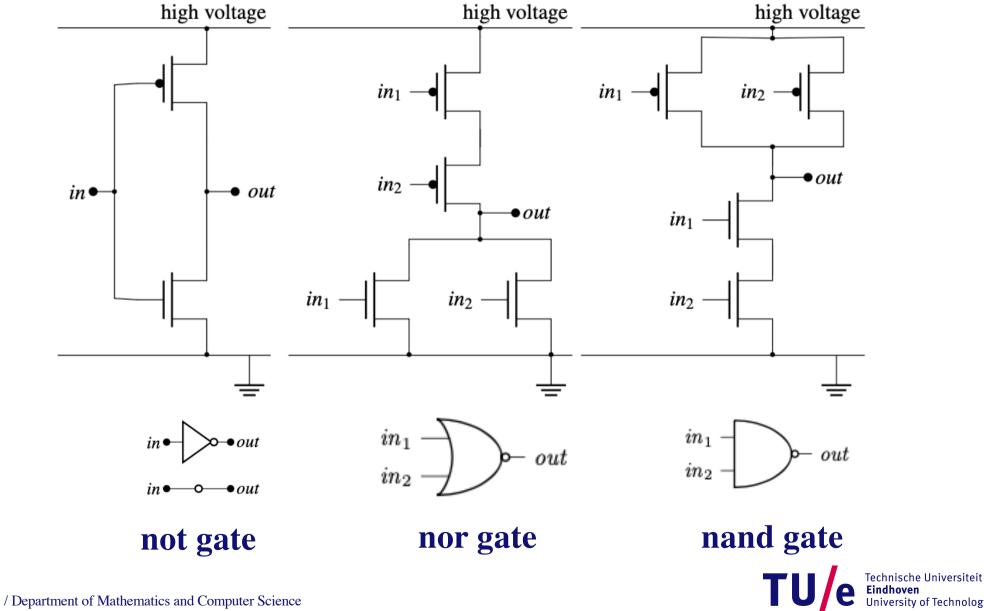
$$Q = (a+b)'$$

$$Q = a \leftrightarrow b$$

$$Q = (a \oplus b)$$



Gates with Field Effect Transistors.



Duality principle

- □ 1 is the dual of 0 (*true* is the dual of *false*).
- \square \land is the dual of \lor .

- ☐ The dual is obtained by applying negation. Properties:

- $\square x \lor (\neg x \land y) = x \lor y$



Rules for switching/boolean algebra (1)

$$\square x \lor x = x$$

$$\square x \land x = x$$

$$\square x \lor 1 = 1$$

$$\Box x \wedge 0 = 0$$

$$\square x \lor 0 = x$$

$$\square x \land 1 = x$$

 $\square x \lor \neg x = 1$

 $\Box x \land \neg x = 0$

Idempotence

Zero elements

Identity elements

Double negation

Excluded middle

Contradiction

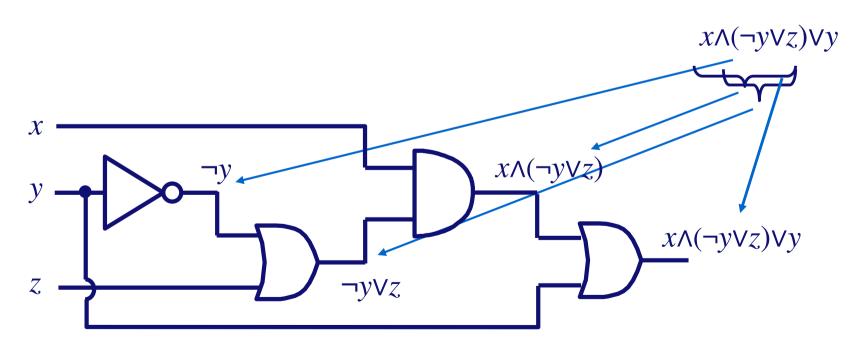
Red rules are complete, i.e., sufficient to derive all others (Ninomiya & Mukaidono, 2003).

Rules for switching/boolean algebra (2)



From gates to boolean expressions and v.v.

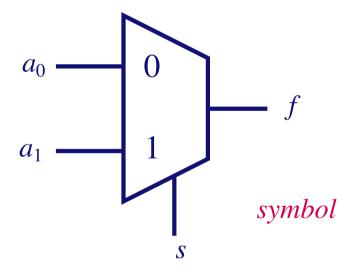
- ☐ Any switching function can be written as a boolean expression over the input signals.
- □ A boolean expression has a 1-1 correspondence with a gate implementation:





How to systematically design a circuit from a truth table?

2 input multiplexer.



multiplexer

a_0	a_1	\int
0	0	0
0	1	0
1	0	1
1	1	1
0	0	0
0	1	1
1	0	0
1	1	1
	0 0 1 1 0 0	0 0 0 1 1 0 1 1 0 0 0 1 1 0

2-input multiplexer

$$\begin{array}{c|cc}
s & f \\
\hline
0 & a_0 \\
1 & a_1
\end{array}$$



Minterms and maxterms

• Every line in the truth table where the function has value 1 corresponds to a (so-called) *minterm*;

Example:

if f = 1 for a = 1, b = 0, and c = 1, the minterm is: $a \land \neg b \land c$.

a	b	c	f	f'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0



Minterms and maxterms

• Every line in the truth table where the function has value 0 corresponds to a (so-called) *maxterm*;

Example:

if f = 0 for a = 0, b = 1, and c = 0, the maxterm is: $a \lor \neg b \lor c$.

a	b	c	f	f'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0



Two Canonical Forms

- *Disjunctive Normal Form*: every boolean function can be written as the *disjunction* of a set of *minterms*.
- *Conjunctive Normal Form*: every boolean function can be written as the *conjunction* of a set of *maxterms*.



Disjunction of minterms (canonical)

Truth tables and disjunctions of minterms (in fixed order) are canonical representations

Unfortunately very verbose!



Rules for switching algebra (2)



Disjunction of minterms (canonical)

 $f = \neg a \wedge b \wedge c \vee a \wedge \neg b \wedge \neg c \vee a \wedge \neg b \wedge c \vee a \wedge b \wedge \neg c \vee a \wedge b \wedge c$

Truth tables and disjunctions of minterms (in fixed order) are canonical representations

Unfortunately very verbose!

CHECK:
$$f' = \neg(a \lor b \land c) = \neg a \land (\neg b \lor \neg c) = \neg a \land (\neg b \lor b \land \neg c) = \neg a \land \neg b \lor \neg a \land b \land \neg c = \neg a \land \neg b \land (c \lor \neg c) \lor \neg a \land b \land \neg c = \neg a \land \neg b \land c \lor \neg a \land b \land \neg c \lor \neg a \land b \land \neg c$$

 $= a \wedge \neg b \vee \neg a \wedge b \wedge c \vee a \wedge b$

 $= a\Lambda(\neg bVb) V \neg a\Lambda b\Lambda c$

 $= a \vee \neg a \wedge b \wedge c$

 $= a \vee b \wedge c$



Disjunction of minterms

$_{a}$	b	c	f	f′	$f = a \lor b \land c$
0	0	0	0	1	$f' = \neg a \wedge \neg b \vee \neg a \wedge \neg c$
0	0	1	0	1	
0	1	0	0	1	
0	1	1	1	0	
1	0	0	1	0	
1	0	1	1	0	
1	1	0	1	0	
1	1	1	1	0	
1	a — b —	utics and C	Completer S	Science	$f = a \lor b \land c$ $f' = \neg a \land \neg b \lor \neg a \land \neg c$ $TU/e \xrightarrow{\text{Eindhoven}} \text{University of Technolo}$

Conjunction of maxterms (canonical)

a	b	c	Maxterms	f	f'
0	0	0	a \vee b \vee c = M_0	0	1
0	0	1	a $\lor b \lor \neg c = M_1$	0	1
0	1	0	$a \lor \neg b \lor c = M_2$	0	1
0	1	1	a $\vee \neg b \vee \neg c = M_3^2$	1	0
1	0	0	$\neg a \lor b \lor c = M_{4}^{3}$	1	0
1	0	1	$\neg a \lor b \lor \neg c = M_5$	1	0
1	1	0	$\neg a \lor \neg b \lor c = M_6$	1	0
1	1	1	$\neg a \lor \neg b \lor \neg c = M_7$	1	0
			·		

Maxterm:

Disjunction of signals in which every variable or its complement occurs exactly once but not both!

Maxterm form for function f:

Lines with f = 0

Input 0 : take variable

Input 1: take complement of input

Conjunction of maxterms

$$f = (a \lor b \lor c) \land (a \lor b \lor \neg c) \land (a \lor \neg b \lor c)$$
$$f' = (a \lor \neg b \lor \neg c) \land (\neg a \lor b \lor \neg c) \land (\neg a \lor \neg b \lor \neg c) \land (\neg a \lor \neg b \lor \neg c)$$



Rules for switching algebra (2)



Two level canonical forms and de Morgan

Disjunction of minterms of f' to the conjunction of maxterms of f

$$f' = \neg a \wedge \neg b \wedge \neg c \vee \neg a \wedge \neg b \wedge c \vee \neg a \wedge b \wedge \neg c$$
Using de Morgan to get **f**:
$$f = \neg (f') = (\neg a \wedge \neg b \wedge \neg c \vee \neg a \wedge \neg b \wedge c \vee \neg a \wedge b \wedge \neg c)$$

$$= (a \vee b \vee c) \wedge (a \vee b \vee \neg c) \wedge (a \vee \neg b \vee c)$$

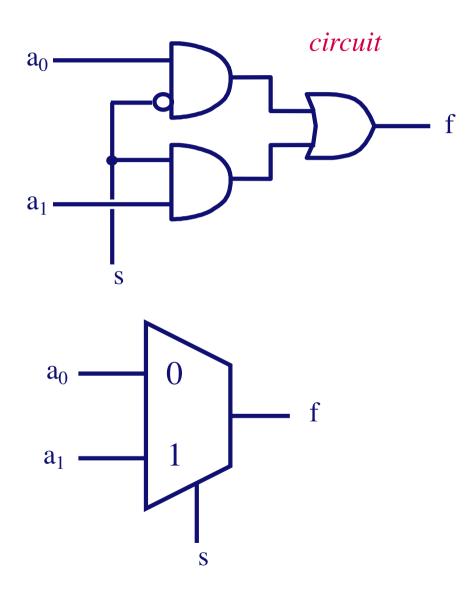
Conjunction of maxterms of f' to disjunction of minterms of f

$$f' = (a \lor \neg b \lor \neg c) \land (\neg a \lor b \lor c) \land (\neg a \lor b \lor \neg c) \land (\neg a \lor \neg b \lor \neg c)$$
Using de Morgan to get **f**:
$$f = \neg(f') = \neg((a \lor \neg b \lor \neg c) \land (\neg a \lor b \lor c) \land (\neg a \lor b \lor \neg c) \land (\neg a \lor \neg b \lor \neg c))$$

$$= \neg a \land b \land c \lor a \land \neg b \land \neg c \lor a \land \neg b \land c \lor a \land b \land \neg c \lor a \land b \land c$$



How to design a circuit from a truth table?



multiplexer

S	\mathbf{a}_0	\mathbf{a}_1	$\lfloor f \rfloor$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1
		'	•



Questions?



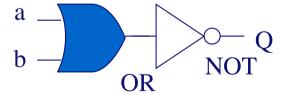


Functional completeness of a set of gates.

☐ Important question:

- ➤ Which gates do we need to implement ALL possible switching functions?
- ➤ Observe: the NOR is not necessary



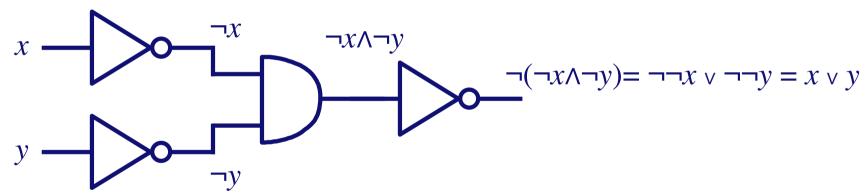




Completeness of a set of gates

- □ A set of gates is "complete" iff any switching function can be implemented by them.
- □Of course { AND, OR, NOT } is functionally complete (consider min- and maxterm implementations).

However:



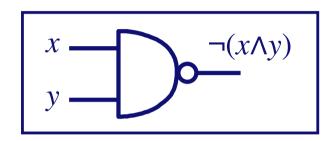
☐ Hence, one can build OR using only AND and NOT.

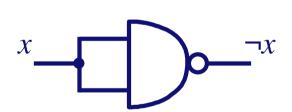
{ AND, NOT } is functionally complete (idem: { OR, NOT } is functionally complete).



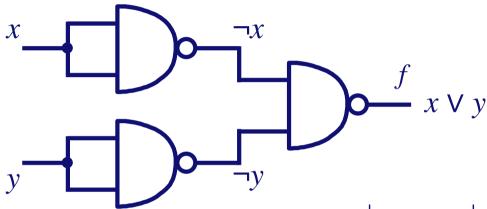
Completeness of sets of gates

A NAND gate output is 0 if and only if all inputs are 1:





The NOT, OR and AND can be built with NAND gates!

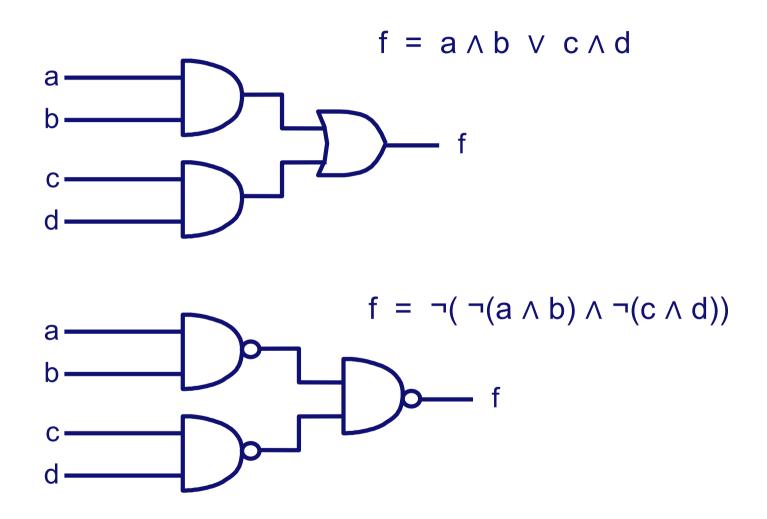


\mathcal{X}	y	$\neg x$	$\neg y$	\int
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

{ NAND } is functionally complete (idem: { NOR } is functionally complete).



Two-level AND-OR equals NAND-NAND





Questions?





Karnaugh maps: optimising circuits.

- □ Each cell corresponds to one row from the truth table.
- ☐ The upper line and left column are "neighbors" from the bottom line and right column respectively.
- ☐ Two neighbors differ on exactly one input bit.

a	b	С	a	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	.1	0	0	0
nt of Ma	ithemat	tics and (Computer	Science

\ ab				
cd	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	1	1	1	1
10	1	0	0	1



Karnaugh maps: optimising circuits.

a	b	c	d	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

ab	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	1	1	1	1
10	1	0	0	1



Minterms in Karnaugh maps

\ ab				
cd	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

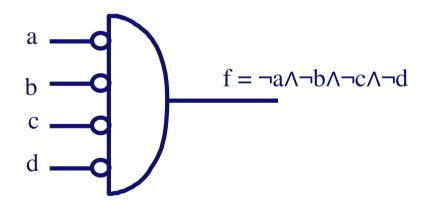
minterm = $\neg a \land \neg b \land \neg c \land \neg d$ (that is where output is 1)

		b			
	1	0	0	0	
	0	0	0	0	٦
c	0	0	0	0	d
	0	0	0	0	
			a		



Minterms in Karnaugh maps

\ ab				
cd	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0



minterm = $\neg a \land \neg b \land \neg c \land \neg d$ (that is where output is 1)



Minterms and maxterms in Karnaugh maps

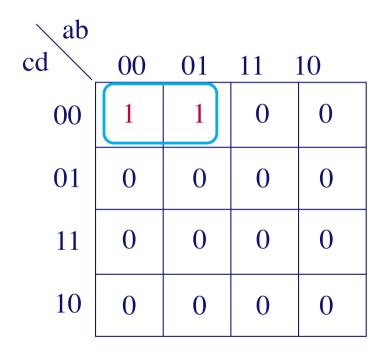
ab				
cd	00	01	11	10
00	1	1	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

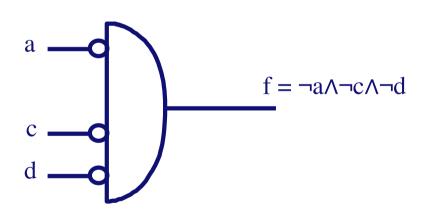
		b			
	1	1	0	0	
	0	0	0	0	.1
	0	0	0	0	d
C	0	0	0	0	
			a		

minterm = $\neg a \land \neg c \land \neg d$ (that is where output equals 1)



Minterms and maxterms in Karnaugh maps

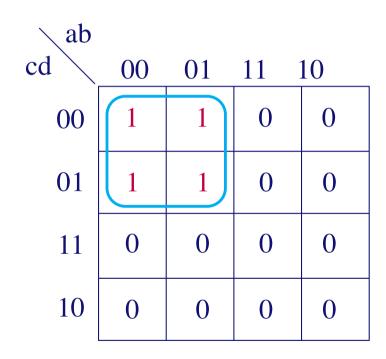




minterm = $\neg a \land \neg c \land \neg d$ (that is where output equals 1)



Minterms and maxterms in Karnaugh maps



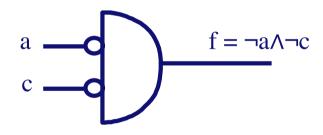
		b			
	1	1	0	0	
	1	1	0	0	a
0	0	0	0	0	d
C	0	0	0	0	
			a		

minterm = $\neg a \land \neg c$ (that is where output equals 1)



Minterms and maxterms in Karnaugh maps

\ ab				
cd	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

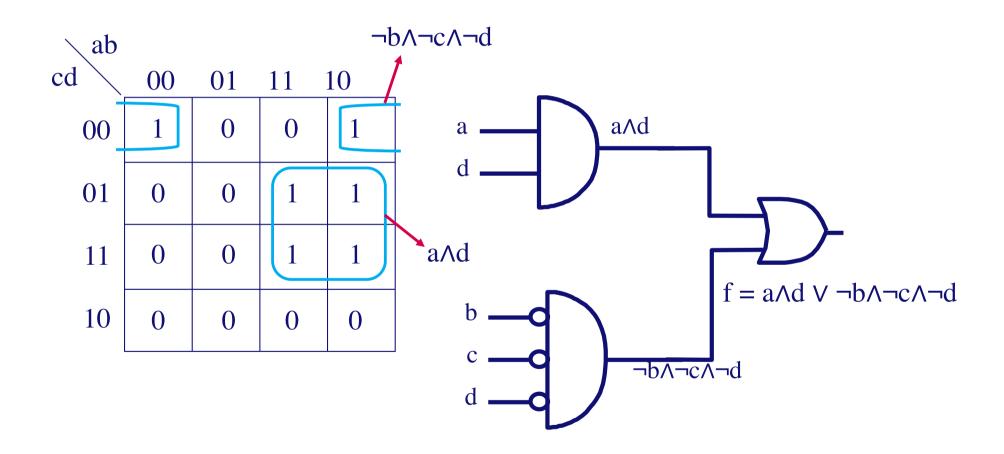


minterm = $\neg a \land \neg c$ (that is where output equals 1)



Minimal 2 level expressions

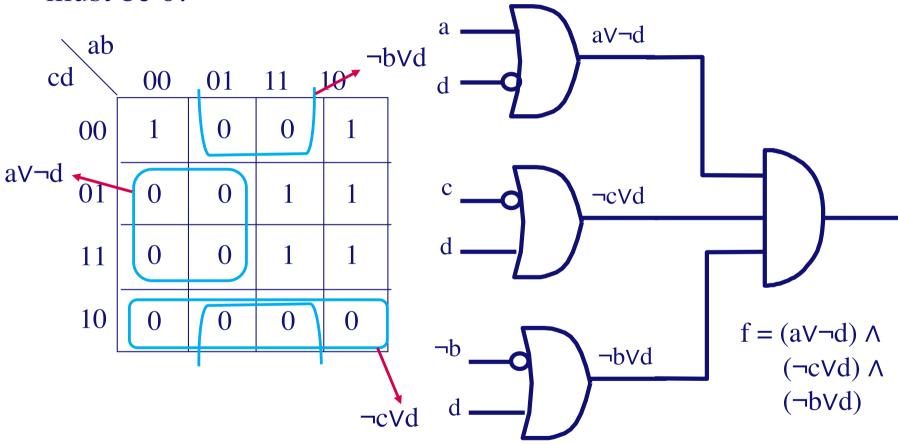
In a Karnaugh map, group rectangular areas of size $2^{N} \times 2^{M}$:





Karnaugh maps with maxterms.

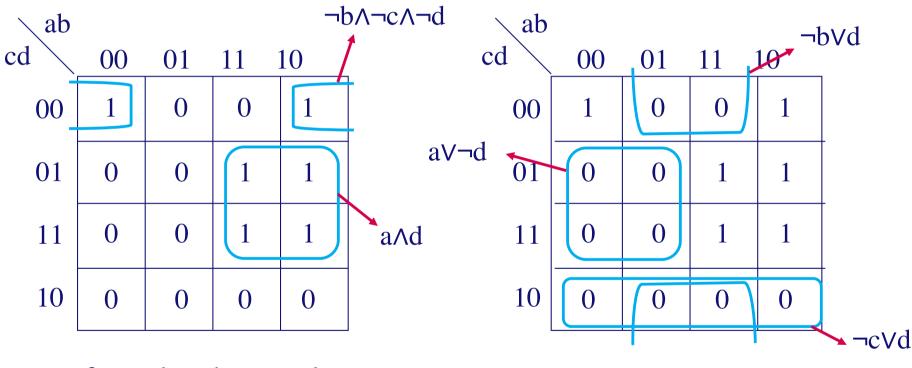
Dual approach: using maxterms we indicate where the output must be 0.





Minimal 2 level expressions

In a Karnaugh map, group rectangular areas of maximal size $2^{N} \times 2^{M}$:



 $f = a \wedge d \vee \neg b \wedge \neg c \wedge \neg d$

minimal disjunction of minterms

$$f = (aV \neg d) \land (\neg cVd) \land (\neg bVd)$$

minimal conjunction of maxterms

Everybody makes mistakes. Double checking is a good idea!!!!



"Don't cares"

"Don't cares" are function values that are irrelevant: they may be chosen by the circuit designer

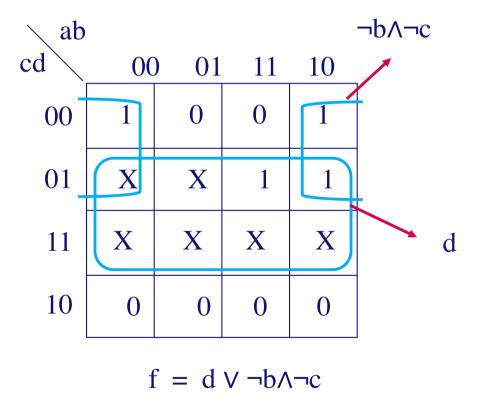
a	b	c	d	f
0	0	0	0	1
0	0	0	1	X
0	0	1	0	0
0	0	1	1	X
0	1	0	0	X 0 X 0 X
0	1	0	1	X
0	1	1	0	0
0	1	1	1	
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	X 0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	X

√ ab					
cd	00	01	11	10	
00	1	0	0	1	
01	X	X	1	1	
11	X	X	X	X	
10	0	0	0	0	

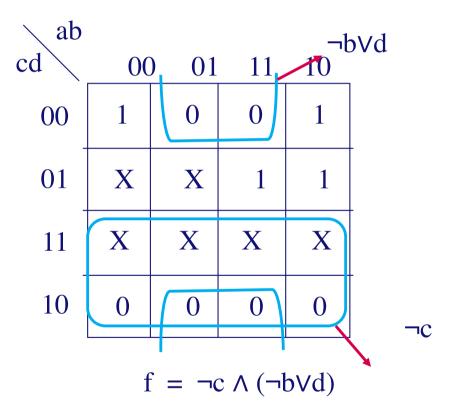


Karnaugh maps with "don't cares"

"Don't cares" are function values that are irrelevant: they may be chosen by the circuit designer



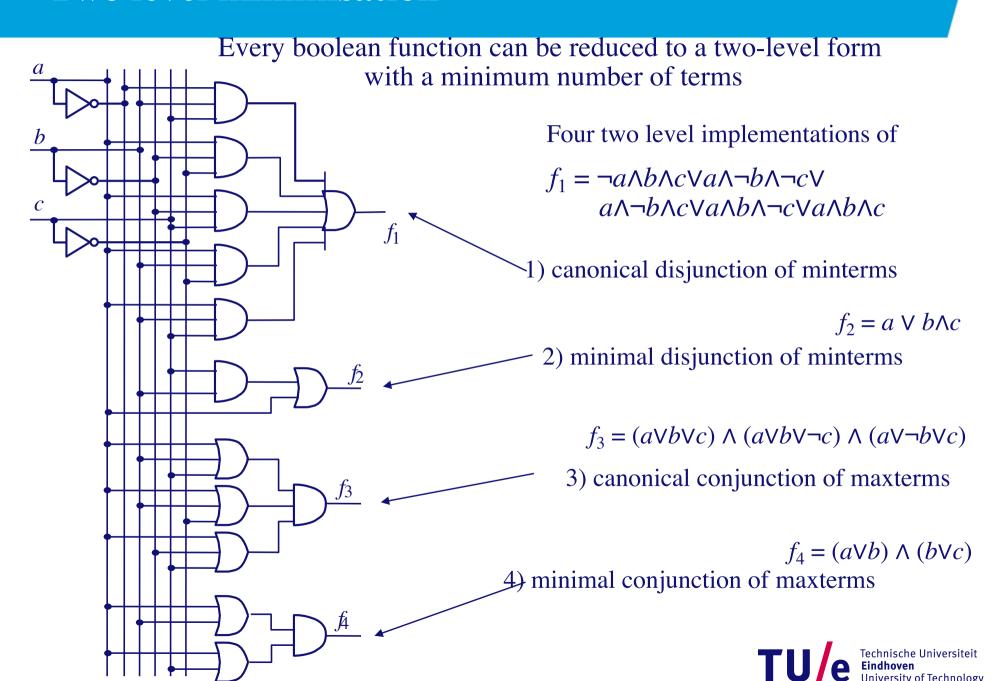
minimal disjunction of minterms



minimal conjunction of maxterms



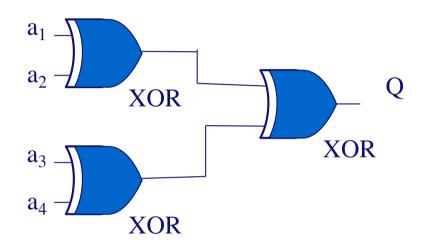
Two level minimisation



A circuit to determine the parity.

The parity of the input is 1 if the number of inputs that is 1 is odd.

a_1	a_2	\mathbf{a}_3	a_4	f
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



For inputs $a_1,...,a_n$ there are n-1 XOR gates with a depth of log(n) rounded up.

For inputs $a_1,...,a_n$ a two layer solution needs an exponential number of gates.

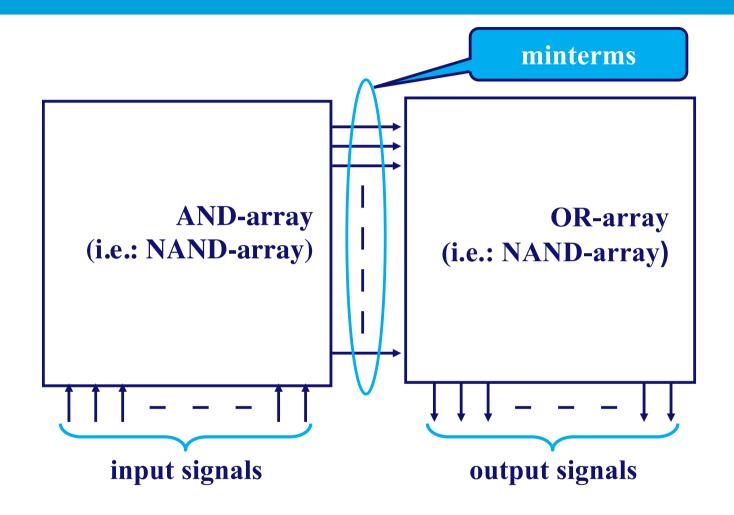


Questions?



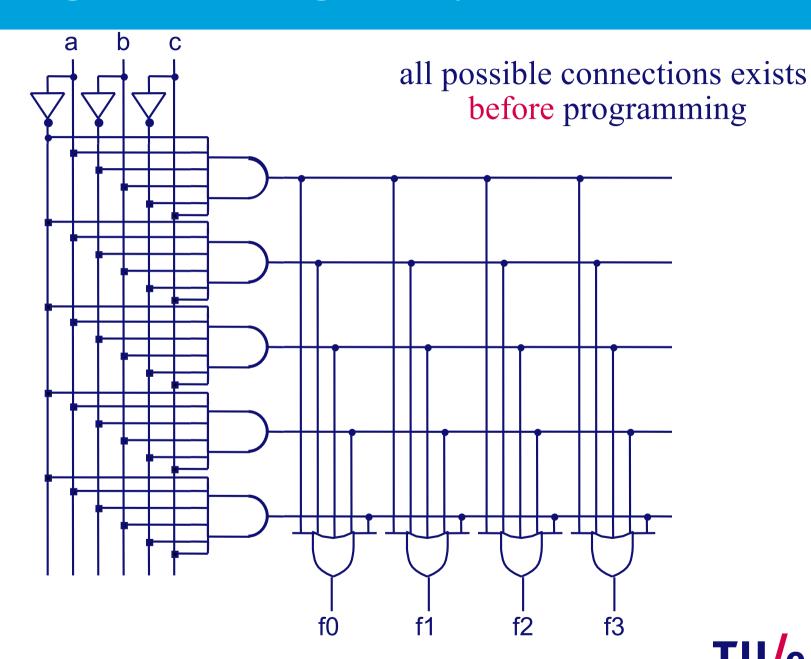


Programmable Logic Array (PLA)



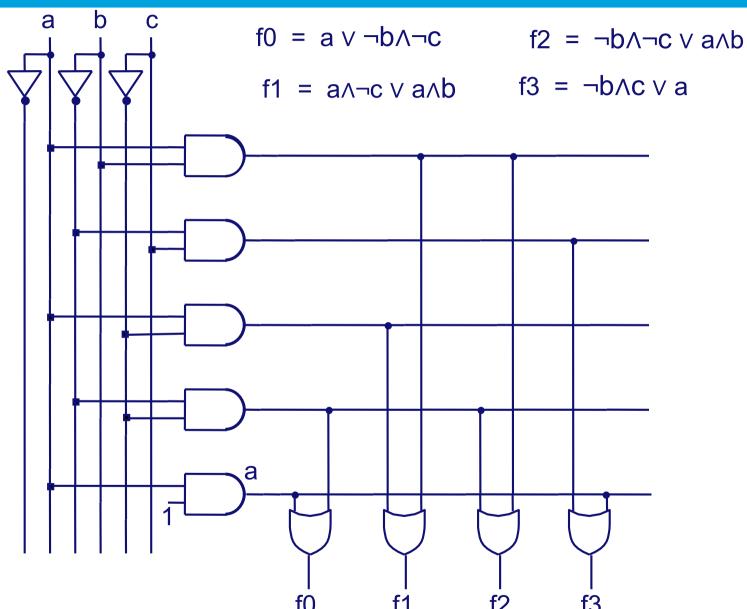


Programmable Logic Array (PLA)





Programmed Logic Array: connections removed





Summary?





Summary

What did you learn:

- Maxterms, minterms, conjunctive and disjunctive normal form.
- How to translate a circuit to a formula and truth table, and vice versa.
- How to design a minimal circuit; use Karnaugh diagrams and boolean algebra.
- Know that there are several ways to optimize circuits. There is not always a single good way.

