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Optimization of Central Source Contact Length to Mitigate Temperature Variation and Thermal Crosstalk in Multi-Finger AlGaN/GaN HEMTs: Reliability-based Simulation

Chae-Yun Lim, Jae-Hun Lee, Tae-Sung Kim, Yeong-Hyun Won, Byoung-Gue Min, Dong Min Kang, and Hyun-Seok Kim

Abstract—**Thermal crosstalk and temperature variations among gate fingers hinder the operation of multi-finger AlGaN/GaN high-electron-mobility transistors (HEMTs) by increasing channel lattice temperatures and exacerbating the degradation of device performance. These thermal phenomena intensify channel temperature variations, further accelerating performance degradation and elevating failure rates in multi-finger HEMTs. Although self-heating effects in AlGaN/GaN HEMTs have been widely investigated, the thermal issues with multi-finger configurations, including thermal crosstalk and temperature non-uniformity, have not been extensively studied. This study investigates the thermal and DC characteristics of single-finger and multi-finger HEMTs to mitigate thermal crosstalk and inter-finger temperature variations. The design of a four-finger HEMT is optimized by adjusting the central source contact length to 6 μm, which increases the spacing between the second and third gate fingers to reduce thermal interaction and ensure uniform temperature distribution. The proposed configuration enhances the DC and thermal characteristics, delivering a more uniform temperature distribution among the fingers than the conventional structure, albeit at the expense of reduced area efficiency, which reveals a trade-off between performance and spatial utilization. Nevertheless, the optimized design improves the thermal stability and reliability of multi-finger HEMTs, addressing key concerns with AlGaN/GaN power devices.**

Index Terms—**multi-finger, thermal crosstalk, gallium nitride (GaN), high−electron−mobility transistor (HEMT).**

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I. INTRODUCTION

Over the past several decades, silicon has maintained its position as a major focus for the semiconductor industry. However, in recent years, wide-bandgap (WBG) semiconductors have gained significant attention [1], [2] as they offer superior performance compared with silicon-based semiconductors, including higher breakdown voltages (3.5×10^6 V/cm for SiC, 2×10^6 V/cm for GaN, and 0.3×10^6 V/cm for Si) [3] and melting points (3100 °C for SiC, 2277 °C for GaN, and 1414 °C for Si) [4], [5], [6]. Considering these exceptional material and electrical properties, WBG semiconductors represent an excellent alternative for high-voltage applications and high-efficiency power converters. Among WBG semiconductors, GaN high-electron-mobility transistors (HEMTs) are particularly notable due to their advantages in high-temperature, high-voltage, and high-frequency operations [7]. The wide bandgap (3.4 eV for GaN and 1.12 eV for Si) and high operating temperature limit (700 °C for GaN, 300 °C for Si, and 600 °C for SiC) of GaN enable stable operation under extreme conditions. Furthermore, the unique characteristics of the AlGaN/GaN heterojunction, known as the two-dimensional electron gas (2-DEG), provide high electron mobility and remarkably fast switching speeds [8]. Because of these attributes, GaN HEMTs are highly competitive for radio-frequency (RF) circuits, radar systems, and communication applications [9]. A key advantage of this layout is that it reduces the extrinsic gate resistance, which strongly affects the RF noise performance and the maximum frequency oscillation (f_{max}) [10]. In high-power RF device design, the multi-finger gate structure, where multiple gate fingers are arranged in parallel to enhance performance, has been widely adopted [11], [12]. However, this configuration introduces mutual interference between gate fingers, which not only degrades electrical performance but also causes thermal issues, ultimately reducing the device's lifetime [13], [14], [15]. With the growing importance of thermal management in device reliability and performance, thermal crosstalk—which results in temperature variations and additional temperature rises in multi-finger HEMTs compared with single-finger devices—has become a significant challenge,

particularly for power-efficient designs [14], [16]. In this study, we conducted a reliability-based technology computer-aided design (TCAD) simulation using measured device characteristics to analyze the impact of thermal crosstalk under various conditions. To mitigate thermal crosstalk in a four-finger HEMT, we optimized the central source contact length by varying it from 3 to 9 µm. The results confirmed that a 6 µm central source contact length was the most effective in achieving uniform distribution of heat across the gate fingers and alleviating thermal crosstalk. This optimization yielded significant improvements in key performance metrics, including saturation drain current, transconductance, and channel temperature uniformity. The remainder of this article is organized as follows: Section II provides an overview of the fabrication process and the modeling of the reference AlGaN/GaN HEMT. Section III describes the setup for simulating the operational and thermal characteristics of the device. Section IV discusses the simulation results, focusing on the impact of thermal crosstalk in multi-finger HEMTs. Subsequently, we detail the analysis of the device's electrical performance with the optimized central source contact length in a four-finger configuration and discuss its correlation with area efficiency and the temperature distribution among the fingers. Finally, Section V summarizes the study, highlighting its contributions to improving thermal management in multi-finger GaN HEMTs.

II. DEVICE FABRICATION AND MODELING

Fig. 1(a) shows a transmission electron microscopy (TEM) image of the fabricated planar-gate, four-finger HEMT structure, and Fig. 1(b) depicts the device layout. Fig. 2 presents a cross-sectional view of this device. We used a 0.15-µm planar-gate AlGaN/GaN HEMT fabricated on a 4-inch SiC substrate as the reference device for comparison. The epitaxial layers—comprising a 0.2-µm-thick nucleation layer, a 2-µm-thick Fe-doped GaN buffer layer, and a 25-nm-thick $Al_{0.255}Ga_{0.745}N$ barrier layer—were grown via metal-organic chemical vapor deposition. Ohmic contact metallization was performed by sequentially depositing Ti (30 nm), Al (100 nm), Ni (30 nm), and Au (100 nm) via electron-beam evaporation, followed by rapid thermal annealing at 775 °C for 30 s. Device isolation was achieved through a P+ ion implantation process, with plasma-enhanced chemical vapor deposition (PECVD)–deposited SiN and a photoresist as the masks. Thin-film resistors were fabricated using NiCr to achieve a sheet resistance of 20 Ω/sq; this involved image-reversal photoresist patterning using a stepper, followed by a lift-off process. For the first metal interconnection, vias were opened by etching the PECVD SiN layer using inductively coupled plasma. The gate head was fabricated using double resist layers (co-polymer/poly methyl methacrylate resist) through an electron-beam lithography process, followed by Ni/Au deposition and a lift-off process. The SiN dielectric layer was deposited via PECVD. Subsequently, a source-connected field plate was formed by depositing Ti/Au and then performing a lift-off process. The device was modeled based on the geometrical parameters listed in Table I. Fig. 3(a) and 3(b) respectively present a top view and cross-sectional view of the device, which was used for TCAD modeling.
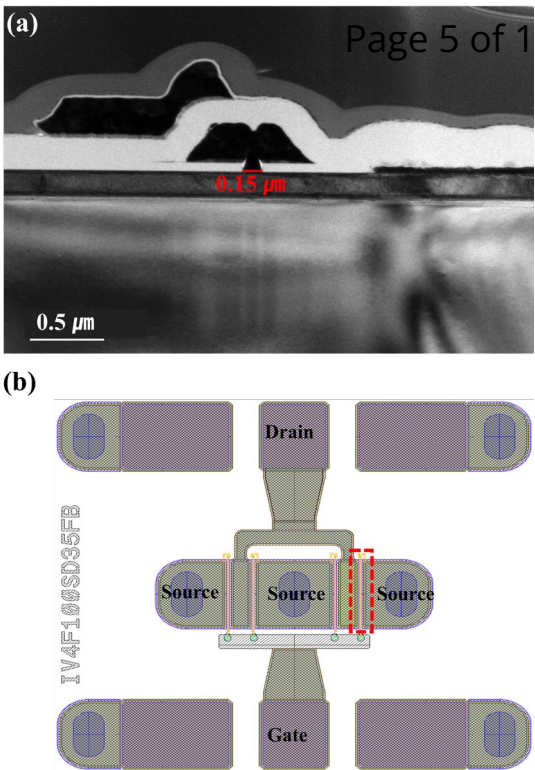
Fig. 1. (a) TEM image and (b) device layout of fabricated planar-gate, four-finger HEMT structure; the dashed red box outlines the one-finger gate electrode.
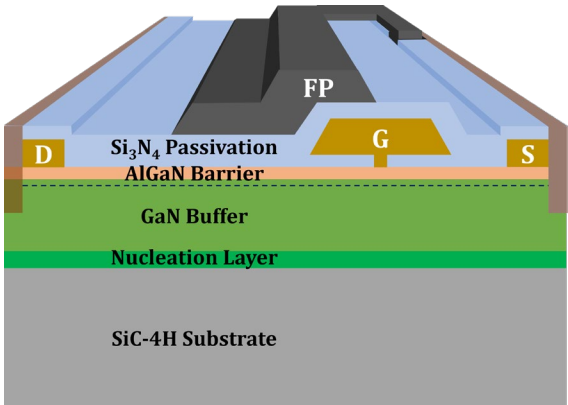
Fig. 2. Cross-sectional schematic of fabricated planar-gate AlGaN/GaN HEMT with source-connected field plate.

TABLE I
GEOMETRICAL PARAMETERS OF PLANAR-GATE HEMT

Parameter	Value (µm)	Parameter	Value (µm)
SiC substrate	5	L_{GD}	1.5
Nucleation layer	0.2	$L_{G.HEAD\_TOP}$	0.8
GaN buffer	2	$L_{G.HEAD\_BOT}$	1.0
AlGaN barrier	0.025	$L_{FP.TOP}$	1.4
1st Si_3N_4 passivation	0.05	$L_{FP.BOT}$	1.6
2nd Si_3N_4 passivation	0.25	L_{SOURCE}	3.0
L_{SD}	3	L_{DRAIN}	1.0
$L_{G.FOOT}$	0.15	L_{SG}	0.5

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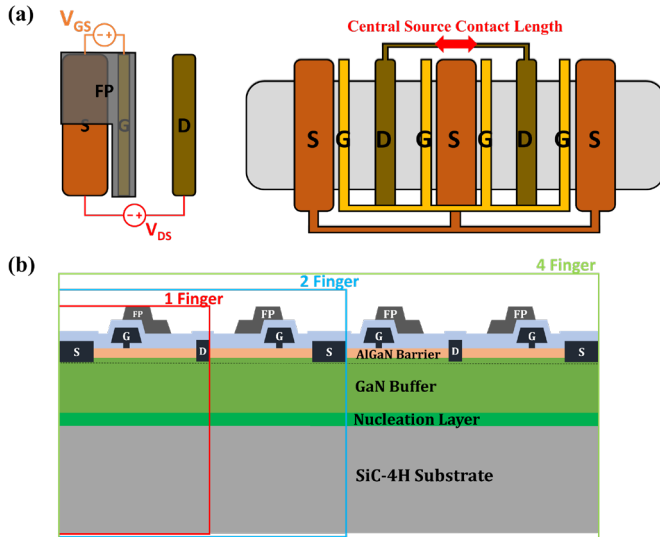
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Fig. 3. (a) Top view of planar-gate AlGaN/GaN HEMT showing the layout of the source (S), gate (G), and drain (D) contacts. (b) Schematic of modeling structure up to four-finger configuration for simulation.

III. Simulation Setup

TABLE II
THERMAL PARAMETERS OF PLANAR-GATE HEMT

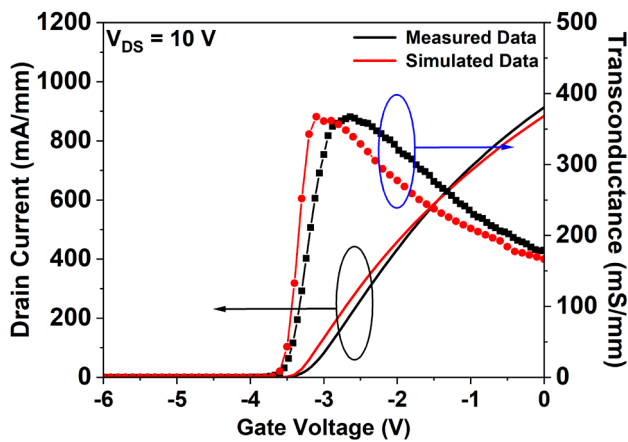| Parameter	Unit	GaN	AlGaN	SiC
TC.CONST	W/cm·K	1.3	0.4	3.3
TC.NPOW	–	0.43	0	1.61

Fig. 4. Measured and simulated results for planar-gate HEMT: I_{DS}–V_{GS} characteristics at a drain bias (V_{DS}) of 10 V.

We investigated the operational behavior of AlGaN/GaN HEMT devices through TCAD simulations. To solve the lattice heat flow equation, at least one thermal boundary condition must be defined. We established the required boundary condition using the following relationship:

$$\sigma\left(\vec{J_{tot}^{\,\vec{u}}} \cdot \vec{s}\right) = \alpha(T_L - T_{ext}), \qquad (1)$$

where σ is either 0 or 1, $\vec{J_{tot}^{\,\vec{u}}}$ is the total energy flux, and $\vec{s}$ represents the unit external normal vector at the boundary. The energy flux projection along the normal vector is expressed as

$$\left(\vec{J_{tot}^{\,\vec{u}}} \cdot \vec{s}\right) = -\kappa\frac{\partial T_L}{\partial n} + (T_L P_n + \phi_n)\vec{J_n} \cdot \vec{s} \\ + (T_L P_p + \phi_p)\vec{J_p} \cdot \vec{s}. \qquad (2)$$

For $\sigma = 0$, Equation (1) defines a Dirichlet boundary condition, which corresponds to a fixed temperature boundary. Such a boundary condition can be applied to either external surfaces or specific internal electrodes within the device. When $\sigma = 1$, Equation (1) adopts the following form:

$$\left(\vec{J_{tot}^{\,\vec{u}}} \cdot \vec{s}\right) = \frac{1}{R_{th}}(T_L - TEMPER). \qquad (3)$$

TEMPER denotes the external boundary temperature of the device, serving as a parameter necessary for calculating the heat distribution accurately. Here, the thermal resistance R_{th} represents the heat transfer resistance between the substrate and its external environment. It is inversely related to thermal conductance and is vital in regulating the heat flow across the boundary. We performed simulations by setting the thermal boundary resistance value $(1/\alpha)$ of the SiC-4H substrate by 2.5×10^{-8} m²K/W, a value consistent with the actual range at the interface between any material and GaN [17]. To enable thermal crosstalk analysis, thermal effects were integrated into the operational models. The heat generated by self-heating effects (SHEs) was accounted for through the following heat generation equation [18]:

$$H = \left[\frac{|\vec{J_n}|^2}{q\mu_n n} + \frac{|\vec{J_p}|^2}{q\mu_p p}\right] + q(R - G)\left[\phi_p - \phi_n + T_L(P_p - P_n)\right] \\ - T_L\left(\vec{J_n}\nabla P_n + \vec{J_p}\nabla P_p\right). \qquad (4)$$

The first term, $\left[\frac{|\vec{J_n}|^2}{q\mu_n n} + \frac{|\vec{J_p}|^2}{q\mu_p p}\right]$, represents Joule heating, and second term, $q(R - G)\left[\phi_p - \phi_n + T_L(P_p - P_n)\right]$, describes the heating and cooling effects of carrier recombination (R) and carrier generation (G). Here, ϕ_p and ϕ_n are the quasi-Fermi levels for holes and electrons, while P_p and P_n are the corresponding thermodynamic pressures, respectively. The lattice temperature (T_L) influences these effects, highlighting the interaction between electrical and thermal phenomena. The last term, $T_L\left(\vec{J_n}\nabla P_n + \vec{J_p}\nabla P_p\right)$, represents the Peltier and Joule–Thomson effects. Considering the substantial impact of thermal conductivity on thermal effects, we adopted a thermal conductivity model; Table II summarizes the essential parameters for thermal modeling, where TC.CONST and TC.NPOW denote the room-temperature constant and the calibration factor, respectively [19]. Various simulation models and material property parameters were applied to the HEMT structure to accurately replicate the physical mechanisms governing semiconductor device operation. Models such as Fowler–Nordheim tunneling, Shockley–Read–Hall recombination, and Fermi–Dirac statistics were implemented. Additionally, two distinct field-dependent electron mobility

TABLE III
MATERIAL PARAMETERS FOR SIMULATION AT ROOM TEMPERATURE

Parameter	Unit	GaN	AlGaN
Bandgap energy	eV	3.39	3.88
Electron affinity	eV	4.2	2.3
Dielectric constant	–	9.5	9.38
Low-field electron mobility	–	Farahmand modified Caughey–Thomas model	
High-field electron mobility	–	GANSAT model	
Electron saturation velocity	cm/s	1.9×10^7	1.12×10^7
Hole saturation velocity	cm/s	1.9×10^7	1.0×10^6
Electron Shockley–Read–Hall lifetime	s	1.0×10^{-8}	1.0×10^{-8}
Hole Shockley–Read–Hall lifetime	s	1.0×10^{-8}	1.0×10^{-8}

models were employed: the Farahmand Modified Caughey–Thomas model for low-field mobility and the GANSAT model for high-field mobility. The material parameters of GaN and AlGaN, such as bandgap energy, electron affinity, and dielectric constant, were carefully calibrated. Table III provides a comprehensive summary of the models and parameters used to simulate device operation [20]. To ensure reliable simulation, all modeling parameters were calibrated based on experimental data obtained from the fabricated devices. Fig. 4 compares the simulated and measured drain current–gate voltage (I_{DS}–V_{GS}) curves for the planar-gate HEMT at a drain voltage of 10 V. The simulated drain current at a gate voltage of 0 V was 884.32 mA/mm, which closely aligns with the measured value of 913.80 mA/mm. Additionally, the simulated and measured values of maximum transconductance were 367.34 and 367.17 mS/mm, respectively, which are nearly identical. Therefore, the measured and simulated I_{DS}–V_{GS} curves agreed well, with a maximum error rate of only 3.32%, while the threshold voltage was maintained at −3.5 V.

IV. RESULTS AND DISCUSSION

A. Thermal Crosstalk–Induced Degradation of DC Characteristics in Multi-Finger HEMTs

We focused on device characteristics such as the temperature variation between gate fingers, maximum drain current ($I_{D,MAX}$), and on-resistance (R_{ON}) in GaN HEMTs, with a particular emphasis on the effects of thermal crosstalk in multi-finger devices. The degradation of electrical performance due to thermal crosstalk was analyzed by comparing planar-gate devices featuring one, two, four, and eight fingers to examine the channel lattice temperature distribution and its impact on DC characteristics. Fig. 5(a) illustrates the channel lattice temperature distribution at a V_{GS} of 0 V and V_{DS} values of 20 V and 40 V. Fig. 5(b) presents a boxplot summarizing the maximum, minimum, and average lattice temperatures from Fig. 5(a). The rise in the temperature of an HEMT device is attributed to two factors: SHEs and thermal crosstalk. Thermal crosstalk, defined as the difference between the peak temperature of a single-finger device and that of multi-finger devices, intensifies self-heating issues, leading to uneven temperature distributions and ultimately affecting the device's reliability [14], [21]. At the V_{DS} of 40 V, thermal crosstalk–induced temperature increases of 9.03 K, 27.03 K, and 34.98 K were observed for the two-, four-, and eight-finger devices,
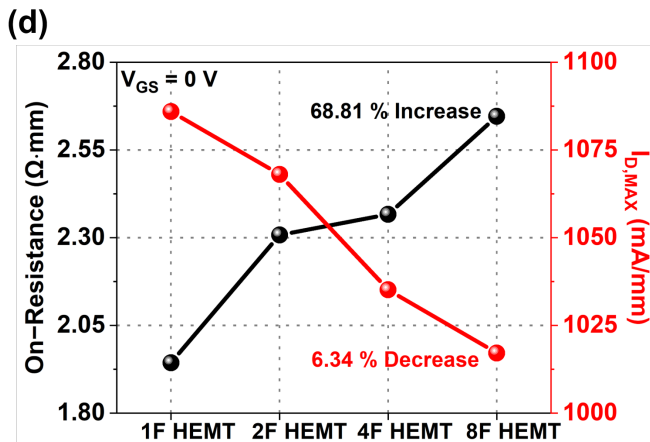
(a)

(b)

(c)

(d)
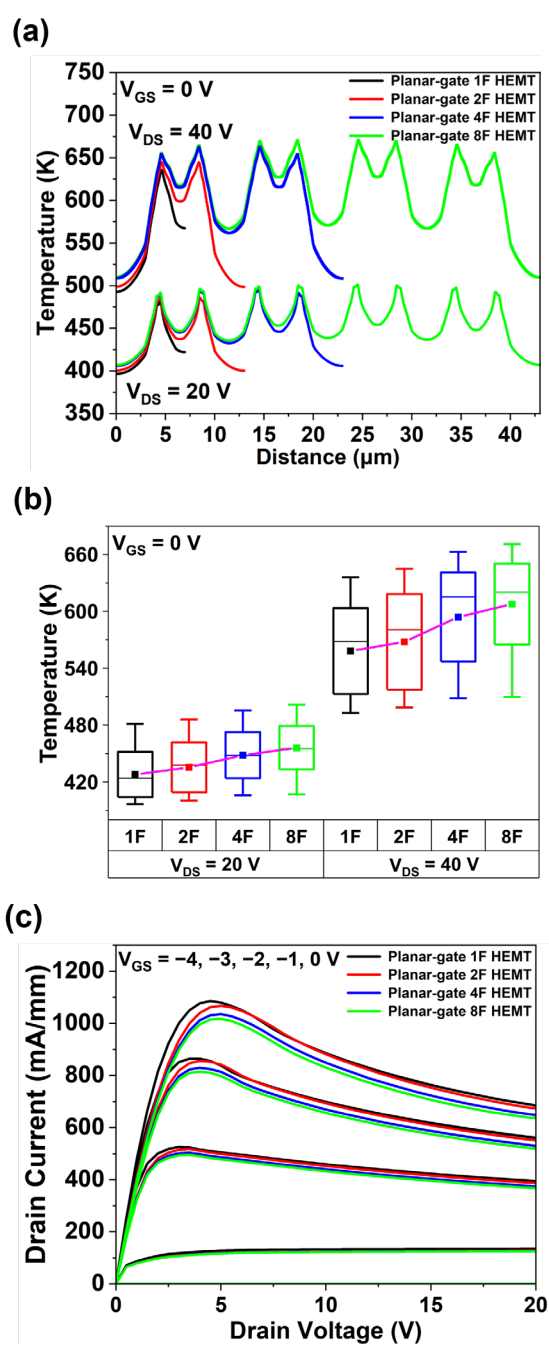
Fig. 5. Simulation results for planar-gate HEMT devices with one, two, four, and eight fingers: (a) Lattice temperature distribution along 2-DEG channel at V_{DS} of 20 V and 40 V. (b) Boxplots of lattice temperature at V_{DS} of 20 V and 40 V. (c) I_{DS}–V_{DS} characteristics at V_{GS} of −4, −3, −2, −1, and 0 V. (d) Variations in R_{ON} and $I_{D,MAX}$.

respectively. Notably, the average device temperature increased significantly, rising by 9.58 K, 35.77 K, and 49.53 K for the two-, four-, and eight-finger devices, respectively. The minimum channel temperature also increased by approximately 16.83 K for the eight-finger configuration. As V_{DS} increased, the difference in peak temperatures between the devices became more pronounced, causing thermal crosstalk to have a greater impact on device performance. Fig. 5(c) presents the I_{DS}–V_{DS} output characteristics, demonstrating that the drain current decreased as the number of fingers increased, primarily

due to heat accumulation within the device. R_{ON} was extracted from the slope of the I_{DS}–V_{DS} curve near a V_{GS} of 0 V under a V_{GS} of 0 V. Fig. 5(d) demonstrates a 68.61% increase in R_{ON} and a 6.34% decrease in $I_{D,MAX}$ with an increasing number of fingers, which reflects a simultaneous deterioration in both parameters [22], [23]. This increase in R_{ON} led to greater conduction losses, poorer switching performance, and a lower power density in the GaN HEMTs [24].

B. Widening Central Source Contact Multi-Finger Design to Mitigate Thermal Crosstalk

The previous subsection demonstrated that increasing the number of gate fingers from one to eight significantly enhanced thermal crosstalk, particularly under a high drain voltage of 40 V. By analyzing configurations with up to eight gate fingers, we observed a progressive intensification of thermal crosstalk and its substantial impact on the operational and thermal performance of the device. To mitigate this issue, we introduced an optimization strategy that involved extending the length of the central source contact between the second and third gate fingers—the region where the heat was the most concentrated—from 3 μm to 6 μm in 1 μm increments. To ensure reliable simulation results, a fabricated four-finger HEMT was utilized as the baseline device for simulation analysis. Fig. 6(a) illustrates the lattice temperature distribution in the channel at a V_{DS} of 40 V, showing that the peak temperature decreased as the central source contact length increased. Specifically, the maximum thermal crosstalk in the 6 μm configuration was 9.39 K, which represents a reduction of 17.64 K (65.27%) from the 27.03 K in the 3 μm configuration; this reduction significantly alleviated heat concentration on the
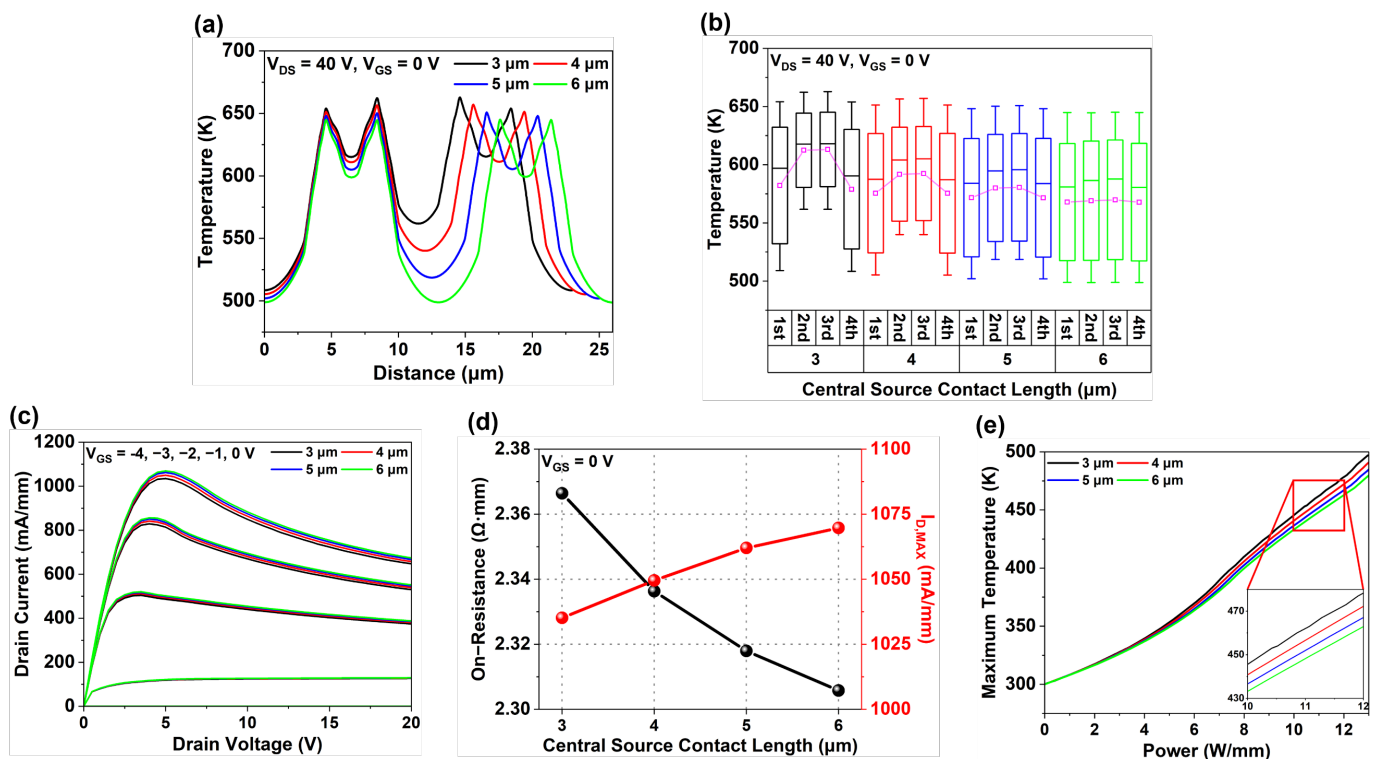

Fig. 6. Thermal and DC properties of four-finger HEMT for central source contact lengths of 3–6 μm: (a) Lattice temperature distribution along 2-DEG channel at V_{DS} of 20 V and 40 V. (b) Temperature variation among gate fingers at V_{DS} of 40 V and V_{GS} of 0 V. (c) I_{DS}–V_{DS} characteristics at V_{GS} of −4, −3, −2, −1, and 0 V. (d) R_{ON} and $I_{D,MAX}$ at V_{GS} of 0 V. (e) Device temperature as a function of power density.

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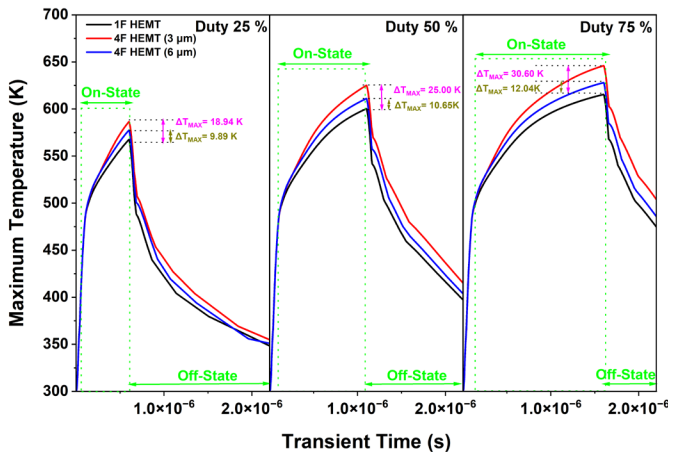
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Fig. 7. Transient thermal responses under 25%, 50%, and 75% duty cycles with V_{DS} pulsed between 0 V and 40 V for a total on/off duration of 2 µs.

TABLE IV
ΔT_{MAX} AS A FUNCTION OF CENTRAL SOURCE CONTACT LENGTH AND DUTY CYCLE WITHIN A SINGLE PULSE

Central source contact length (µm)	Duty cycle (%)	ΔT_{MAX} (K)
3	25	18.94
	50	25.00
	75	30.60
6	25	9.89
	50	10.65
	75	12.04

second and third gate fingers. Fig. 6(b) presents a boxplot illustrating the temperature distribution across the four-finger device, which was divided into four zones, with the temperature distribution in each zone represented by maximum, minimum, and average values. As the source contact length increased, the average temperature difference between the outer fingers (1, 4) and the central fingers (2, 3) decreased from 32.27 K to 1.59 K. Additionally, the overall average temperature difference between the single-finger and four-finger configurations decreased significantly, from 38.55 K at 3 µm to 10.52 K at 6 µm. As illustrated in the figure, the temperature distribution between the fingers became exceptionally uniform, highlighting a significant improvement in thermal uniformity from the 3 µm to the 6 µm configuration. Fig. 6(c) depicts the improvement in drain current with the increase in the central source contact length, particularly at higher gate voltages. The 6 µm configuration achieved the highest drain current across all tested drain voltages, reflecting the effectiveness of reduced thermal crosstalk in enhancing thermal and electrical performance. Furthermore, Fig. 6(d) highlights the significant reduction in on-resistance with the increase in the central source contact length, accompanied by a concurrent rise in maximum drain current. These trends underscore the operational benefits of optimizing the central source contact length. Finally, Fig. 6(e) presents the temperature differences across configurations under varying power densities. While differences were less pronounced at lower power densities, the advantages of extending the central source contact length became increasingly evident at higher power densities, particularly at 10–12 W/mm. For instance, at a power density of 12 W/mm, the overall device

temperature for the 6 µm configuration was approximately 17.45 K lower than that for the 3 µm configuration. Steady-state temperature measurements and simulations have shown that thermal resistance is influenced by design parameters such as finger count, finger width, and gate pitch [14]. However, steady-state analysis is inherently limited to evaluating fixed design factors and cannot account for the dynamic evolution of thermal crosstalk during device operation. This limitation underscores the necessity of time-dependent thermal analysis for fully understanding the impact of on-time duration on thermal behavior. In transient thermal analysis, when the lattice heat flow equation is solved, the global device temperature corresponds to the maximum temperature at any mesh point in the device. Hence, the device temperature at any given instant represents the maximum temperature, whereby time-dependent temperature differences constitute a direct measure of thermal crosstalk. Herein, the maximum time-dependent thermal crosstalk (ΔT_{MAX}) is defined as the largest temperature difference between the single-finger and multi-finger configurations during the on-state of a single applied pulse. The thermal response was analyzed within a single applied pulse alternating between an on-state (V_{GS} of 0 V and V_{DS} of 40 V) and an off-state (V_{GS} and V_{DS} of 0 V). The total pulse duration was fixed at 2 µs, while the on-state duration was increased progressively from 0.5 µs to 1.5 µs, with the off-state duration adjusted accordingly. By examining the transient temperature profiles under these conditions, we evaluated the evolution of thermal crosstalk with varying on-time durations. As shown in Fig. 7 and Table IV, the time dependence of the thermal crosstalk became evident with an increasing on-state duration. For the 3 µm configuration, ΔT_{MAX} increased significantly, from 18.94 K at a 25% duty cycle (0.5 µs on-state) to 25.00 K at 50% (1.0 µs on-state) and further to 30.60 K at 75% (1.5 µs on-state). This substantial increase reflects the exacerbation of thermal crosstalk with extended on-times, which intensifies heat accumulation and reduces cooling efficiency during off-times. In contrast, the optimized 6 µm configuration exhibited much smaller increases in ΔT_{MAX}, starting at 9.89 K for a 25% duty cycle and rising modestly to 10.65 K at 50% and only 12.04 K at 75%.

C. Thermal and Area Efficiency Issues with Widening Central Source Contact beyond 6 µm

When the central source contact length exceeded 6.0 µm, the temperature distribution across individual fingers underwent significant changes, as shown in Fig. 8(a). Increasing the length to 7–9 µm diminished the thermal coupling effect between fingers, thereby lowering both the maximum and average temperatures of the central fingers (2 and 3) as well as slightly reducing those of the outer fingers (1 and 4). However, this improvement was achieved at the expense of increased temperature variation among the fingers, with a notable rise of approximately 35.66 K in the average temperature difference between the outer fingers (1 and 4) and the central fingers (2 and 3) when the length was increased to 9 µm. The specific on-resistance ($R_{ON,SP}$) represents R_{ON} normalized by the area of the device. Fig. 8(b) compares R_{ON} with $R_{ON,SP}$, which quantifies area efficiency, across different lengths of the central source contact [25]. While R_{ON} exhibited a negligible reduction of 0.85%, $R_{ON,SP}$ increased significantly, by 17.74%. This
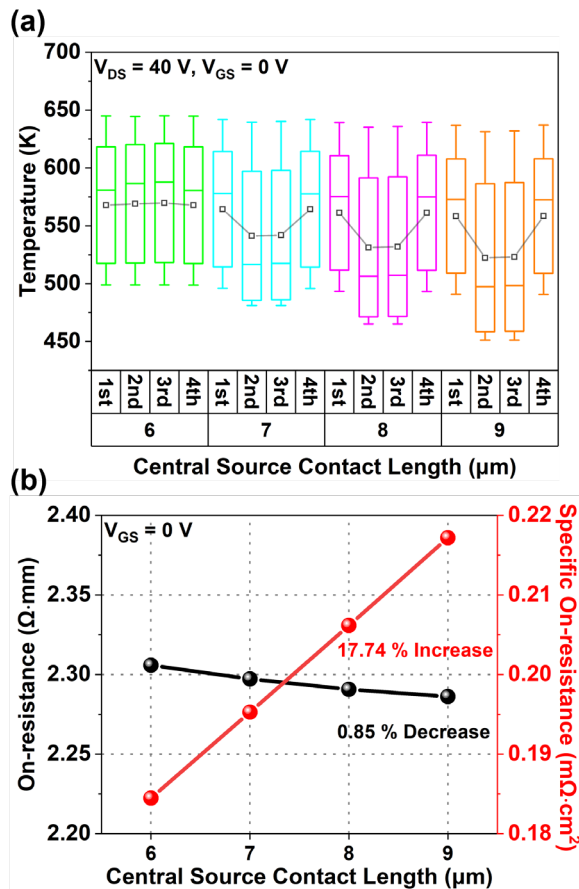
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Fig. 8. (a) Temperature distribution across gate fingers for central source contact lengths of 6–9 μm at V_{DS} of 40 V and V_{GS} of 0 V. (b) R_{ON} and $R_{ON,SP}$ as functions of central source contact length.

substantial rise in $R_{ON,SP}$ reveals a critical drawback: the area efficiency of the device decreased significantly as the central source contact' length increased. Thus, while the DC characteristics improved only minimally, the longer source contact occupied an excessive area, resulting in inefficient utilization of the device's active area. Therefore, extending the central source contact length beyond 6 μm introduced a suboptimal trade-off, with minor enhancements in DC performance being outweighed by a significant reduction in area efficiency. Thus, the design would become undesirable for high-performance applications, where compactness and efficiency are crucial. These findings underscore the importance of balancing thermal, electrical, and area efficiency considerations when optimizing device design.

V. Conclusion

This study explored thermal crosstalk in multi-finger GaN HEMTs through detailed simulations, emphasizing the adverse effects of this phenomenon on device performance and reliability. Our analyses revealed that increasing the number of gate fingers intensifies thermal crosstalk in the central fingers, thus compromising DC and thermal characteristics. To mitigate this issue, we proposed a four-finger structure featuring an extended centrally located source contact. Based on simulation results, the proposed structure delivered a 65.27% reduction in maximum thermal crosstalk for a four-finger HEMT with a 6-μm-long source contact. The thermal crosstalk in the central

finger was reduced by approximately 18 K, while the temperature distribution among the fingers was significantly uniformized. These enhancements highlight the potential of multi-finger GaN HEMT devices for high-power and high-efficiency applications.

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