

DirectX



INTRODUCING FIDELITYFX **VARIABLE SHADING**

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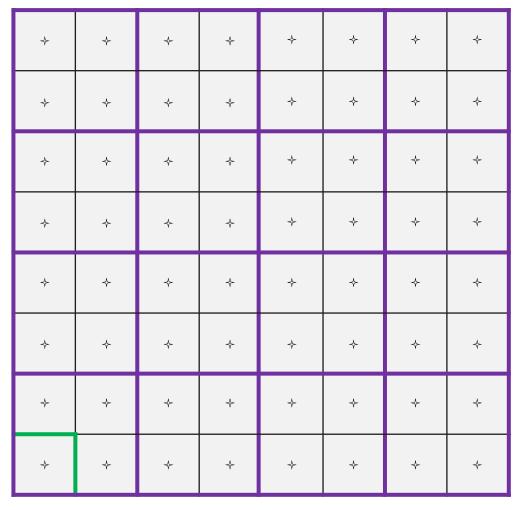


AMDA

INTRODUCTION TO VARIABLE RATE SHADING

- Variable Rate Shading (VRS) is a feature of DirectX®12 Ultimate
- Goal of VRS is to save GPU work (where it does not significantly contribute to the final frame)
- Games today are usually played at very high resolution
 - Pixels are very small on screen
 - Adjacent pixels often have similar color (if they belong to the same primitive)
- Post-processing effects like Antialiasing, Depth of Field, or Motion Blur further reduce the difference between adjacent pixels





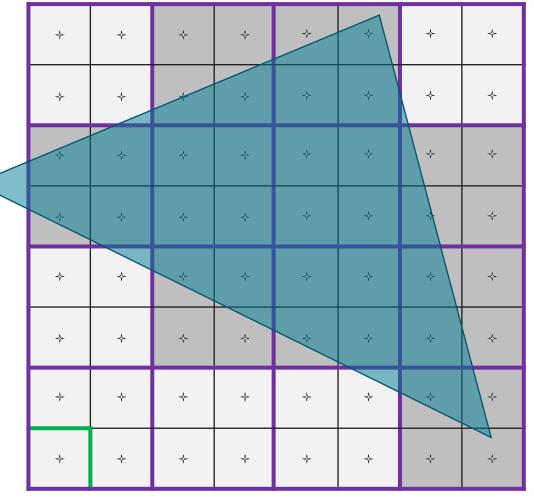
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Pixel

Quads



 Without VRS, 4 pixel shader (PS) threads are getting generated for every quad of which at least one pixel is covered by a primitive

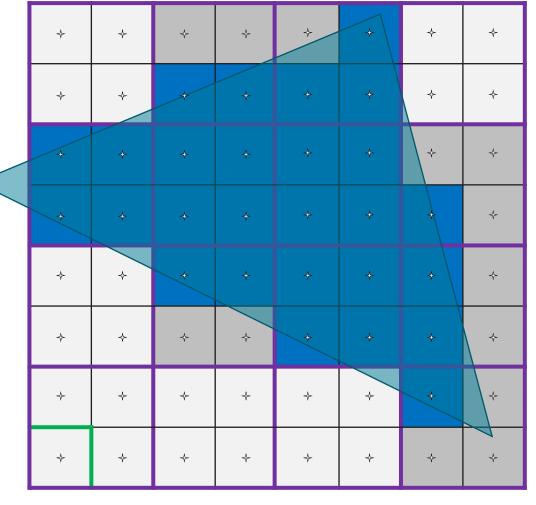




* Sample position



- Without VRS, 4 pixel shader (PS) threads are getting generated for every quad of which at least one pixel is covered by a primitive
 - For every pixel where the sample-position is covered by the primitive, the result of the PS gets written to the render target
 - Example: 10 Quads/40 PS threads (27 active)



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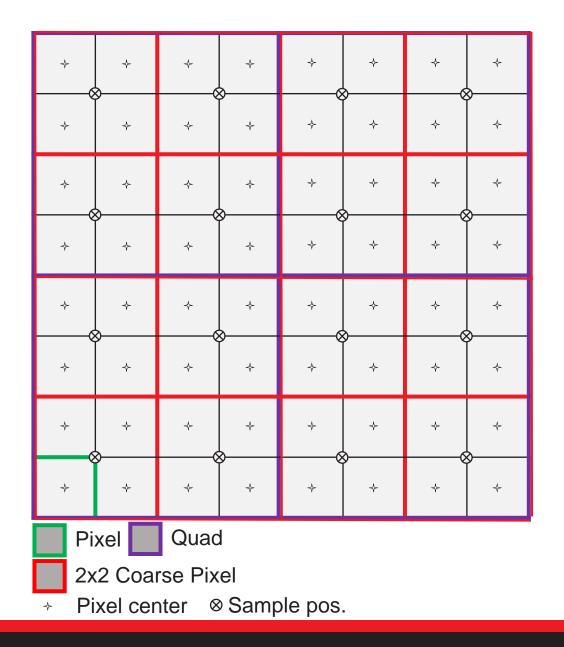




Sample position

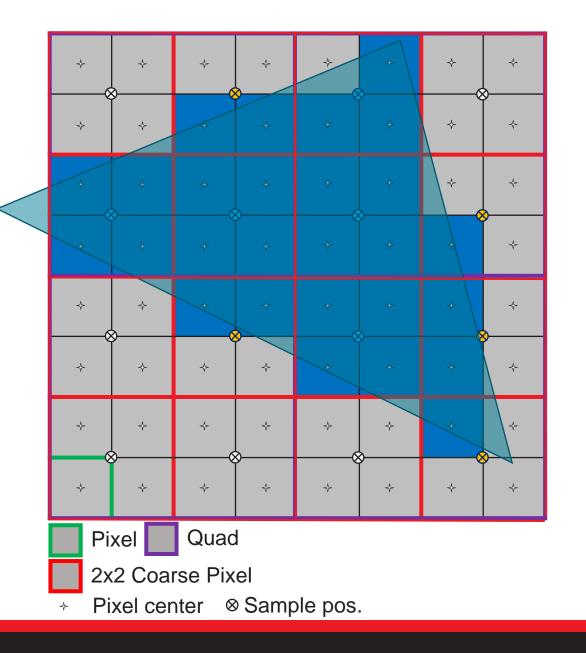


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- With VRS one or multiple pixels form a coarse pixel (2x2 in this example)
 - Example:4 Quads/16 PS threads (10 active)
 - VRS only reduces shading quality within a triangle, the geometry edges are preserved

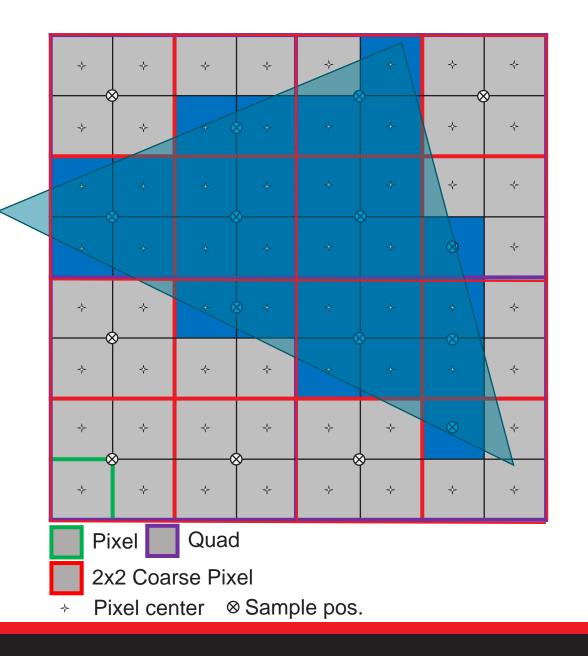




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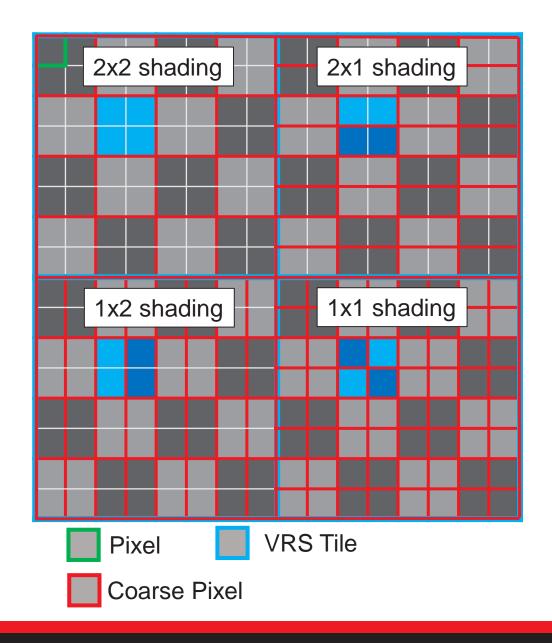
Make sure to use centroid interpolation!





VRS ON RDNA2

- VRS has multiple ways to control shading rate
 - Per drawcall (VRS tier 1)
 - Per primitive (VRS tier 2, VS/GS output)
 - Per screen tile (VRS tier 2, Image Based)
 - 8x8 pixel tile size
 - Small tile size provides fine grained control
- Additional shading rates not supported
 - At common resolutions 4x can hardly be used without generating visual artifacts
 - Additional shading rates make image generation more complex
- VRS image gets copied into H-tile on bind
 - Small (but not negligible) overhead when binding the VRS image
 - No overhead during rendering!





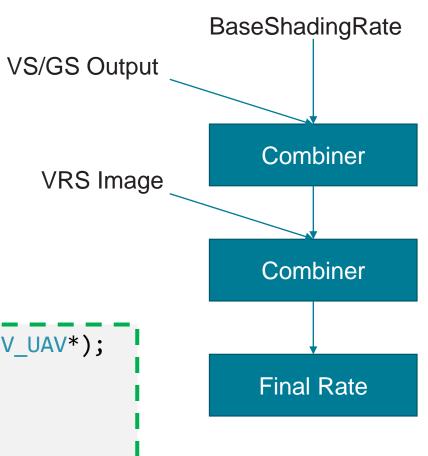
IMPLEMENTING VRS (INITIALIZATION)

- Query Hardware details:
 - Is VRS supported / which shading rates?
 - Supporting 4x4 shading rate makes the image generation shader more complex
 - 4x4 is likely to cause visible quality degradation at common resolutions
 - Is tier 2 (Shader or Image Based VRS) supported?
 - For image based: What is the tile size?
- Create VRS Image & generation shader



IMPLEMENTING VRS (RENDERING)

- Compute VRS image
- Bind VRS image
- Set base shading rate and combiners
- Unbind VRS image when done
- [Render VRS image as overlay for debugging]





FIDELITYFX VARIABLE SHADING (CPP)

```
Istruct FFX VariableShading CB
        uint32 t width, height;
        uint32_t tileSize;
        float varianceCutoff;
        float motionFactor;
static void FFX VariableShading GetVrsImageResourceDesc(
        const uint32_t rtWidth, const uint32_t rtHeight,
        const uint32 t tileSize,
        CD3DX12 RESOURCE DESC& VRSImageDesc);
 static void FFX VariableShading GetDispatchInfo(
        const FFX_Variable_Shading_CB* cb,
        const bool useAditionalShadingRates,
        uint32 t& numThreadGroupsX, uint32 t& numThreadGroupsY)
```



FIDELITYFX VARIABLE SHADING (HLSL)

```
// Define: FFX VARIABLESHADING TILESIZE
// Optional: FFX_VARIABLESHADING_ADDITIONALSHADINGRATES
// Constant Buffer
cbuffer FFX_VariableShading_CB0 {
        int2      g Resolution;
        uint g_TileSize;
        float g_VarianceCutoff;
        float g_MotionFactor;
 // Forward declaration of functions that need to be implemented
 // by shader code using this technique
float FFX_VariableShading_ReadLuminance(int2 pos);
float2 FFX VariableShading ReadMotionVec2D(int2 pos);
       FFX_VariableShading_WriteVrsImage (int2 pos, uint value);
void
```



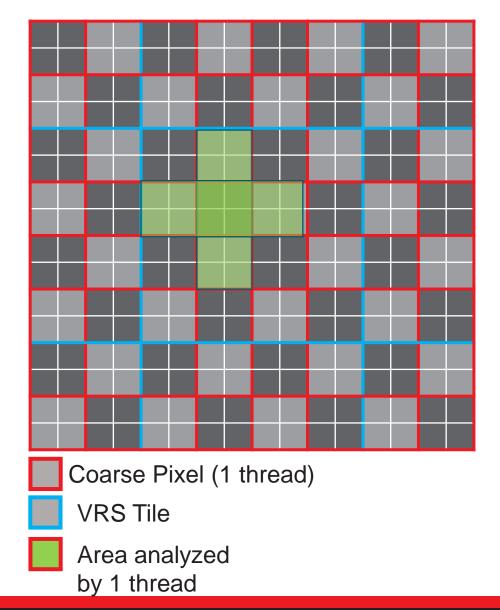
FIDELITYFX VARIABLE SHADING (HLSL USAGE)

```
// define FFX_VARIABLESHADING_TILESIZE on compile!
// may define FFX_VARIABLESHADING_ADDITIONALSHADINGRATES
RWTexture2D<uint> imgDestination: register(u0);
                  texColor : register(t0);
Texture2D
                  texVelocity : register(t1);
Texture2D
#define FFX HLSL 1
#include "ffx_variable_shading.h"
float FFX_VariableShading_ReadLuminance(int2 pos) {
       float3 color = texColor[pos].xyz;
       return dot(color, float3(0.30, 0.59, 0.11));
float2 FFX_VariableShading_ReadMotionVec2D(int2 pos) {
       return texVelocity[pos].xy * float2(0.5f, -0.5f) * g_Resolution;
```



HOW THE SHADER WORKS

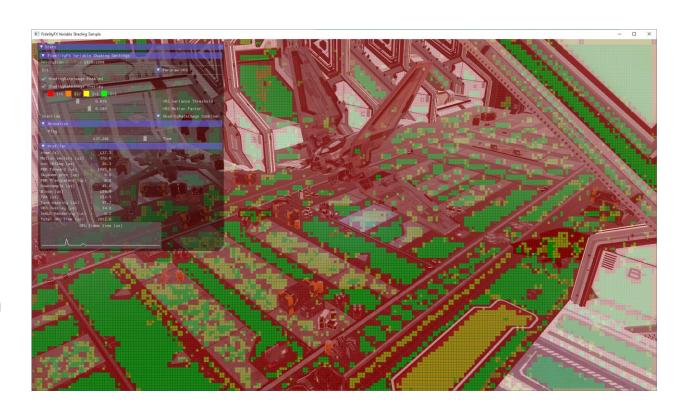
- 1. One threadgroup computes between 1 and 4 tiles
 - Without additional shading rates, and 8x8 tile size, each group of 8x8 threads computes the shading rate for 4 tiles.
- 2. Analyze pairs of pixels within 2x2 region
 - Using LDS
 - Each thread also takes pixels outside the 2x2 box into account. This avoids burn-in (i.e. Low VRS rate because it was low in last frame)
 - Reduce luminance delta by motion influence
- Compute largest luminance delta within tile
 - 1. Using wave intrinsics
- Compare against threshold
- 5. Write out VRSImage





VRS OVERLAY

- Display VRS image as overlay for debugging tweaking
- Ready to use code in VrsOverlay.hlsl
- Easy to integrate:
 - Build VS/PS pipeline and bind it
 - Provide constant buffer containing resolution and tile size
 - (same as for VRS image generation)
 - Draw a single triangle (No vertex or index buffers required)

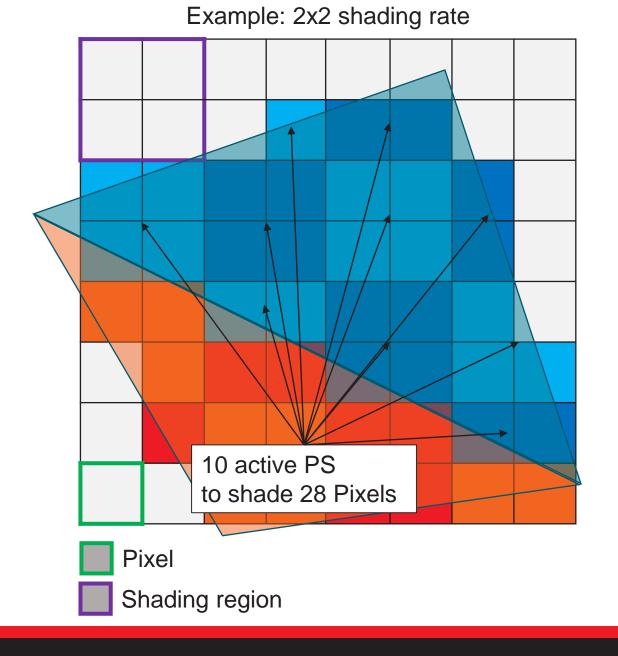






Since VRS works by reducing number of PS executions:

- No benefit in depth/stencil only passes
- No benefit in fill rate bound scenarios
- No benefit in compute passes
- Very little benefit if average triangle size is very small (think of quad utilization)





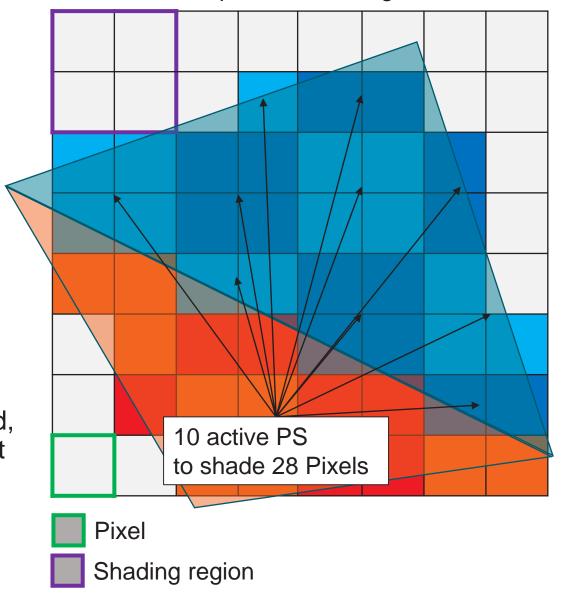


Features that cause shading rate to drop to 1x1

- Depth export
- Post-depth coverage
- Raster Order Views
- 16xMSAA

Minimize the number of times per frame the VRS image gets bound or unbound!

 If VRS needs to get disabled for a few draw calls while the same depth buffer is being used, (e.g. to render alpha-tested geometry) the best practice is to leave the VRS image bound and disable VRS by modifying the combiners.



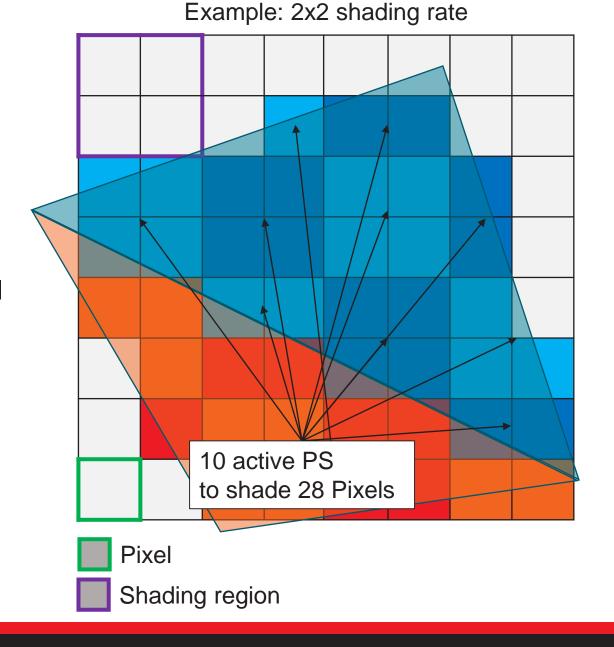
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Example: 2x2 shading rate



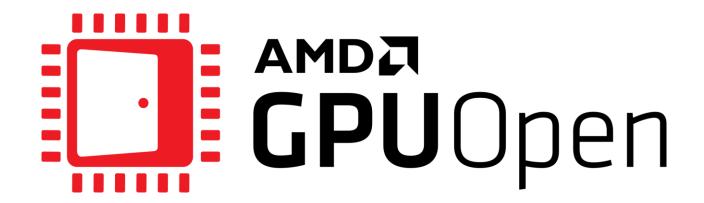
TAKEAWAY

- Easy to integrate
 - Free performance
- VRS preserves triangle edges
 - Also depth/stencil information
- Experiments show that 2x2 shading rate is ideal for commonly used resolutions





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