CS2022 Computer Architecture

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Project 2

MICROCODED INSTRUCTION SET PROCESSOR

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Description:

The second project will implement a Microprogrammed Instruction Set Processor. This builds on the VHDL model from the first project.

The following modifications are required:

- Increase the number of registers in the register-file from 8 to 9.
- This requires an additional select bit for the two multiplexers (Bus A and Bus B) and the destination decoder. These are separate signals (TD, TA, TB) from the Control Memory. See Figure 1. The size of the registers in the register-file is 16 bits.
- Consequently all components of the Datapath (e.g. MUXs in the register-file, decoder in the Register file, Arithmetic/logic Unit, Shifter and MUXs) are 16 bit operations.
- Add and test Memory M (512 x 16) and Control Memorll (256 x 28) to your project. MUX M will feed 16 bit addresses from ether the Bus A or the PC into the Memory M entity but only the 9 least significant address bits will be used to index into the array. This restricts the memory size to 512.
- Implement all the components shown in Figure 1 on page 3.
- Design reset logic for PC and CAR registers. This will enable you to start your program.
- Write microprogramms for the Control Memory that implement the following instructions:
    - ADI, LD, SR, INC, NOT, ADD, unconditional jump, and conditional branch (only one condition).

- Write machine code for the Memory M that demonstrates the use of the following instructions:
    - ADI, LD, SR, INC, NOT, ADD, unconditional jump, and conditional branch (only one condition).

Table 1: FS code definition

FS	MF Select	G Select	H Select	Micro-operation
00000	0	0000	00	$F = A$
00001	0	0001	00	$F = A + 1$
00010	0	0010	00	$F = A + B$
00011	0	0011	00	$F = A + B + 1$
00100	0	0100	01	$F = A + \bar{B}$
00101	0	0101	01	$F = A + \bar{B} + 1$
00110	0	0110	01	$F = A - 1$
00111	0	0111	01	$F = A$
01000	0	1000	00	$F = A \wedge B$
01010	0	1010	10	$F = A \vee B$
01100	0	1100	10	$F = A \oplus B$
01110	0	1110	10	$F = \bar{A}$
10000	1	0000	00	$F = B$
10100	1	0100	01	$F = srB$
11000	1	1000	10	$F = slB$

The Microprogmmmed Instruction Set Processor block diagram is shown in Figure 1 on page 3. Figure 1 is taken from Figure 8-26 in Mano and Kime [2]. Alternatively the drawing may be obtained from Prentice Hall's website [1].
The Functional Unit should have the functionality defined in the Table 1 on page 2.
Discuss your simulation results. The CS2022 lecture notes provide the necessary information to complete the project.

DUE: Friday, 12th April 2019

Please submit your VHDL-code and test-benches including all simulation results to Blackboard.

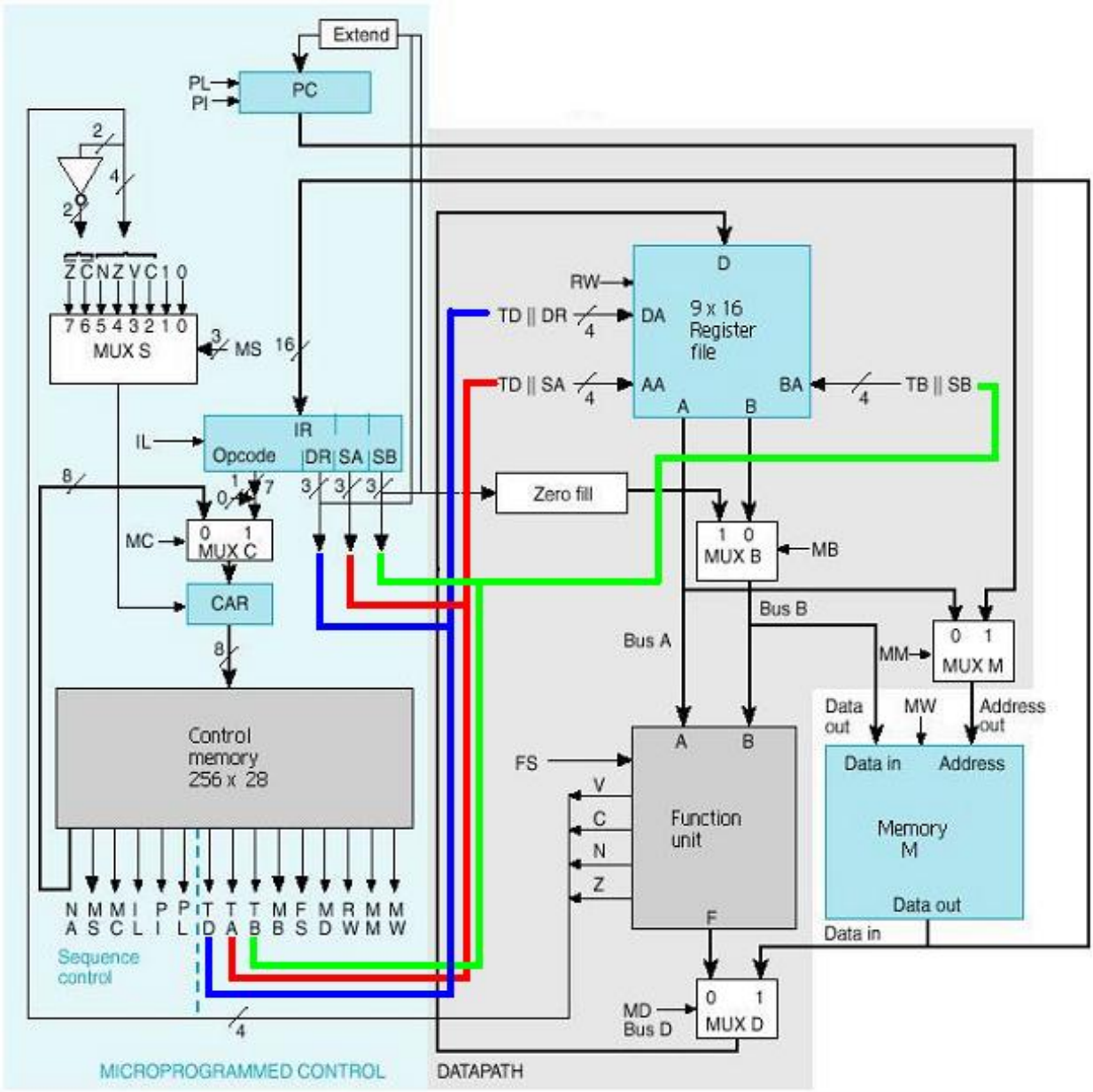

Figure 1: Multiple-Cycle Microprogrammed Control

References:

[1 J Morris Mano and Charles R. Kime. Logic and computer design fundamentals.

http://cwx.prerJralLcorn/bookbind/pubbook5/mano/chapter7/deluxe.html.

[2] M. Morris Mano and Charles R. Kime. Logic and Computer Design Fundamentals:

chapter 7. Prentice Hall, 2nd edition updated edition, 2001.