

CS2022 Computer Architecture

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Project 1 -Datapath Design -Part A

3 February 2019

Description:

The circuit overleaf implements a 4-bit version of the Register file section of the datapath shown in Mano and Kime figure 7-9 (or 4th lecture, page 12), by using components designed in VHDL and connected at the top-level through a schematic.

1. Design the VHDL components (Register, Decoder, and two Multiplexer 16 bit) and interconnect them to build a register file. The schematic shows only four registers. Your solution should implement eight registers.
2. You should provide test benches and simulations that prove the correctness of the following operations:
 - a. Correctly load an arbitrary HEX value into each of the eight registers, i.e. that it can execute the transfers $R_i \leftarrow X_i$ $i=0,7$
 - b. Correctly transfer the contents of any register to any other register, i.e. that it can execute the transfers $R_i \leftarrow R_j$, $i,j=0,7$

DUE: Friday, 15th February 2019

Please submit a copy of your VHDL-code and test-benches including all simulation results (screenshots) to Blackboard.

