CSU34021 Tutorial 5

Q1. The TCD2019 [a 32 bit hypothetical microprocessor] has a MMU that supports a 3 level page table in either 7-7-6-12 or 7-7-5-13 configurations. The MMU contains a KRP (kernel root pointer) and a URP (user root pointer) which point to the root of the kernel and user page tables respectively.

(i) What page sizes are supported by the MMU?

(ii) What are the sizes of the various page tables in the hierarchy (both options)?

(iii) Outline the structure and size of the kernel page table assuming that the kernel's virtual address space [starting at address 0x00000000] is mapped directly onto 16MB of physical memory starting at address physical 0x01000000 [assume a 4Kbyte page size].

(iv) A user process is started which has a code/text size of 0x5fe0 bytes, an initialised data size of 0x6ac bytes, an uninitialised data [bss] size of 0x2888 bytes and 642 bytes of stack data copied from its parent. Outline the structure and size of its initial user page table [assume a 4Kbyte page size].

(v) Given that the TCD2019 processor accesses the following virtual memory addresses when executing the user process outline in (iv) above [U = user address, S = supervisor address], indicate the memory area being accessed and the changes that would be made to the initial page table structure when handling any page faults.

```
U     0x00001000
U     0x00001004
U     0x00001008
U     0x00002000
U     0x00008000
S     0x00001000
U     0x00007000
S     0x00002000
U     0xFFFFE000
U     0xFFFFD000
S     0x00FFE000
S     0x00FFC000
U     0x00002000
U     0x00100000
U     0x00002000
U     0x00009000
```

(v) The TCD2019's MMU has an integral 8 entry fully associative TLB. Outline the organisation of the TLB and explain how kernel and user virtual to physical mappings can share the TLB. Given the above sequence of memory accesses, calculate the TLB hit rate and the resulting contents of the TLB [assume LRU replacement].