

CSU34021 Tutorial 6

Q1. Compute the number of hits and misses if the following list of hexadecimal addresses is applied to caches with the following organisations.

- (i) 128 byte 1-way cache with 16 bytes per line (direct mapped)
- (ii) 128 byte 2-way set associative cache with 16 bytes per line
- (iii) 128 byte 4-way set associative cache with 16 bytes per line
- (iv) 128 byte 8-way associative cache with 16 bytes per line (fully associative)

0000 \Rightarrow 0004 \Rightarrow 000c \Rightarrow 2200 \Rightarrow 00d0 \Rightarrow 00e0 \Rightarrow 1130 \Rightarrow 0028 \Rightarrow
 113c \Rightarrow 2204 \Rightarrow 0010 \Rightarrow 0020 \Rightarrow 0004 \Rightarrow 0040 \Rightarrow 2208 \Rightarrow 0008 \Rightarrow
 00a0 \Rightarrow 0004 \Rightarrow 1104 \Rightarrow 0028 \Rightarrow 000c \Rightarrow 0084 \Rightarrow 000c \Rightarrow 3390 \Rightarrow
 00b0 \Rightarrow 1100 \Rightarrow 0028 \Rightarrow 0064 \Rightarrow 0070 \Rightarrow 00d0 \Rightarrow 0008 \Rightarrow 3394 \Rightarrow

Assume that the first 4 bits of the address is used as the offset within the cache line, the next $\log_2(N)$ bits select the set and the remaining bits form the tag. Furthermore, assume that the all cache lines are initially invalid and that a LRU replacement policy is used.

Q2. Write a program (in C, C++, Java, ...) to solve Q1 (should be less than 200 lines of code). Make sure you can create a generalised cache object with parameters L, K and N.

Please submit your answer to Q2 via Blackboard. It should include the source code and a .pdf document containing evidence that your program generates the correct results.

128 byte 1-way cache with 16 bytes per line (L = 16, N = 8, K=1)

<u>tag</u>	<u>4 word (16bytes)</u>			

Address Format

15																0
----	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	---

<u>address</u>	<u>set</u>	<u>hit/miss</u>
0000		
0004		
000c		
2200		
00d0		
00e0		
1130		
0028		
113c		
2204		
0010		
0020		
0004		
0040		
2208		
0008		
00a0		
0004		
1104		
0028		
000c		
0084		
000c		
3390		
00b0		
1100		
0028		
0064		
0070		
00d0		
0008		
3394		

128 byte 2-way cache with 16 bytes per line (L = 16, N = 4, K=2)

<u>tag (K=0)</u>	<u>tag(K=1)</u>	<u>4 word (16bytes)</u>				<u>4 word (16bytes)</u>			

Address Format

15																0
----	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	---

<u>address</u>	<u>set</u>	<u>hit/miss</u>
0000		
0004		
000c		
2200		
00d0		
00e0		
1130		
0028		
113c		
2204		
0010		
0020		
0004		
0040		
2208		
0008		
00a0		
0004		
1104		
0028		
000c		
0084		
000c		
3390		
00b0		
1100		
0028		
0064		
0070		
00d0		
0008		
3394		