Analog Circuits
Mini Project-2

Sahukari Chaitanya Varun
EE19BTECH11040

Designing Amplifier

October 19, 2021

In this mini-project we design an amplifier with the following specifications :

- Gain : 20 dB i.e, $|\frac{V_o}{V_{in}}| = 10$
- Source Resistance(R_s) : 1kΩ
- Load Resistance(R_L) : 50Ω
- Frequency : 1kHz
- Voltage Supply : 1.1V and Current Source : 10μA ; with maximum swing.

We will use the previously extracted square-model values of long channel NMOS (W=1μm,L=1μm) where:

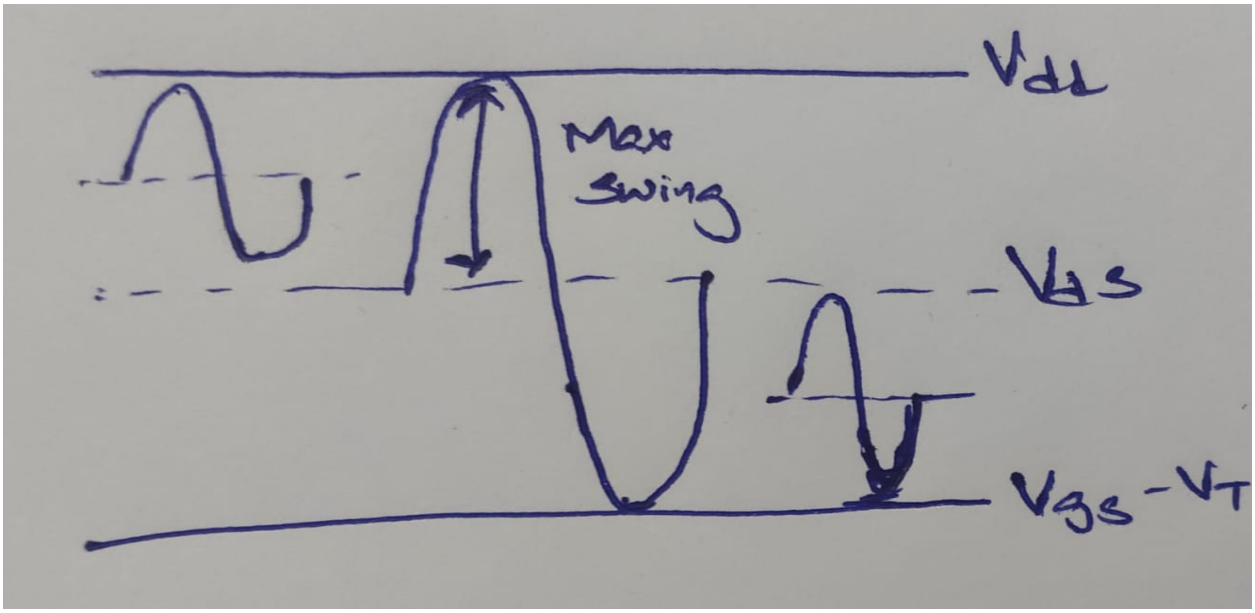
- $V_{gs0} = 577.7093$mV
- $g_{m0} = 12.637\ \mu\mho$
- $V_T = 315.12$mV
- $\beta = 481.246\ \mu\mho\ V^{-1}$
- $I_{ds} = 1.710\mu$A

- $g_{ds0} = 669.2744\mu\mho$
- $\lambda = 0.4033\ V^{-1}$
- Range of V_{gs} for g_m with in 50% error : (485.946mV,656.186mV)

We can see $g_m R_L$ is not high enough to have such a high gain, hence we use a voltage biased common source amplifier and cascade to get high enough gain which when given to the final current biased common source amplifier, gives the required gain across the load.

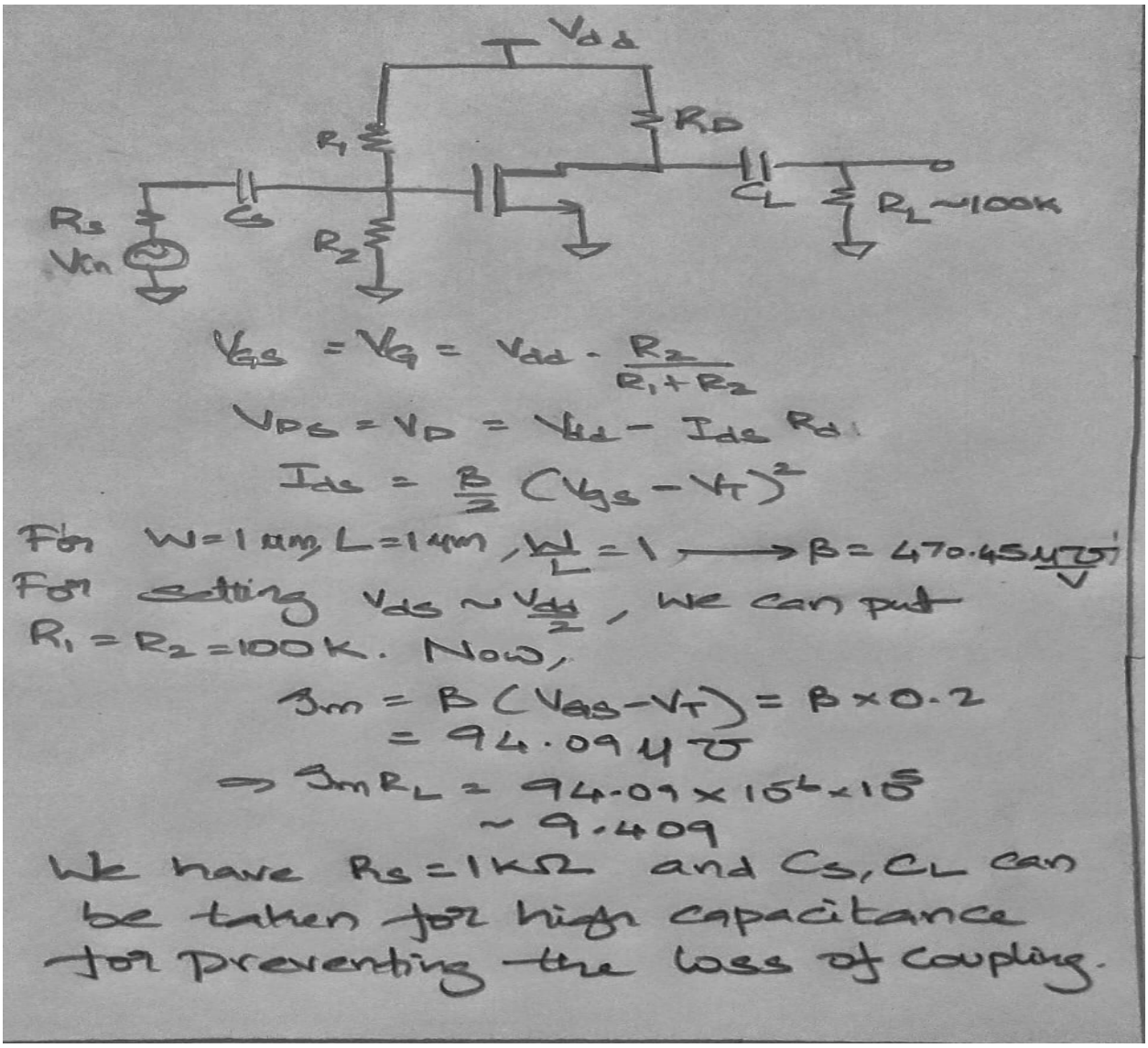
1 Hand Calculation

First we need to observe to maximize the swing in the output, the corresponding V_{ds} has to be such that even at its least, has to ensure saturation and its highest should ensure not to enter cutoff. For a symmetric swing V_{ds} has to be maintained in the middle of V_{dd} and $V_{gs} - V_t$, which nearly comes out to be around 0.55V to 0.6V (error in calculation of gate and threshold voltages) as shown.

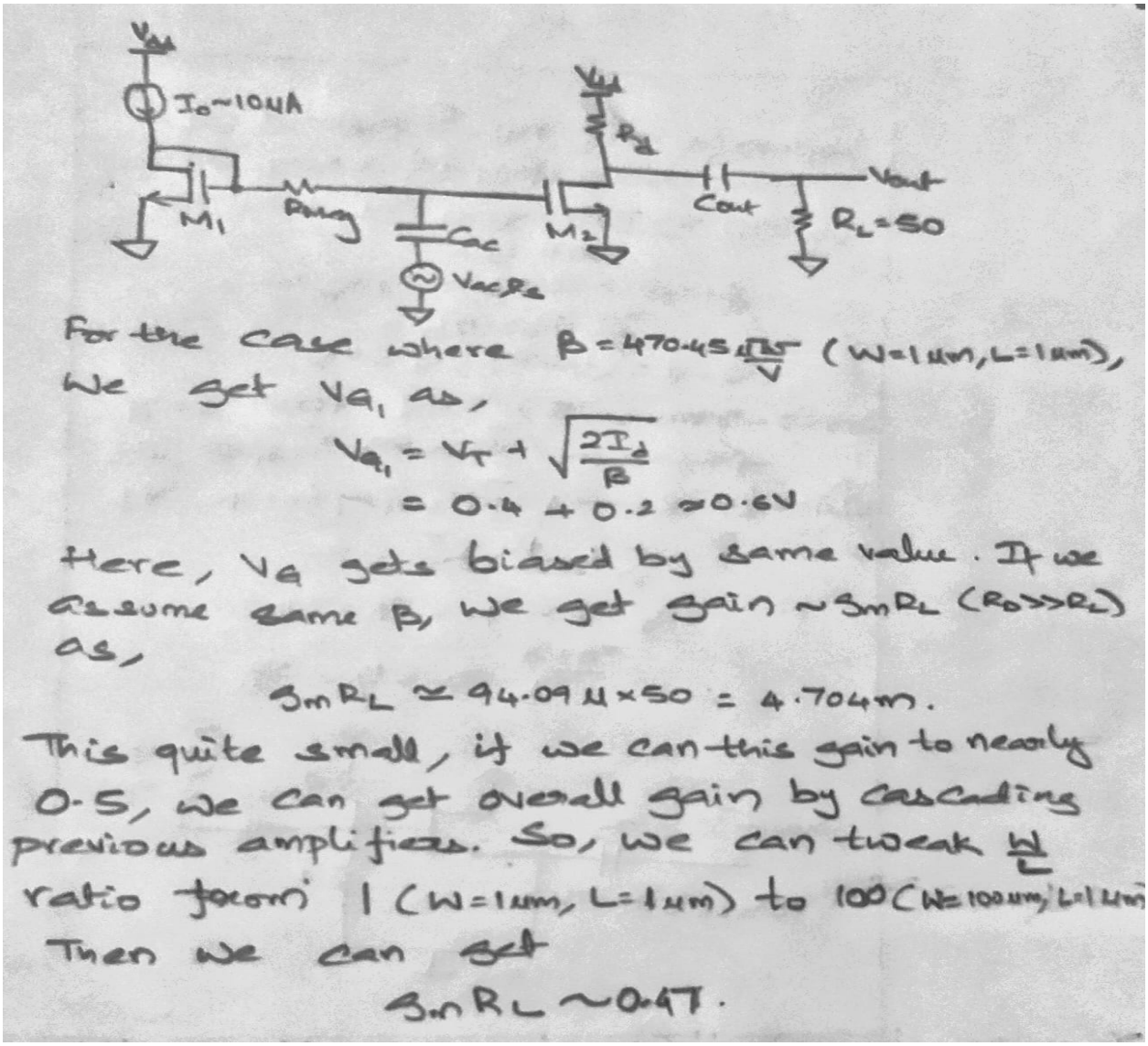


We can thereby adjust V_{gs} to control I_{ds}.

Now we have two kind of circuit blocks, one for amplifying the signal and one to appropriately merge the load to meet the required specification. Firstly, amplifying block : We get $I_{ds} = 9.4\mu$A, $R_d = 63.82\omega$. This nearly



gives us the almost required gain. But when we connect to the low load, the gain drops, hence, we need to cascade to higher gain to get the desired gain. To prevent any kind of coupling loss, we can assume them to be in order 1μH - 10μH. The R_L is taken high to get high gain value. Here V_{ds} is maintained near to half of the supply, i.e, 0.55V to maximize the swing.



For combining the load, we can use the above calculated current biased common source amplifier. Here the gain is nearly 0.5 times the input. Here, Ids is mirrored by 100, and for maintaining V_{ds} near to $V_{dd}/2$, $R_d = 0.55\text{K}\Omega$. The capacitance's can be chosen to be high enough (1μH - 10μH) to prevent any kind of coupling losses.The R_{high} is kept to ensure the effective g_m undisturbed.

By cascading nearly two amplifiers with this load driven amplifier should maintain the effective gain to be around 10, with the assumption of proper coupling of the cascades.

2 Schematic Circuit

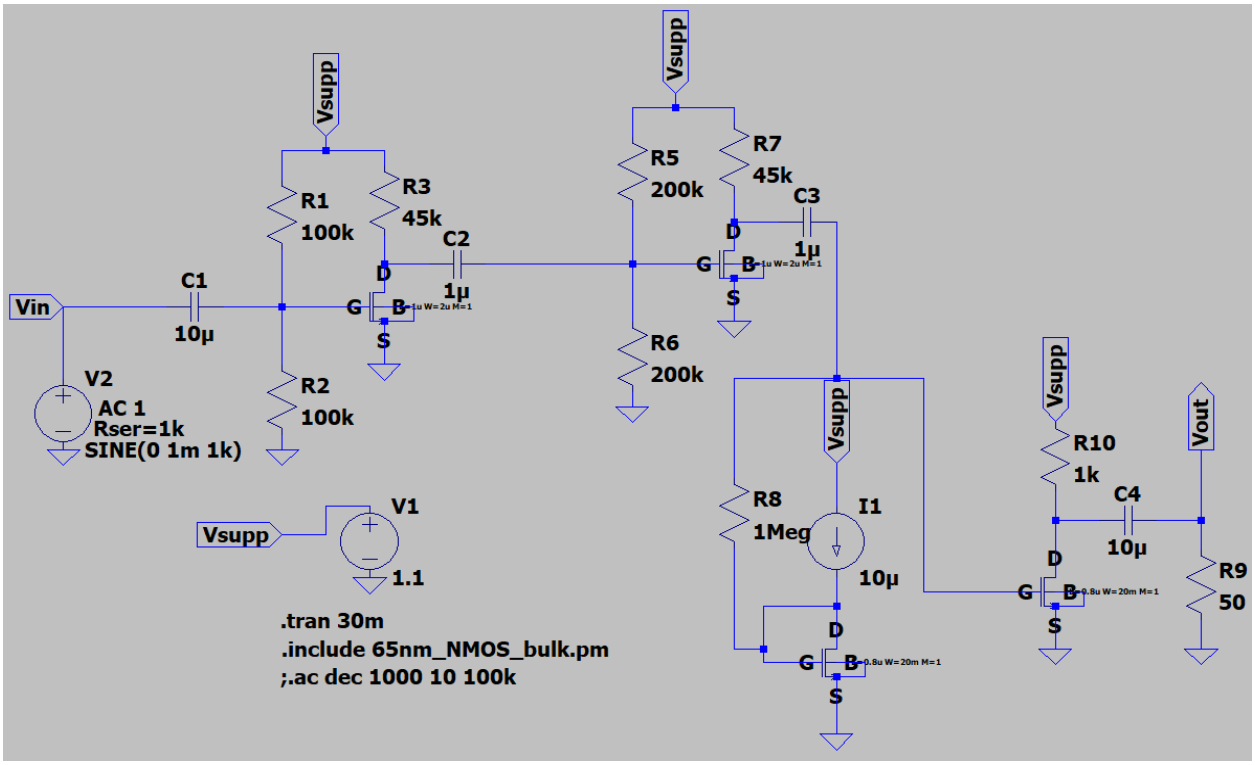


Figure 1: Circuit used for simulation

The final elements are as shown above :

- The amplifiers with larger gain have W = 2μm and L = 1μm and the smaller gain have W = 20mm and L = 0.8μm.
- The Rd for higher gain is chosen to be 45kΩ and for smaller gain to be 1kΩ.
- The biasing resistances are treated to be same 100kΩ. The capacitance's are also taken as per the hand calculation.
- The individual gains are slightly different than the expected gains, due to change in the intrinsic parameters.

The Outputs are shown below :

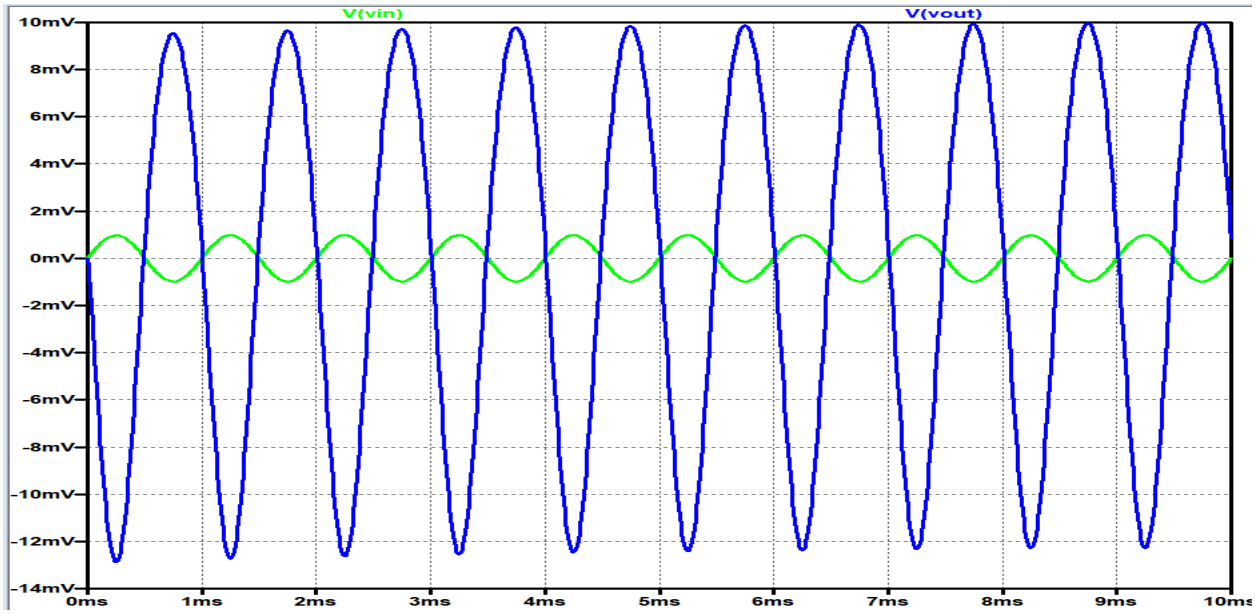


Figure 2: Output for 1mV sinusoidal input

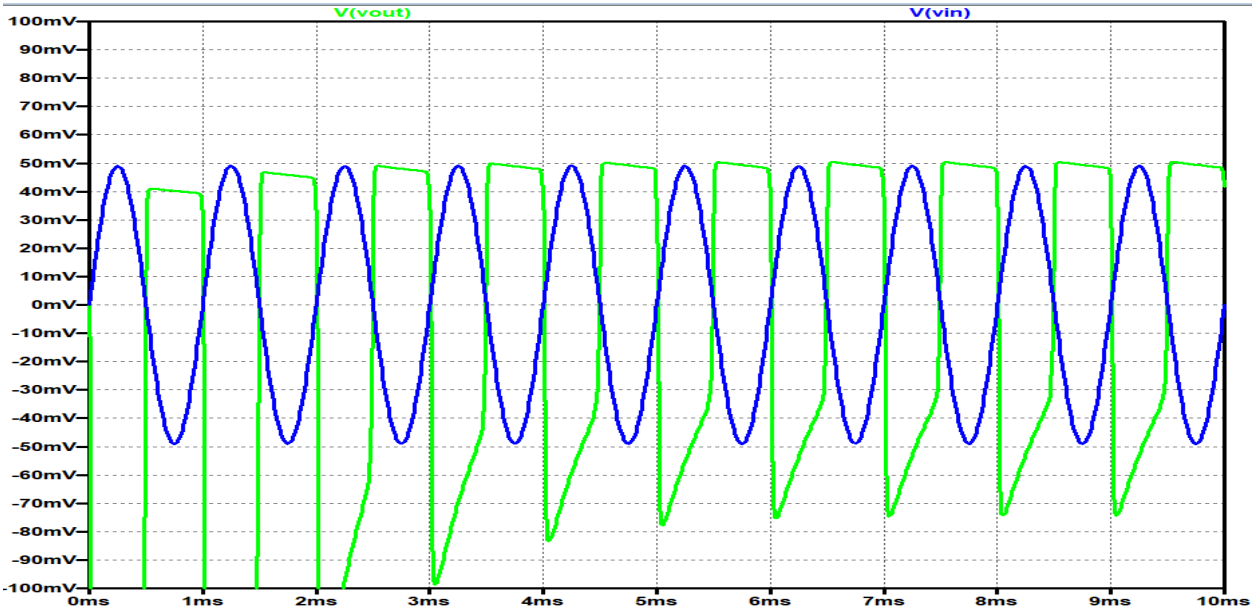


Figure 3: Output for 50mV sinusoidal input

1. Case-1 : The output is amplified and inverted. The initial transient slightly stretches downwards, giving an overall required gain of 10.

2. Case-2 : The output is amplified but also clipped at the top indicating cut-off and the bottom is telling the reaching of triode region. As both cut-off and triode region are visible, the range of amplification is beyond range of operation.

3 Total Harmonic Distortion

It is a measurement for commenting how linear is the system, calculated as

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + ... + V_n^2}}{V_1}$$

where V_k is the rms value of k^{th} harmonic.

3.1 Input Amplitude : 1mV

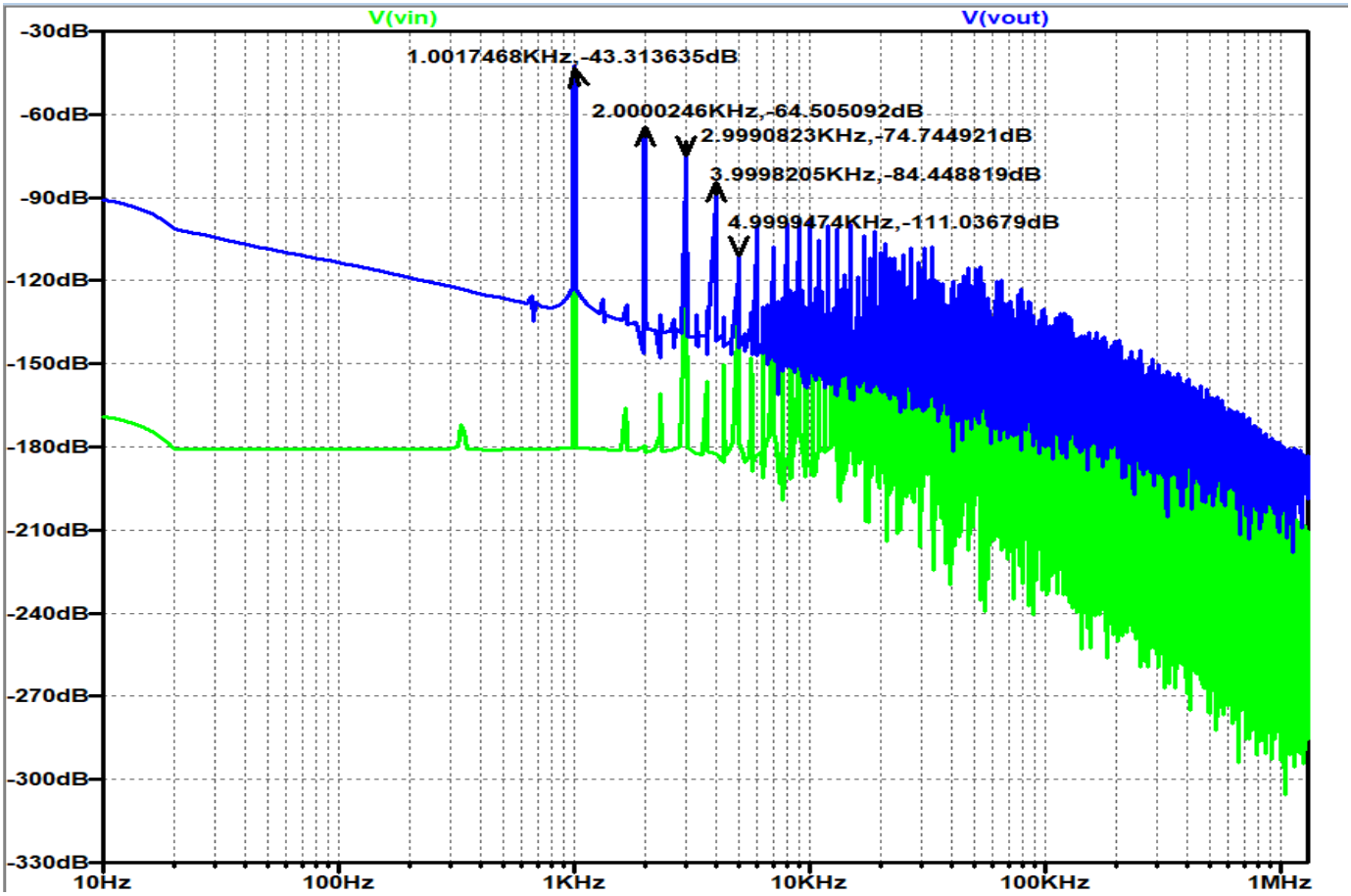


Figure 4: FFT Plot

Calculated THD value = 0.09163577728870441

As the amount of signal in the harmonics is quite low, the system can be said to be very linear for the given input.

3.2 Input Amplitude : 50mV

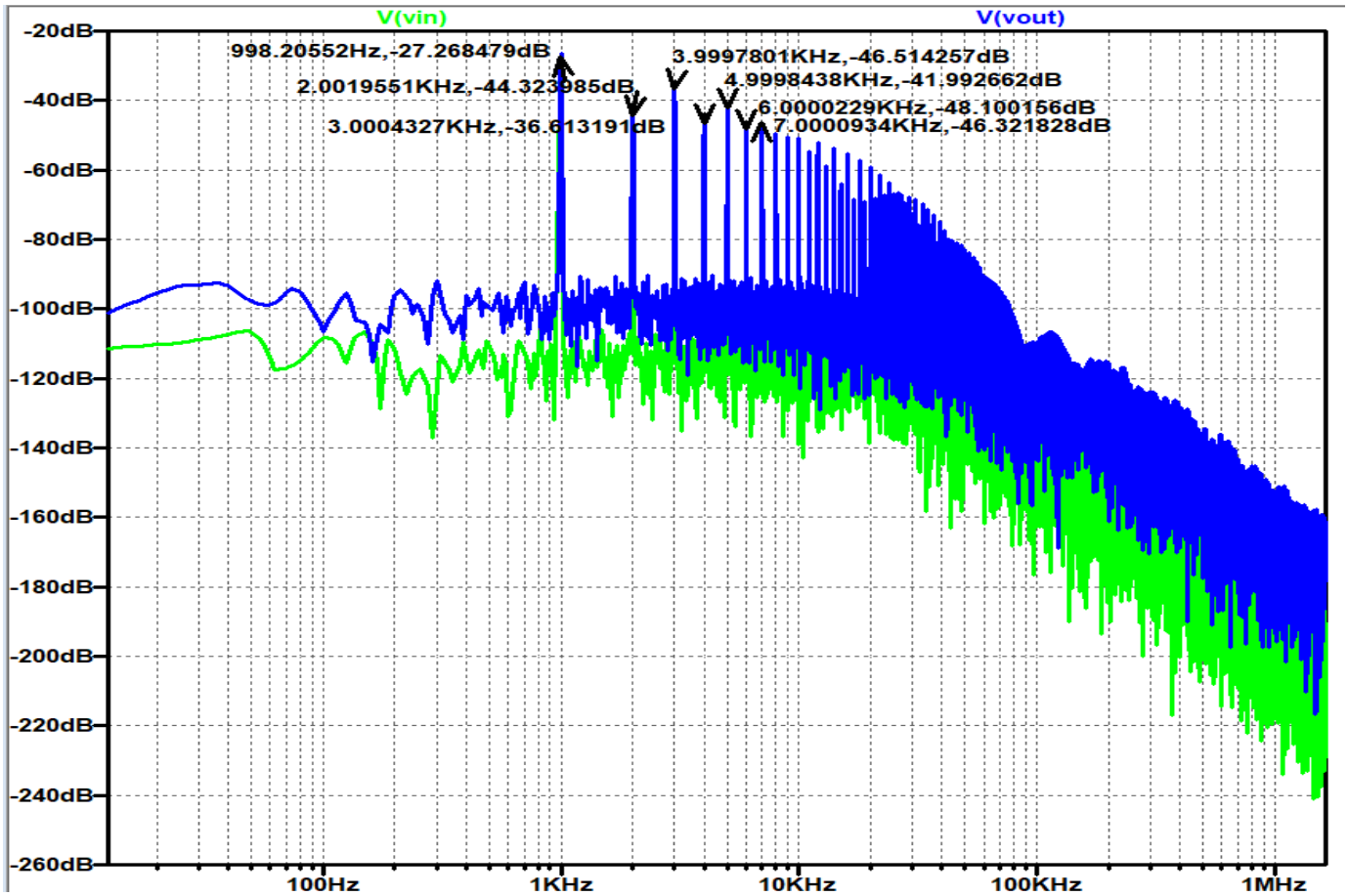


Figure 5: FFT Plot

Calculated THD value = 0.4497456929284516

As the amount of signal in the harmonics is quite significant, the system cant be said to be linear for the given input. This results because of the clipping of the signal.

Note : The code for calculating THD is attached separately. For data-points, we take the harmonics(in dB) as [-27.268479,-44.323985,-36.613191,-46.514257,-41.992662,-48.100156,-46.321828] for 50mV and [-43.313635,-64.505092,-74.744921,-84.448819,-111.03679] for 1mV.

4 AC Analysis

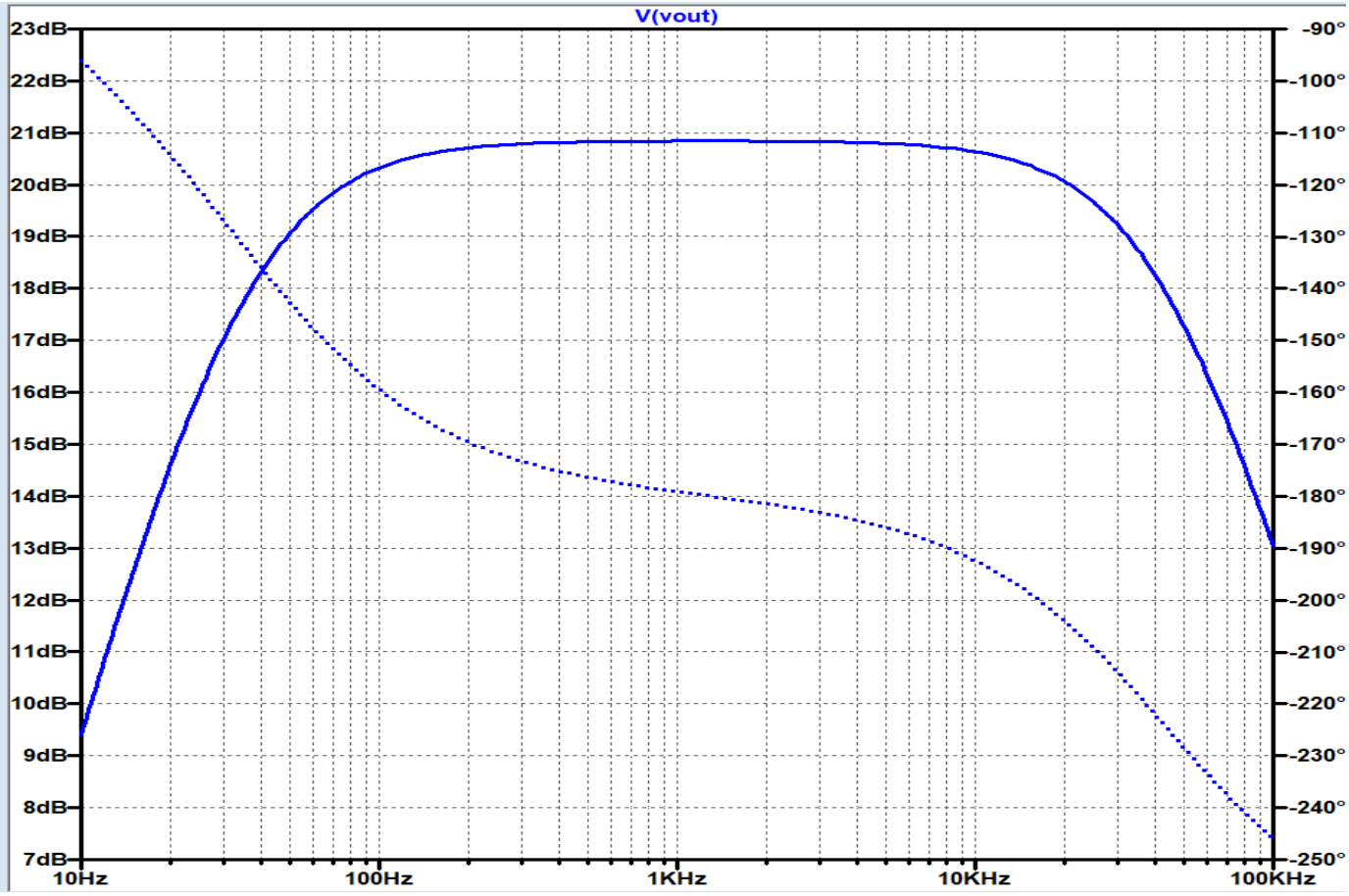


Figure 6: AC analysis

The circuit acts like a bandpass filter, with pass band nearly being from 100Hz - 30kHz, with filter gain being nearly 21dB (slightly higher than 20dB which might be because of the non linear behaviour of the approximated MOSFET model).

5 DC Power consumed by the Amplifier

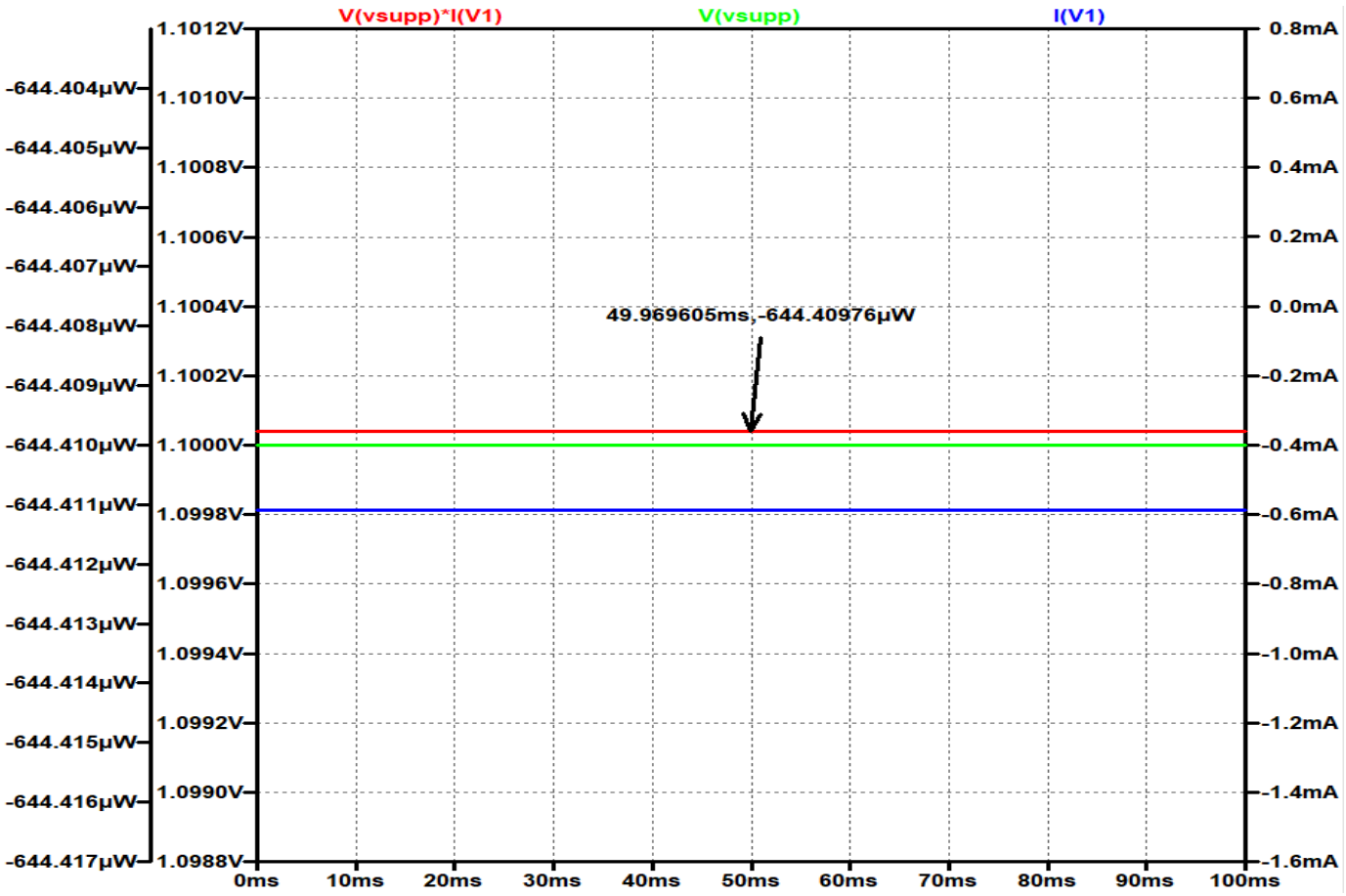


Figure 7: DC Power Consumption

Here we get the net current flowing through the supply is nearly 0.6mA and with the voltage remaining at 1.1V, we nearly get the average DC power to be 644.41mW.

For extracting this value, we remove the input AC signal to prevent any kind of AC losses corrupting the DC power.