Analog Circuits
Mini Project-2

Sahukari Chaitanya Varun
EE19BTECH11040

Designing 2 stage Op-amp

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1 Design of Op-amp

In this mini-project we design an amplifier with the following specifications :

- Supply Voltage : 1.1V
- Input common-mode voltage : 0.55V
- Load Capacitance : 10pF
- Unity Gain Bandwidth : 10MHz
- Phase-Margin : 60 degrees
- DC gain $>$ 40dB
- Slew Rate $>$ 10 V/μs

We will use the previously extracted square-model values of long channel NMOS (W=1μm,L=1μm) and PMOS(W=1μm,L=1μm). The hand calculations are as follows :

1.1 Hand Calculation

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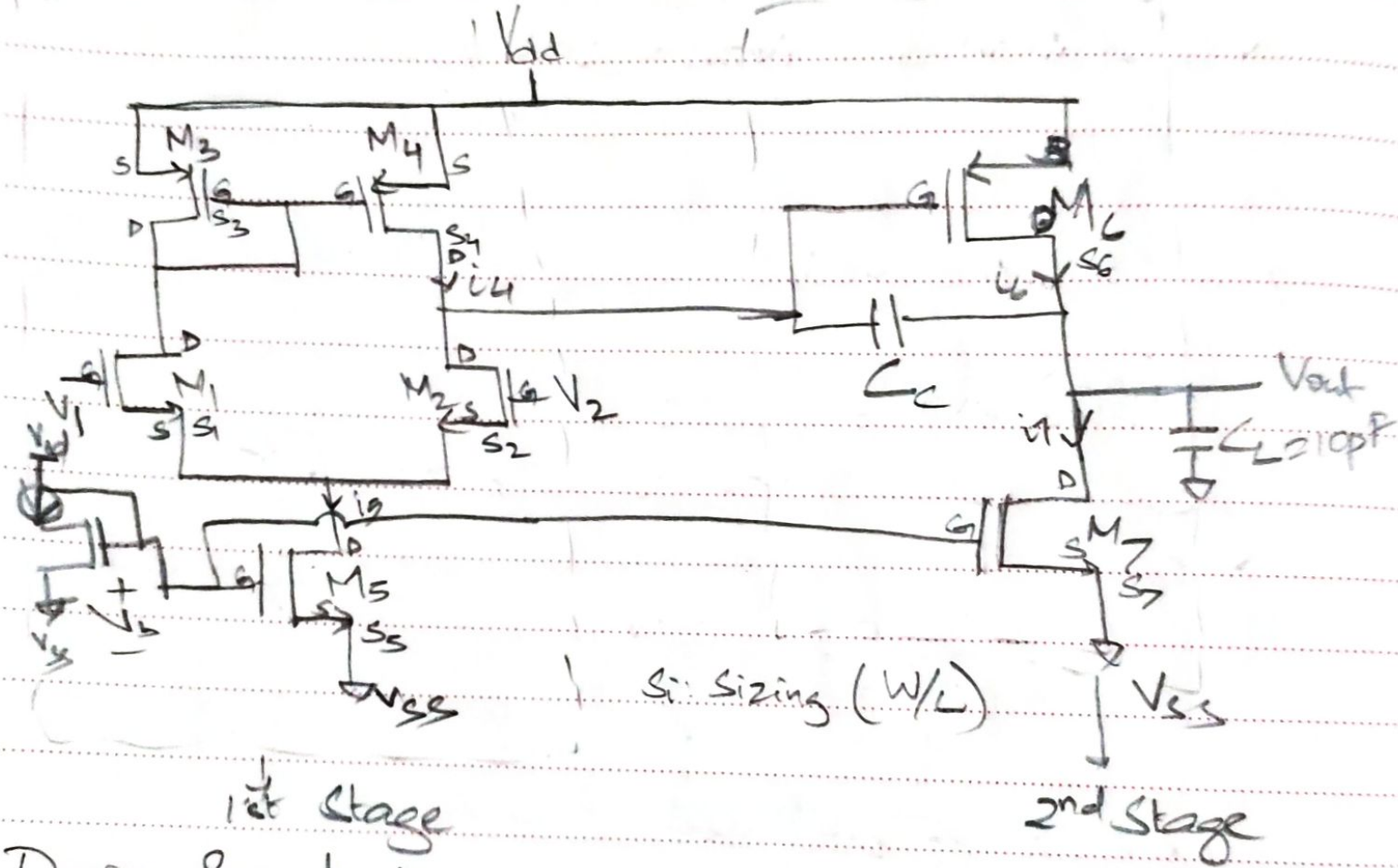
Design: 2-Stage Opamp (Miller Compensated)



Design Specifications:

- Supply Voltage (V_{dd}) = 1.1V
- Input Common Mode Voltage = 0.55V (ICMR)
- Load Capacitance : 10pF
- Unity Gain Bandwidth: 10MHz
- Phase Margin : 60°
- DC gain(A_v) > 40 dB
- Slew Rate > 10V/μs (SR)

From previous experiments, we obtain

$K_N' = 470.45\ \mu A/V^2$ (Long channel : $(W,L) = (1\ \mu m, 1\ \mu m)$)
$K_P' = 481.26\ \mu A/V^2$ (" " " " " ")
$V_{TN} = 0.4V$ $\quad |V_{Tp}| = 0.31V$
$\lambda_N = 0.036V^{-1}$ $\quad \lambda_P = 0.04V^{-1}$

Assume Channel length $L = 1\mu m$, $C_L = 10pF$

Minimum Value of miller cap :

$C_c > 0.22 C_L$ for zero $Z > 10 \times UGB$ (UGB = 10MHz)

$\Rightarrow C_c > 0.22 \times 10pF$

$\Rightarrow \boxed{C_c > 2.2pF}$, let $\boxed{C_c = 3pF}$

From slew rate specification, min tail current is given by

$$I_5 = (SR) \times C_c = 10 \times 10^6 \times 3pF$$
$$= 30\mu A$$

For finding $\left(\frac{W}{L}\right)_3$ using ICMR specs, we get

$$\left(\frac{W}{L}\right)_3 = \frac{I_5}{K_3' [V_{DD} - V_{ICMR} - |V_{T_3}| + V_{T_1}]^2} = \frac{30 \times 10^{-6}}{481.26 \times 10^{-6} [1.1 - 0.55 - 0.31 + 0.4]^2}$$

$$= \frac{30}{481.26 \times (0.64)^2} \simeq 0.152$$

↳ for good results consider $(W/L)_3 = 10$.

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 10$$ (For good mirroring)

Assuming the unity gain bandwidth is established by the dominant node, we have

$$g_{m_1} = UGB \times C_c = 10\times10^6 \times 2\pi \times 3\times10^{-12} = 188.5\,\mu S = g_{m_1}$$

Now $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m_1}^2}{2\times K_N' \times I_5} = \frac{(188.5\times10^{-6})^2}{2\times 470.45\times10^{-6}\times 30\times10^{-6}}$

$= 2.517 \approx 3$

$\Rightarrow S_1 = S_2 = 3$

Next, $V_{DS_5} = 0.2\ V$ (From earlier experiment)

And, chosen $V_{DS} = -V_{dd}$

Choose $V_{SS} = -V_{dd}$

Then $\left(\frac{W}{L}\right)_5 = \frac{2 I_5}{K_5' V_{DS}^2} = \frac{2\times(30\times10^{-6})}{470.45\times10^{-6}\times(0.2)^2}$

Same for M_8

$= 3.188 \rightarrow \left(\frac{W}{L}\right)_5$ can be taken to be 6

For 60° phase margin,

$P_2 = 2.2 \times UGB$

$= 2.2 \times 2\pi \times 70 \times 10^6$

$= 138.23 MHz$

$g_{m6} \geq 10\, g_{m1}$

$10 \times 188.5\mu S = 1885\mu S$

$g_{m1} = \sqrt{\frac{2 \times K_p' (\frac{W}{L})_3 \times I_5}{2}}$

$\Rightarrow \left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{g_{m1}} \left(\frac{W}{L}\right)_1 = \sqrt{2 \times 491.26 \times 10^{-6} \times 30 \times 30 \times 10^{-6}}$

$\Rightarrow = \frac{1885}{665} \times 30$

$= 85.0375$

$g_{m1} = 665\,\mu S$

Now, $i_6 = \frac{g_{m6}^2}{2K_p' (W/L)_6} = \frac{(1885 \times 10^{-6})^2}{2 \times 491.26 \times 10^{-6} \times 85.0375}$

$= 19.966 \times 20\,\mu A$

$P_{diss} = 2V_{dd}(I_5 + I_6)$

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$= 2 \times 1.1 \times 50\,\mu A = 110\,\mu W$

$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 \frac{I_6}{I_5} = 6^2 \times \frac{20}{30} = 4$

Then corresponding $A_V = \frac{2 g_{m1} g_{m6}}{I_5 (\lambda_2 + \lambda_4) I_6 (\lambda_6 + \lambda_7)}$

For obtained values, we get

$$A_V = \frac{2 \times 188.5\times10^{-6} \times 188.5\times10^{-6}}{30\times10^{-6} \times 20\times10^{-6} \times (0.016)^2}$$

$$\approx 2\times10^5$$

$\hookrightarrow$ 106 dB $\rightarrow$ So decrease $\left(\frac{W}{L}\right)_6$ to decrease the gain

1.2 Simulating the model

Based on the calculations, by putting it into the circuit and tweaking it for getting the required specifications, we get the circuit to be The corresponding

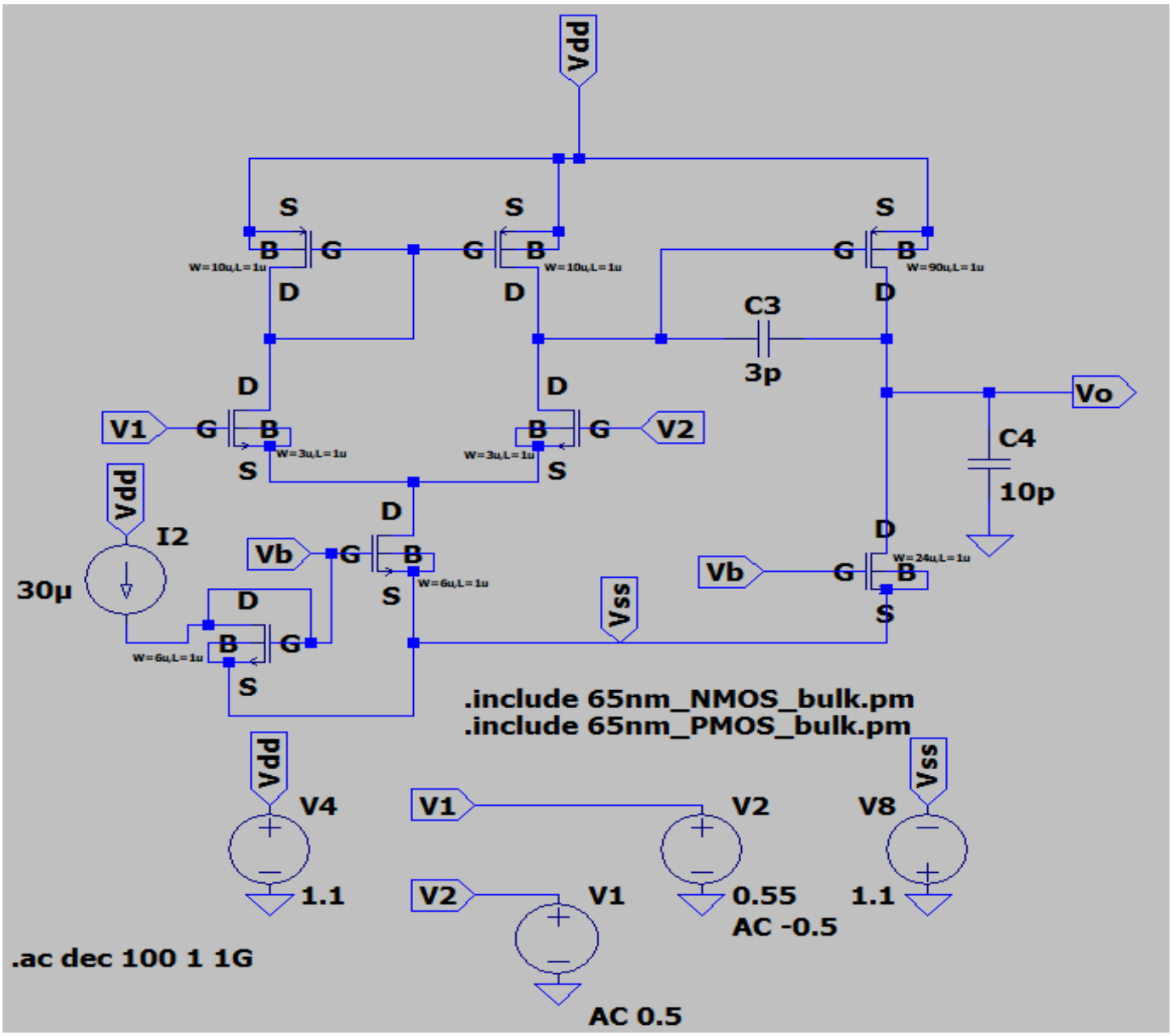

Figure 1: Op-amp Circuit diagram

bodeplot is as follows:

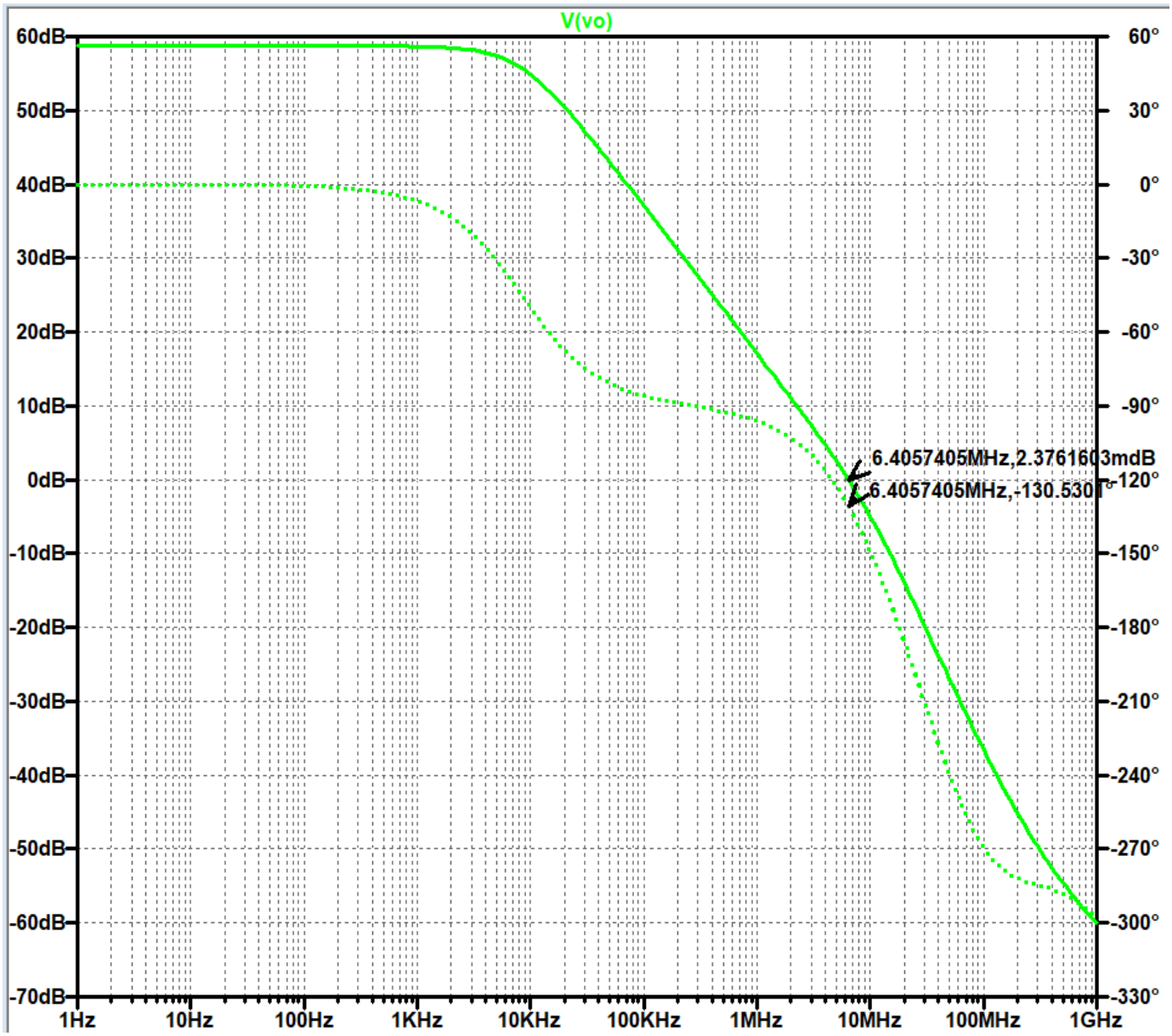

Figure 2: Op-amps resulting bodeplot

Here the, unity gain bandwidth is close to 10MHz(7MHz) with dc gain around 60dB($>$ 40dB). The sizes are kept near to the calculated values. The phase margin is slightly greater than expected 60^o (around 70^o).

1.3 Common-mode rejection ratio (CMRR)

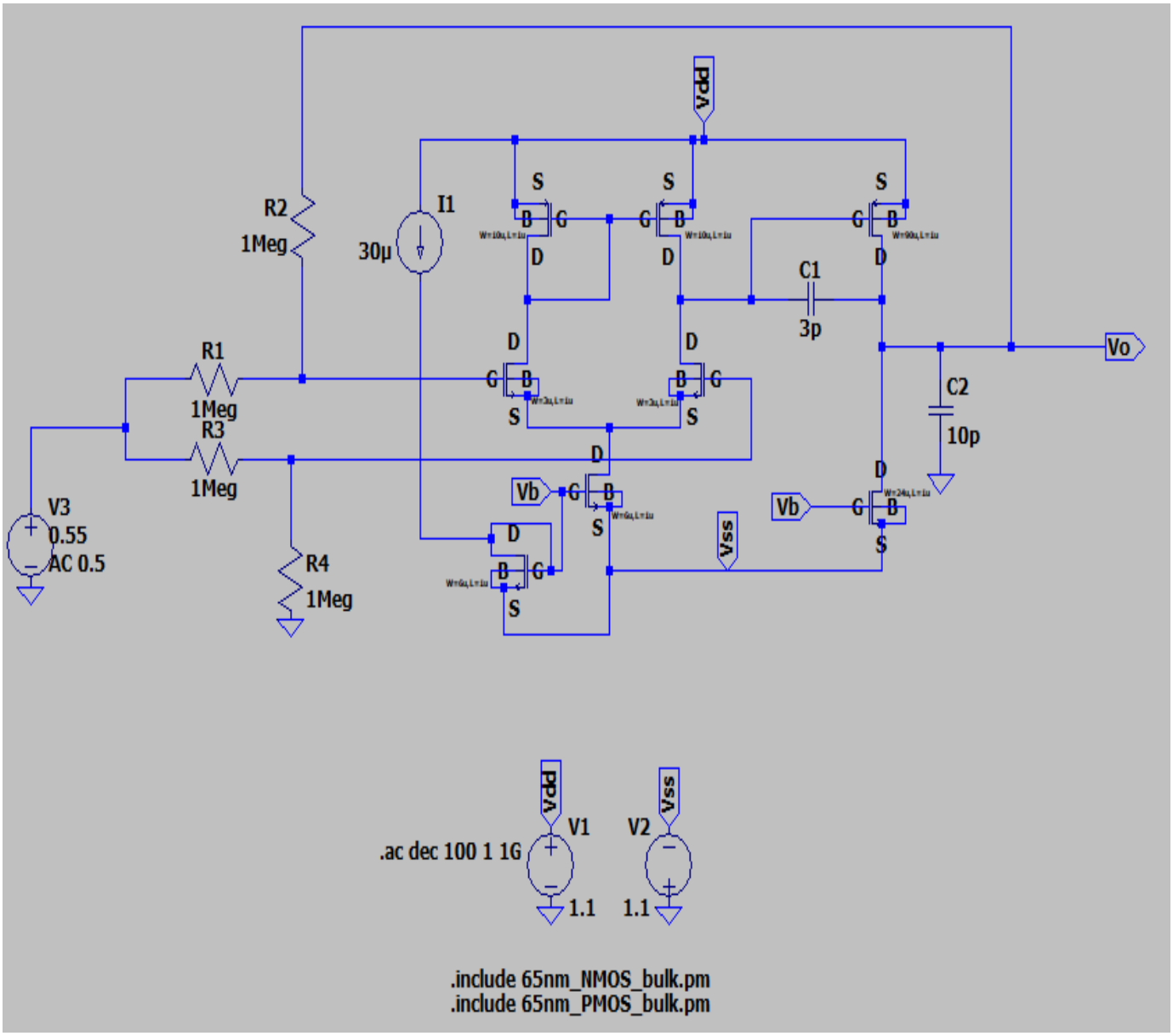

Figure 3: Circuit diagram for simulating CMRR

From the circuit, we can get the CMRR as:

$$CMRR = \frac{\Delta V_{in}}{\Delta V_{out}} \left(1 + \frac{R2}{R1}\right)$$

Here, we can make the equation corresponding to output variation inverse, by making R2=R1, and V_{in} to 0.5.

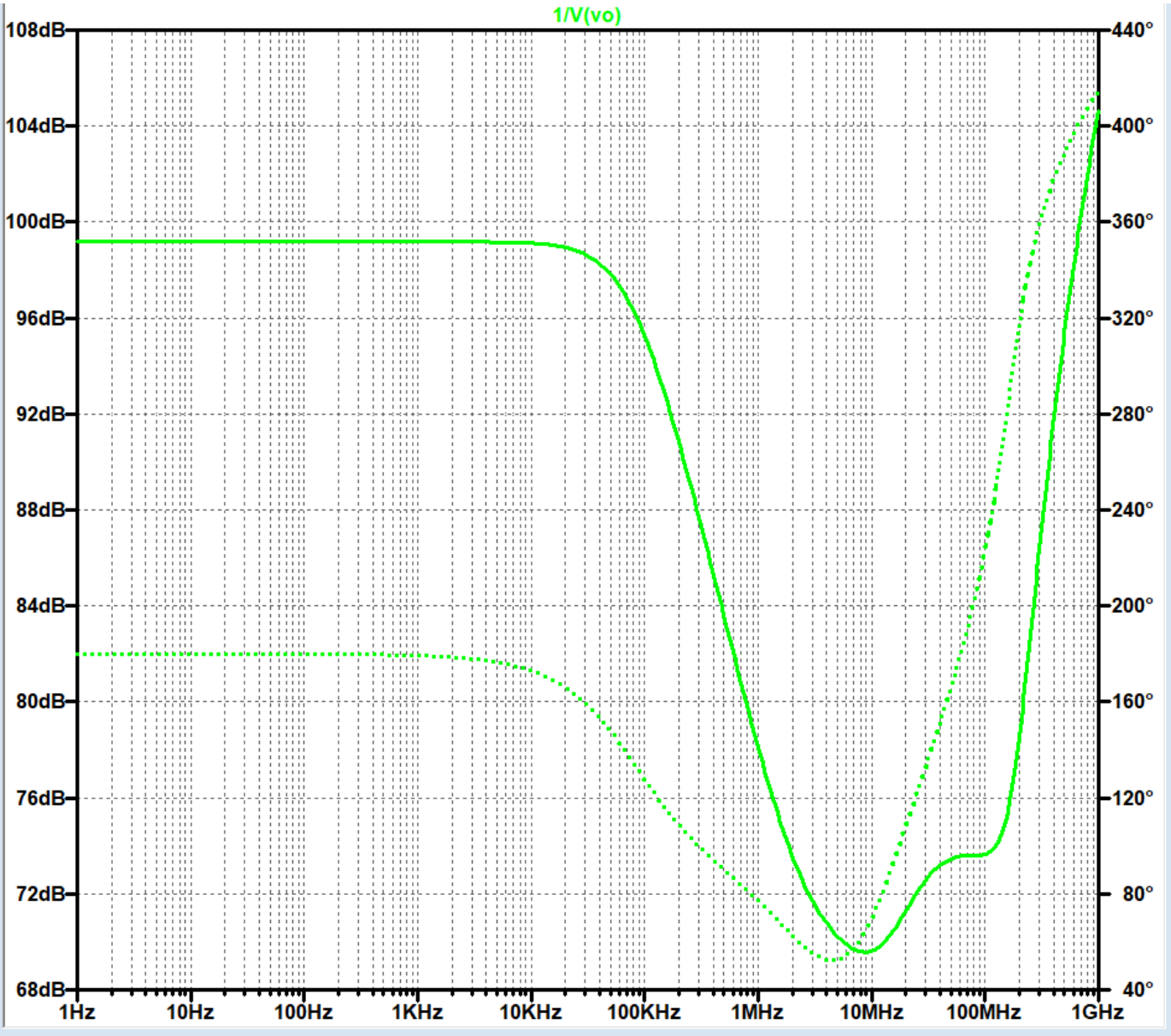

Figure 4: Op-amps resulting CMRR

We can see the CMRR to be large (in ranges of 100dB max), implying that $A_d >> A_{cm}$.

1.4 Power-supply rejection ratio (PSRR)

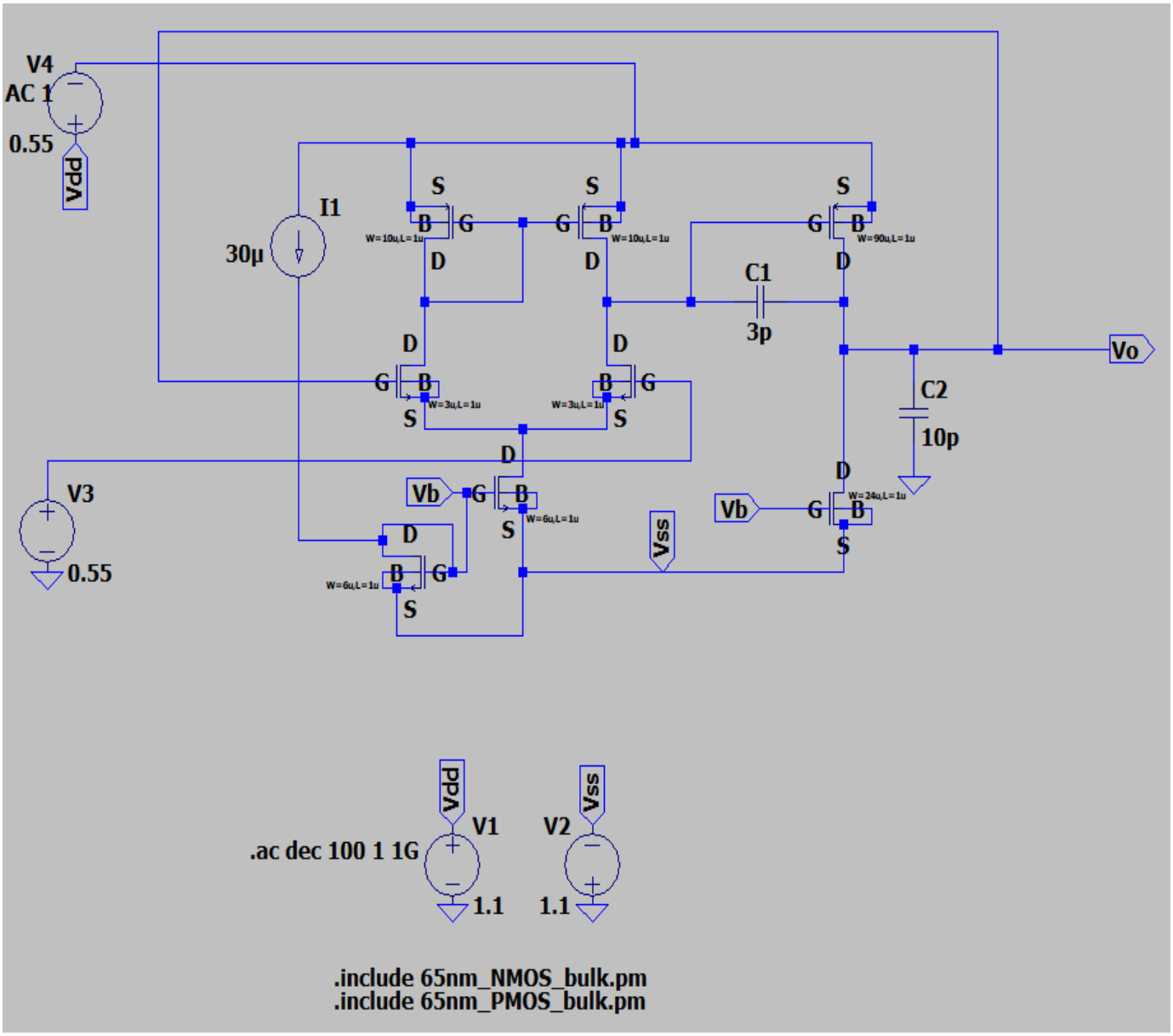

Figure 5: Circuit diagram for simulating PSRR

Here the variation is given to the supply and the corresponding variation in output is observed.

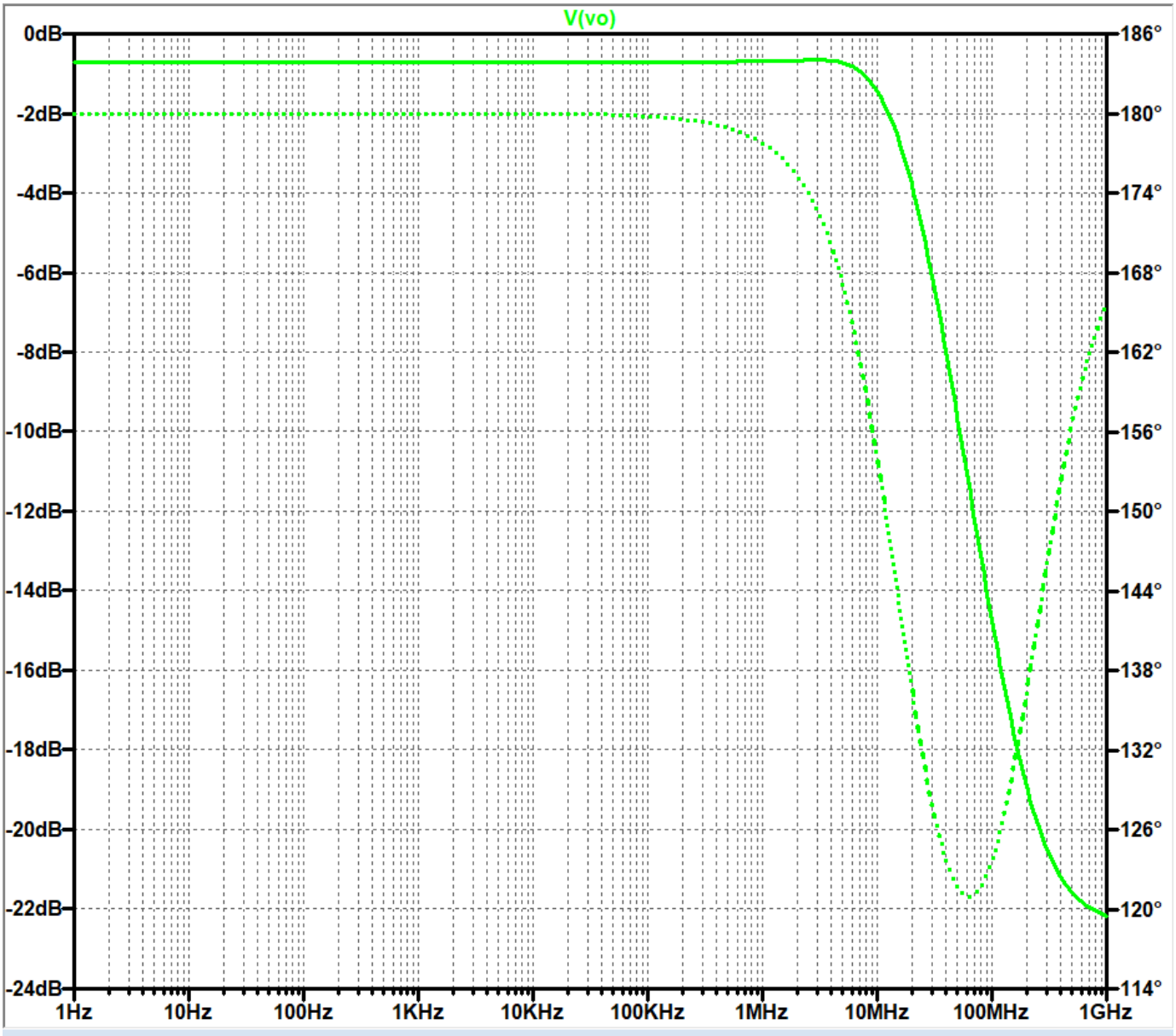

Figure 6: Op-amps resulting PSRR

2 Op-amp in unity gain feedback

2.1 Slewing for Step-response

The circuit for simulation is as follows:

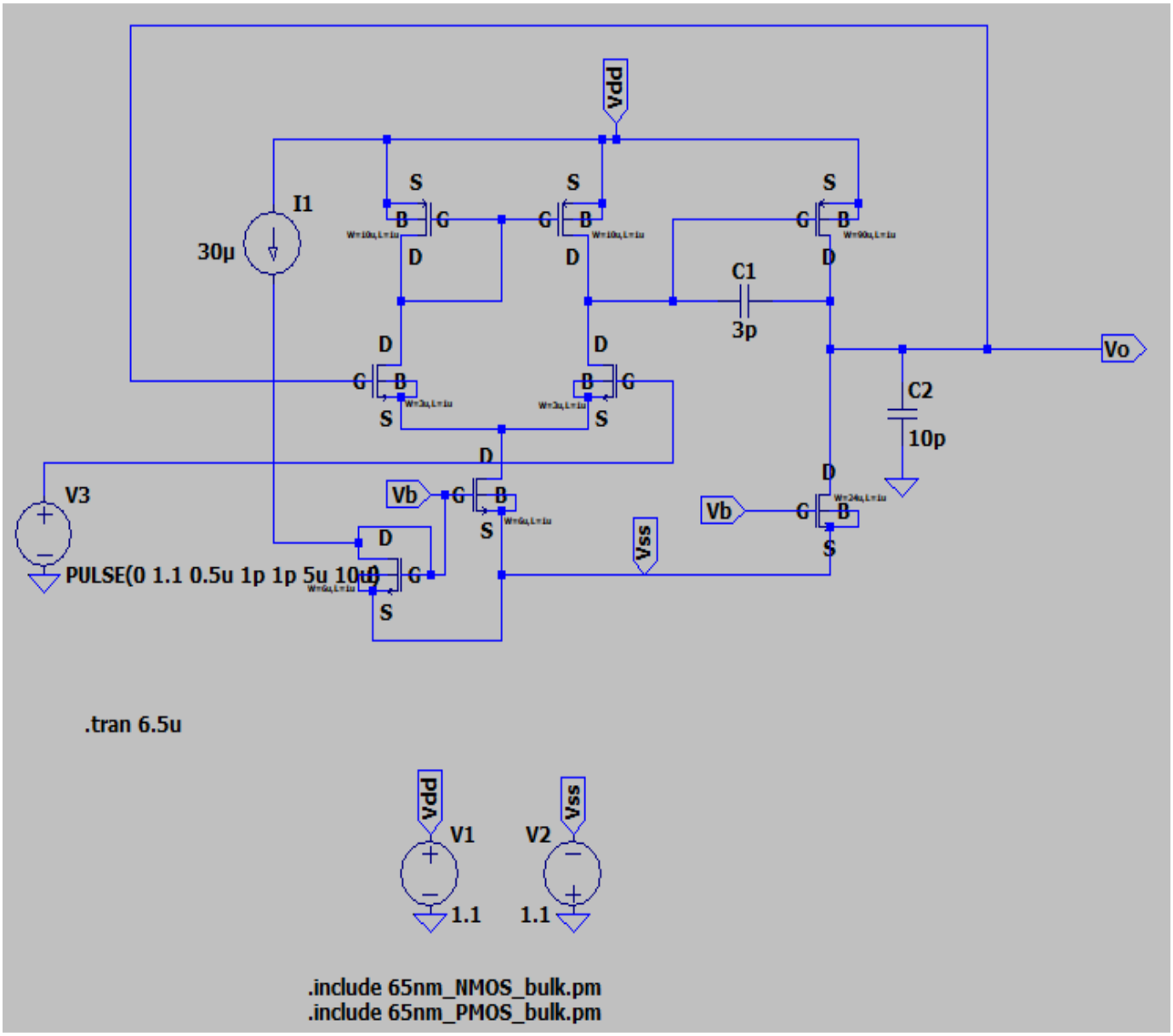

Figure 7: Circuit diagram of Unity gain feedback demonstrating slewing

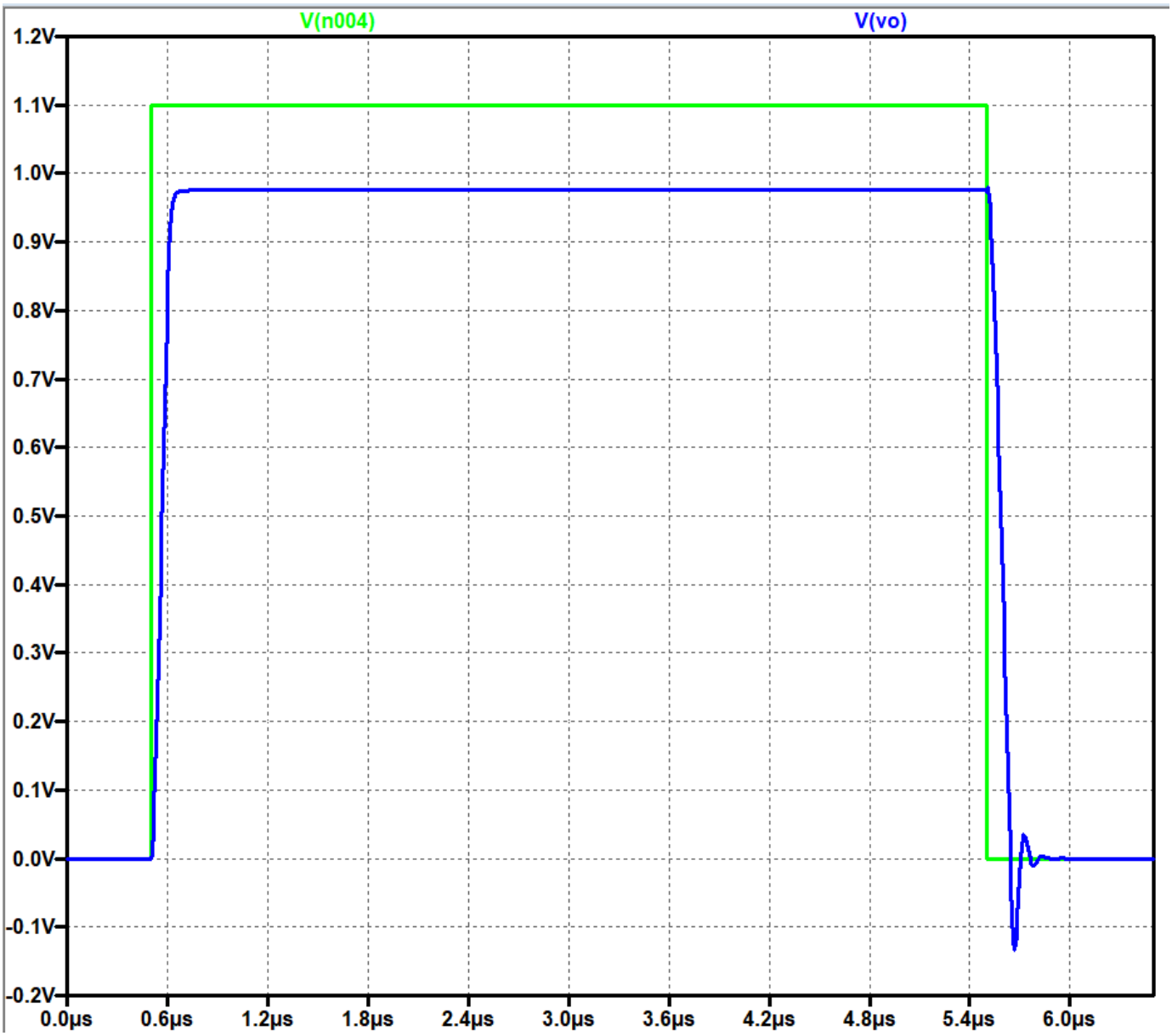

Figure 8: Simulation result of slewing

The slewing effect can be seen in the rise and fall of the input pulse. The output has a reduced swing compared to the input swing which can be reasoned because of the parasthetic capacitance. The output in high to low transition seem to overshoot but settles to zero quick enough. Hence, the design covers the specification for slewing.

2.2 Output vs Input for ramp input

The circuit for simulation is as follows:

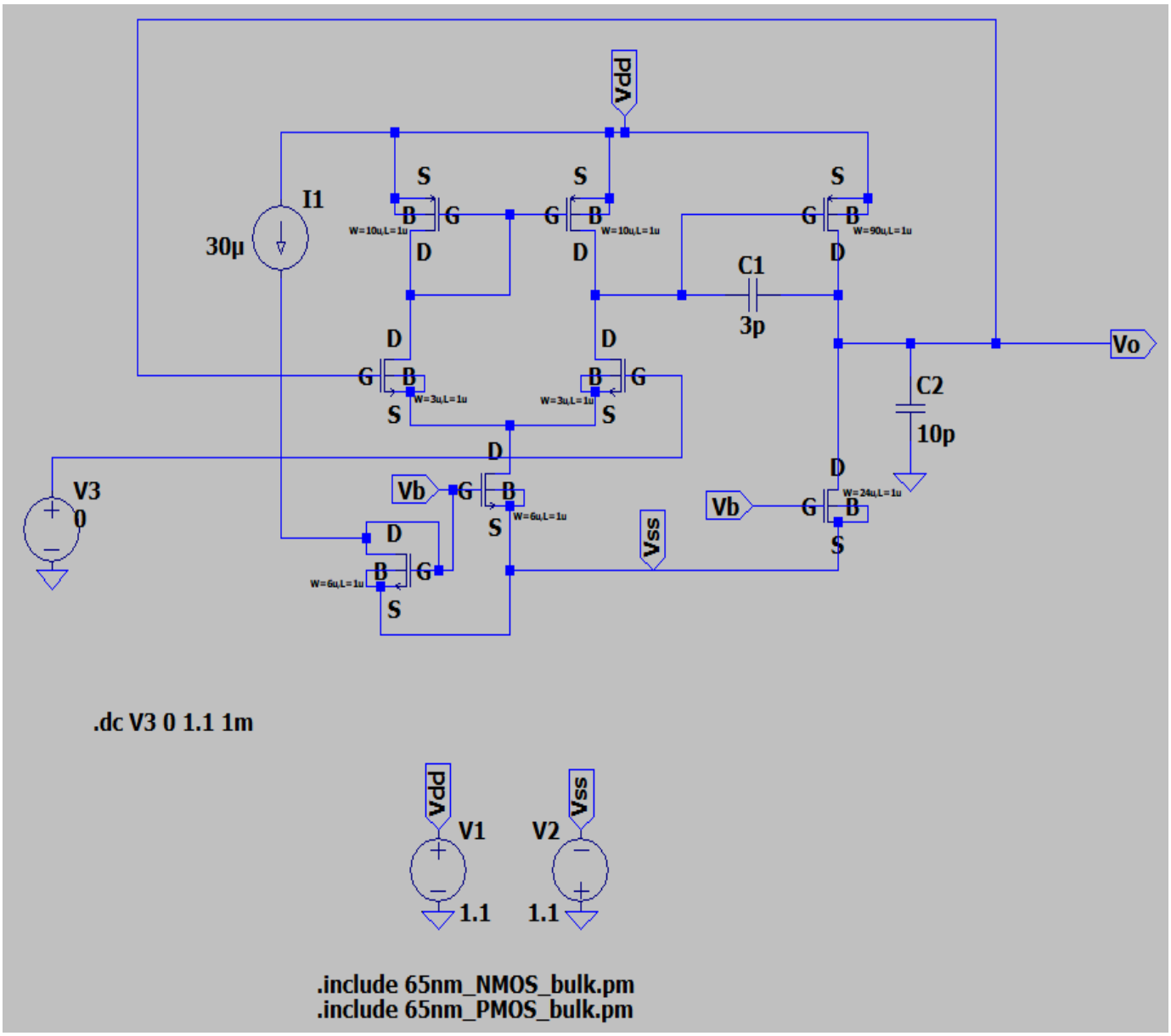

Figure 9: Circuit diagram of Unity gain feedback

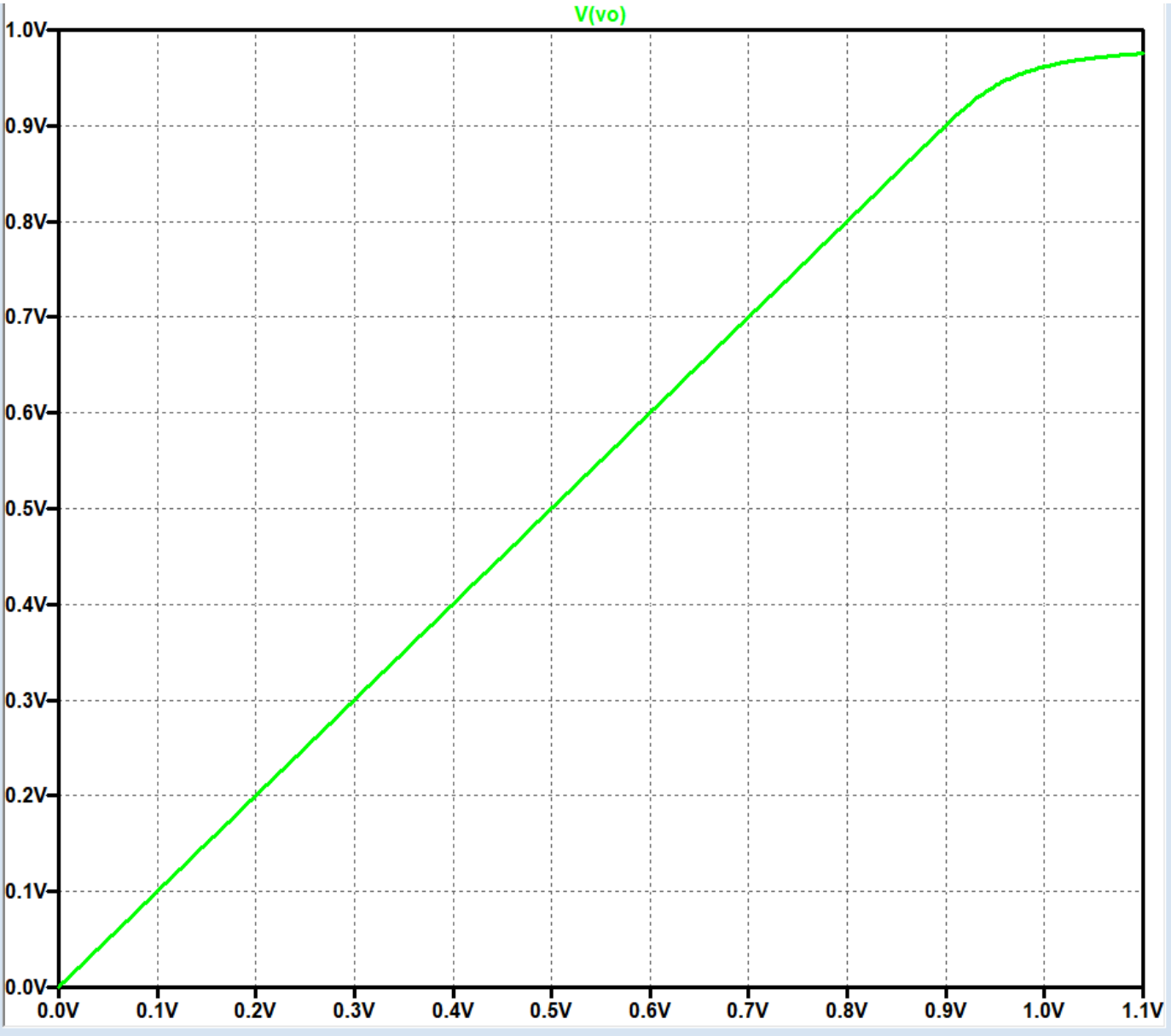

Figure 10: Simulation result ramp input

As the unity feedback op-amp acts like a bufffer, the output voltage goes in hand to hand with the input rise except at when the input voltage crosses the limit which keeps the MOSFETs in saturation. Here we can see, one of the MOS enters to triode region. Hence we can see a slight low rise in output ramp.

2.3 Output Spectrum for sinusoidal input

Te circuit for simulation is as follows:

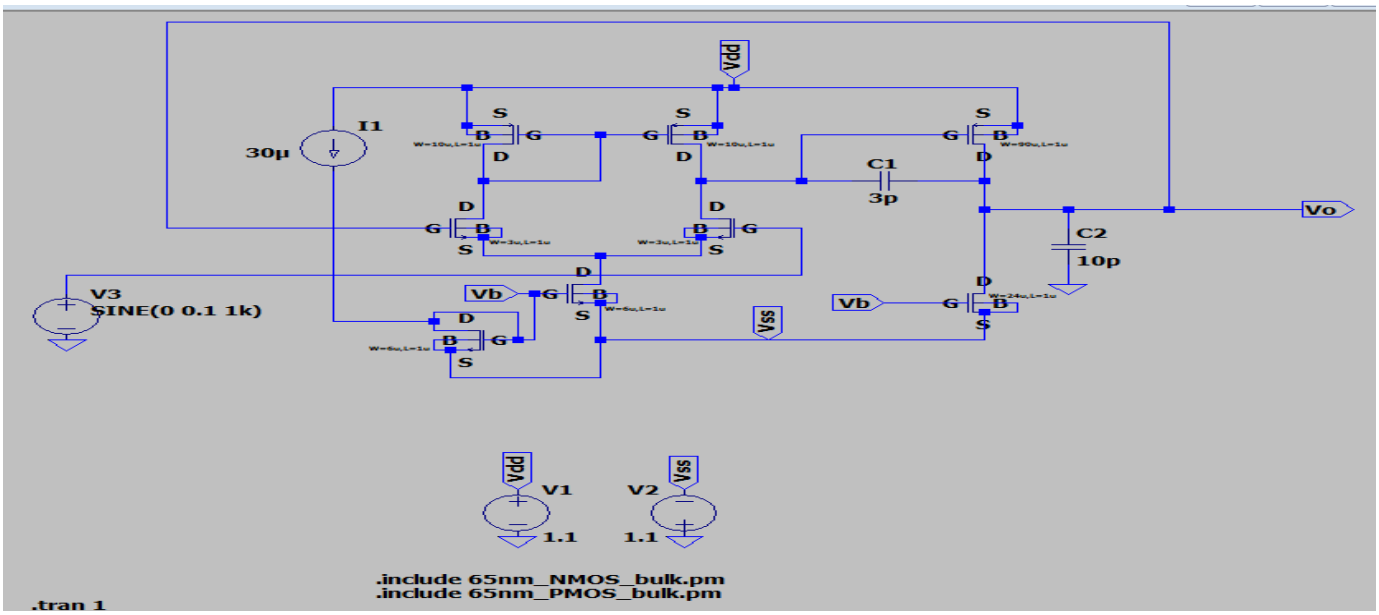

Figure 11: Circuit diagram of Unity gain feedback with sinusoidal input

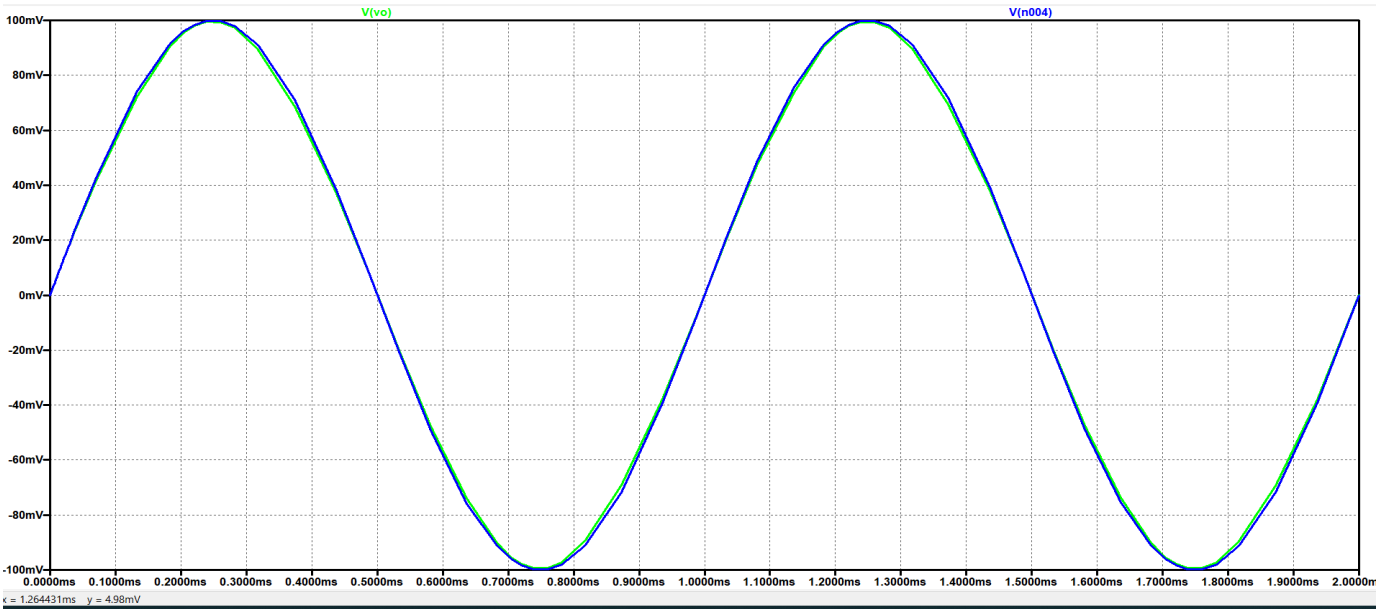

Figure 12: Transient output

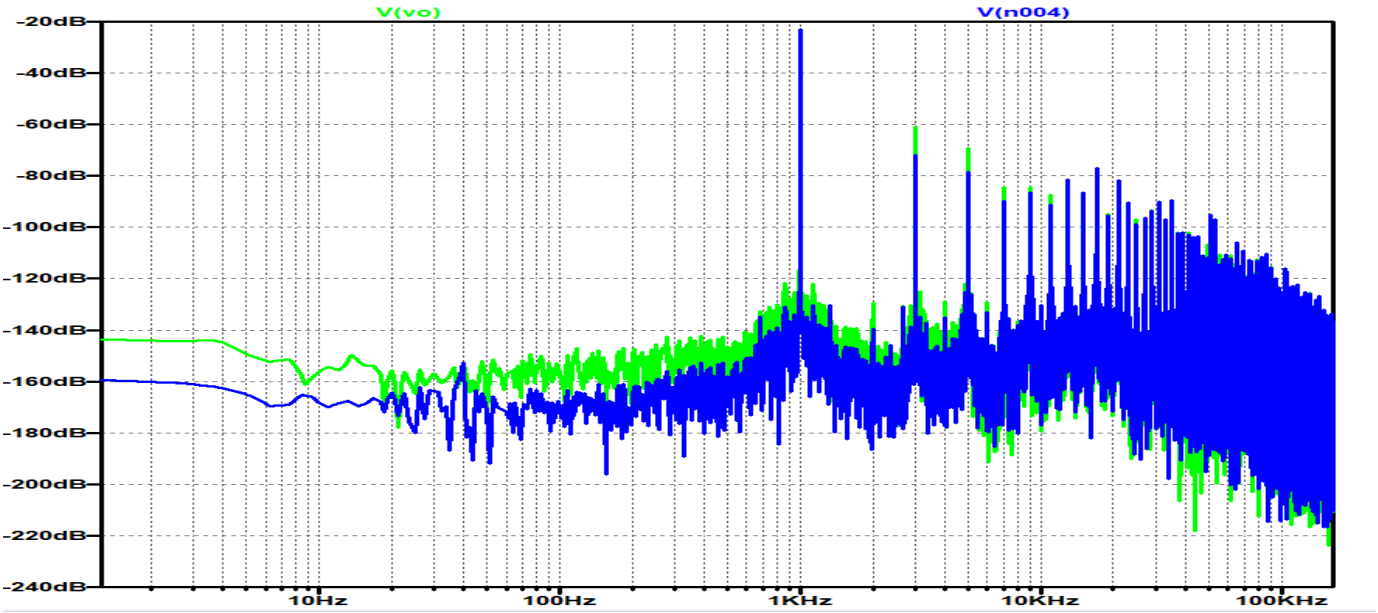

Figure 13: Output spectrum

N-Period=1
Fourier components of V(vo)
DC component:5.9702e-005

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]
1	1.000e+03	9.791e-02	1.000e+00	0.19°
2	2.000e+03	6.907e-06	7.054e-05	-71.11°
3	3.000e+03	1.282e-03	1.310e-02	-164.68°
4	4.000e+03	5.821e-06	5.945e-05	-49.32°
5	5.000e+03	4.970e-04	5.076e-03	6.96°
6	6.000e+03	5.597e-06	5.717e-05	-30.04°
7	7.000e+03	9.490e-05	9.692e-04	-36.21°
8	8.000e+03	5.336e-06	5.450e-05	-17.53°
9	9.000e+03	5.084e-05	5.193e-04	-143.78°

Total Harmonic Distortion: 1.408878%(1.439174%)

Figure 14: THD

Hence the resulting THD is nearly 1.4%.