EE3300/EE5183 2021

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Simulation Exercise 1

1. MOS transistors in nano-scale CMOS processes don't quite follow quadratic I-V characteristics we studied in the class. Their exact models (BSIM, PSP) contain hundreds of parameters, and it is almost impossible to use these models for hand calculations. In this exercise, we will try to extract a simple quadratic model for MOS transistors from the available BSIM4 model.

   Download model files and corresponding LTspice files from the class website.

   Determine the following for NMOS (L=65nm, W=1um) and PMOS (L=65nm, W=1um) transistors from the given model files:

   (Given supply voltage, V_{dd}=1.1 V. Use $V_{ds} = V_{ds0} = V_{dd}/2$, when not specified.)

   - V_{gs0}: V_{gs} value in the middle of the quadratic region of $I_{ds} - V_{gs}$ curve. Use derivative function available in waveform viewer.
   - g_{m0}: g_m at V_{gs0}.
   - V_T: x-axis intercept of tangent at V_{gs0} in $g_m - V_{gs}$ curve.
   - $\beta = \mu C_{ox}$: Using above extracted values and assuming quadratic behaviour.
   - g_{ds0}: g_{ds} at V_{gs0}.
   - λ: Channel-length modulation parameter. ($V_{gs} = V_{gs0}$).

   What is the range of V_{gs} for which error in estimated g_m is less than 50%?

2. Repeat the above exercise for longer channel length devices. NMOS (L=1um, W=1um) and PMOS (L=1um, W=1um).