EE3300: Analog Circuits

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Mini-project

1. Design a two-stage opamp (miller-compensated) in 65 nm CMOS process with the following specifications:

   - Supply voltage: 1.1 V.
   - Input common-mode voltage: 0.55 V.
   - Load capacitance: 10 pF.
   - Unity gain bandwidth: 10 MHz.
   - Phase-margin: 60 degrees.
   - DC gain $> 40\,dB$
   - Slew rate $> 10V/\mu s$.

   Objective is to minimize power consumption while satisfying the above specifications.
   Design should include biasing circuitry.
   Submit hand calculations used to find:

   - First and second stage transconductance.
   - Miller cap and/or zero-nulling resistor.
   - First and second stage bias-current.

   Submit the netlist and the following frequency responses:

   - Bode plot.
   - Common-mode rejection ratio (CMRR).
   - Power-supply rejection ratio (PSRR).

2. Connect the above op-amp in unity-gain feedback and submit the following plots:

   - Step-response when the output starts slewing for both positive and negative steps.
   - Output vs input when input DC voltage is varied from 0 V to supply voltage.
   - Output spectrum when $(0.1 \sin 2\pi 1000t)$ V is applied at the input. Also calculate the total harmonic distortion (THD).