Electronic Devices and Circuits Lab : Report-7

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Contents

1 Aim :

The aim of the experiment was to understand what are mosfets and study their behaviour

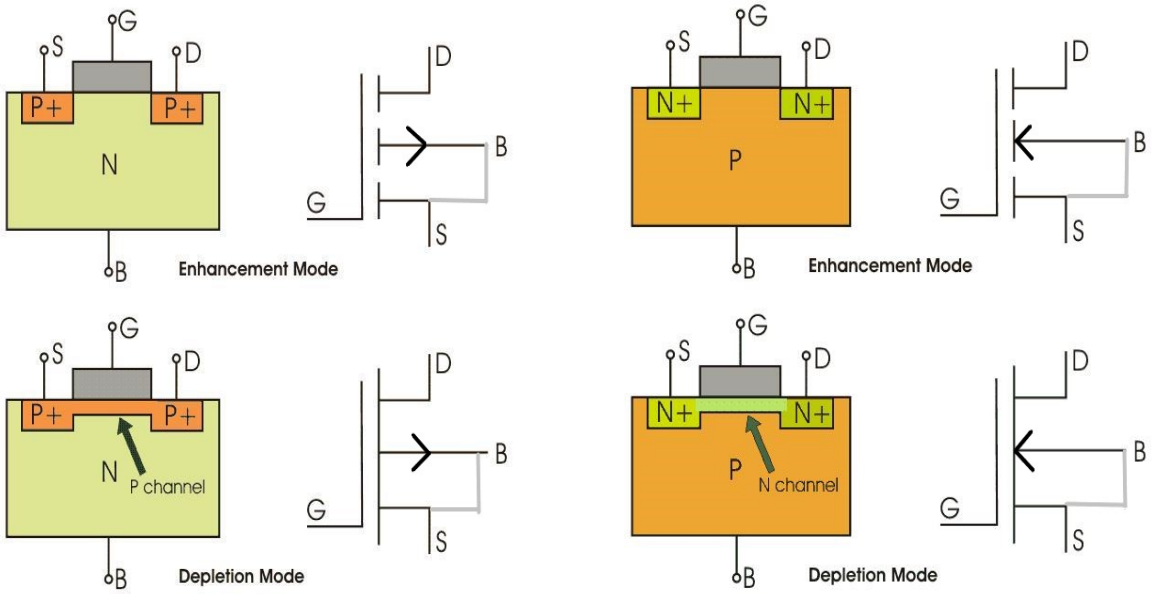
2 Procedure :

MOSFET stands for Metal-oxide-semiconductor-Field-effect-Transistor and is one of the Field Effect Transistors along with JFET, MESFET etc. Unlike the BJT's which are like current dependent amplifying sources, these devices are more voltage-driven and are unipolar - current flow is majorly because of either holes or electrons. The main advantage of MOSFET over BJT is that it requires no input current to control load current, there by providing high input impedance. MOSFET's are large part in the analog electronics industry and almost involved in every electronics application.

MOSFET's are generally of two categories

- Depletion Type : Here conduction channel is initially present and is modified accordingly by applying required bias.
- Enhancement Type : Here the conduction channel is initially absent and is formed along the way while altering the bias, developing channel for conduction.

Basing on the type of channel, they are further categorised to P-channel MOSFET and N-channel MOSFET .The general structure lies the same for both. It has 4-terminals namely, Source(S), Gate(G), Drain(D) and Substrate/Body(B). The body and the source terminal are together connected to ground mostly, effectively making it a 3-terminal device. The symbols used to denote these MOSFET's are as shown. The dashes in the symbols

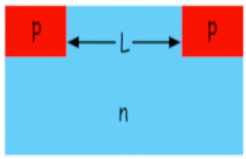


(a) P-channel MOSFET (b) N-Channel MOSFET

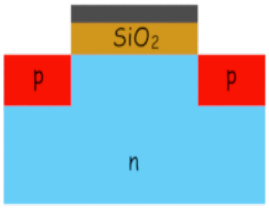
Figure 1: Structure and Symbols

of enhancement mode signify the absence of channel between the source and the drain, whereas in depletion mode, the channel is initially present, hence its symbol has a single connected dash line. And the '+' symbol indicates the excessive doping done to it. The difference between the symbols of n-type and p-type is shown by an arrow at body terminal, outward for P-type, inward for N-type. The arrow indicates movement of carriers from drain to source, hence I_{ds} is positive for n-type, negative for p-type.

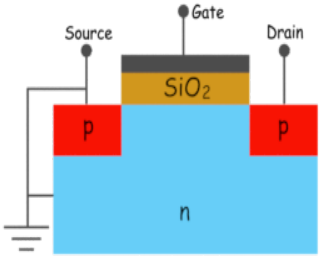
Working of Enhancement mode - PMOSFET



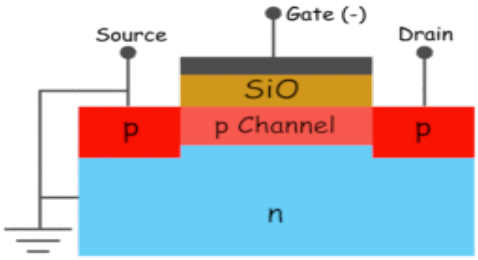
(a) Basic Structure



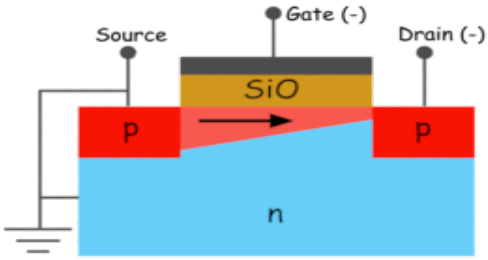
(b) Metal-Oxide-Semiconductor



(c) Terminal connections



(a) Applying Gate bias



(b) Application Drain Bias

P-channel MOSFET or PMOS, has a lightly n-doped substrate forming main body and two heavily doped p-type regions which are there in the body separated by a certain distance L which is referred as channel length. Now, to the top layer of substrate, a thin layer of dielectric which is generally SiO_2 or Al_2O_3, is added upon which metal plate is attached. Together, they effectively form a capacitor with a dielectric on the device. The terminals connected to heavily doped p-regions are source (S) and drain (D), terminal projected from the metal plate is the gate (G) and terminal from substrate is the body terminal. The source, body terminals are together grounded, facilitating the supply and withdrawal of free electrons as per requirement during operation.

Now by applying negative voltage at gate, negative static potential will be created on metal plate. Because of the capacitive action, positive charge gets accumulated just below the dielectric layer, forcing free electrons of n-type to move away. As a result,layers of uncovered positive ions appear. By further increasing the negative bias,after a certain voltage called threshold voltage, due to the electrostatic force, covalent bonds of the crystal start breaking, generating e-h pairs. Because of the applied bias, holes get attracted and

free electrons get repelled from the gate .Hence a p-channel between source and drain is created. Due to the concentration of holes in that channel, it becomes available for conduction of current.

When there is no potential difference between the source and drain, the channel width would be uniform and current is also zero. Now applying the drain bias such that negative voltage appears at drain terminal. Hence, the voltage difference between gate and drain reduces, so does the the width of the conductive channel. But because of the applied potential, the holes drift from source to drain as shown. So current flows from source to drain. By increasing the negative bias at drain, the channel width reduces but also the generation of e-h pairs increases, increasing current. After a certain voltage, the channel width at drain becomes almost constant, the current reaches its saturation value. Hence, By varying the voltage, the current through the device could be controlled.

Characteristics of Enhancement mode - PMOSFET

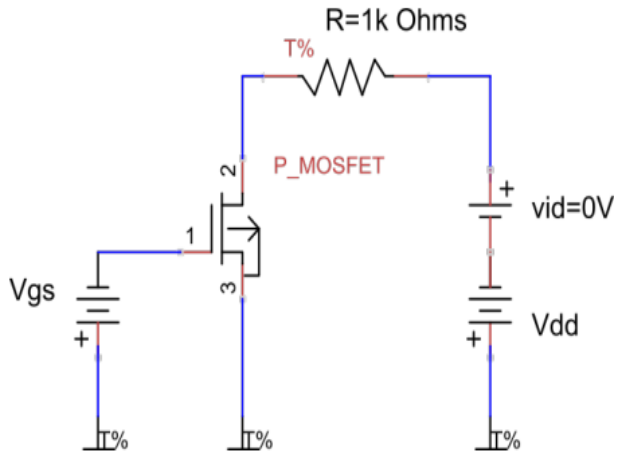


Figure 4: Circuit design for studying the PMOS Characteristics

The above circuit is used for studying the characteristics of the PMOSFET. As can be seen that V_{gs} and V_{ds} are negative as should be the gate bias and drain bias. Assuming that the potential drop across the resistor to be ignorable (drain current is in micro-Amp), we can take V_{dd} is approximately similar to V_{ds}. As needed the source and the body terminal are grounded together. The battery source V_{id} which is zero is used to study the drain current. The main characteristics of the MOSFET are the output characteristics and the transfer characteristics.

Output Characteristic is studying how drain current(I_d) varies with drain bias(V_{ds}), for different gate bias(V_{gs}) constant for a curve.
Transfer Characteristic is studying how drain current(I_d) varies with gate bias(V_{gs}), for different drain bias(V_{ds}) constant for a curve.

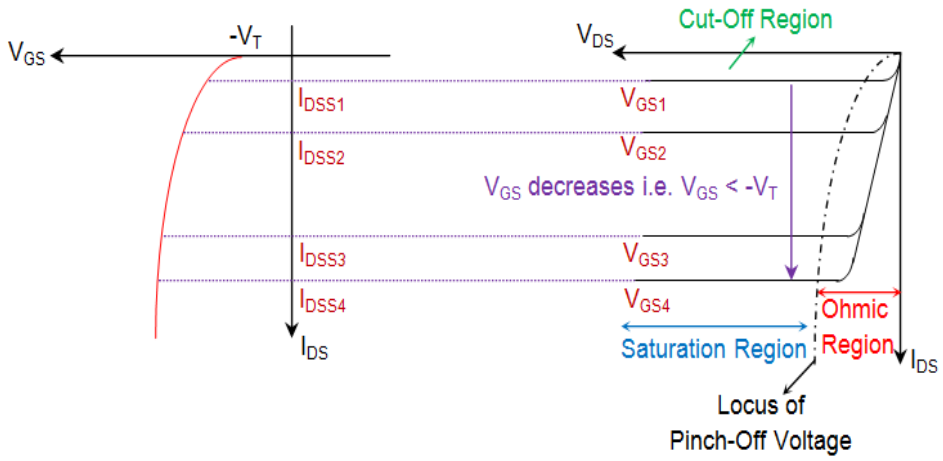


Figure 5: Transfer Characteristic(left) and Output Characteristic(right)

As designed V_{gs},V_{ds},I_{ds} are all negative. From the transfer characteristics it is clear that the drain current is zero, until it reaches the threshold voltage-V_T, as the formation of channel happens only after exceeding this cut-off. After exceeding, the current also increases accordingly with increase in negative gate bias due to more generation of e-h pairs. The drain current will be zero if the drain bias is zero irrespective of gate bias. For more negative V_{ds}, the more will be the current due to increase in drift of holes.
From the output characteristics, there 3 main regions of operation

1. Cut-off Region : Here $|V_{GS}| < |V_T|$, so channel is not fully formed, hence acts like open switch where regardless of the value of V_{ds}, $I_d = 0$.
2. Linear (Ohmic) Region : Here $|V_{GS}| > |V_T|$ and $|V_{DS}| < |V_{pinch-off}|$. Here current varies linearly with drain bias, and is larger for higher gate bias(in magnitude). So acts as a gate voltage-controlled resistance, which can be used for amplification.
3. Saturation Region : Here $|V_{GS}| > |V_T|$ and $|V_{DS}| > |V_{pinch-off}|$. The width of the channel here has reached to its minimum, and the current reaches its maximum (I_{dmax}) remains constant for further increase in drain bias. Hence acts like a closed switch.

The pinch-off voltage is defined as the minimum voltage after which the drain current remains constant. Ideally, it is $|V_{GS}|$-$|V_T|$.

3 Results and Observations

3.1 Transfer Characteristics

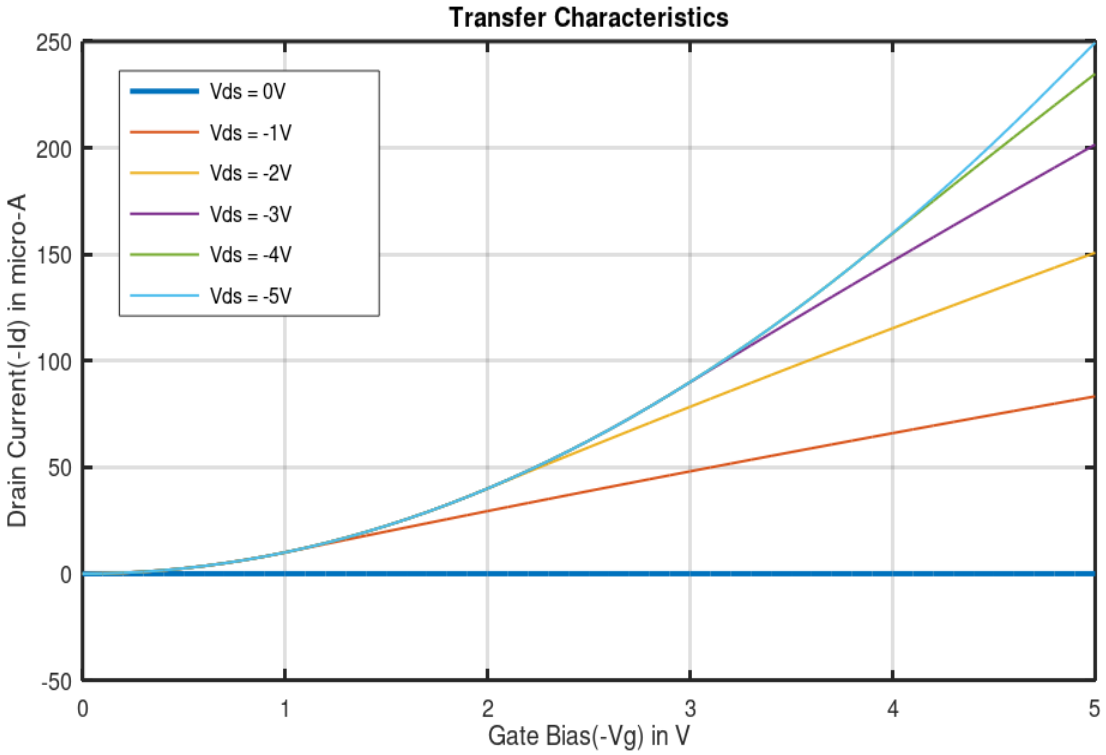


Figure 6: Transfer Characteristics - I_D vs V_G for different V_D

Observations

- The gate bias(V_{gs}),drain bias(V_{ds}),drain current(I_d), all are negative, implying that source terminal is at higher potential and the current flow is from source to drain.
- The drain current(I_d) is zero irrespective of the gate bias(V_{gs}) when drain bias(V_{ds}) is zero.
- The drain current is also zero when $|V_{gs}|$ is less than 0.2V nearly, which could be the threshold voltage.
- As the gate bias increases, the drain current also increases.
- For higher $|V_{ds}|$, the raise in drain current for an increase in gate bias is higher.

3.2 Output Characteristics

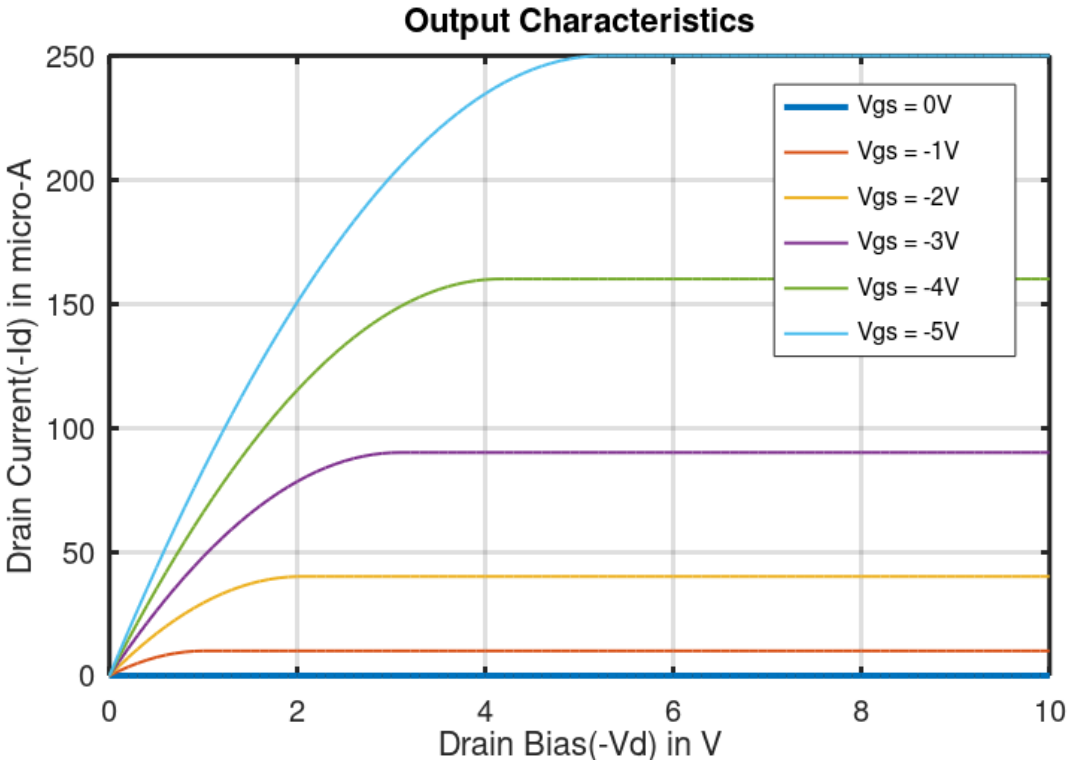


Figure 7: Output Characteristics - I_D vs V_D for different V_G

Observations

- The gate bias(V_{gs}),drain bias(V_{ds}),drain current(I_d), all are negative, implying that source terminal is at higher potential and the current flow is from source to drain.
- The drain current is zero when either $|V_{gs}|$,$|V_{ds}|$ is zero.
- The drain current initially varies linearly with $|V_{ds}|$ and then saturates to a constant value, whose value increases with increase in $|V_{gs}|$.
- The minimum voltage for saturation($V_{pinch-off}$), increases with increase in $|V_{gs}|$.
- The saturation current seems to vary quadratically with $|V_{gs}|$.

4 Conclusions

1. MOSFET's are alternates to BJT's, which are voltage driven amplification sources.

2. They have advantage of providing high input impedance and are unipolar devices providing more stability.

3. MOSFET's are categorised as Enhancement and Depletion type based on the presence of channel, which is further categorised as P-type or N-type based on the nature of channel.

4. MOSFET's have 4 terminals-source,gate,drain and body where source and body are connected together making it effectively 3 terminal device.

5. The basic structure of EMOSFET has 2 heavily doped small semiconductors grafted into a lightly and oppositely doped semiconductor with a dielectric on the top layer of substrate with a metal plate over it.Hence, it is also symmetric.

6. The channel develops when the gate bias is sufficiently applied and helps in conduction of current. By applying the drain bias the magnitude of current can be controlled.

7. In PMOSFET, the gate bias(V_{gs}),drain bias(V_{ds}),drain current(I_d), all are negative whereas in NMOSFET they are all positive.

8. There 3 regions of operation for MOSFET each having their own application as - Cut-off region as open switch, Ohmic region as amplification and saturation region as closed switch.

9. The width of channel can be increased by increasing the proper gate bias, which helps in generation of more e-h pairs. Hence for higher gate bias, we can get higher saturation current.

10. The gain in MOSFET's is less when compared to that in BJT, which is observed from the characteristics.