Electronic Devices and Circuits Lab : Report-8

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Contents

1 Aim :

The aim of the experiment was to understand how to model logic gates using mosfets and study their behaviour.

2 Procedure

2.1 NOT gate

A NOT gate inverts the input i.e, for input signal be high, the output would be low and vice-versa. The truth table is given as

Input	Output
0	1
1	0

Implementation of NOT gate using CMOS

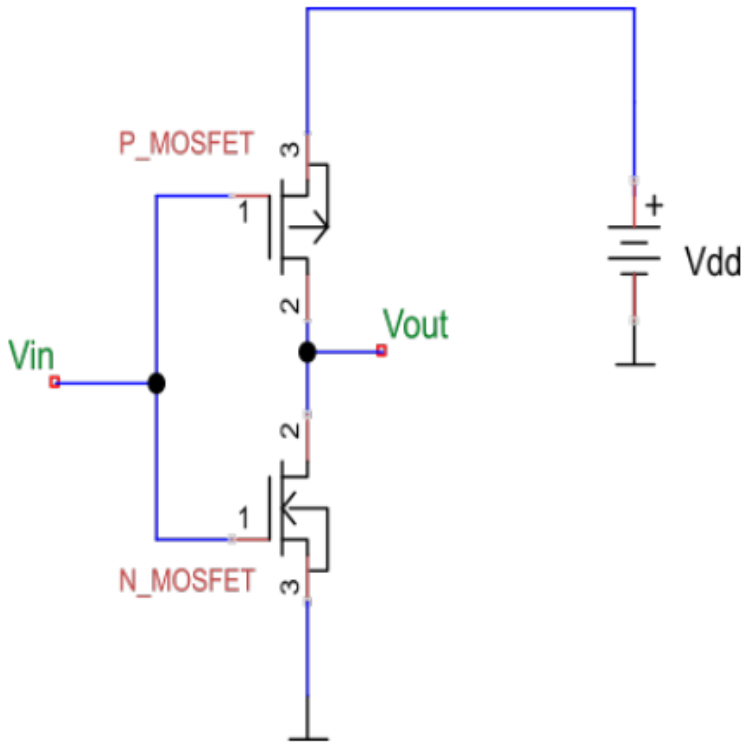


Figure 1: NOT gate

It can be seen that the circuit consists of a PMOSFET and a NMOSFET, a Voltage bias (V_{dd}=5V) and input-output terminals. A binary '1' implies that the voltage is high which is considered 5V and for binary '0' implies that the voltage is low which is taken as 0V. The body terminals of both the MOSFET's are connected to their source terminals. Both the gates are biased by same V_{in} and the drains of both are connected to the output terminal V_{out}. The source of PMOS is biased by V_{dd} whereas the source terminal of NMOS is grounded.

The inverting logic can easily be be observed. When V_{in} is low i.e, 0V, the V_{GS} for PMOS is -5V where as for NMOS is 0V. So PMOS acts as closed switch and the NMOS acts like an open switch making $V_{out} \approx V_{dd}$ =5V, i.e, high or logically '1'. Similarly, when the input is high, V_{GS} is 0V for PMOS and +5V for NMOS. So the PMOS acts like open switch and the NMOS acts like a closed switch making the output voltage 0V or low i.e, logically '0'. Note that in either cases, no static current flows into the inverter as well as from the input making it good for voltage sensing.

Transfer Characteristics of the NOT gate - V_{out} vs V_{in}

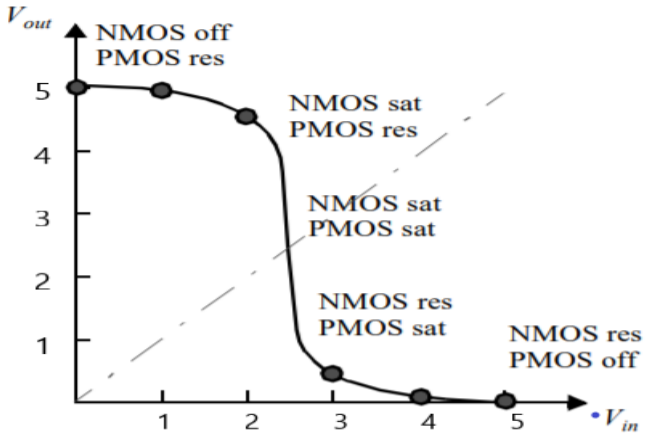


Figure 2: Transfer Characteristic, annotations-res(istive), or sat(urated)

Each MOSFET has its own threshold voltage depending on its geometrical dimensions ad doping concentrations. Considering the threshold voltage for NMOSFET as V_{Tn} and for PMOSFET as V_{Tp}. The switching threshold, V_m, is defined as the point where V_{in}=V_{out}. The different dots show the different stages in the CMOS inverter.

- $0 < V_{in} < V_{Tn}$: PMOS operates in linear region and NMOS operates in cut-off.
- $V_{Tn} < V_{in} < V_m$: PMOS still acts in linear region as there is still required bias whereas the NMOS now operates in saturation because of V_{DS} across it.
- V_{in}=V_m : Both devices have enough forward bias voltage to drive them to saturation.
- $V_m < V_{in} < V_{dd}$-V_{Tp} : Here NMOS is conducting in linear region but the PMOS still remains in saturation because of the V_{DS} across it.
- $V_{in} > V_{dd}$-V_{Tp} : Now, the PMOS will be be in cut-off state due t low V_{GS} and the NMOS acts in linear range but has I_D almost zero, making V_{out}= 0V.

Switching Threshold - V_m

When $V_{in} = V_m = V_{out}$, both the mosfets are in saturation as V_{DS}=V_{GS}. Ignoring the length modulation effects, assuming identical oxide thicknesses for PMOS and NMOS, identical channel lengths and V_{dd} be large compared to threshold and saturation voltages, analytical expression can be given as

$$V_m \approx \frac{rV_{DD}}{1+r}$$

where r is the ratio of widths of channel in PMOS and NMOS respectively. Ideally, for equal channel width, the switching threshold would be around $V_{dd}/2$. Hence, in the given question where we have r=10, the switching threshold can be expected around 10(5)/11 i.e, 4.5V. This shift can also be intuitively explained as the channel length is more, the bias V_{DS} has to be more for turning the MOSFET to saturation as the potential drop occurs over larger length. Hence, the shift can be seen where PMOS is in linear region for larger input voltage.

2.2 NOR gate

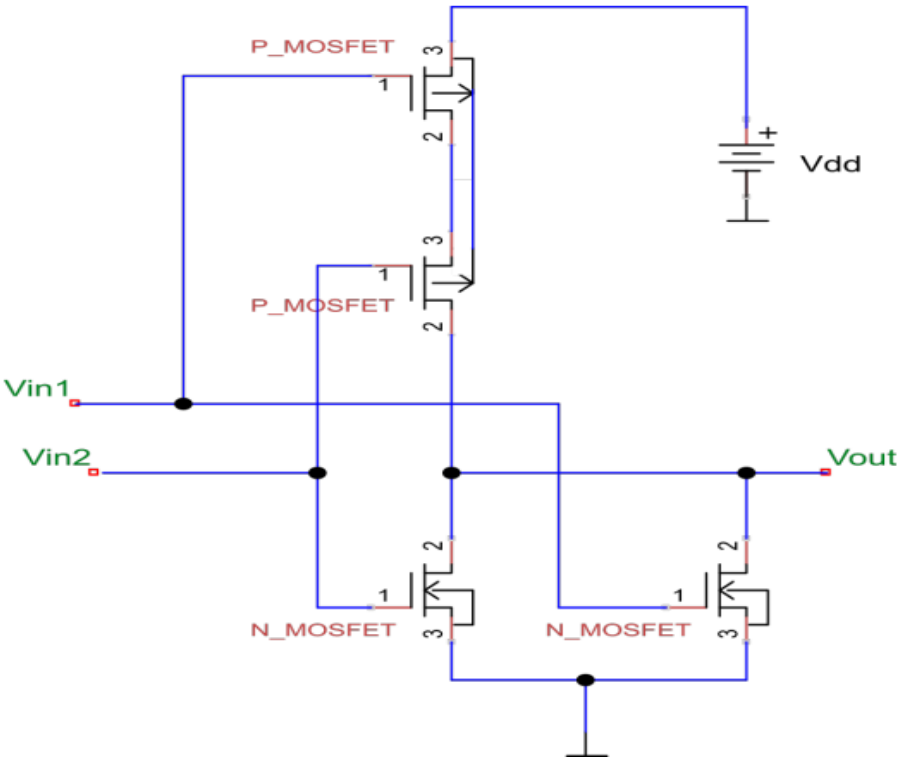


Figure 3: NOR gate implementation

NOR gate is considered as Universal gate along with NAND. The NOR gate gives output high when both the inputs are low. The truth table is as shown

Input1(A)	Input2(B)	Output($\overline{A+B}$)
0	0	1
0	1	0
1	0	0
1	1	0

The circuit for implementing the NOR gate using CMOS is shown above. The implementation of logic can be seen as

- Vin1=0,Vin2=0 : When inputs are low, the PMOSFET's are enough biased(V_{GS}=-V_{dd}), hence act like closed switches whereas the NMOSFET's acts like open switches because of the low bias, channel itself is not formed. So the output voltage is same as that of V_{dd}, hence high.

- Vin1=0,Vin2=1 : Here PMOSFET-1 is ON and NMOSFET-1 is OFF, PMOSFET-2 is OFF and NMOSFET-2 is ON. So output terminal gets grounded through the NMOSFET-2, so will logically low or '0'.

- Vin1=1,Vin2=0 : It is exactly complemented to the previous state. PMOSFET-1 is OFF and NMOSFET-1 is ON, PMOSFET-2 is ON and NMOSFET-2 is OFF. So output terminal gets shorted to ground through the NMOSFET-1, so will logically low or '0'.

- Vin1=1,Vin2=1 : When both the inputs are high both PMOS will be acting as open switches and both the NMOS will be acting closed switches, so again the output is grounded, which implies low or '0'.

2.3 OR gate using NOR and NOT gate

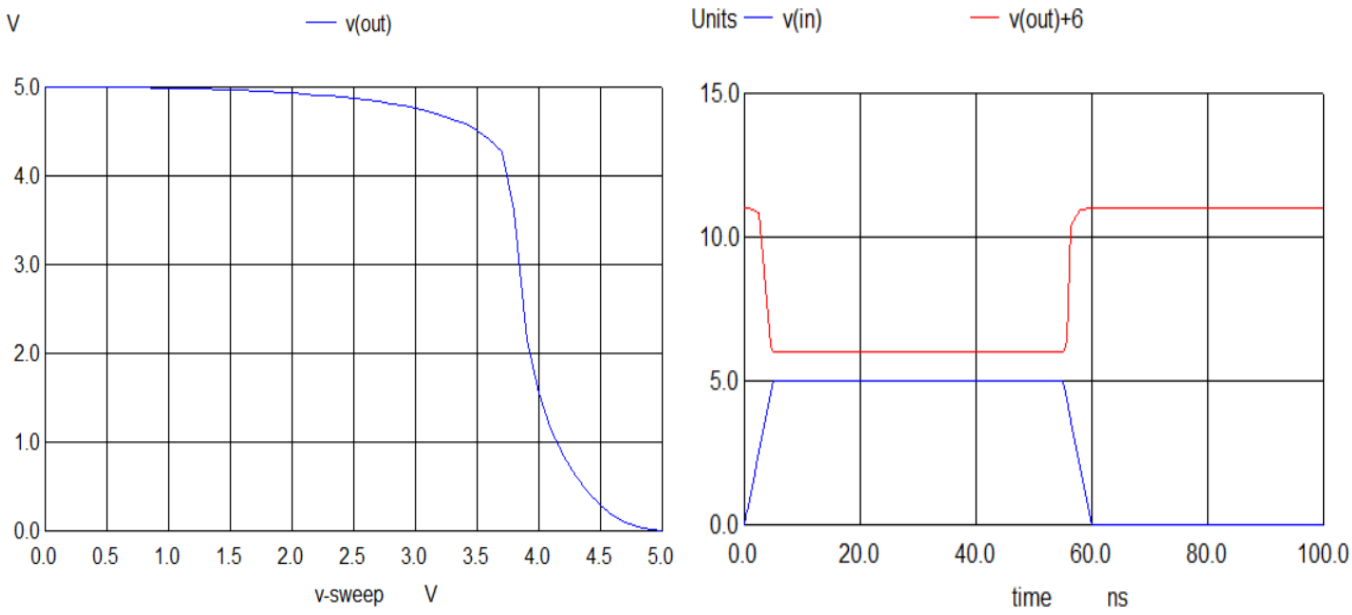
By cascading the NOR gate and NOT gate we can get the logical function of OR gate. As for input signals A and B,

$$\overline{\overline{A+B}} = A+B$$

where $\overline{A+B}$ is output of NOR and complementing it, we get OR.

3 Graphs and Understanding

3.1 NOT gate



(a) Transfer characteristics (b) Transient simulation

Figure 4: Simulation Outputs for NOT gate

Observations

- The NOT gate function can be seen inverting the output. For high signal, we get a low output an vice-versa.
- The switching threshold is around 3.7V . The graph suggests that the output stays at nearly high for larger range of input voltage. So making width of PMOS larger than the NMOS affects the switching threshold to move right.
- Though the inversion when the input is exactly high and low is perfect, when the voltage is in between, it does not perfectly invert.
- The voltage reached when high depends on the biasing voltage V_{dd}, which is 5V.

3.2 NOR gate

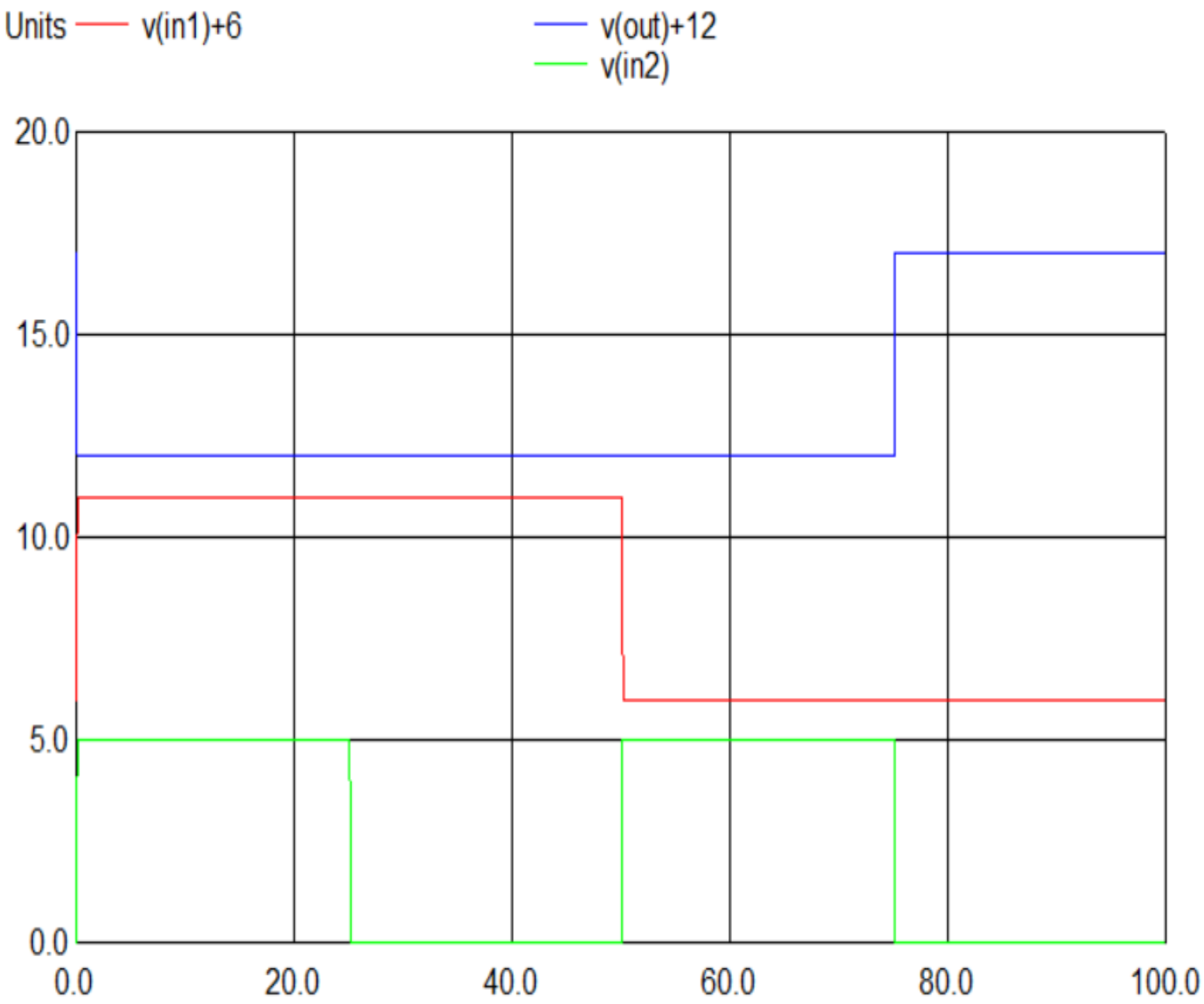


Figure 5: Simulation output for NOR gate

Observations

- The output goes high only when both inputs are low.
- The time for switching is very fast and does not have lag.
- The logic function can be given as $\overline{A}.\overline{B}$.

3.3 OR gate

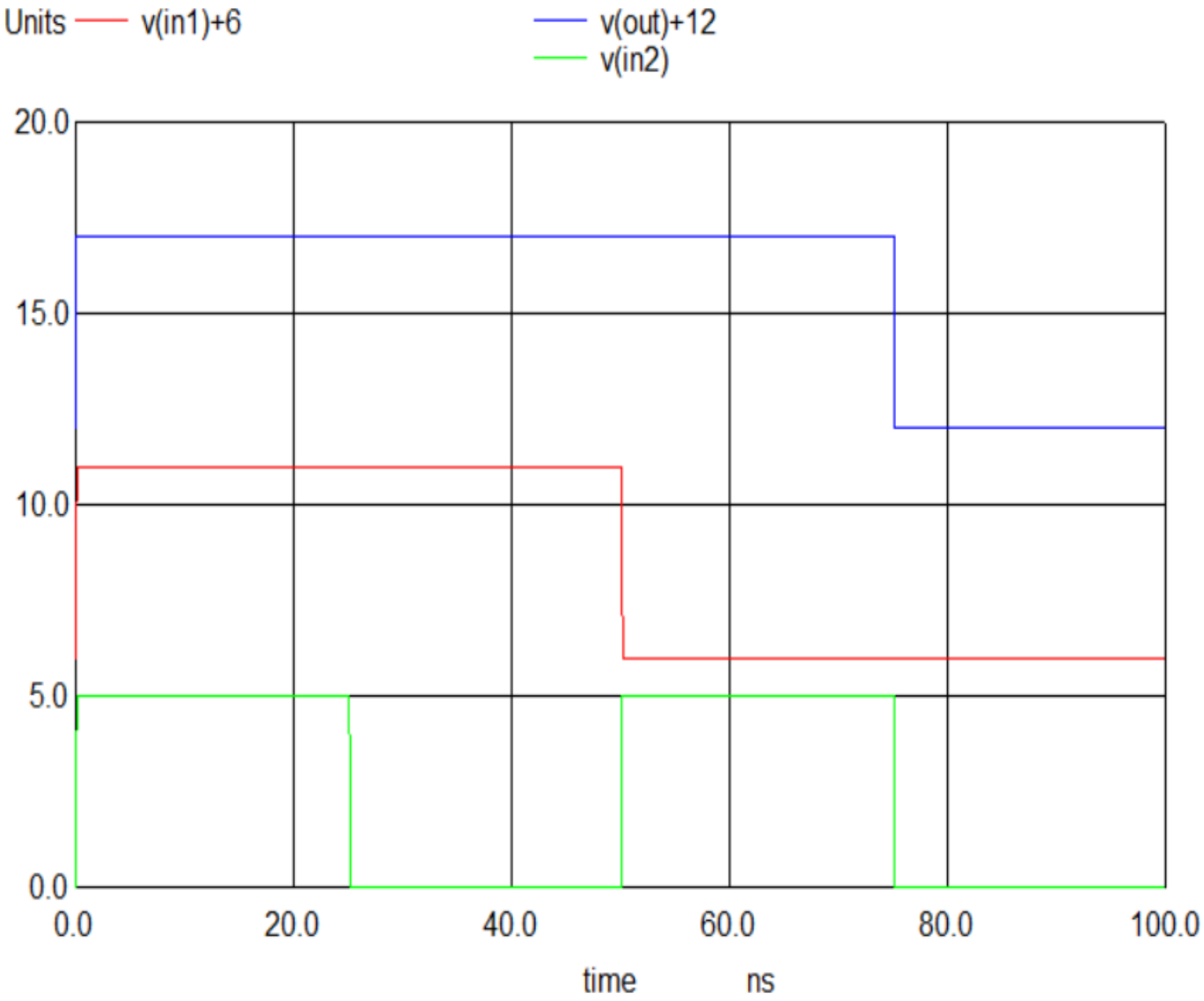


Figure 6: Simulation output for OR gate

Observations

- The output is always high except when both the voltages are low.
- The time for switching is fast and does not have any lag.
- The output is same as when the NOR output gets complemented.
- The logic function can be given as A+B .

4 Conclusions

1. The logic gates can be implemented using MOSFETs.
2. NOT gate can be implemented using a PMOSFET and NMOSFET. The output is the inverted input.
3. The current taken from the input source and the drain current at operation is zero.
4. The transfer characteristics of NOT gate depends on various factors, one such being the channel width.
5. For relatively higher channel width of PMOS, the switching threshold shifts right.
6. The output voltage when high is driven by the bias voltage V_{dd}.
7. NOR gate gives output which is high only when both the input voltages are low.
8. It can be implemented by a couple of PMOSFETs and couple of NMOSFETs.
9. Cascading the NOR gate and NOT gate, we can get the logical OR gate.
10. The output of OR gate is always high except only when both the inputs are low.