Electronic Devices and Circuits Lab : Report-3

Sahukari Chaitanya Varun
EE19BTECH11040
Group-4

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Contents

1 Aim :

The aim of the experiment was to understand the fundamental properties and characteristics of p-n junction diode.

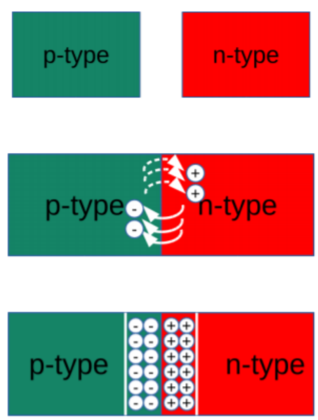
2 Procedure :

A p-n junction is formed when a p-type doped semiconductor is grafted with a n-type doped semiconductor, which shows different useful behaviours as a whole. There different methods of fabrication for forming a p-n junction diode.
As part of group-4, for the experiment purpose, we take the Donor doping concentration(N_d) as 5e18 cm^{-3} and Acceptor doping concentration(N_a) as 5e15 cm^{-3}. The length of both semiconductors is taken as 6μm. The temperature is maintained at 300k for all simulations. All simulations are done in nanohub.

2.1 Electron and Hole concentration on the p-side and n-side

When there the p-type semiconductor is grafted with a n-type semiconductor, at the junction, there are large number holes in the p-type and large number of electrons in the n-type compared to each other, resulting in concentration gradient. Hence diffusion of holes takes place from the p-type semiconductor to n-type leaving behind a positive charge on the p-side of the junction. Similarly the electrons diffuse from the n-type semiconductor to the p-type semiconductor leaving behind positive charge on the n-side. Due to development of charge between the junctions, it produces electric field opposing the direction of diffusion there by creating barrier for exchange of carriers. The layer formed between them is called depletion region, as its in dearth of carriers.

As the phenomenon occurs at the junction, the rest of the diode remains unaffected, even in terms of concentration. So the holes concentration in p-type and electrons concentration in n-type, away from depletion region almost remains unaltered.



At equilibrium, we have

$$np = n_i^2$$

$$\frac{p_p}{p_n} = \frac{n_n}{n_p} = e^{qV_o/kT}$$

where p_p and n_p are hole concentration and electron concentration at end of p-type semiconductor respectively. Similarly p_n and n_n are hole and electron concentrations at end of n-type semiconductor respectively on either side of the junction.V_o is the barrier potential formed between the junction.

When bias is applied across the diode, the depletion region gets affected accordingly. As considered that the semiconductor has less length as compared to its area, the effective resistance is quite low and major potential drop occurs in the depletion region. So the effective potential is now V_o-V_a, if bias is positive(forward), the depletion layer decreases due to increase in carrier diffusion. If applied oppositely(reverse), the effective potential increases as V_o+V_a. In similar fashion, the depletion layer widens there by inhibiting maximum carrier diffusion.
When bias voltage V is applied, we have from the previous equation

$$\frac{p_p}{p_n} = \frac{n_n}{n_p} = e^{q(V_o - V)/kT}$$

So the excess hole concentration in the edge of n-type of the depletion region is given by

$$\Delta p_n = p_n(e^{qV/kT} - 1)$$

where V is bias voltage. Similarly, the excess electron concentration in the edge of p-type of the depletion region is

$$\Delta n_p = n_p(e^{qV/kT} - 1)$$

These excess concentration leads to distribution of excess carriers inside semiconductor.For holes, if the n-region is long compared with the hole diffusion length L_p , the solution is exponential and similar argument holds for electrons in p-region.And the distribution of these minority carriers is given as

$$\delta p(x) = p_n(e^{qV/kT} - 1)e^{-x/L_p}$$

$$\delta n(x) = n_p(e^{qV/kT} - 1)e^{-x/L_n}$$

where x is distance measured from the junction as reference. L_p is diffusion length of holes in n-type and L_n is diffusion length of electrons in the p-type for given bias V (which can be forward or reverse). In forward bias the distribution of minority carriers increases and in reverse bias, the minority carriers are almost zero.

2.2 Band Structure

Initially, before the grafting, the semiconductors have their own band structure. The p-type semi conductors have fermi level closer to E_v and in the n-type, the fermi level is closer to E_c. When the two semiconductors are grafted, potential barrier is formed. The separation of the energy bands is a direct function of the electrostatic potential barrier at the junction given by qV where V is the potential drop across the transition region.

At equilibrium, when no bias voltage is applied, the fermi level has to stay

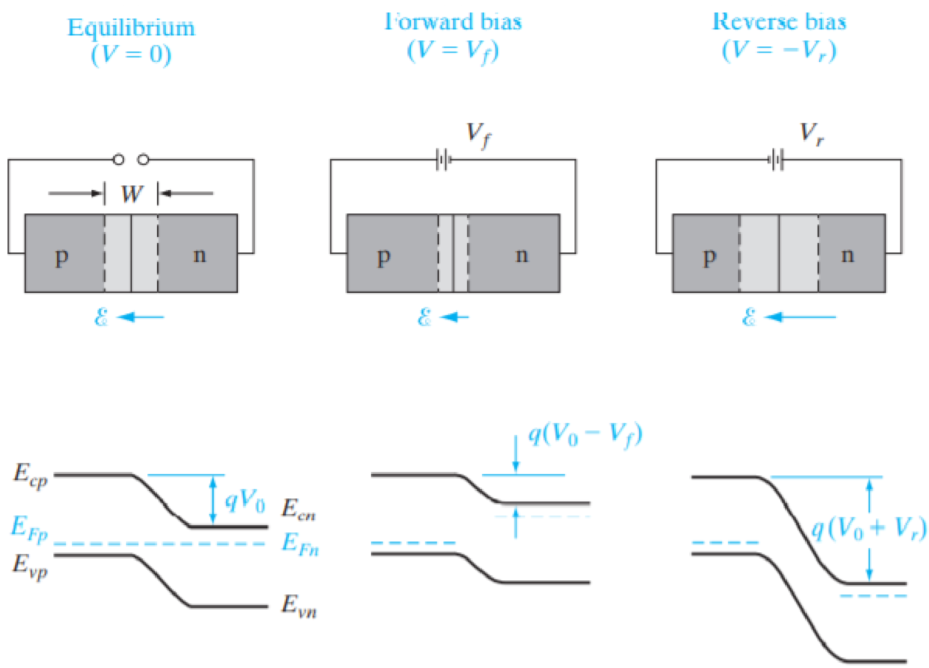


Figure 1: Band structure at equilibrium(left), Forward bias(middle), Reverse bias(right)

constant throughout the diode. But the fermi level is closer to E_p in p-type semiconductor and closer to E_n in the n-type semi conductor. So because of potential drop of V_o across transition region, the energy bands are separated by qV_O.

When forward bias is applied, the potential drop across the junction changes to (V_o-V_f), so the bands are separated by q(V_o-V_f). Similarly in the reverse bias, the potential drop across the junction changes to (V_o+V_r), so the bands are separated by q(V_o+V_r). When the bias is applied, the fermi level breaks down to two quasi fermi levels namely E_{fn} - quasi Fermi level for electrons and E_{fp} - quasi Fermi level for holes.

2.3 Electric field in the device

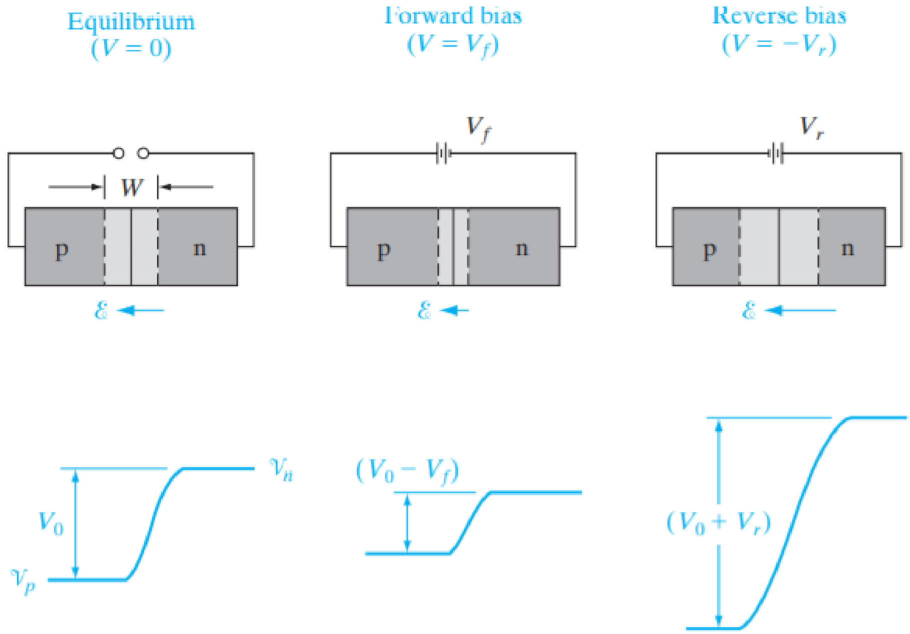


Figure 2: Potential difference at equilibrium(left), Forward bias(middle), Reverse bias(right)

The electric field is defined as the potential drop per distance.

$$E(x) = -\frac{dV(x)}{dx}$$

At equilibrium, the potential is higher at n-side than at p-side, so the direction of field is opposite to the direction of increasing potential, i.e from n-side to p-side, hence is negative. By neglecting the carriers in the depletion region (holes-electrons), from Poisson's equation we get

$$\frac{dE(x)}{dx} = \frac{q}{\epsilon}(p - n + N_d + N_a)$$

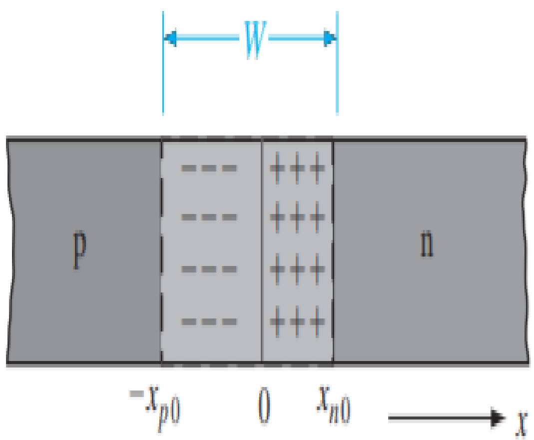
$$\implies \frac{dE(x)}{dx} = \frac{q}{\epsilon}N_d$$

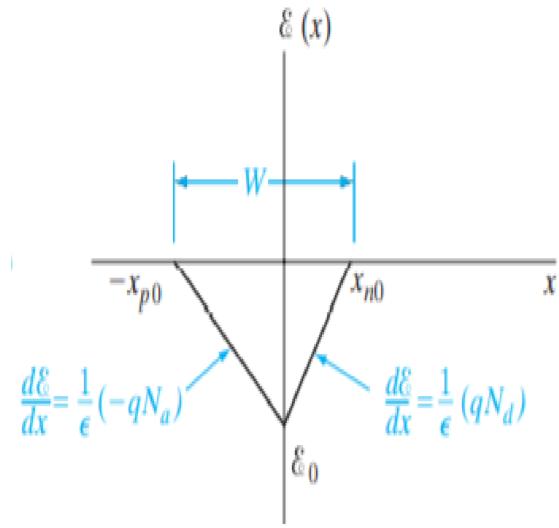
when x is in n-type region.

$$\implies \frac{dE(x)}{dx} = -\frac{q}{\epsilon}N_a$$

when x is in p-type region.

Hence, from the both equations we find that,in magnitude electric field is increasing when moving from the p-type junction edge to a maximum, there by decreasing when moving towards the n-type region as shown.





Hence the maximum magnitude of the field occurs at the junction. On calculating we get,

$$E_o = -\frac{q}{\epsilon}N_d x_{n_o} = -\frac{q}{\epsilon}N_a x_{p_o}$$

Now when bias is applied, the potential drop across the transition region gets changed . Hence, the potential now becomes V_o-V. But at the same time, the width of the depletion layer will also change. The width of depletion region for applied potential V, with doping concentrations N_a, N_d is given by

$$W = \left[\frac{2\epsilon(V_o - V)}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]$$

It can be seen that W decreases for positive V(forward bias), increases for negative V(reverse bias).

As a result, electric field, i.e, the ratio of potential difference per length remains almost unaffected. The maximum magnitude of the field at the junction is same irrespective of the forward bias applied.

2.4 Current-Voltage characteristics

The current in the semiconductor takes place because of the carriers drift and diffusion. The majority carriers in p-type are holes and in n-type are electrons. When the semiconductors are grafted, at equilibrium, the net current must be zero. So the current due to diffusion cancels out current due to drift.

When bias voltage is applied, the diode current is given as

$$I = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)(e^{(qV/kT)} - 1) = I_o(e^{(qV/kT)} - 1)$$

Here V is the voltage bias applied, A is the area of cross-section of the semiconductor,T is temperature,p_n is the hole concentration on the edge of depletion region in the n-side and n_p is the electron concentration on the edge of depletion region in the p-side.

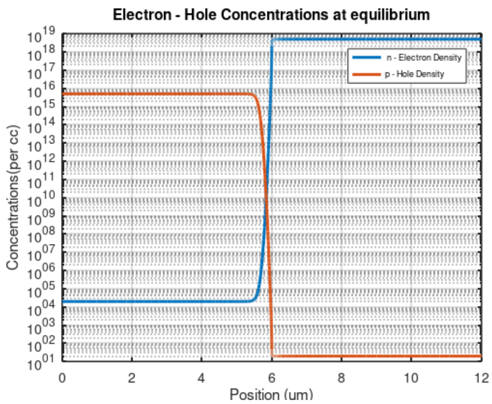
From the above relation, it can be observed that at forward bias, the current is significantly higher. This current is majorly attributed to diffusion. Due to decrease in the potential barrier it makes the carrier easy to diffuse than before.The holes in the p-type diffuse to the n-type and similarly electrons in the n-type diffuse to p-type, thus the sum of two movements giving the observed current. Here, the current increases exponentially with forward bias as the exponential term is much greater than unity (kT/q *approx* 0.0259 at 300K). Though the directions of diffusion are different, because of the charge of carriers, their currents are in the same direction i.e from p to n side.

Similarly in the reverse bias, the diffusion is decreased by factor of $e^{(qV_r/kT)}$, where V_r is reverse bias voltage. The exponential term approaches zero as V_r increases and gives current -I_o, which means direction of current is from n to p. This current rises mostly because of the drift component of field generated minority carriers in depletion region. Once, an electron-hole pair is generated, the field in the depletion region drifts the hole to p-side and electrons to the n-side, rising the net current from n-type to p-type. But this current is quite less in magnitude when compared to the current in forward bias.

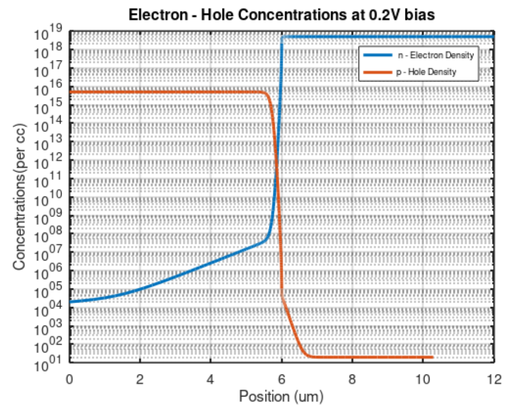
So current flows relatively freely in the forward direction of the diode, but almost no current flows in the reverse direction.

3 Results and discussion

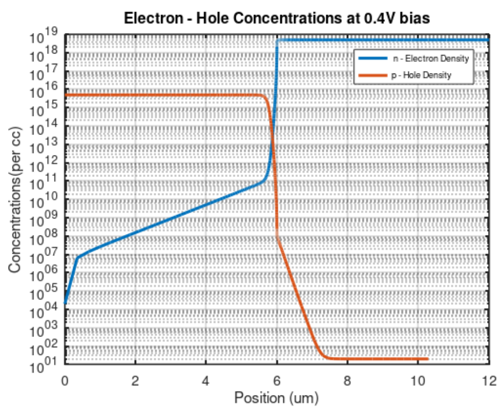
3.1 Electron Hole concentrations



(a) At equilibrium



(b) At V$_a = 0.2V$

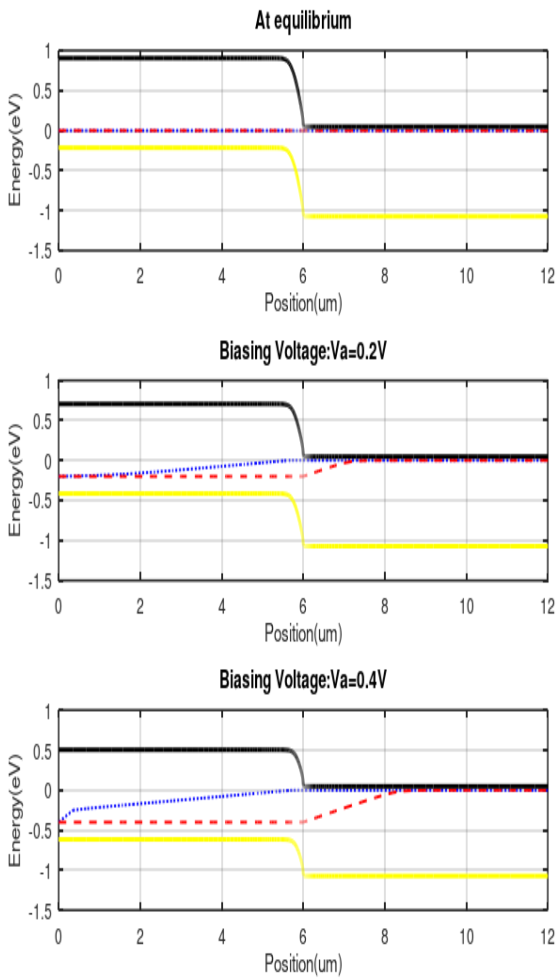


(c) At V$_a = 0.4V$

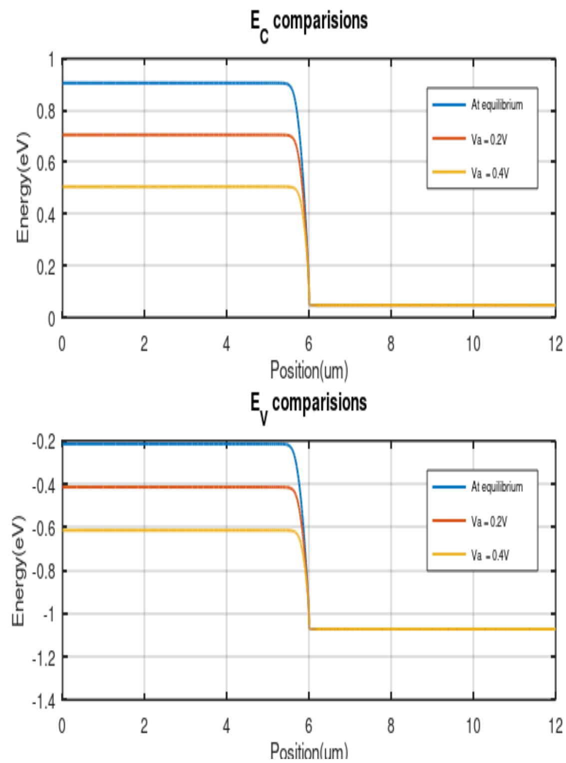
Figure 4: Simulation Outputs

- The majority carrier concentration of a semiconductor does not vary much with bias.
- The minority carrier concentration in each semiconductor of diode increases with increase in biasing voltage .
- The change in concentration nearer to junction is more affected than the farther region.
- Due to more number of electrons in the n-type semiconductor($N_d > N_a$), the increase in minority carriers in p type is greater than increase in minority carriers in n type semiconductor.

3.2 Band Structure



(a) E_c(black),E_v(yellow),E_{fn}(blue),E_{fp}(red)



(b) Comparing E_c and E_v

Figure 5: Simulation outputs

It can be observed that

- The difference between the energy levels of the n-type and p-type is decreasing as the bias voltage increases.
- At equilibrium both the quasi fermi levels overlap as single fermi level where as they breakdown and diverge when bias voltage increases.
- Though the difference between the energy levels vary between the n and p type, the difference between E_c and E_v of a semiconductor does not vary .

3.3 Electric Field inside the device

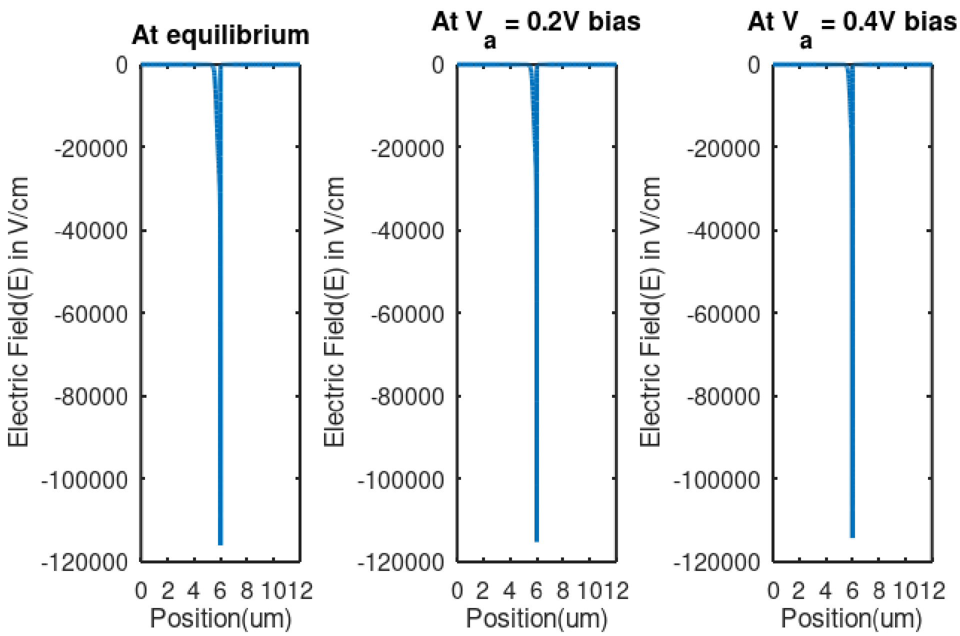


Figure 6: Simulation output

From the graph, we can observe that

- The Electric field variation across the device is almost independent of the forward voltage bias.
- Electric field is always negative.
- The maximum magnitude of the electric field occurs at p-n junction and is a very large constant.
- The electric field is only between the depletion region and is zero everywhere else.

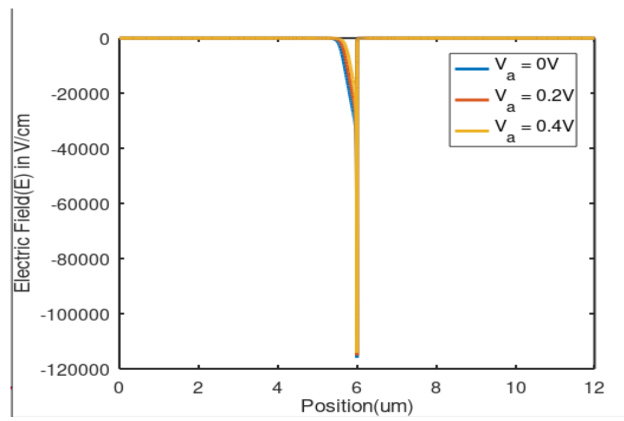
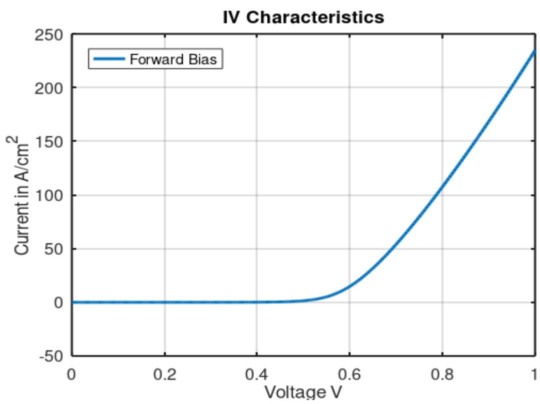
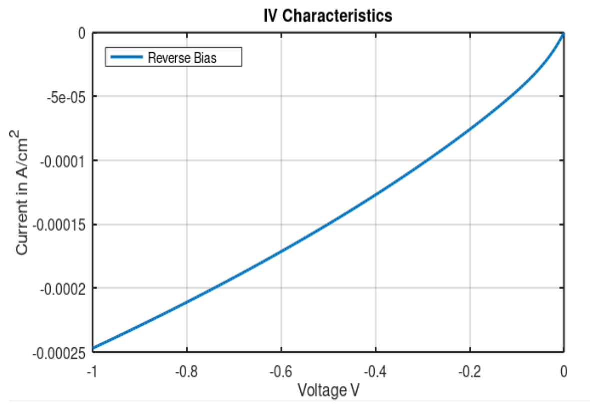


Figure 7: E for different V_a

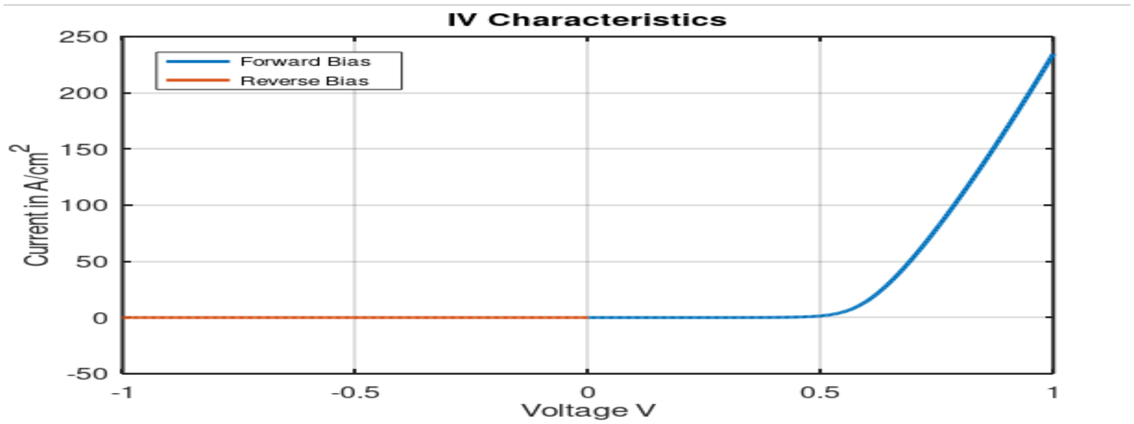
3.4 IV Characteristics



(a) Forward bias Characteristics



(b) Reverse bias characteristics



(c) IV characteristics

Figure 8: Simulation outputs

From the graphs, it is observed that

- The reverse bias current is very small compared to forward bias current which is much higher.
- In the forward bias, the current increases exponentially with increase in bias voltage.
- Even though the magnitude of reverse current is quite less, it increases with increasing reverse bias voltage.
- There is sharp rise in slope of IV characteristics in forward bias around V = 0.6V. The rise is faster thereafter.

4 Conclusions

1. The minority carrier carrier concentration increases in semiconductor of a diode under forward bias because of diffusion. More is the forward bias, more is the diffusion hence more is the minority carrier concentration.

2. The major changes in a diode happen around the junction, the farther ends remain less affected.

3. When bias is applied across the diode, the band structure changes between n-type and p-type. For forward bias the gap between them reduces and for reverse bias the gap between them increases.

4. In forward bias, the potential across transition region is decreased and so is the width of depletion region.Similarly in reverse bias the potential difference across the transition region increases and so is the depletion region. So effectively, the electric field across the diode is unaltered.

5. The electric field is always negative i.e is in the direction of n to p, its maximum magnitude occurs at the junction.

6. The current in diode is majorly due to drift and diffusion.

7. At equilibrium, there is no net current in the diode.

8. In the forward bias, the diffusion current increases and is more dominant. Whereas in the reverse bias the generated electron-holes produce the drift current.

9. Forward bias current significantly much larger than reverse bias current. So, it can be said that the diode allows current flow in forward bias and restricts current flow in reverse bias.