Electronic Devices and Circuits Lab : Report-9

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Contents

1 Aim :

The aim of the experiment was to understand how to implement any logical function by just using NAND and NOR gates.

2 Procedure

Input 1	Input 2	Output 1	Output 2
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 1: Logic Table

In the given logic table, for output-1 is '1' when only one of the inputs is '1' which is logically XOR gates output and for output-2, it is '1' only when both the inputs are '1' which is output of logical AND gate. Together, they implement the logic of Binary Adder where output-1 is the sum and output-2 is the carry.
Now, implementation of XOR and AND gates can be done using solely one of the universal gates, NAND and NOR gates. Here, we study the how to implement it with NOR gates.

2.1 XOR gate implementation using NOR gates

Consider that the inputs are A (input1) and B (input2), C be the output of XOR. Note that A (NOR) B can be written as $\overline{A+B}$ or $\overline{A}.\overline{B}$ as shown.

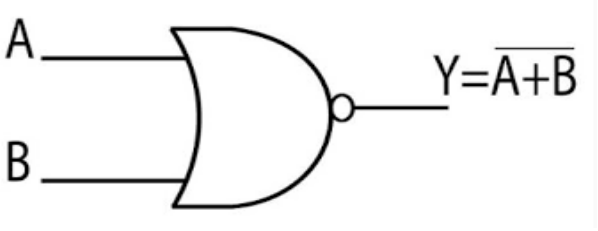

Figure 2: NOR gate

And A (XOR) B is $\overline{A}$.B+A.$\overline{B}$ or (A+B).($\overline{A}$+$\overline{B}$) and is denoted as A$\oplus$B .

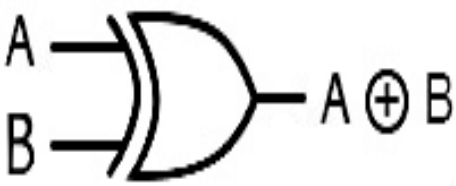

Figure 3: XOR gate

The logic can be implemented as

$$C = A \oplus B = (A+B).(\overline{A}+\overline{B})$$
$$\implies C = (\overline{A}.\overline{B}).(\overline{A.B}) = (\overline{A.B+\overline{A}.\overline{B}}) = (A.B)(NOR)(\overline{A}.\overline{B})$$
$$\implies C = ((\overline{A})(NOR)(\overline{B}))(NOR)(A(NOR)B)$$
$$\implies C = ((A(NOR)A)(NOR)(B(NOR)B))(NOR)(A(NOR)B)$$

So, effectively we need 5 NOR gates to implement a XOR gate.

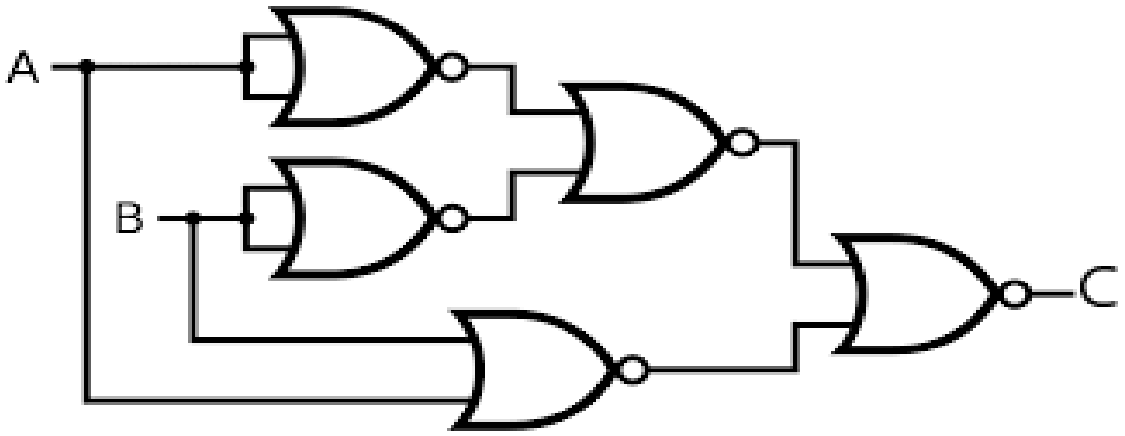

Figure 4: Circuit of XOR gate implemented using NOR gates

2.2 AND gate implementation using NOR gates

Consider that the inputs are A (input1) and B (input2), C be the output of AND gate . As we know that

$$C = A.B = \overline{\overline{A} + \overline{B}}$$

$$C = \overline{A}(NOR)\overline{B}$$

$$\implies C = (A(NOR)A)(NOR)(B(NOR)B)$$

So we effectively need 3 NOR gates to implement the operation of a AND gate.

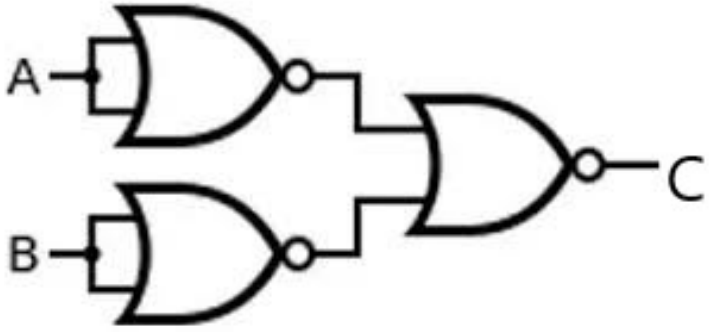

Figure 5: Circuit of AND gate implemented using NOR gates

3 Results And Observations

3.1 XOR gate

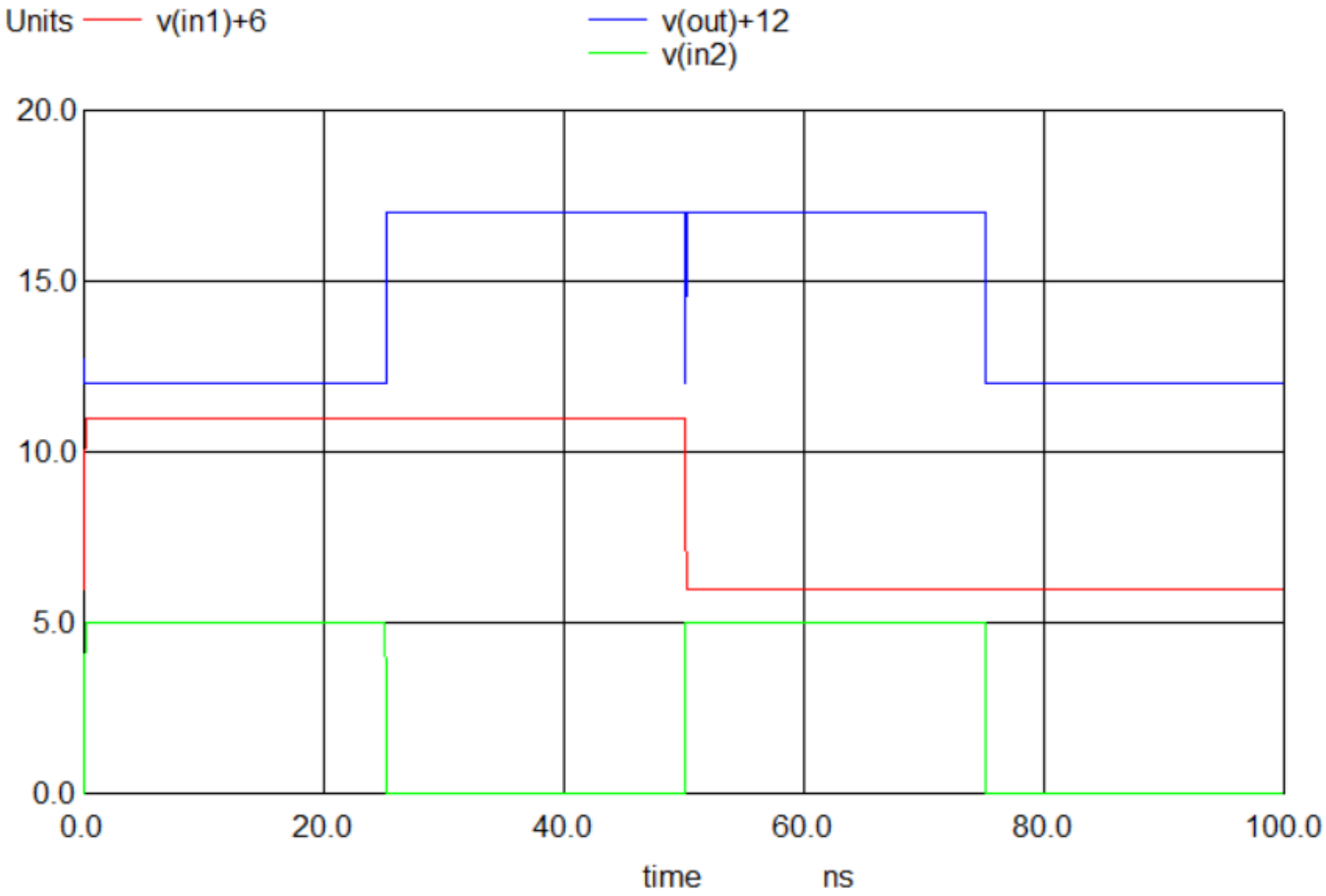

Figure 6: Simulation of output for XOR using NOR

Observations

1. The output is high only when only one of the input is high.
2. There is a small spike which occurs because of the finite rise and fall time of the input pulses.

3.2 AND gate

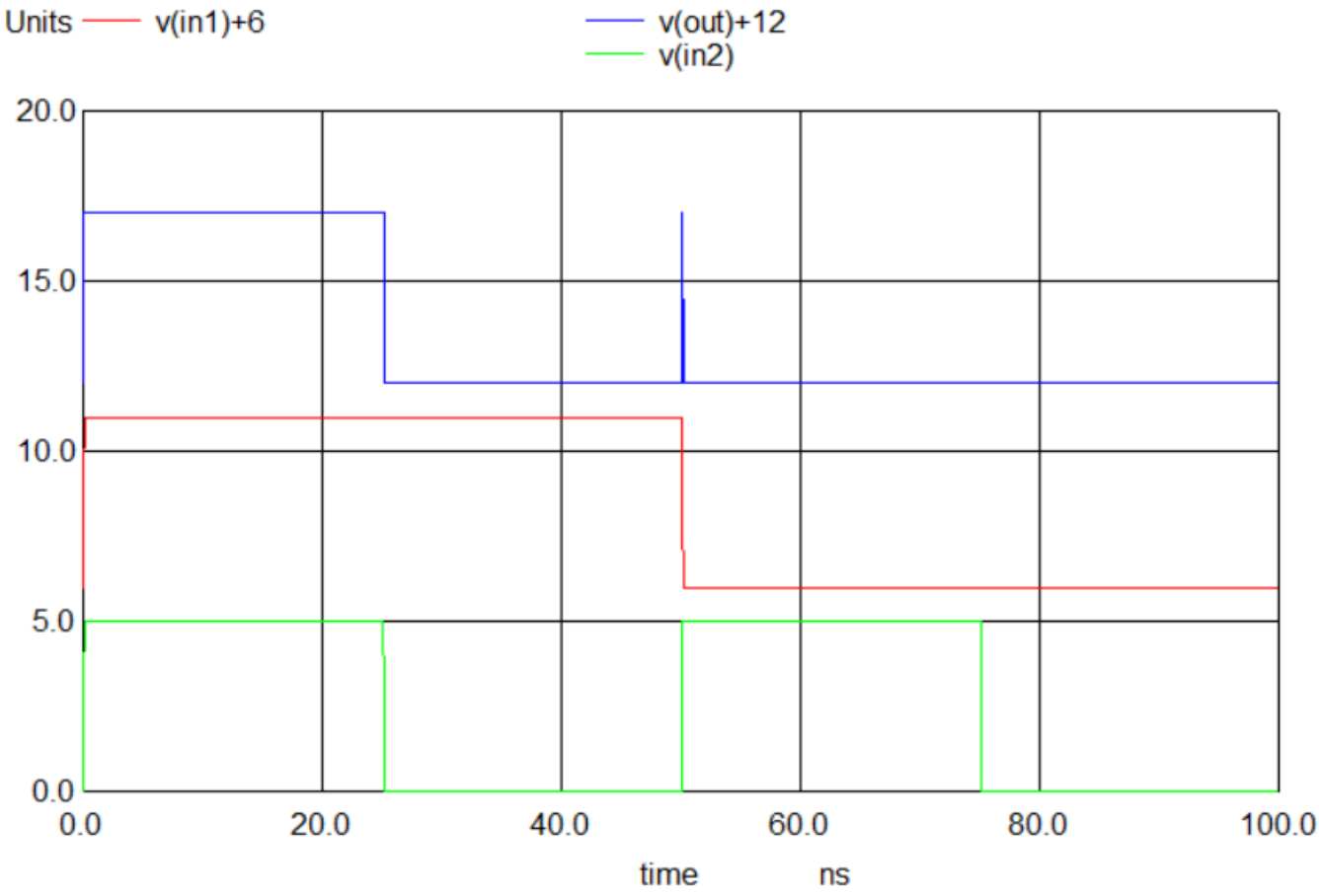

Figure 7: Simulation of output for AND using NOR

Observations

1. The output is high only when both the inputs are high.
2. There is a small spike which occurs because of the finite rise and fall time of the input pulses.

4 Conclusion

Any logical function can be implemented solely using NOR gates, hence signifying it as an universal gate.