VLSI Design
Assignment-3

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EE19BTECH11040

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1 SRAM Operation

1.1 Implementation

The circuit diagram used for simulation is

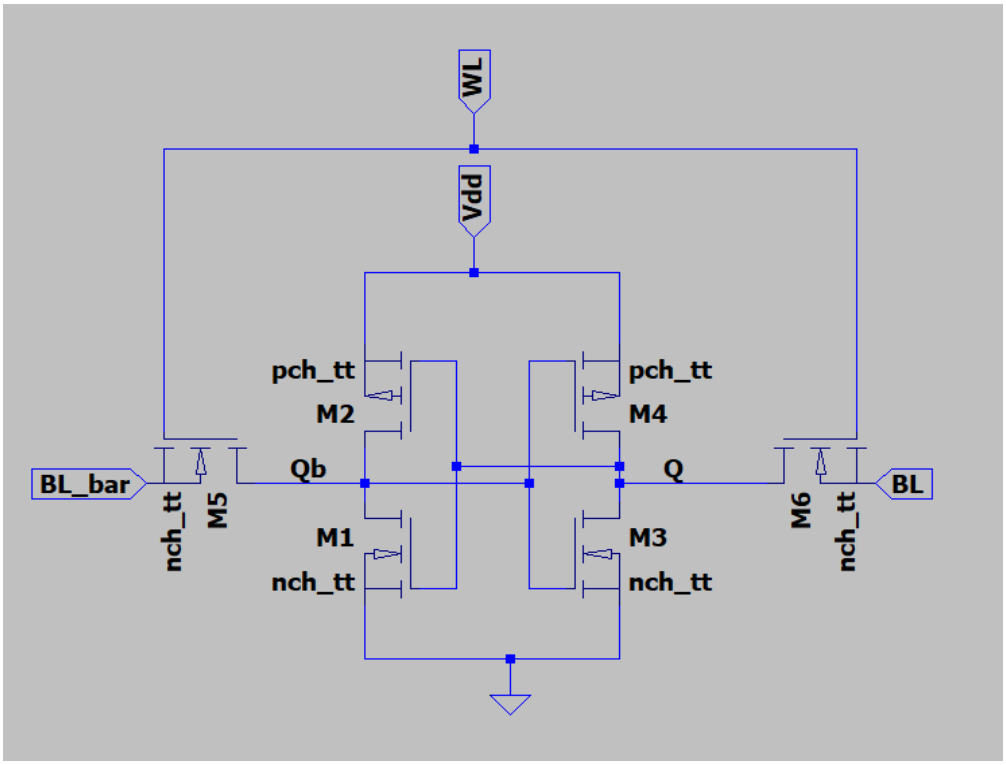


Figure 1: Circuit Diagram of SRAM cell with proper scaling

Netlist :

```
M1 Qb Q 0 0 nch_tt W=720n,L=180n
M3 Q Qb 0 0 nch_tt W=720n,L=180n
M2 Qb Q Vdd Vdd pch_tt W=270n,L=270n
M4 Q Qb Vdd Vdd pch_tt W=270n,L=270n
M5 Qb WL BL_bar BL_bar nch_tt W=360n,L=180n
M6 Q WL BL BL nch_tt W=360n,L=180n
V1 Vdd 0 1.8
V2 WL 0 PULSE(0 1.8 0 1f 1f 10 10 1)
.model NMOS NMOS
.model PMOS PMOS
.lib LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.backanno
.end
```

The sizing for MOSFETs is done as given : Pull down transistors M1 and M3 are of size $8/2\lambda$ i.e, (720 nm,90 nm), pull up transistor M2 and M4 are of size $3/3\lambda$ i.e, (270 nm, 270 nm) and access transistors M5 and M6b are of size $4/2\lambda$ i.e, (360 nm, 180n nm).

1.2 Read Operation

For read operation, we set the bitlines to floating 1 (i.e, 1.8V) and turn ON the write lines. The corresponding lines (along with parameter for measuring delay) are to be added to the netlist :

```
.ic V(Q)=0 V(Qb)=1.8 V(BL)=1.8 V(BL_bar)=1.8
.tran 100p
.meas TRAN Td FIND time WHEN V(bl)=0.9
```

Here we are trying to read bit zero from Q into the bitline BL.
The output turns out to be as shown :

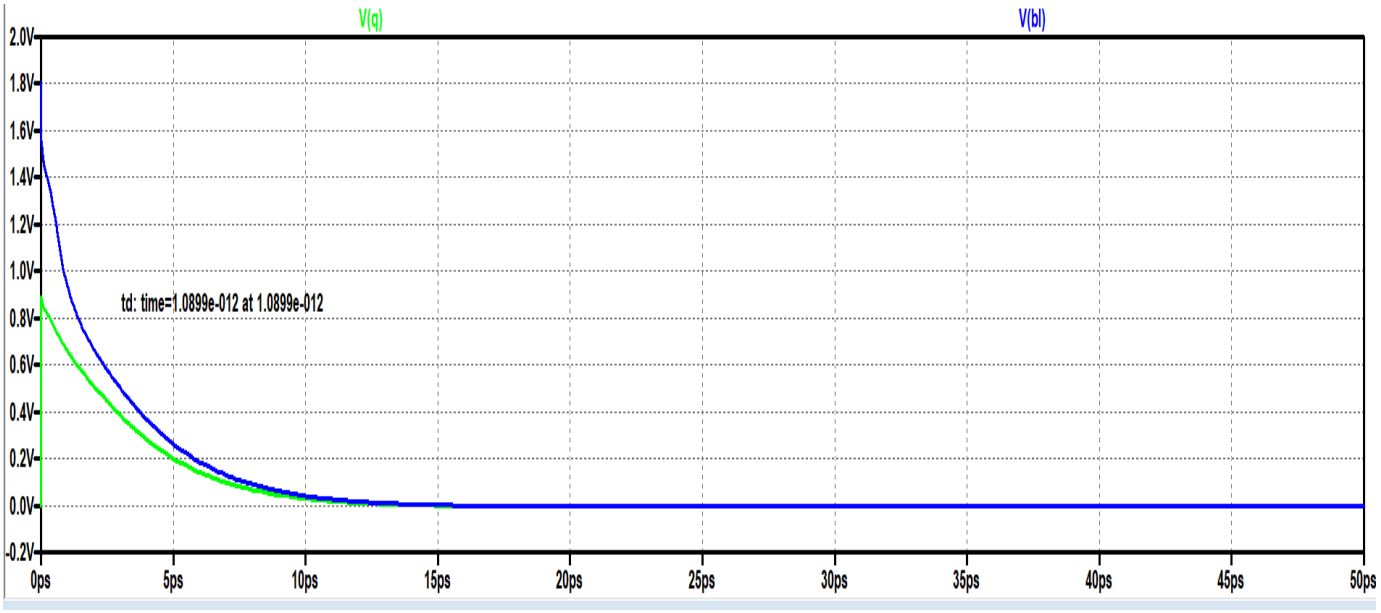


Figure 2: Read Operation result

Hence when the WL is enabled BL will switch to zero.The delay or t_{pHL} turns out to be around 1.09ps.

1.3 Write operation

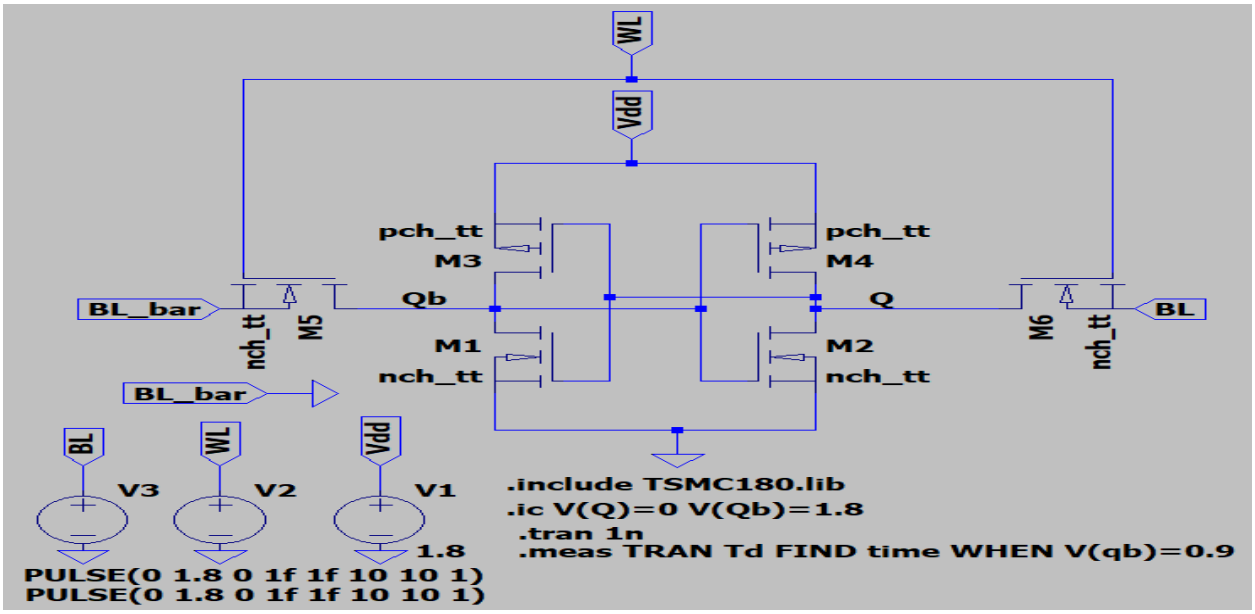


Figure 3: Circuit for simulating Write operation in a SRAM cell

Netlist :

```
M1 Qb Q 0 0 nch_tt W=720n,L=180n
M2 Q Qb 0 0 nch_tt W=720n,L=180n
M3 Qb Q Vdd Vdd pch_tt W=270n,L=270n
M4 Q Qb Vdd Vdd pch_tt W=270n,L=270n
M5 Qb WL 0 0 nch_tt W=360n,L=180n
M6 Q WL BL BL nch_tt W=360n,L=180n
V1 Vdd 0 1.8
V2 WL 0 PULSE(0 1.8 0 1f 1f 10 10 1)
V3 BL 0 PULSE(0 1.8 0 1f 1f 10 10 1)
.model NMOS NMOS
.model PMOS PMOS
.lib LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.ic V(Q)=0 V(Qb)=1.8
.tran 1n
.meas TRAN Td FIND time WHEN V(qb)=0.9
.end
```

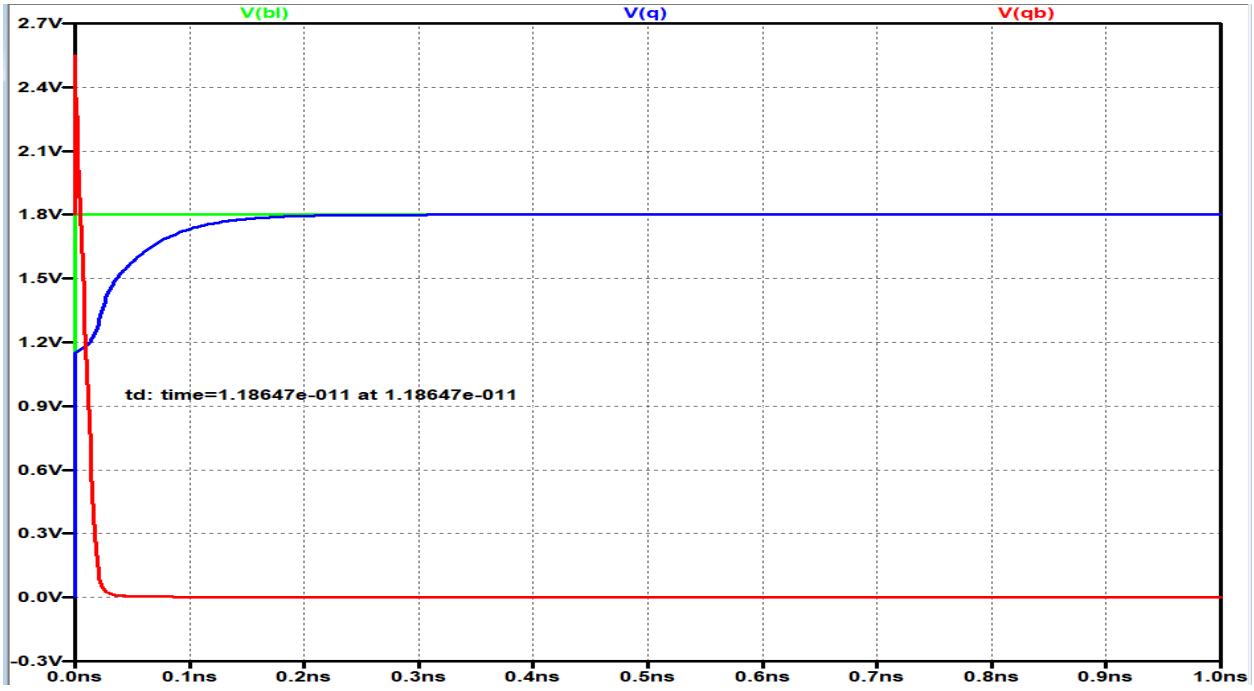


Figure 4: Write Operation result

Hence when WL is enabled Q will be overwritten from 0 to 1. The delay (t_{pLH}) turns out to be 11.86 ps.

1.4 Max Operating Frequency Range

The delays for read and write turns out to be 1.09 ps and 11.86 ps, so to accommodate both of the delays, the driving signal should not change between these delay gaps. Hence

$$f_{max} = \frac{1}{max(t_{read}, t_{write})} = 1/t_{write}$$

$$f_{max} = 84.3GHz$$

2 Impact of Sizing on Performance

The design for designing an inverter of required V_M=V_{dd}/2, we find that (W/L) for PMOS is 1000nm/180nm and for NMOS is 180nm/180nm. The circuit and the resulting VTC are as shown,

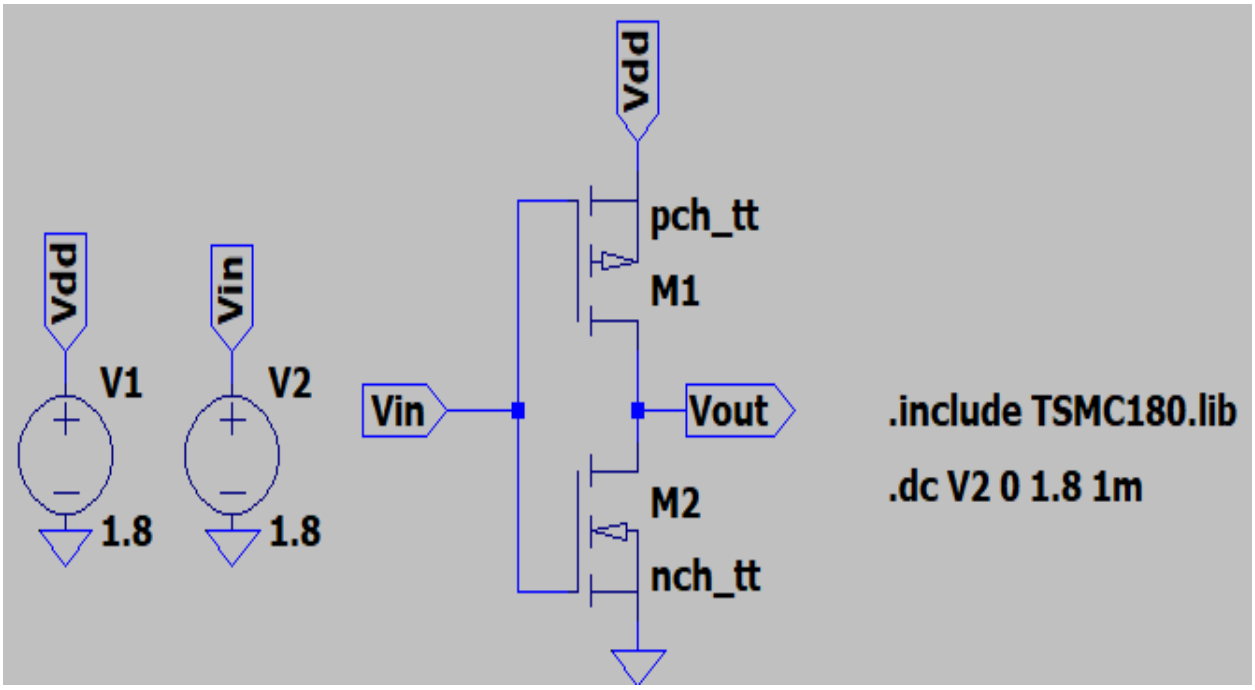


Figure 5: Circuit Diagram for Inverter

Netlist

```
V1 Vdd 0 1.8
M1 Vout Vin Vdd Vdd pch_tt W=1u, L= 0.18u
M2 Vout Vin 0 0 nch_tt W=180n, L=180n
V2 Vin 0 1.8
.model NMOS NMOS
.model PMOS PMOS
.lib LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.dc V2 0 1.8 1m
.backanno
.end
```

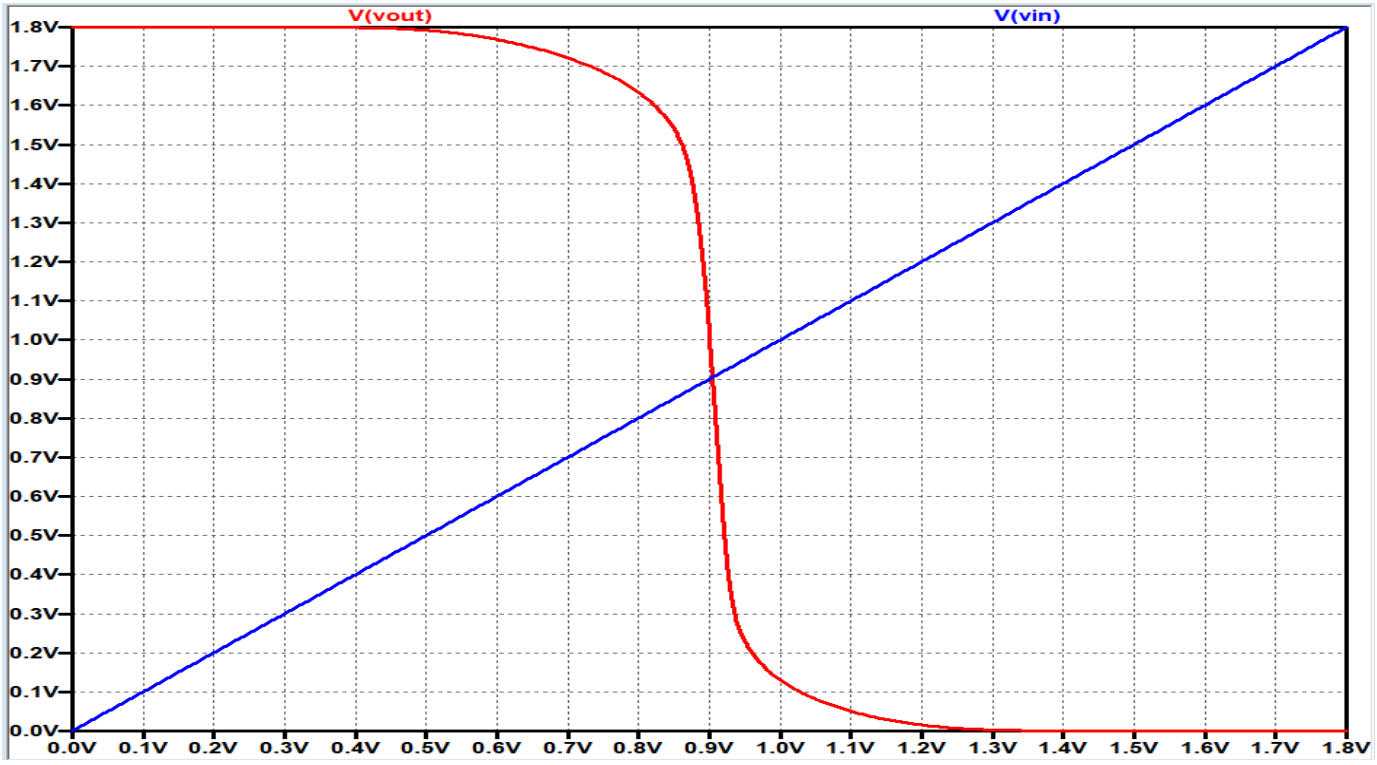


Figure 6: VTC for the designed inverter

2.1 Impact of Scaling Inverter (both NMOS and PMOS)

2.1.1 Without Load

Netlist Used :

```
V1 Vdd 0 1.8
M1 Vout Vin Vdd Vdd pch_tt W={x}, L= 0.18u
M2 Vout Vin 0 0 nch_tt W={y}, L=180n
V2 Vin 0 PULSE(0 1.8 0 0 0 10n 20n 5)
.model NMOS NMOS
.model PMOS PMOS
.lib LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
.dc V2 0 1.8 1m
;tran 50n
.meas TRAN t1 V(Vout) when V(Vout) = {0.9} fall=1
.meas TRAN t2 V(Vout) when V(Vout) = {1.8} fall=1
.meas TRAN tphl PARAM (t1-t2)
.step param i 1 5 1
.param x=table(i, 1,1u, 2,2u, 3,3u, 4,4u, 5,5u )
.param y=table(i, 1,180n, 2,360n, 3,540n, 4,720n, 5,900n )
.meas TRAN t3 V(Vout) when V(Vout) = {0.9} rise=2
.meas TRAN t4 V(Vout) when V(Vout) = {0.0001} rise=2
.meas TRAN tplh PARAM (t3-t4)
.meas TRAN tp PARAM (tplh+tphl)/2
.backanno
.end
```

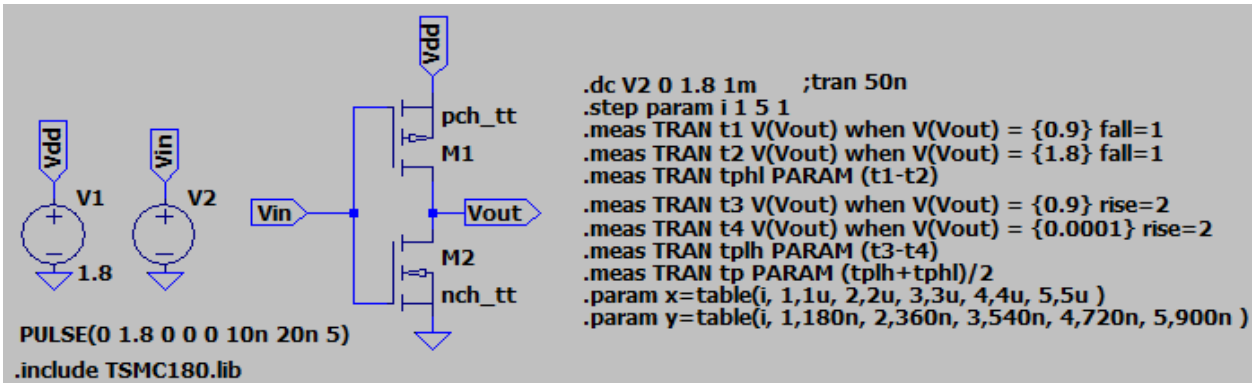


Figure 7: Circuit Diagram

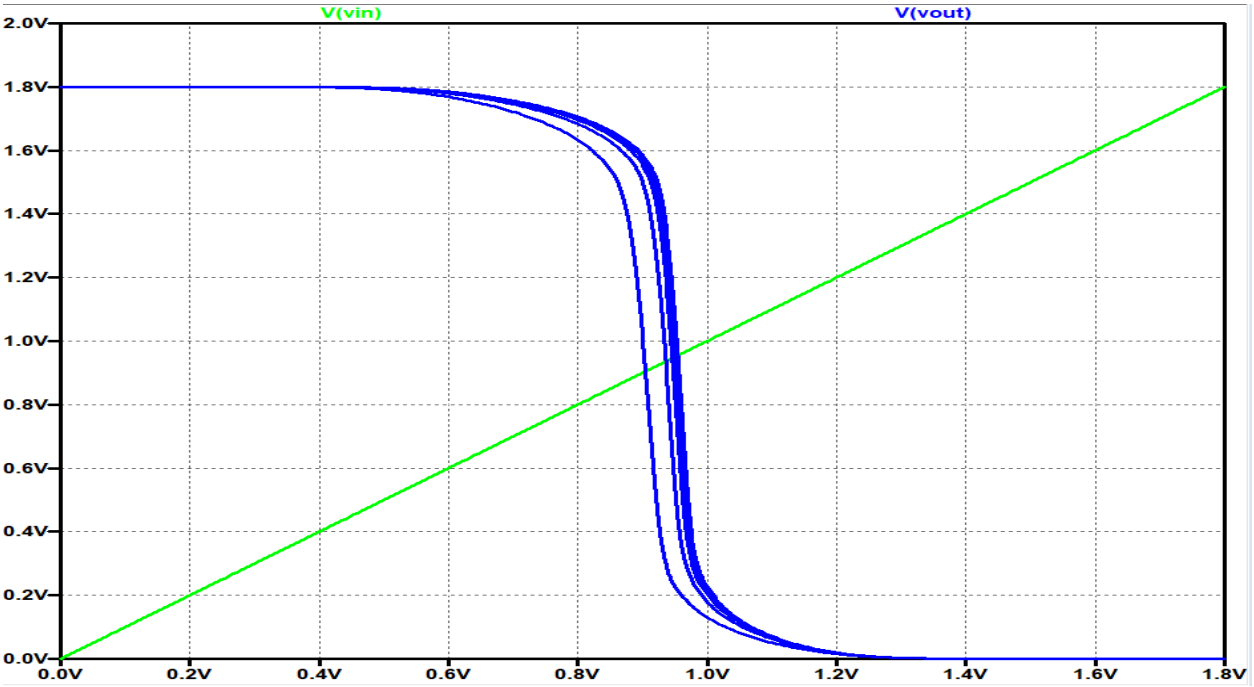


Figure 8: VTC variation for different scales

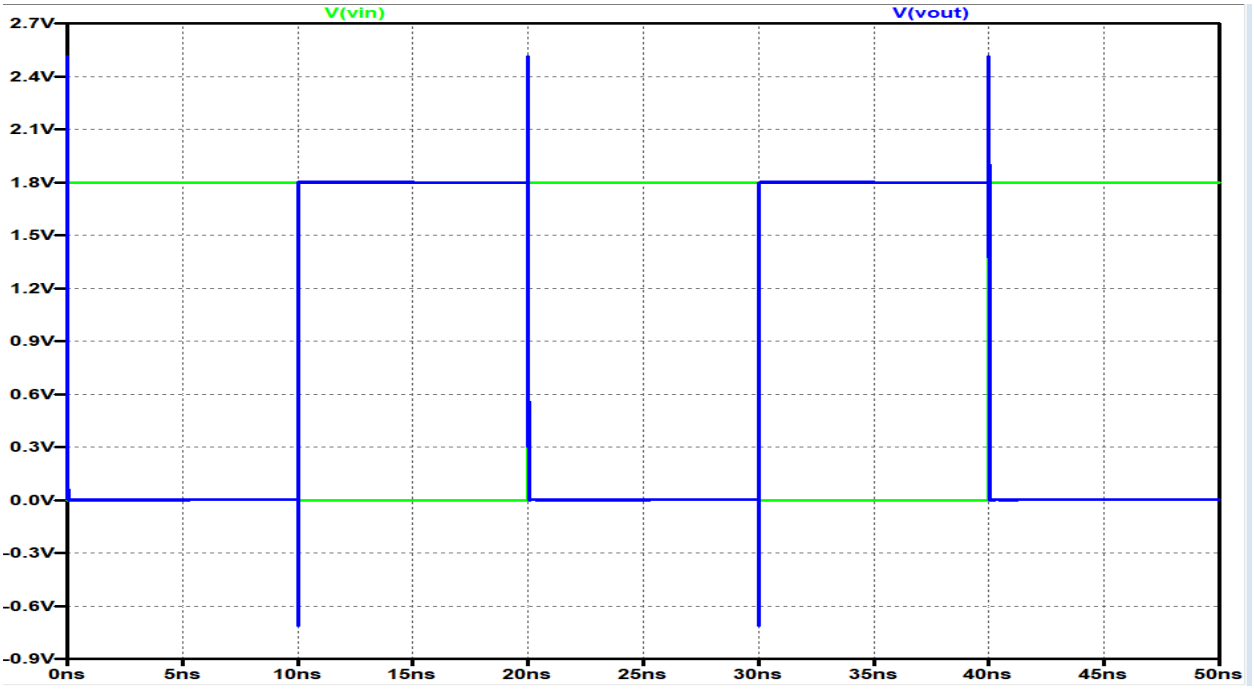


Figure 9: Transient Simulation

The propagation delay (tp) determines the performance of the inverter, the lower the delay better is its performance. And it is estimated as

$$t_P = \frac{t_{pLH} + t_{pHL}}{2}$$

For various scaling factors we get the variation in propagation delay as:

Scaling Factor	Propagation Delay(t_p in ps)
1	4.21
2	4.85
3	5.07
4	5.318
5	5.317

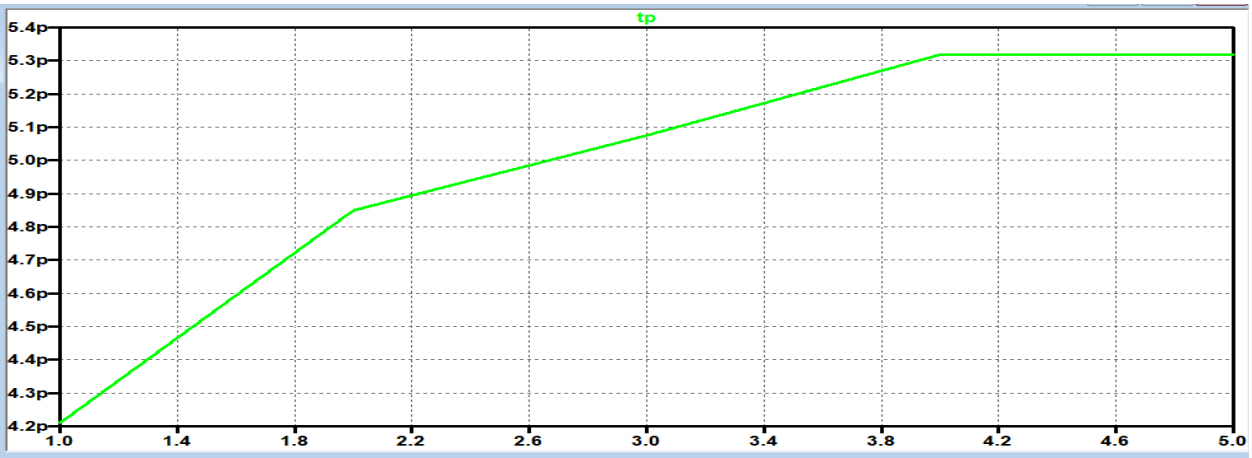


Figure 10: t_p variation with S

As seen that the variation is not very strong as the driving capacitance is just intrinsic capacitance. The slight increase in delay can be attributed to the effective increase of capacitance over the decreasing resistance, as both gate and drain amplify the affect of increasing capacitance.For this slight change in overall RC, the charging and discharging time periods does not vary significantly.

2.1.2 With load of $C_L = 20$ pF

Netlist

```
V1 Vdd 0 1.8
M1 Vout Vin Vdd Vdd pch_tt W={x}, L= 0.18u
M2 Vout Vin 0 0 nch_tt W={y}, L=180n
V2 Vin 0 PULSE(0 1.8 0 1p 1p 10u 20u 5)
C1 Vout 0 20p
.model NMOS NMOS
.model PMOS PMOS
.lib LTspiceXVII\lib\cmp\standard.mos
.include TSMC180.lib
;.dc V2 0 1.8 1m
.tran 50u
.meas TRAN t1 V(Vout) when V(Vout) = {0.9} fall=1
.meas TRAN t2 V(Vout) when V(Vout) = {1.8} fall=1
.meas TRAN tphl PARAM (t1-t2)
.step param i 1 5 1
.param x=table(i, 1,1u, 2,2u, 3,3u, 4,4u, 5,5u )
.param y=table(i, 1,180n, 2,360n, 3,540n, 4,720n, 5,900n )
.meas TRAN t3 V(Vout) when V(Vout) = {0.9} rise=2
.meas TRAN t4 V(Vout) when V(Vout) = {0.01} rise=2
.meas TRAN tplh PARAM (t3-t4)
.meas TRAN tp PARAM (tplh+tphl)/2
.backanno
.end
```

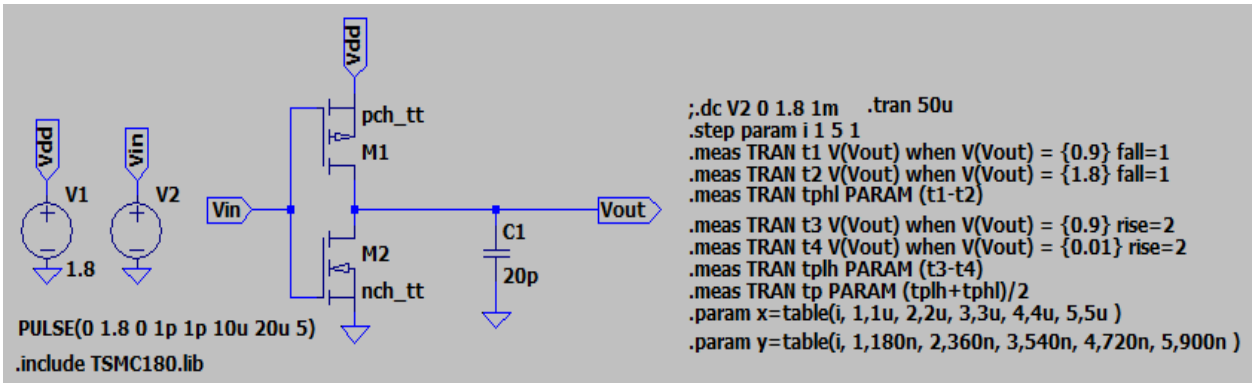


Figure 11: Circuit Diagram

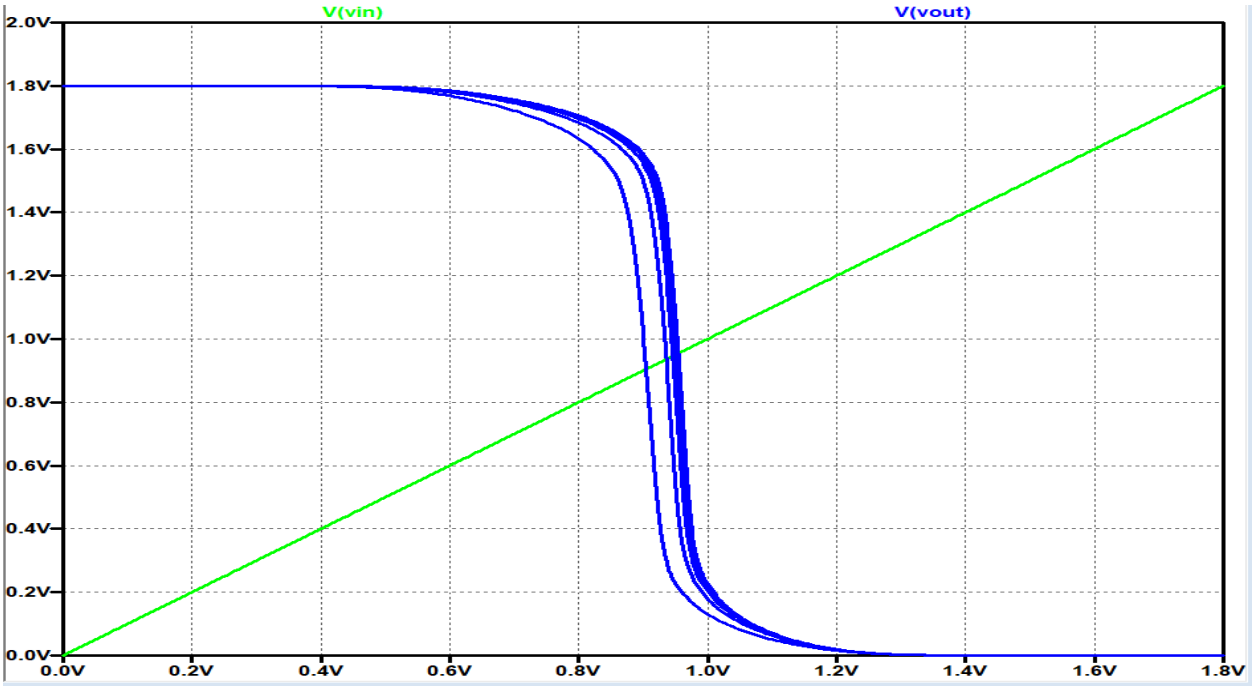


Figure 12: VTC variation for different scales

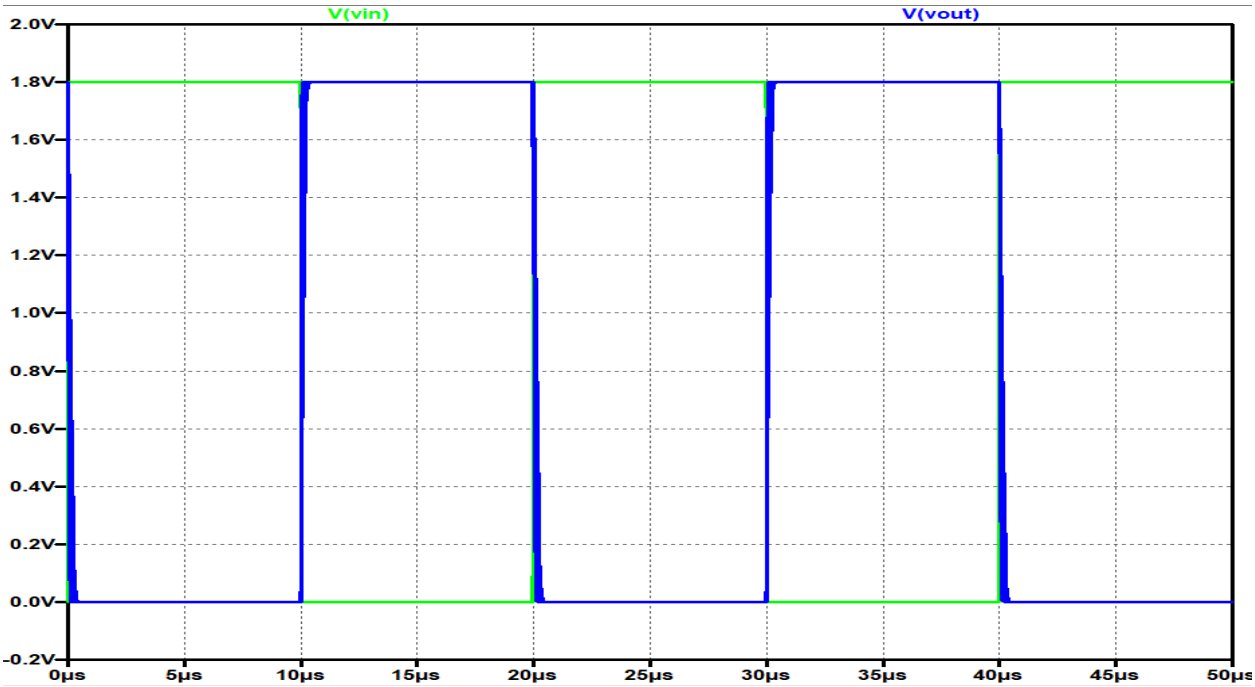


Figure 13: Transient Simulation

Note that the time duration of the pulse here is different from that compared to the earlier case as the time for charging and discharging would be higher for loading capacitor.

For various scaling factors we get the variation in propagation delay as:

Scaling Factor	Propagation Delay(t_p in ns)
1	97.01
2	58.17
3	40.80
4	31.75
5	26.03

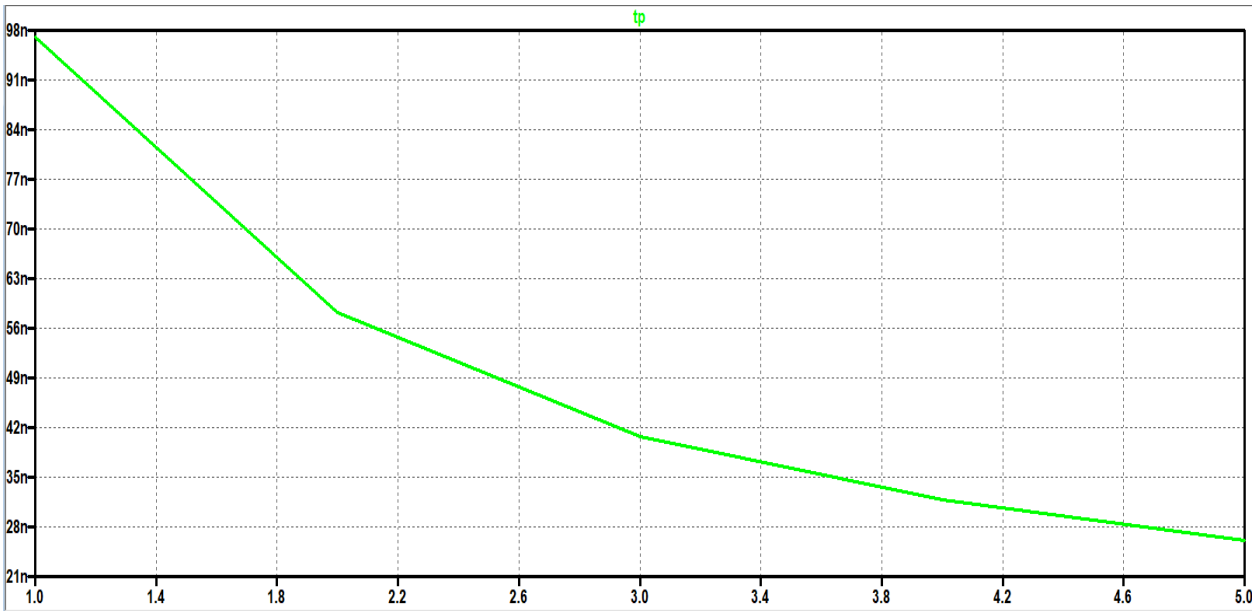


Figure 14: t_p variation with S

From the graphs and tables result, we observe that the delay reduces drastically with increase in the scaling of inverter size. This can be reasoned as, the delay (t_{pLH} and t_{pHL}) are generally driven by the RC product. In this case, increasing the inverter size decreases the resistance (R/S), but the capacitance remains dominantly constant to the load value (C_L). As a result, the propagation delay decreases in totality.

2.2 Impact of changing W_p or W_n on t_{pHL} and t_{pLH}

We use the same inverter used above with load of 20pF, and vary the W_p and W_n to study the affects of them on the propagation delay.

First case, lets observe the affect of variation of W_p by scaling it while keeping other parameters constant.

Scaling Factor	t_{pLH}	t_{pHL}	t_p
1	77.84 ns	116.18 ns	97.01 ns
2	41.07 ns	116.34 ns	78.71 ns
3	27.70 ns	116.27 ns	71.98 ns
4	20.89 ns	116.31 ns	68.60 ns
5	16.60 ns	116.35 ns	66.48 ns

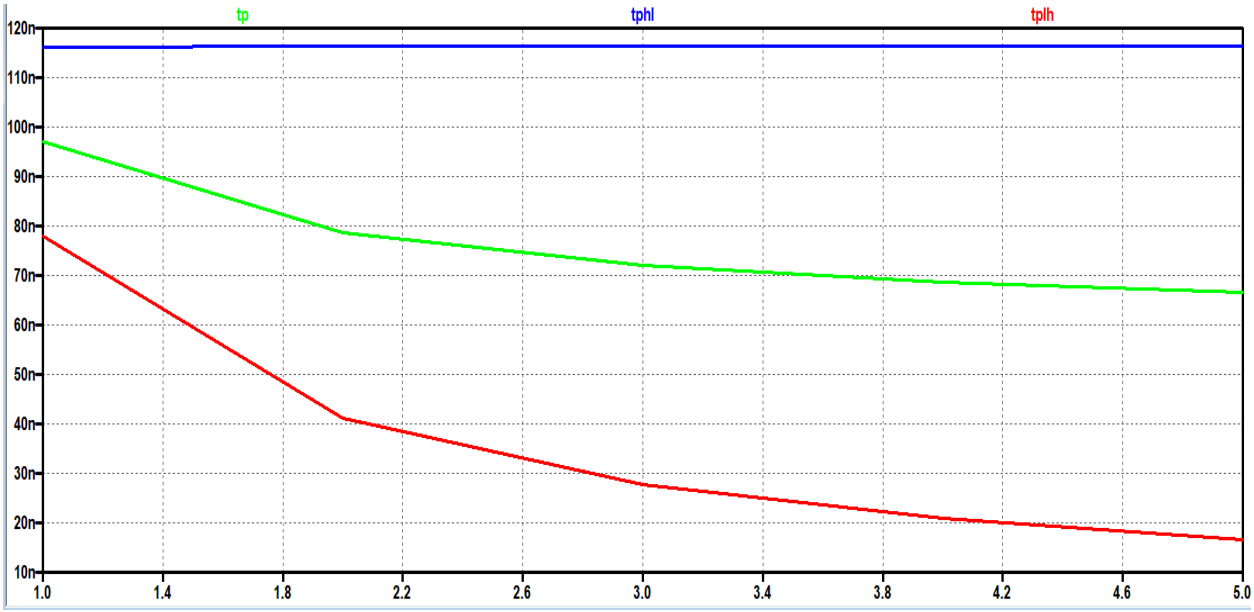


Figure 15: Propagation delays variation with S for PMOS

From the graph and tables it is evident that scaling the PMOS has effect on t_{pLH} and does not affect much the t_{pHL} value, hence directly reflecting on the overall t_p varying with t_{pLH}. This can be explained as the effect of increasing W_p decreases the R_{eq} of PMOS, hence affecting the low to high transition which handled by pull up PMOS. As the R_{eq} decreases the cap charging would be faster resulting smaller delays.

Now, lets observe the affect of variation of W_n by scaling it while keeping other parameters constant.

Scaling Factor	t_{pLH}	t_{pHL}	t_p
1	77.84 ns	116.18 ns	97.01 ns
2	77.84 ns	74.74 ns	76.29 ns
3	77.84 ns	55.32 ns	66.58 ns
4	77.84 ns	42.18 ns	60.01 ns
5	77.84 ns	34.66 ns	56.25 ns

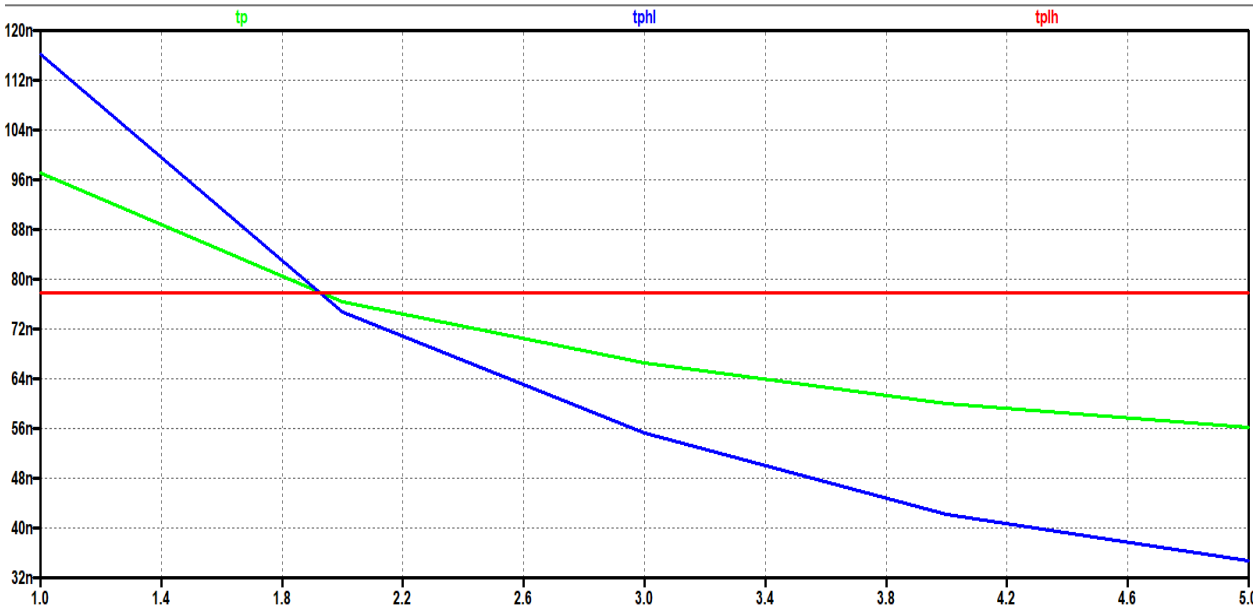
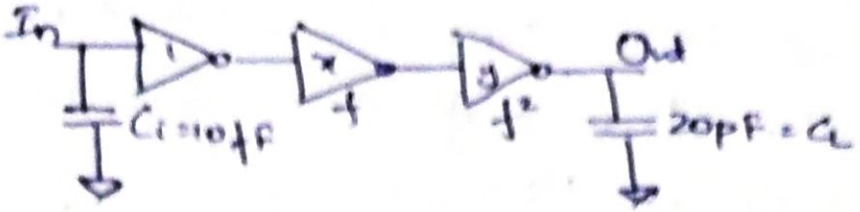


Figure 16: Propagation delays variation with S for NMOS

From the graph and tables it is evident that scaling the NMOS has effect on t_{pHL} and does not affect much the t_{pLH} value, hence directly reflecting on the overall t_p varying with t_{pHL}. This can be explained as the effect of increasing W_n decreases the R_{eq} of NMOS, hence affecting the high to low transition which handled by pull down NMOS. As the R_{eq} decreases the cap discharging would be faster resulting smaller delays.

3) Sizing of Inverters:



$t_{p_0} = 70ps$

Net Fanout (F) = $\frac{C_L}{C_i} = \frac{20p}{10f} = 2 \times 10^3$

a) For minimum propagation delay with the given chain of 3 inverters, happens to be when the capacitances scale up in geometric ~~ratio~~ progression with ratio f, so the scaling would be

$$\Rightarrow f^3 = \frac{C_L}{C_i} = F \Rightarrow f = F^{1/3} = 12.6$$

Then the propagation delay (t_p) = $3 \times t_{p_0}\left(H + \frac{f}{\gamma}\right)$

Assuming $\gamma = 1$, $t_p = 3 \times t_{p_0}(1+f)$

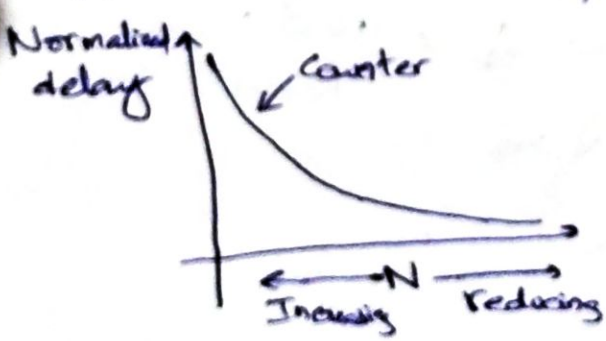
$= 3 \times 70p \times 13.6$

$= 2856ps = 2.856ns$

b) For optimum delay, $f = 3.6$ for $\gamma = 1$. Then the number of stages required would be

$$f = F^{1/N} \Rightarrow N = \frac{\ln F}{\ln f} = \frac{\ln(2000)}{\ln(3.6)} = 5.9338$$

And we know that, $t_{p_{min}} = N t_{p_0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)$



At N = 5,

$t_{p,min} = 5 \times 70p\left(1 + \sqrt[5]{2000}\right)$

$= 1950.5678ps$

At N = 6,

$t_{p,min} = 1910.8053ps$

Hence we see that at N = 6, we get least propogation delay

So by chaining additionally 4 inverter with min sized inverter gives up optimum result. But for functionality of inverter N must be odd, then N = 5 can be chosen.

c) (i) The advantage in (b) is that the delay is low, so faster is the system than compared to that in (a).

ii) The effective fanout for each inverter has also reduced in (b) than (a).

iii) But the disadvantage comes in the form of space on the chip as more area & material is required, which also increases the power consumption.

d) The dynamic power consumption of an inverter is given as

$$P_{dyn} = C \times V_{dd} \times \Delta V_d \times f_0$$ where f_0 = freq

Here for chain of inverters, considering contribution of only capacitance of gates ($\gamma = 0$), $C_g = C_i$

$$P_{dyn} = \sum_{K=0}^{N} C_g V_{dd}^2 f_0 \cdot f^K \quad ; f \text{ is effective fanout}$$

$$= C_g V_{dd}^2 f_0 \sum_{K=0}^{N} f^K$$

$$= 10 \times 10^{-15} \times (2.5)^2 \times f_0 \times \frac{f^{N+1} - 1}{f - 1}$$

For $N = 3$, $P_{dyn} = 10^{-14} \times (2.5)^2 f_0 \times \frac{(2.6)^4 - 1}{2.6 - 1}$

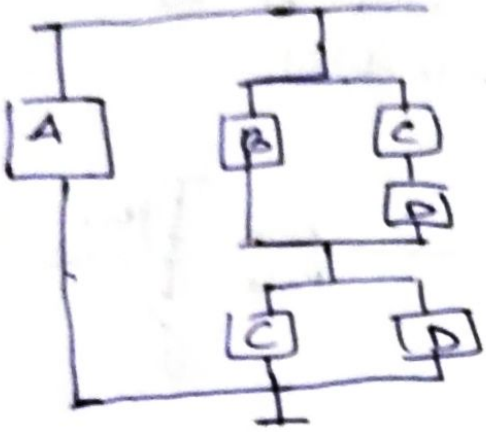
$$= 135.8 f_0 pW$$

$$= \frac{135.8}{T} pW \qquad T = 1/f_0$$

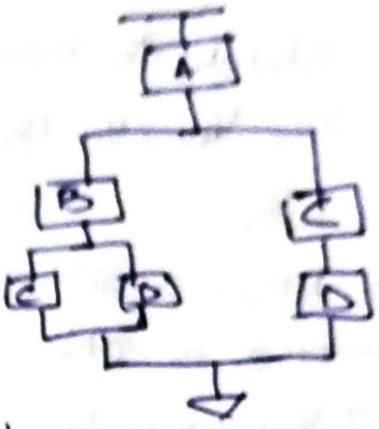
4) Given Logic:

$$f(A,B,C,D) = \overline{A(BC+CD)+CD}$$

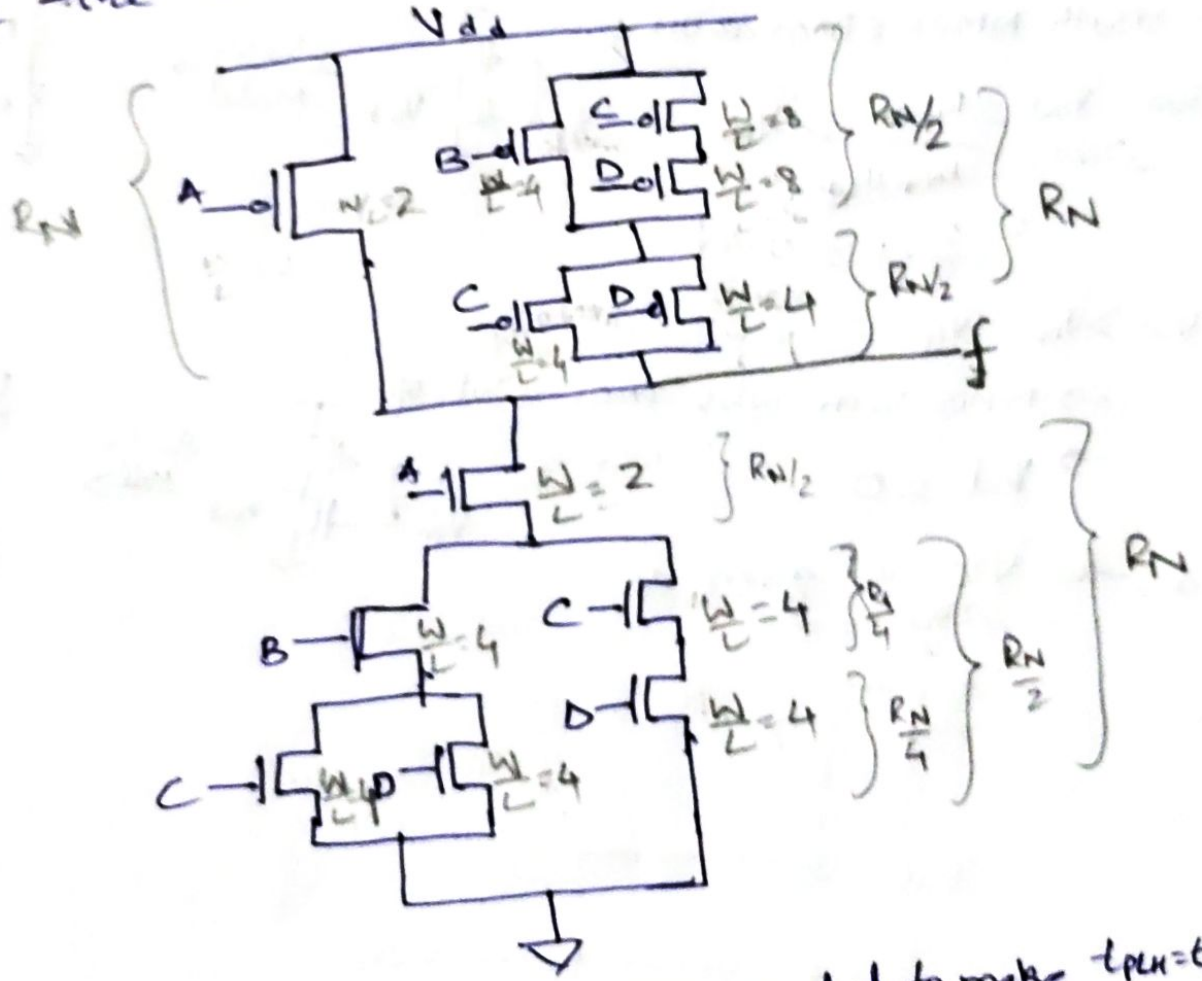
The pull up network is:



The pull down network is



Hence the circuit would be (with sizing)



Assume $R_P = 2R_N$, the PMOS & NMOS are scaled to make $t_{PLH} = t_{PHL} = t_p$ where t_p is the inverter delay (unit). This ensures the best performance.

5) Given for a particular technology, the parameters

$V_{Tn} = 0.2V$ $|V_{Tp}| = 0.3V$ $R_n = 2k\Omega \times 1\mu m$

$R_p = 3k\Omega \times 1\mu m$

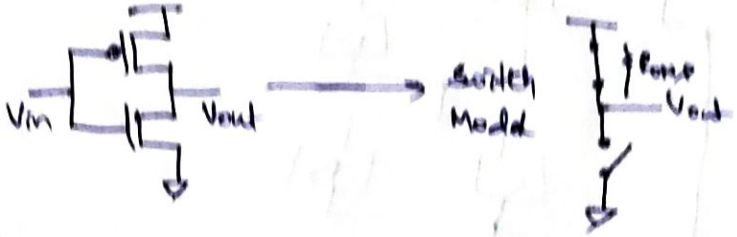
At $V_{DD} = 1V$, $W_p = W_n = 1\mu m$, so $R_n = 2k\Omega$ $R_p = 3k\Omega$. For the VTC sketch, the main turn out points would be at $V_{in} = 0V$, V_{Tn}, $V_{DD} - |V_{Tp}|$, V_{DD}. Lets look in detail:

i) $V_{in} < V_{Tn}$:

→ NMOS is OFF

→ PMOS is ON

→ $V_{out} = V_{dd} = 1V$



ii) $V_{Tn} < V_{in} < V_{DD} - V_{Tp}$

→ Both NMOS & PMOS are ON :

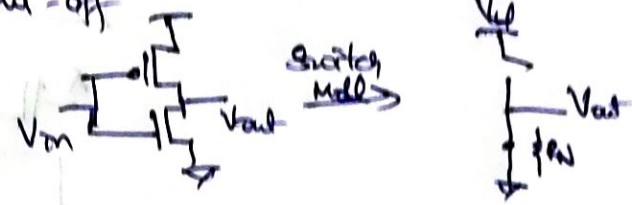
Then $V_{out} = \frac{R_{N,ON}}{R_{N,ON} + R_{P,ON}} \times V_{DD}$

$= \frac{2}{5} \times 1 = 0.4V$

iii) $V_{in} > V_{DD} - |V_{Tp}|$:

→ NMOS is ON while PMOS is cut-off

→ $V_{out} = 0$



Hence, the VTC is given as: