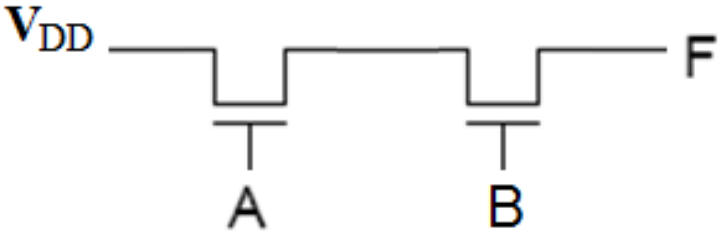
Pass Transistor and Transmission Gate Logic

Building Logic Circuits

- In designing digital systems in MOS technology there are 2 basic ways of building logic circuits:
  - Switch Logic
    - Pass Transistor Logic
    - Transmission Gate Logic
  - Gate (Restoring) Logic

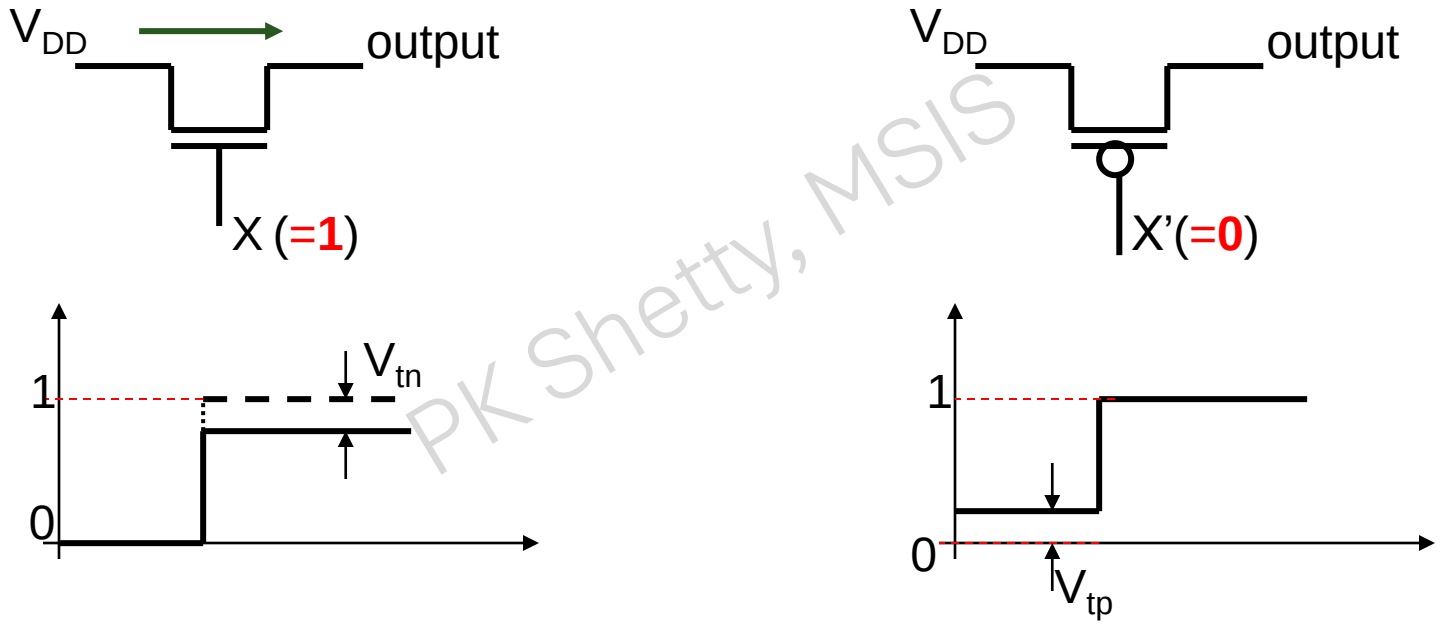
Pass Transistor Logic



- Approach is faster for smaller arrays
- The path through each switch is isolated from the signal activating the switch
- **N** transistors instead of **2N**
- No static power consumption
- Ratioless
- Bidirectional (versus unidirectional)

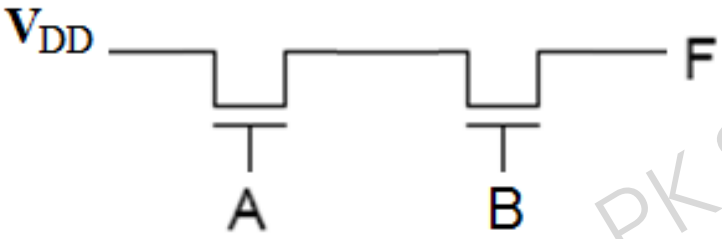
Pass Transistor - Drawbacks

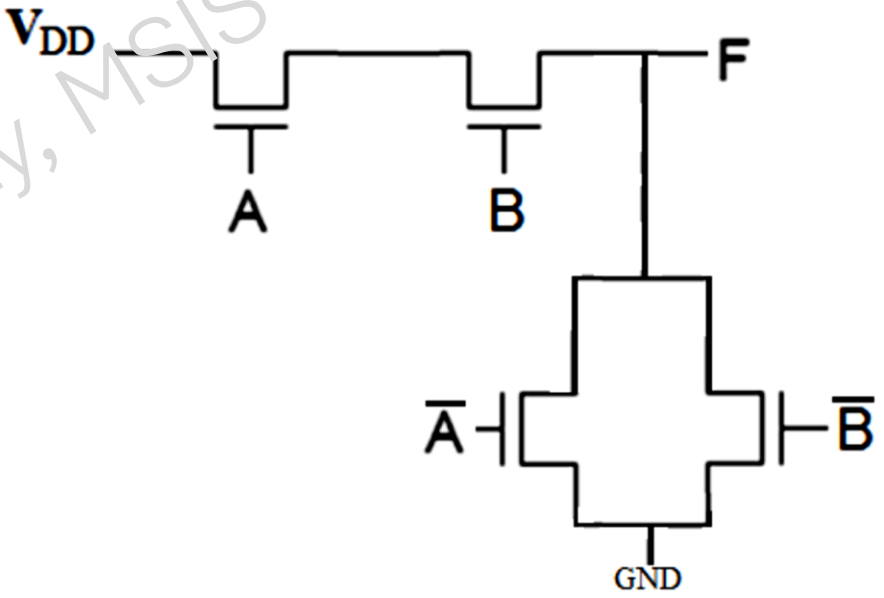
- Undesirable threshold voltage effects which give rise to the loss of logic levels (Logic level degradation)



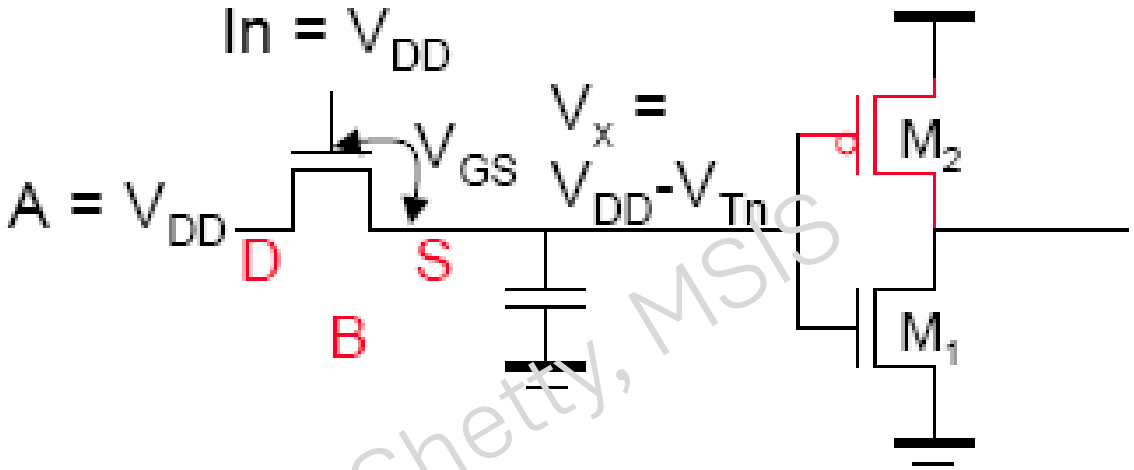
- Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)

- Problem of floating output



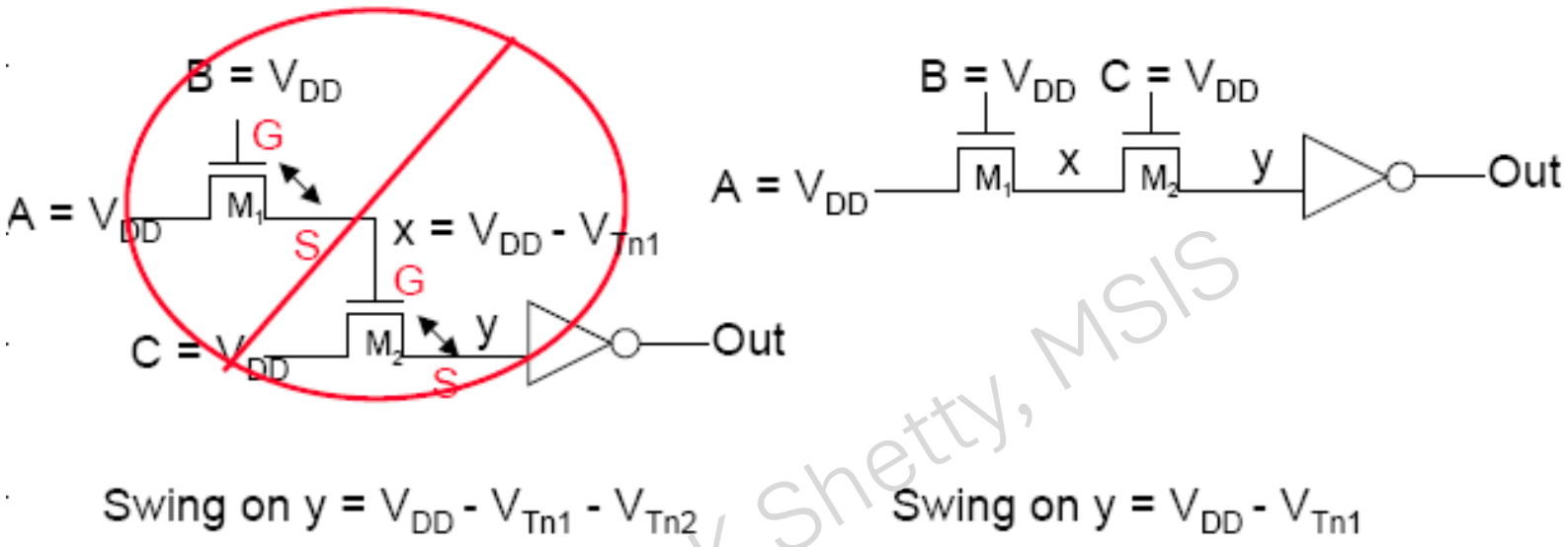


NMOS Only PT Driving an Inverter



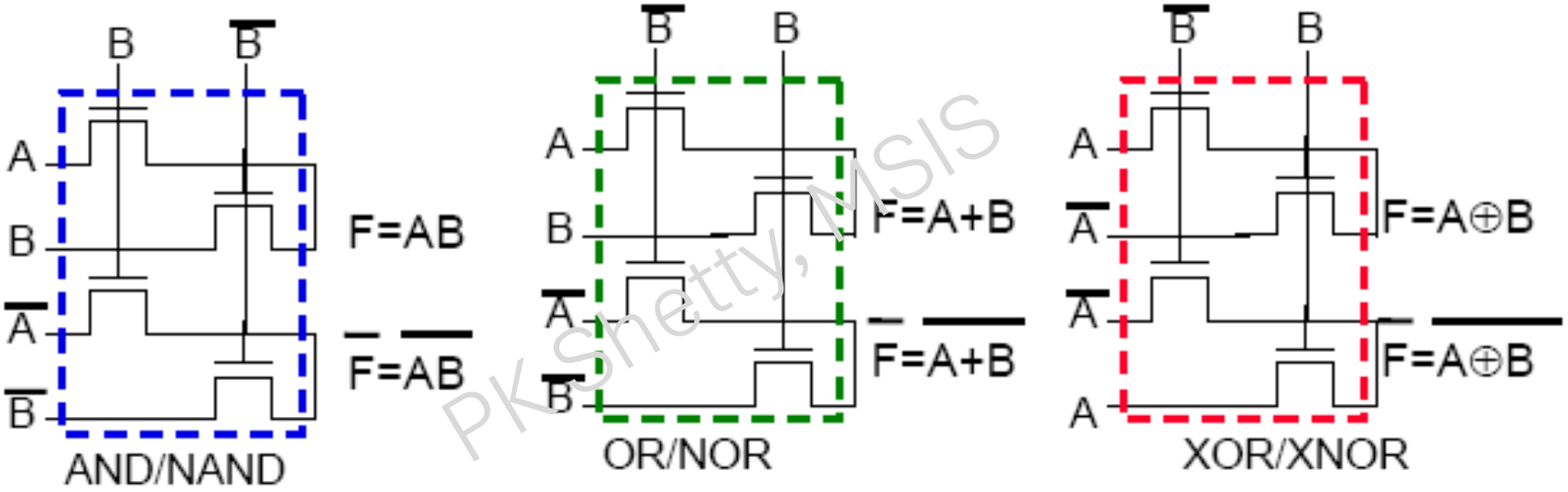
- V_x does not pull up to V_{DD}, but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power consumption (M_2 may be weakly conducting forming a path from V_{DD} to GND)
- Notice V_{Tn} increase of pass transistor due to body effect (V_{SB})

Cascaded NMOS Only PTs



- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins

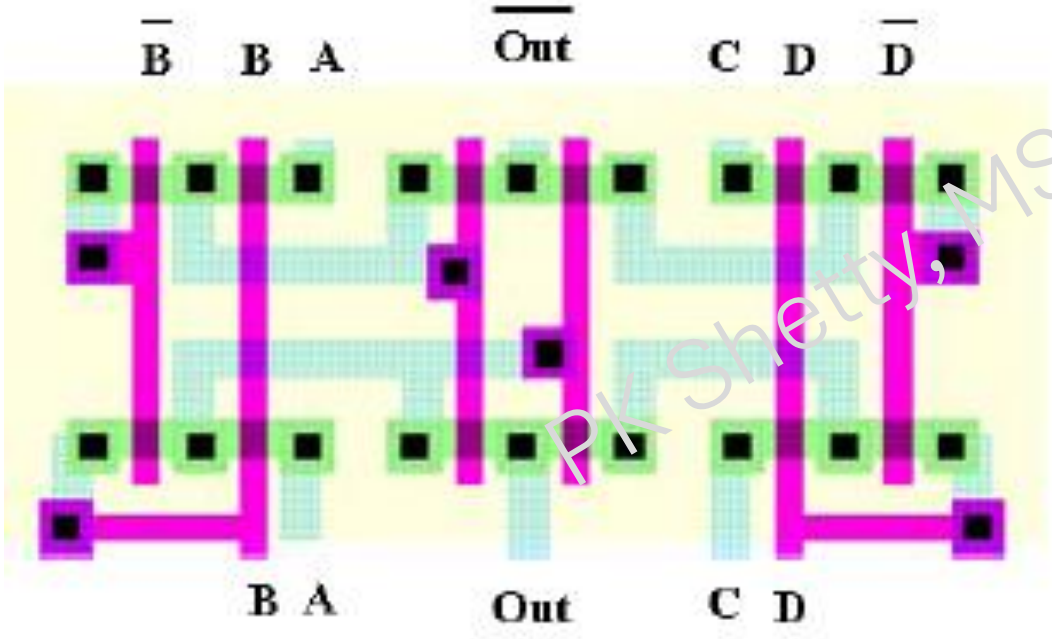
Complementary PT Logic (CPL)

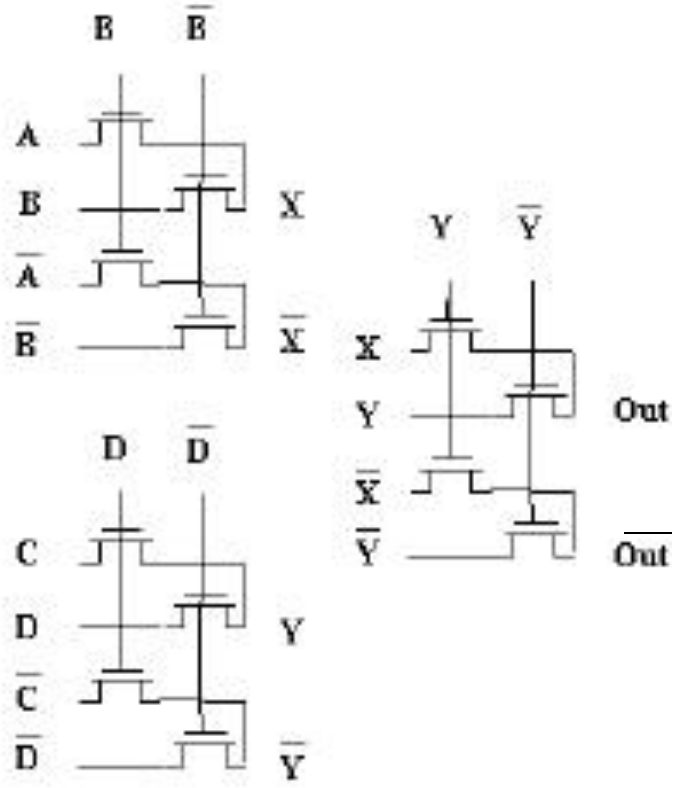


CPL Properties

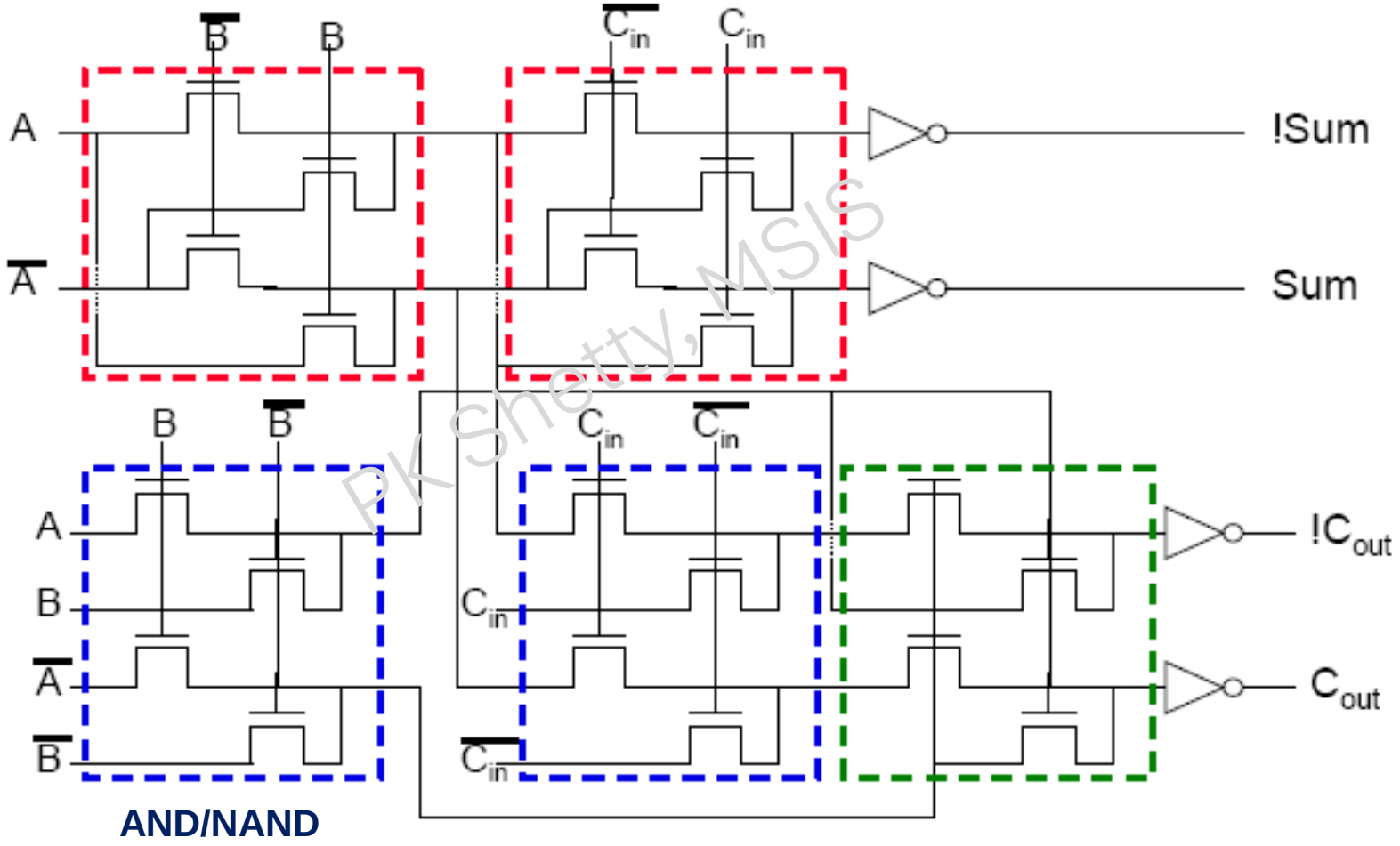
- Differential; so complementary data inputs and outputs are always available (so don't need extra inverters)
- Still static, since the output defining nodes are always tied to V_{DD} or GND through a low resistance path
- Design is modular; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like adders
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems

4-input NAND in CPL



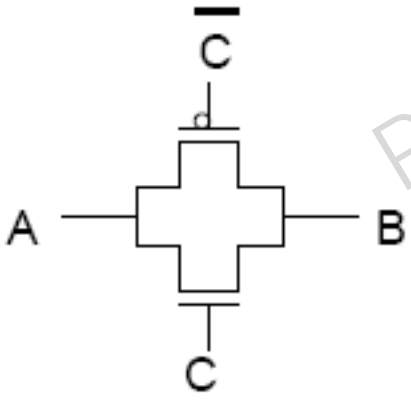


CPL Full Adder

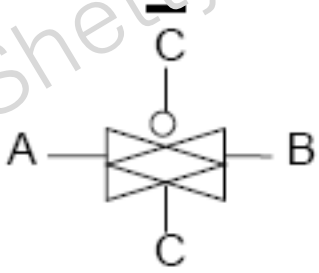


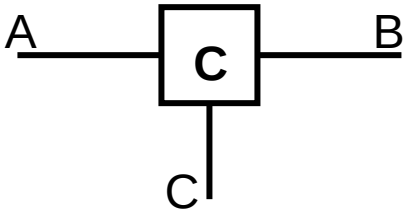
Transmission Gate (TG) Logic

- The degradation of logic levels in simple n or p switches can be overcome by using transmission gates, comprising an n-pass and p-pass transistors in parallel.
- Also called as Complementary switch or C-Switch



Transmission Gate



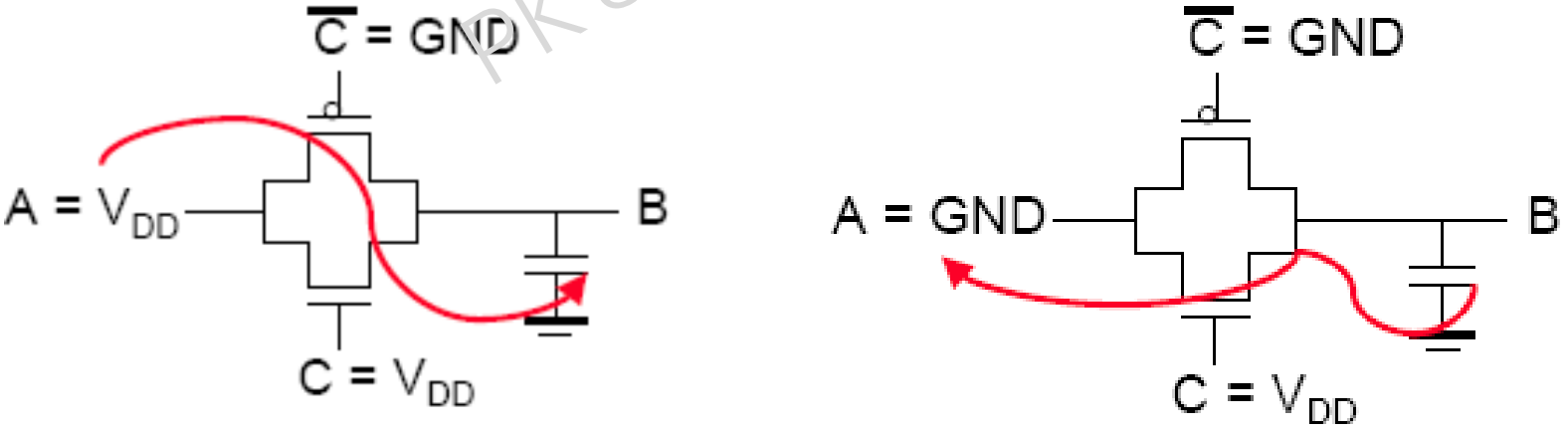


Symbols Used

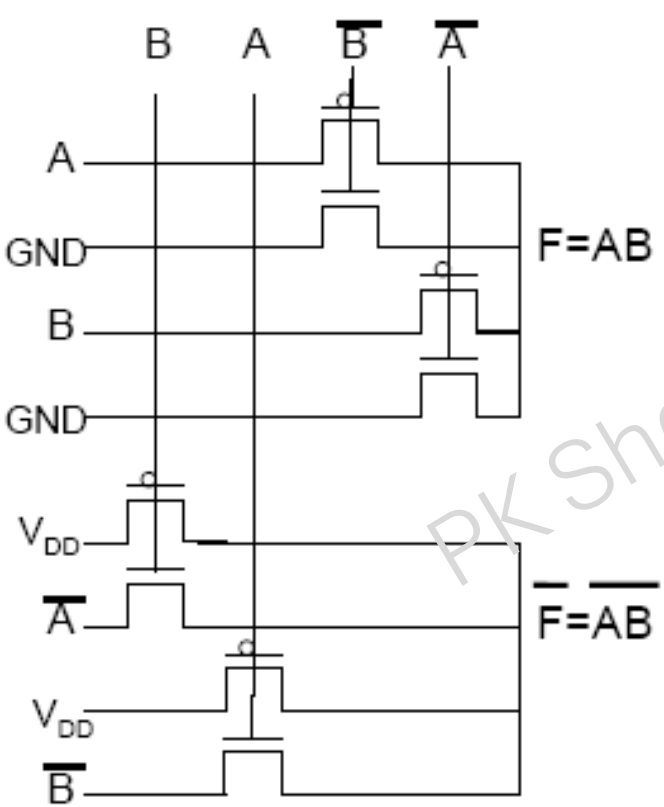
Transmission Gates (TG)

- Most widely used
- Full swing bidirectional switch controlled by the gate signal C.

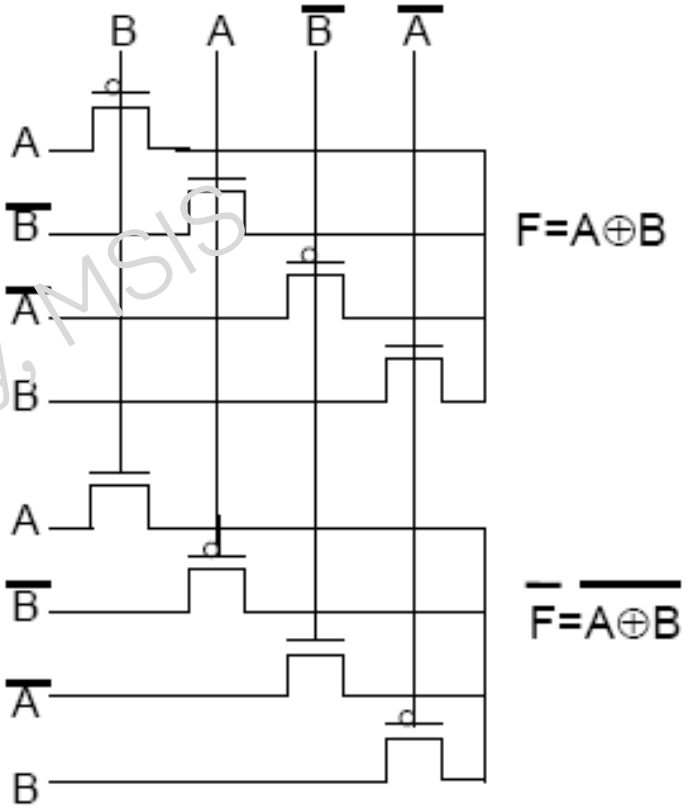
A = B if C = 1



Differential TG Logic



AND/NAND



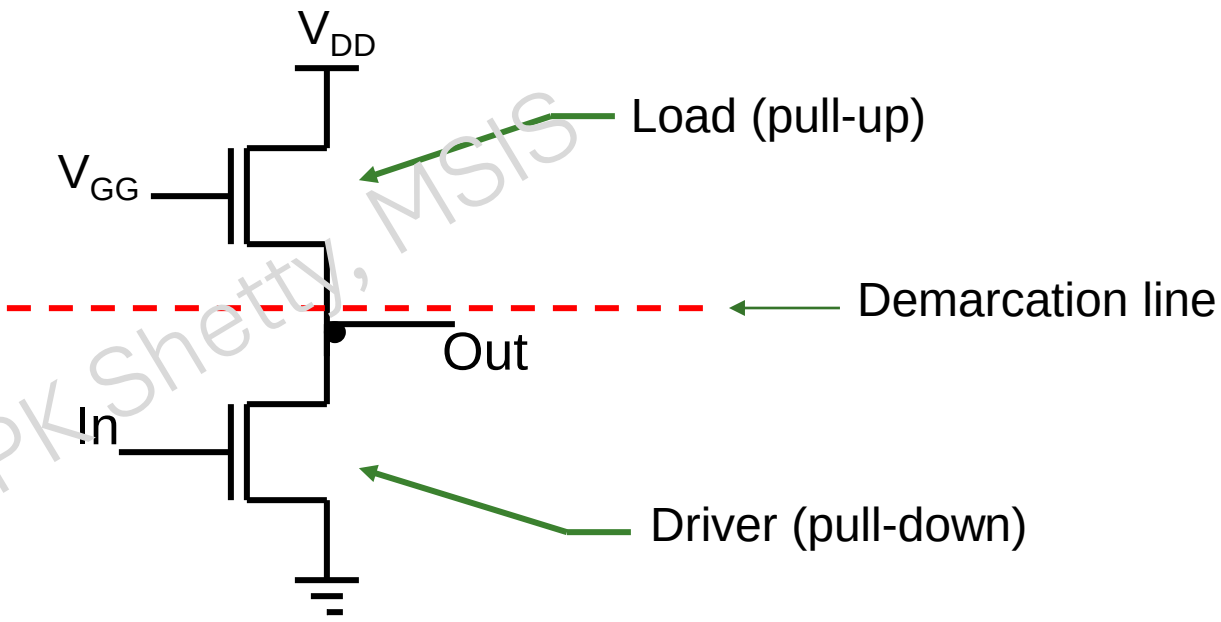
XOR/XNOR

Transmission Gate - Drawbacks

- Occupies more area – one pass transistor is replaced by 2 transistors
- Requires complementary signals to drive it

Gate Logic

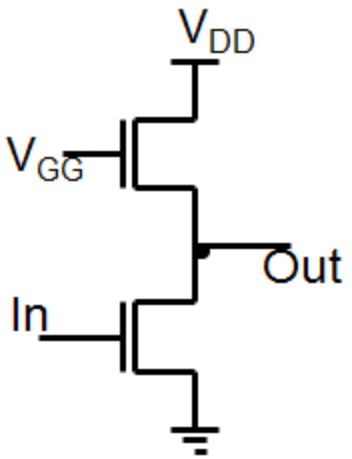
- **Inverter** – the most basic gate



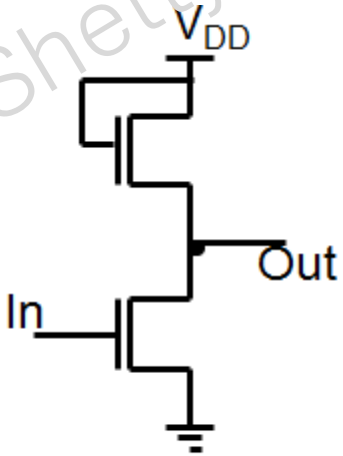
Note: The driver transistor is enhancement mode device to satisfy I/O compatibility.

Basic Single Channel Inverters

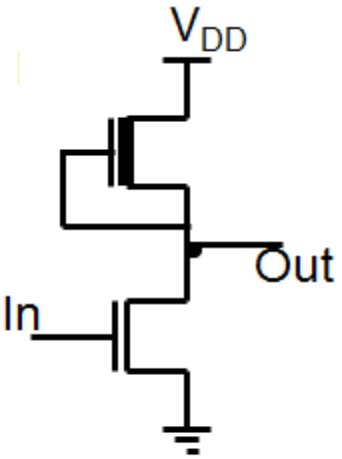
1. If $V_{GG}–V_T > V_{DD}$ then the load is said to be **NELT** (N-channel Enhancement Load in Triode region) – Needs a separate supply.
2. If the load is maintained in the saturation region throughout, then the load is said to be **NELS** (N-channel Enhancement Load in Saturation)
3. HMOS (High performance MOS) – Trademark given to Intel.



1. NELT



2. NELS



3. HMOS

HMOS

- The load is a depletion mode transistor.
- Advantages:
  - Good noise margin
  - High speed
  - Low power consumption
  - High packing density
- Limitations:
  - It is difficult to fabricate both enhancement and depletion mode MOSFETs together

$$\beta_R = \frac{(W/L)_{Load}}{(W/L)_{Driver}}$$ → Determines the performance of the Inverter.

Power Dissipation in Single Channel Inverters

- $I_{DS} = \frac{1}{2} \beta_n C_{ox} W/L(V_{GS}-V_T)^2$

Power, $P = V_{DD} \times I_{DS}$

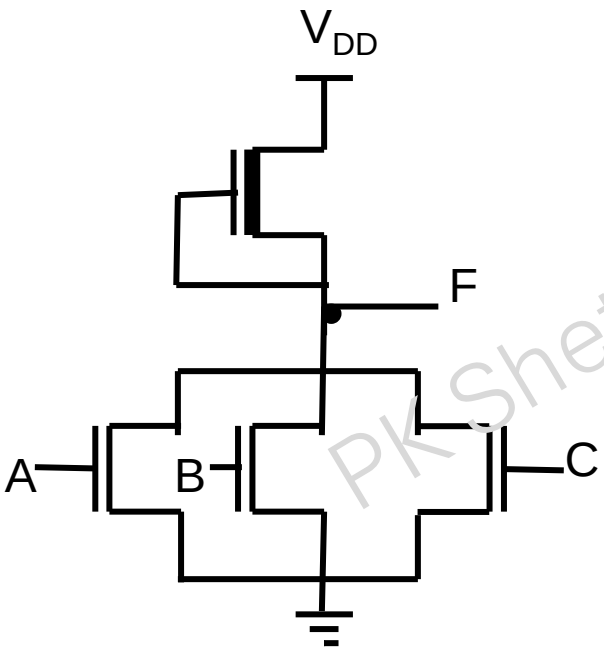
$P \propto V_{DD} \times (V_{GG})^2$

$P \propto V_{DD}^3$

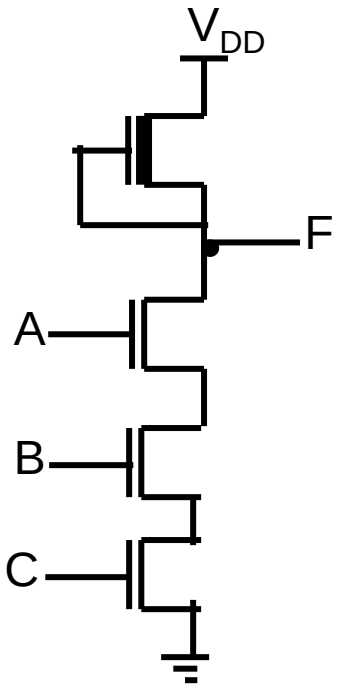
Power Dissipation in Single Channel Inverters

- NELS : $P \propto V_{DD}^3$
- NELT : $P \propto V_{DD}^3$
- HMOS: $P = \frac{1}{2}\beta_L V_{DD} V_P$;
  $P \propto V_{DD}$

Realization of Basic Gates



1. NOR Gate



2. NAND Gate