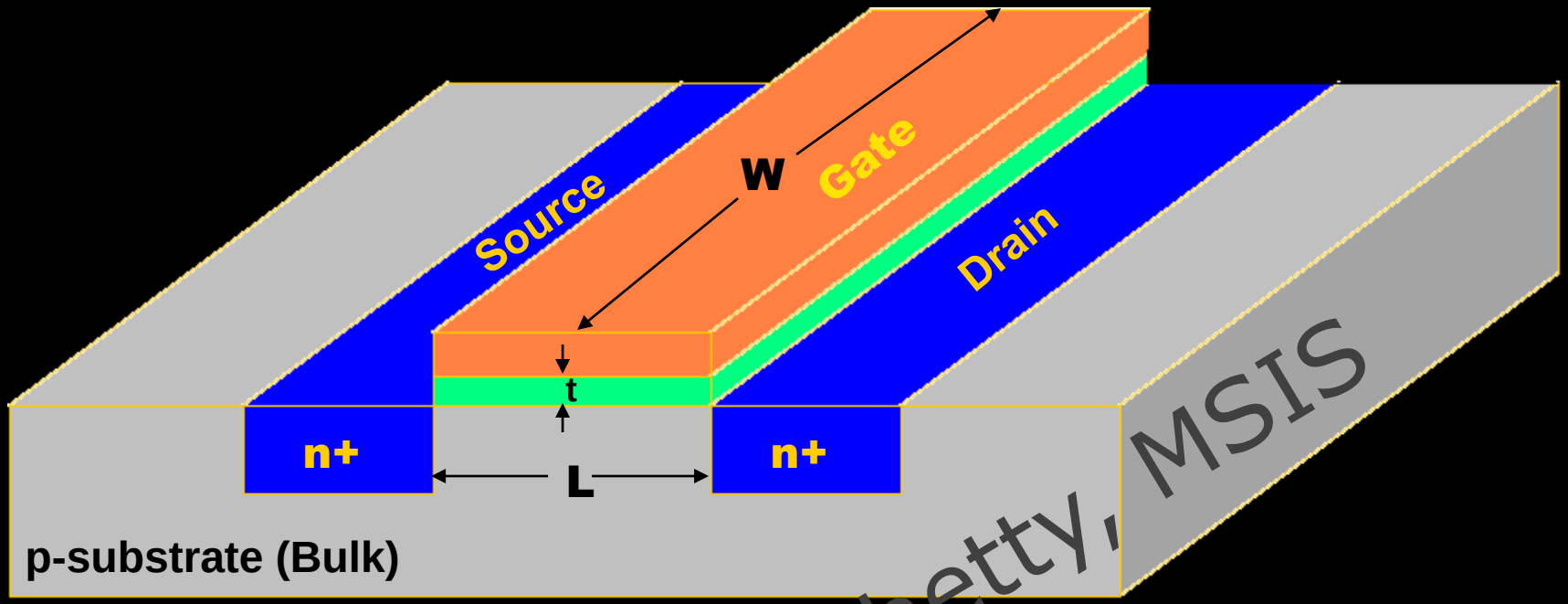
MOSFET Basics

MOSFET Structure

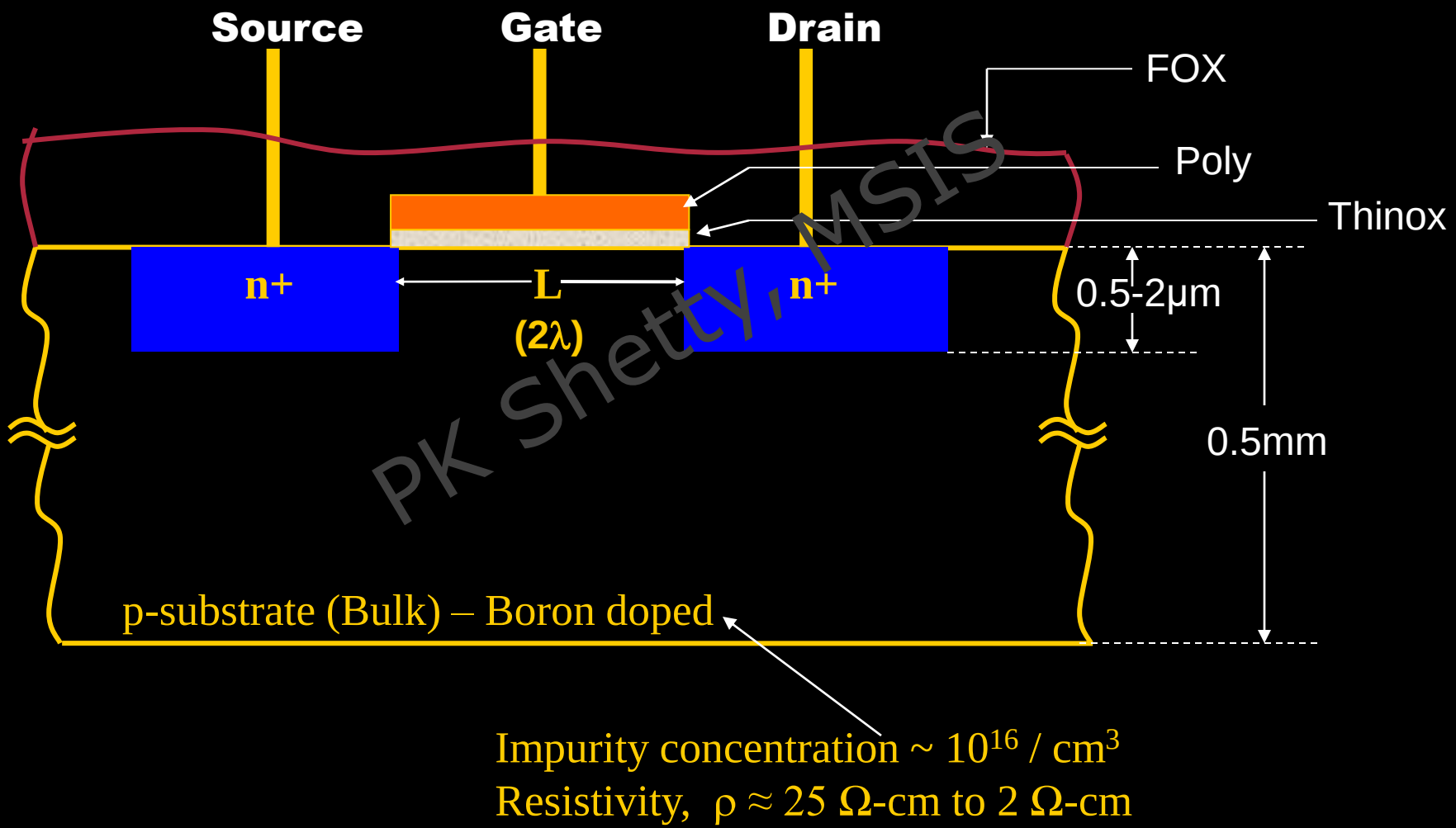


As of 2019, the highest transistor count in any IC chip

- Chip name : eUFS
- Capacity (bits) : 8 Tb
- Flash type : Stacked 4-bit V-NAND
- Transistor count : 2,048,000,000,000
- Date of introduction: 2019
- Manufacturer : Samsung
- Process : 7nm
- Area : 150 mm² [≈1.2cm×1.2cm]

eUFS – Embedded Universal Flash Storage

MOSFET Structure



Gate Oxide Requirements

- High quality, Stable, Ultra thin (t_{ox} = 17A)
- Very high resistivity ($\approx 10^{15}$ to 10^{16} Ω.cm)
- High breakdown strength ($\approx 2 \times 10^{6}$ V/cm)

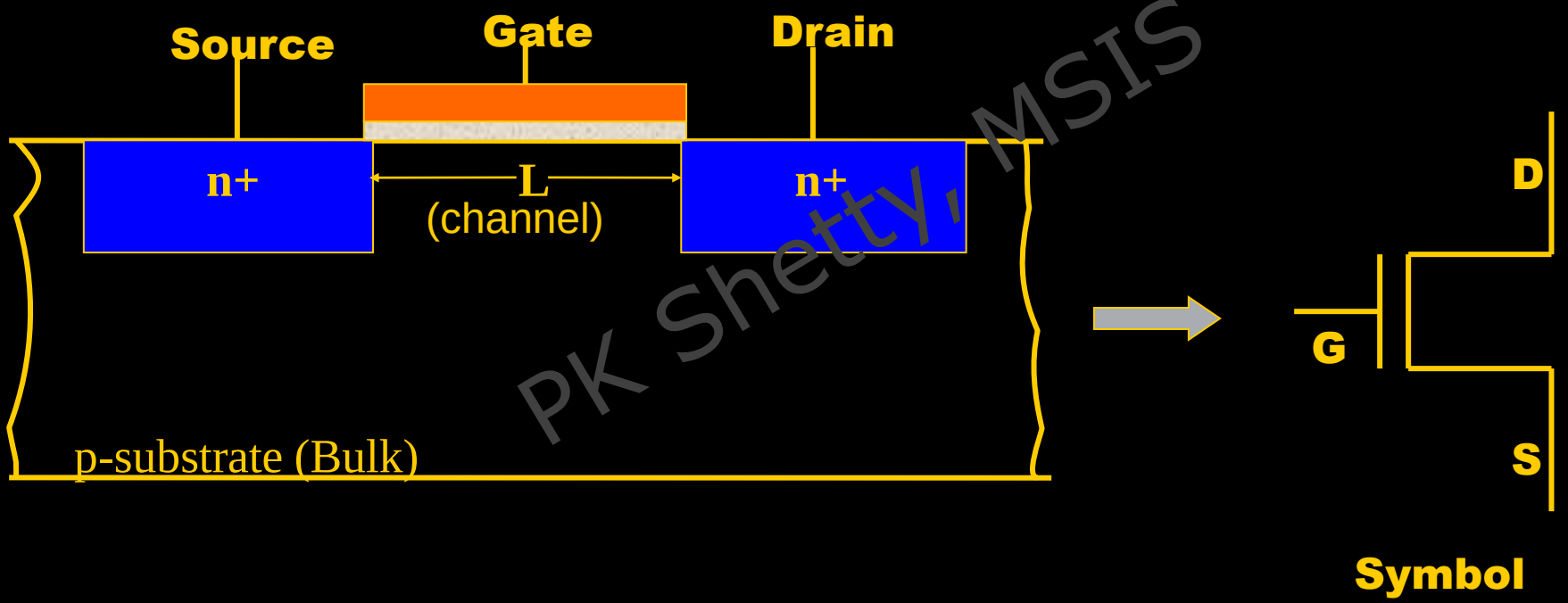
Advantages of MOSFETs

- Very high input resistance
- Very low power consumption
- Very high packing density
- Bilaterally symmetrical
- Self Isolated
- Can be used both as drivers and loads

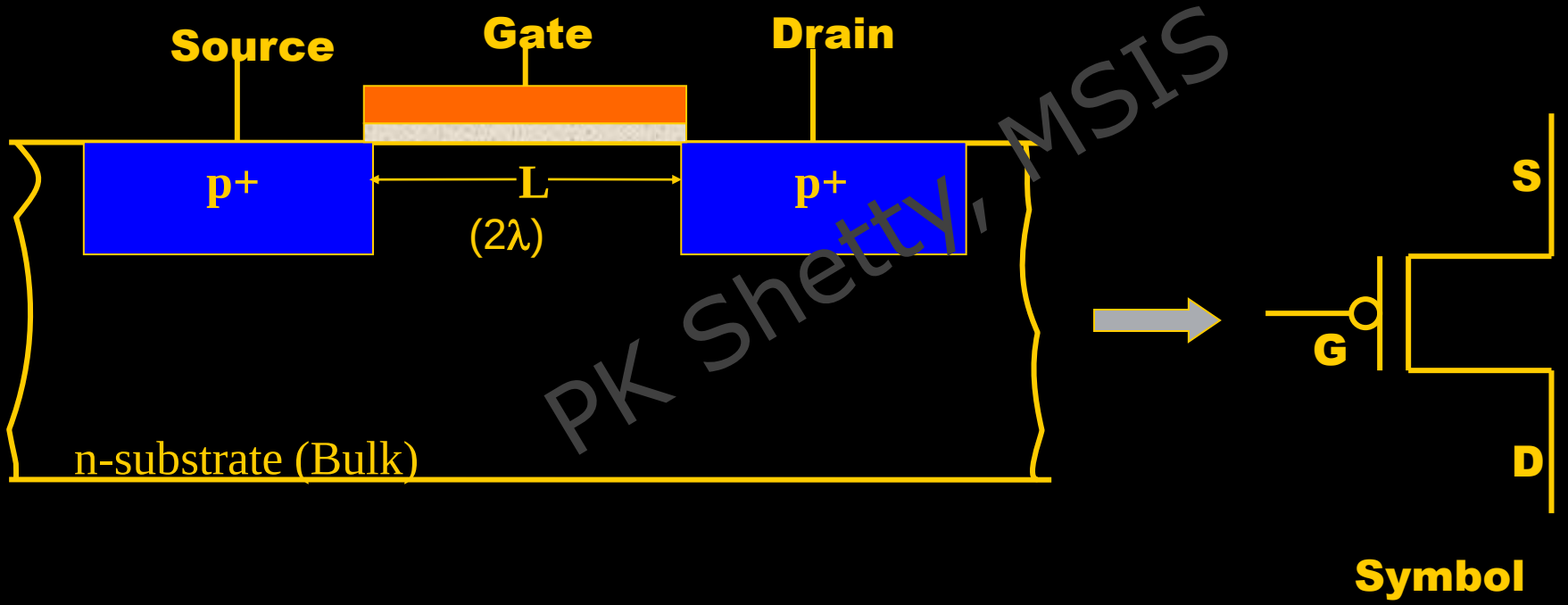
Bipolar Advantages

- Can handle large power
- Faster
- More suitable for analog circuit realization.
  - BiCMOS

N-Channel MOSFET



P-Channel MOSFET

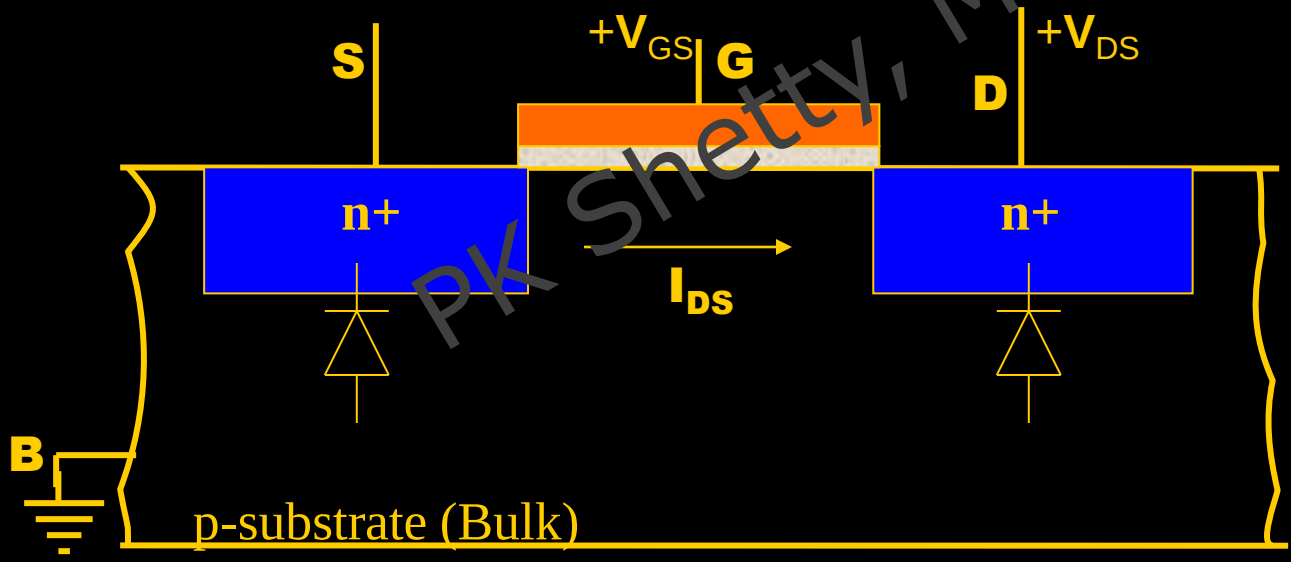


How it works?

When V_{GS} = 0;

And V_{DS} = a +ve voltage w.r.t. Source;

I_{DS} = 0.

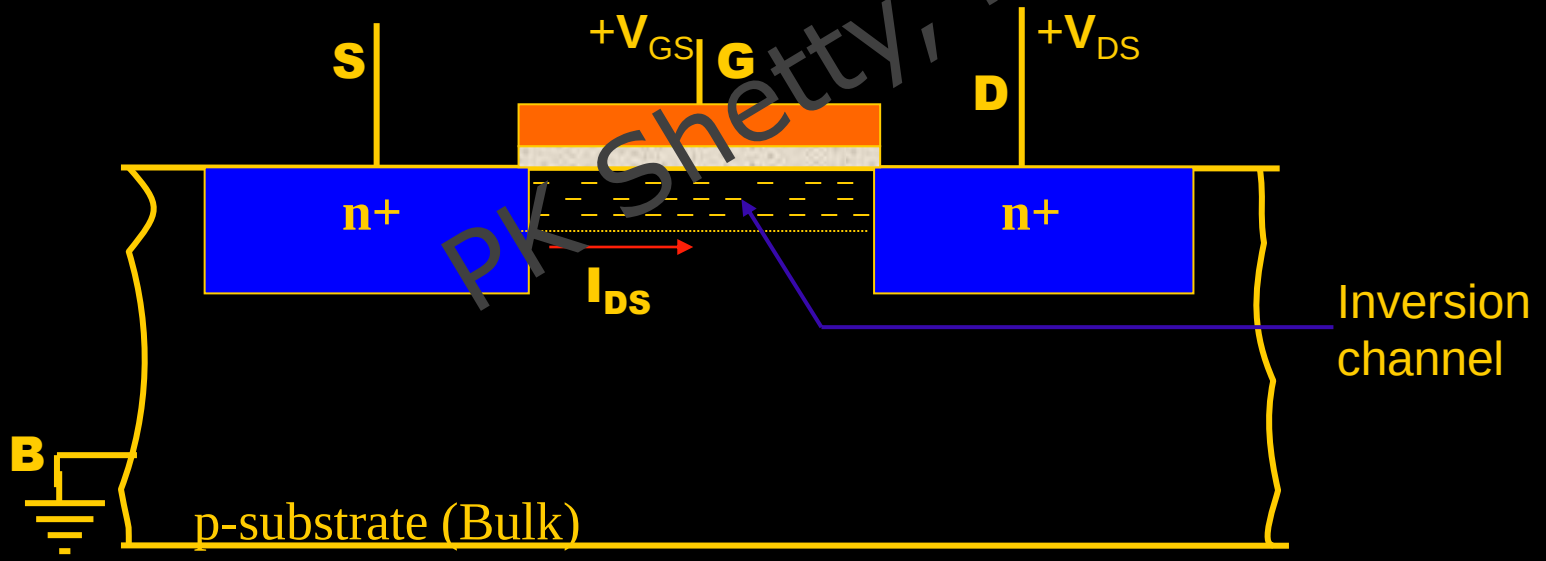


How it works?

When V_{GS} = a +ve voltage w.r.t. Source;

And V_{DS} = a +ve voltage w.r.t. Source;

I_{DS} starts flowing.



Threshold voltage

- " The voltage applied between the gate and the source of a MOSFET below which the drain-to-source current I_{DS} effectively drops to zero"
- This is denoted by $\mathbf{V_{TH}}$.
- Therefore, the effective voltage applied across the gate, $V_G = (V_{GS}-V_{TH})$

Threshold voltage

$$V_{TH} = V_{TH0} + \gamma[(2\Phi_b + |V_{SB}|)^{½} - (2\Phi_b)^{½}]$$

Where, $\gamma = (t_{ox}/\varepsilon_{ox})(2q\,\varepsilon_{Si}N_A)^{½}$

$\Phi_b = kT/q\ ln(N_A/N_i)$;

N_i – carrier concentration in Intrinsic silicon.

Threshold voltage is a function of the following parameters:

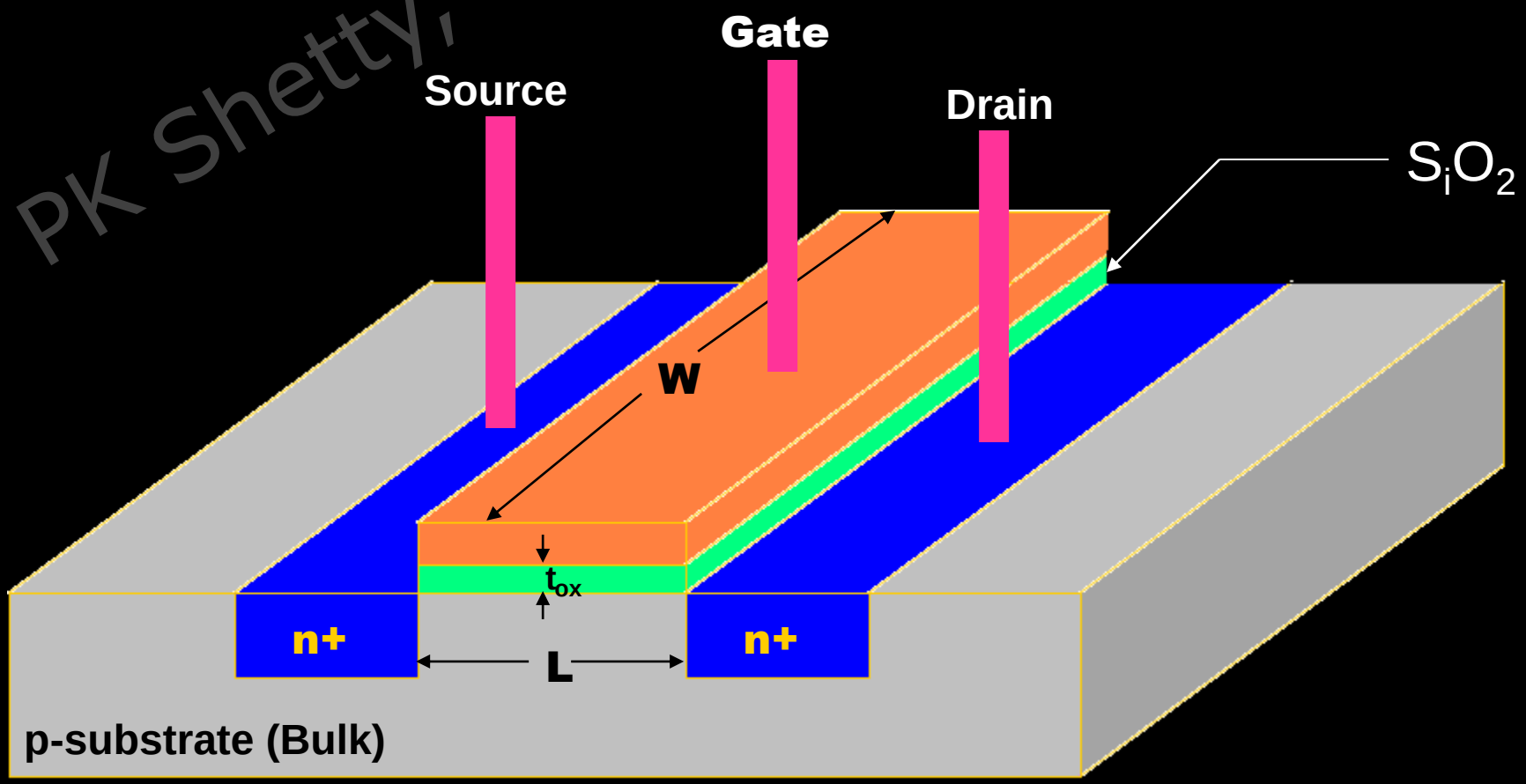
- Gate conductor material
- Gate insulation material
- Gate insulator thickness
- Impurities at the silicon-insulator interface
- Voltage between the source and the substrate, V_{SB}

Regions of Operation

Depending upon the biasing, a MOSFET may be operating in one of the 3 regions:

1. Cut-off region
2. Linear region
3. Saturation region

MOSFET Structure



- Since charge induced in the channel depends on V_{gs}. I_{ds} depends on both V_{gs} and V_{ds}

$$I_{ds} = -I_{sd} = \frac{\text{charge induced in channel } (Q_c)}{\text{Electron transit time } (\tau_{sd})}$$

$$\tau_{sd} = \frac{\text{Length of channel (L)}}{\text{Electron Velocity (v)}} \qquad v = L/t$$

But velocity, $\mathbf{v = \mu E_{ds}}$, where μ = electron / hole mobility

E_{ds} = Drain to source electric field

and, $\mathbf{E_{ds} = \frac{V_{ds}}{L}}$

$$\therefore \mathbf{v} = \frac{\mu V_{ds}}{L} \Rightarrow \text{Or, } \tau_{sd} = \frac{L^2}{\mu V_{ds}}$$

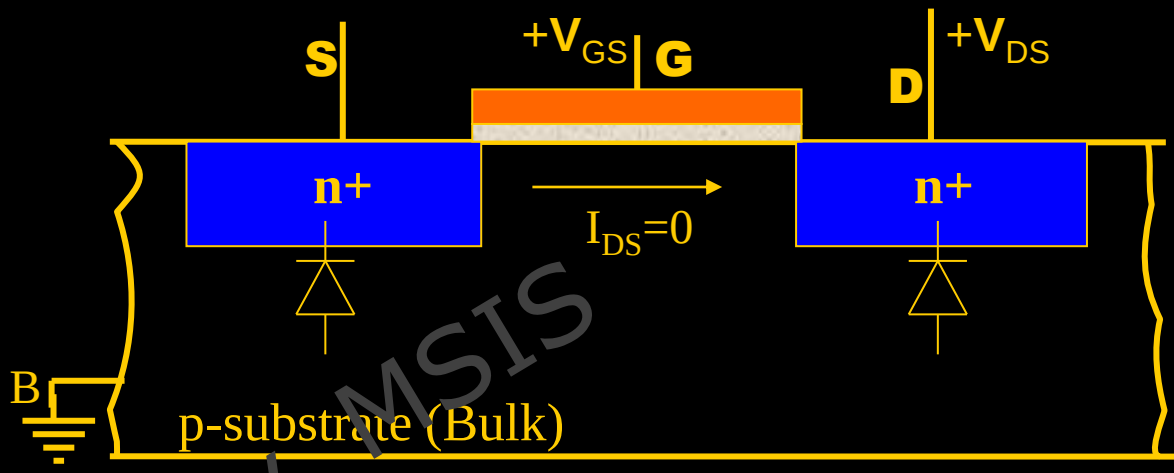
$$\boxed{I_{ds} = -I_{sd} = \frac{\mu V_{ds} Q_c}{L^2}}$$

Typical values of μ at room temperature:

- $\mu_n = 650\ cm^2 / v\ sec$
- $\mu_p = 240\ cm^2 / v\ sec$

$$\mu_n \approx 2.5\ \mu_p$$

1. Cut-off region:

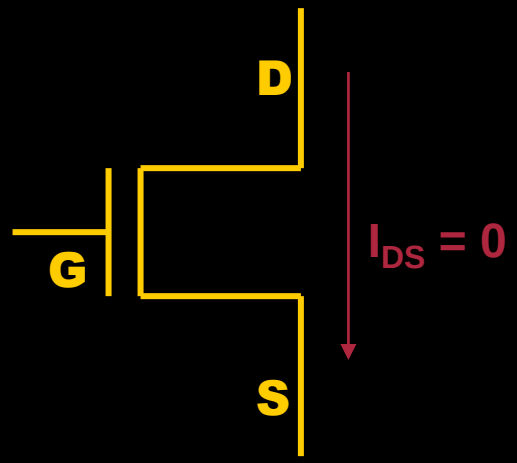


$V_{GS} < V_T$;

No channel formed, $Q_c = 0$;

hence irrespective of the value of V_{DS},

$I_{DS} = 0$;



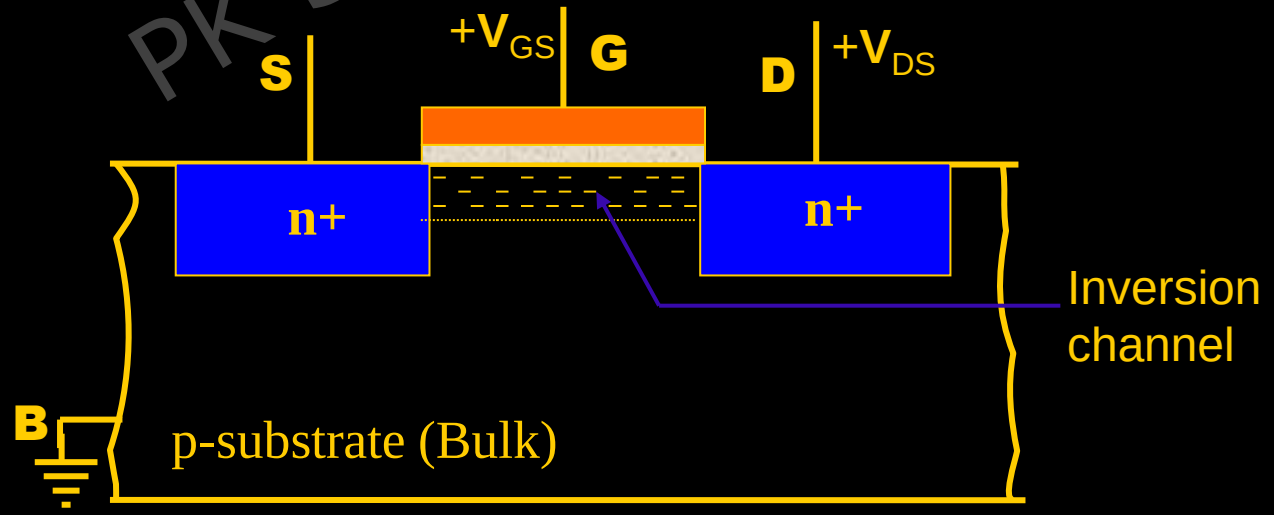
2. Linear region:

$V_{GS} >= V_T$;

Or, Effective gate voltage, $V_g = V_{GS} - V_T$

= excess gate voltage

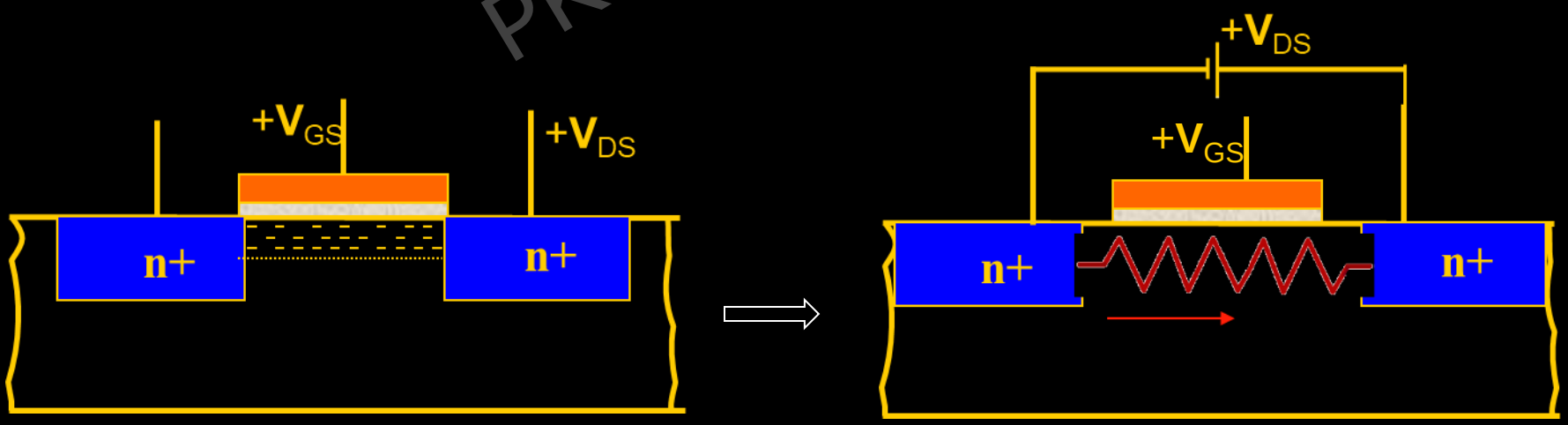
= overdrive voltage



2. Linear region:

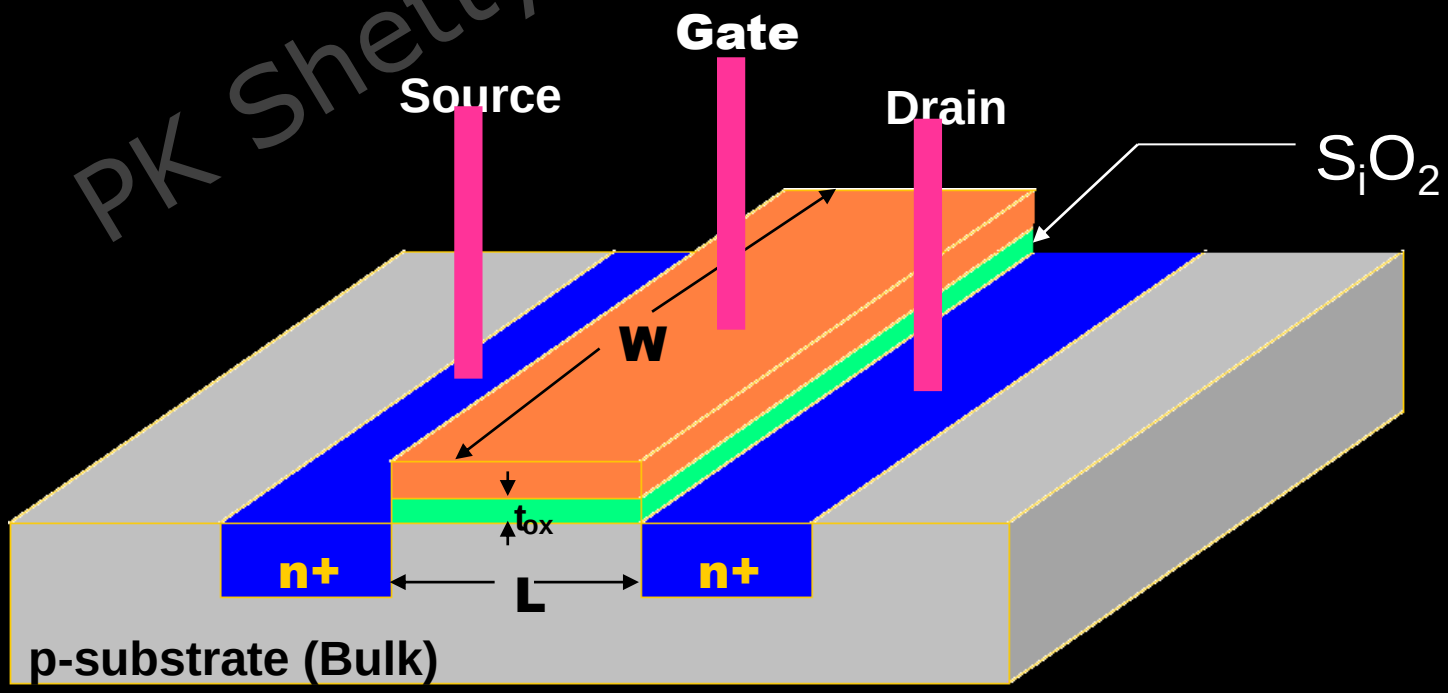
- When a $+V_{DS}$ is applied, current I_{DS} starts flowing.
- Now voltage along the channel varies linearly with distance ‘x’ from source due to IR drop with an average value = $V_{DS}/2$
- Now the net voltage across gate and channel is,

$$V = (V_{GS} - V_T) - V_{DS}/2$$



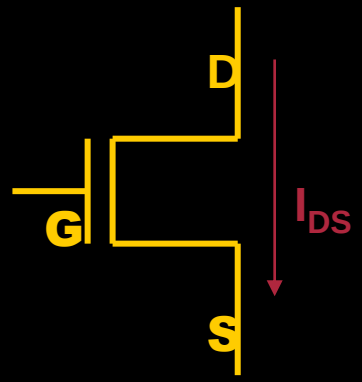
MOSFET Structure

$$I_{ds} = -I_{sd} = \frac{\mu V_{ds} Q_c}{L^2}$$



2. Linear region:

$$I_{ds} = -I_{sd} = \frac{\mu V_{ds} Q_c}{L^2}$$



$$Q_c = C\,V$$

$$= \frac{\varepsilon_{ox} WL}{t_{ox}} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right]$$

$C = \varepsilon_{ox} A/d$

$C = \varepsilon_{ox} WL/t_{ox}$

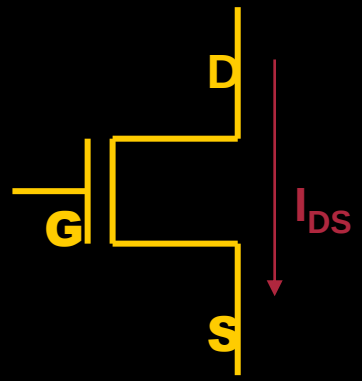
$V = (V_{GS} - V_T) - V_{DS}/2$

$$I_{DS} = \frac{\mu_n V_{DS}}{L^2} \times \frac{\varepsilon_{ox} WL}{t_{ox}} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right]$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

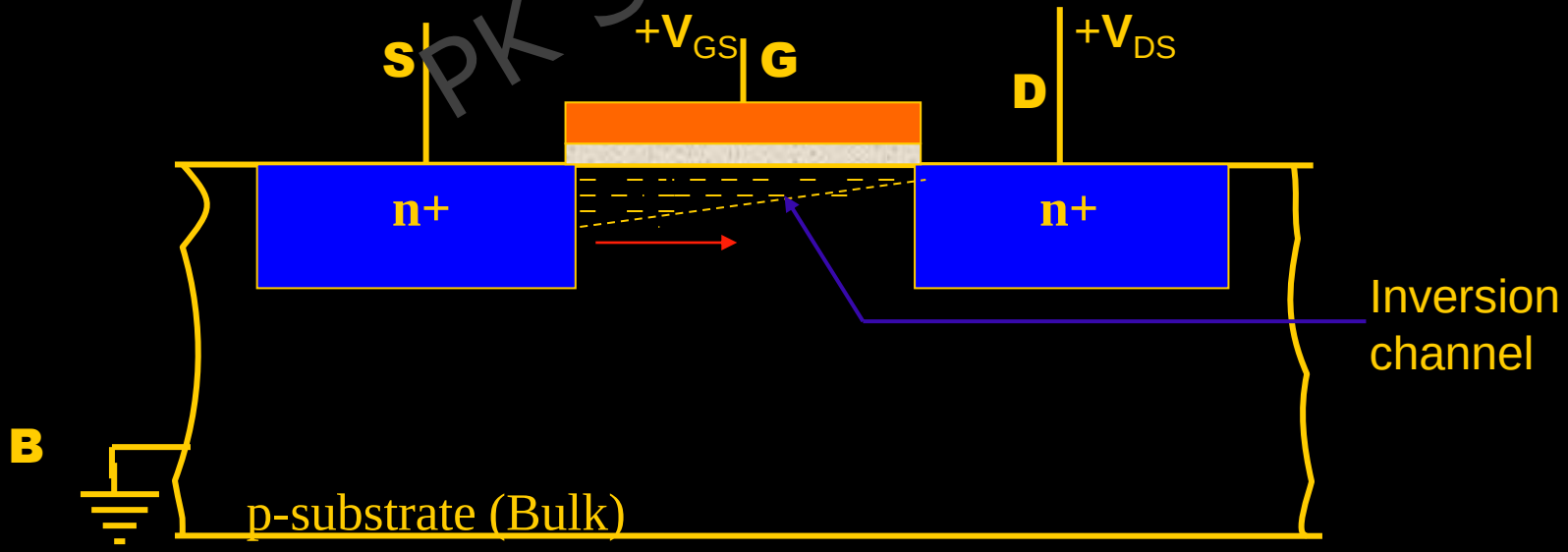
$$I_{DS} = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS} - V^2_{DS}/2]$$

2. Linear region:



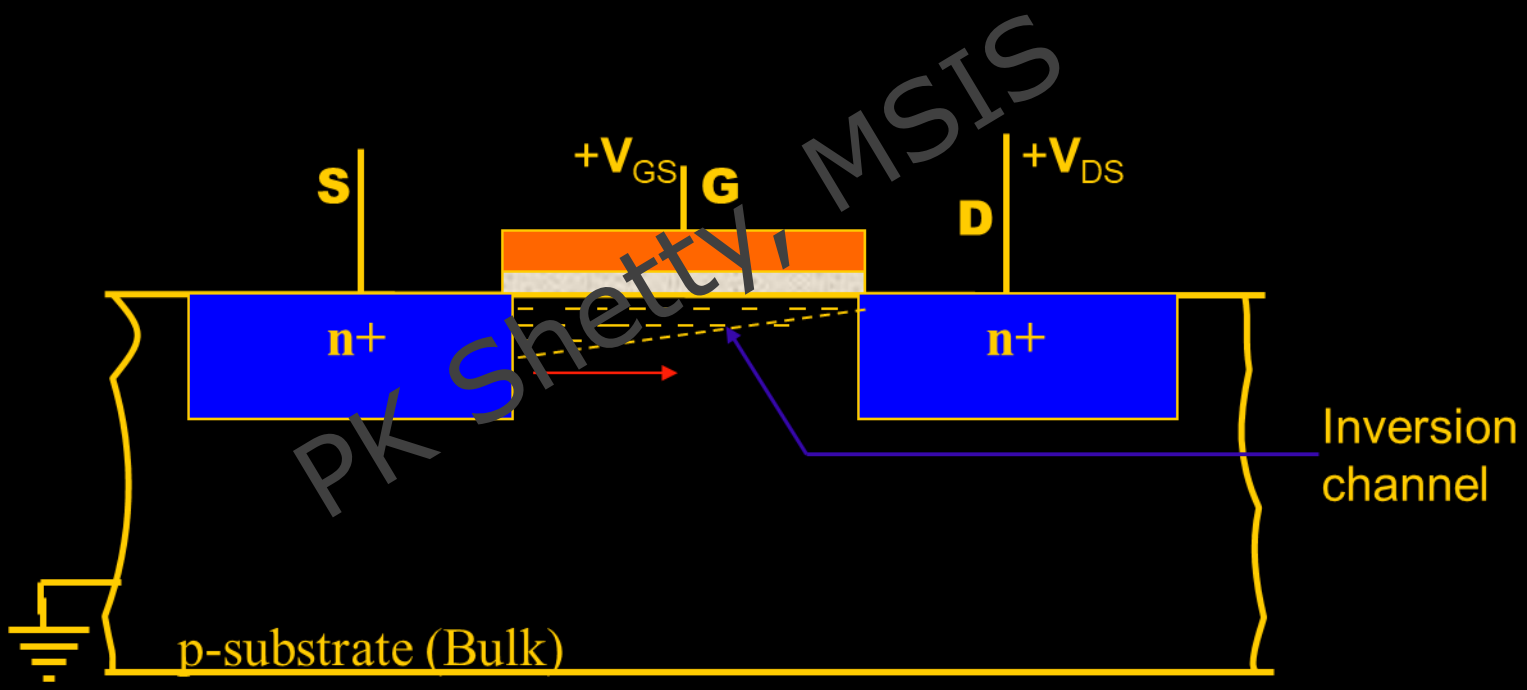
$V_{GS} >= V_T$; $V_{DS} < (V_{GS}-V_T)$

$$I_{DS} = \mu_n C_{ox} W/L[(V_{GS}-V_T)V_{DS} - V^2_{DS}/2]$$



Say, V_{GS} = 2V, V_T = 0.5V $\Longrightarrow$ (V_{GS}–V_T) = 1.5V

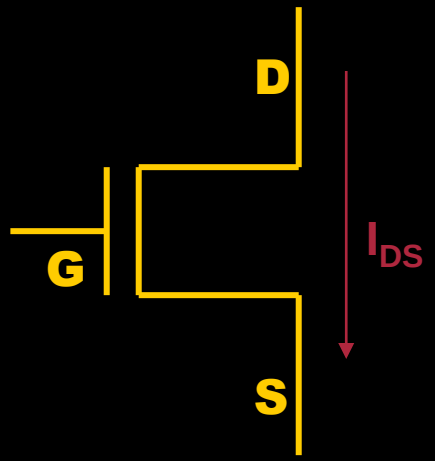
If V_{DS} = 1V then…

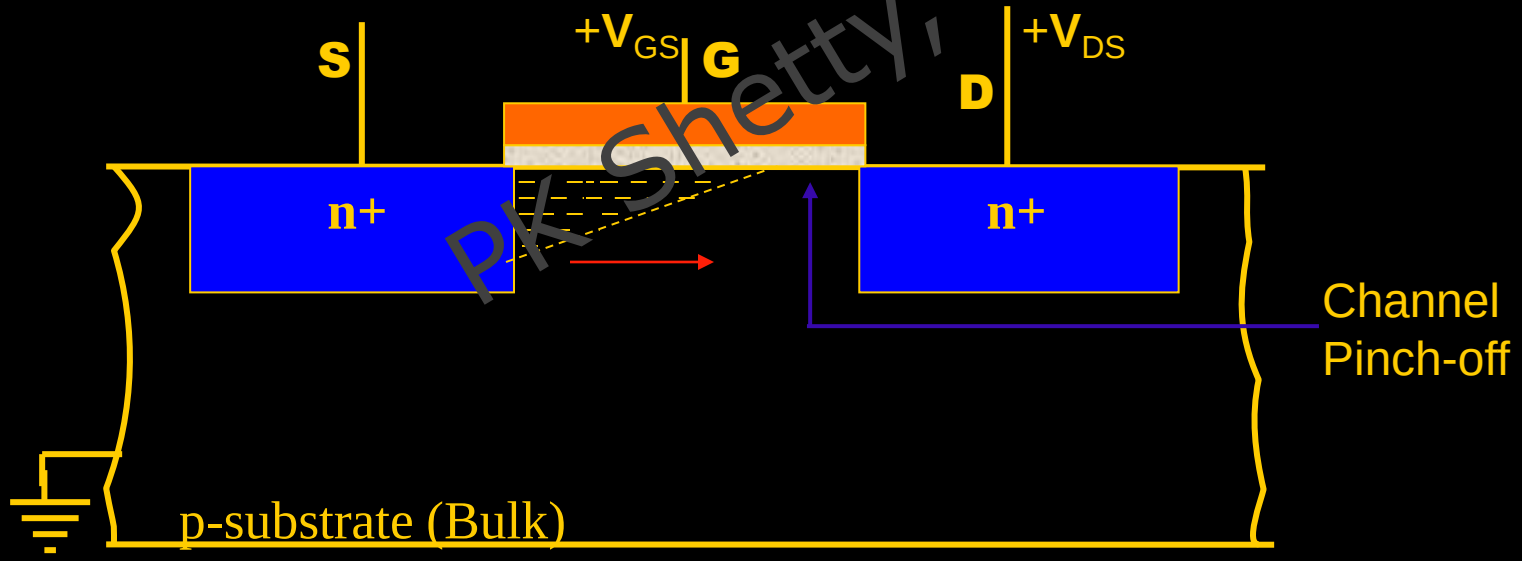


3. Saturation region:

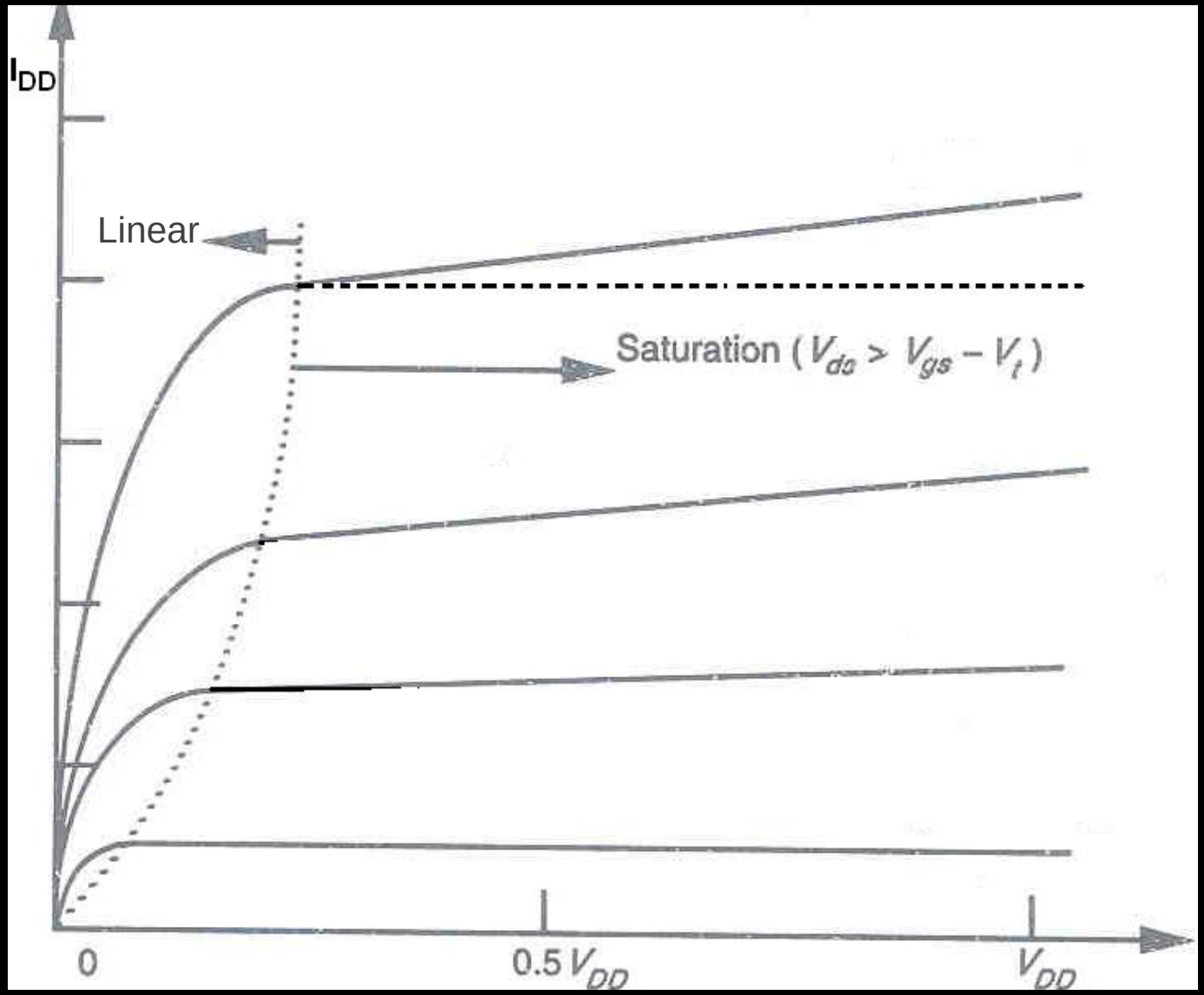
$V_{GS} >= V_T$; $V_{DS} >= (V_{GS}-V_T)$

$$I_{DS} = \tfrac{1}{2}\, \mu_n C_{ox}\, W/L(V_{GS}-V_T)^2$$



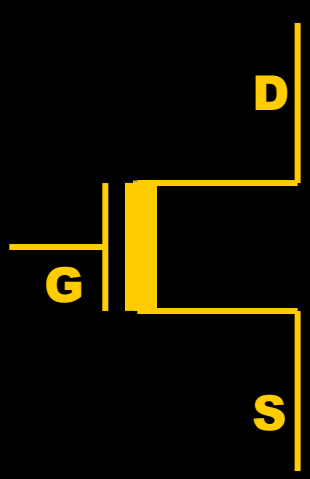


V-I Characteristics

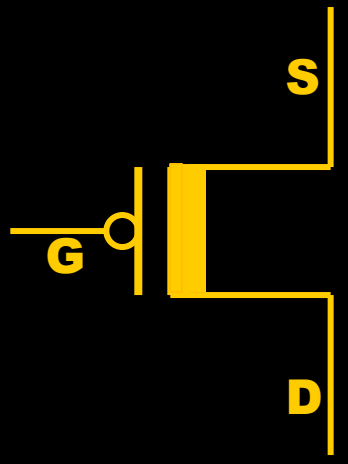


MOSFET Modes

- Enhancement Mode MOSFET
- Depletion Mode MOSFET



Depletion mode NMOS



Depletion mode PMOS

Secondary effects

1. Body Effect
2. Channel - length Modulation
3. Mobility Variation
4. Drain Punchthrough
5. Impact Ionization

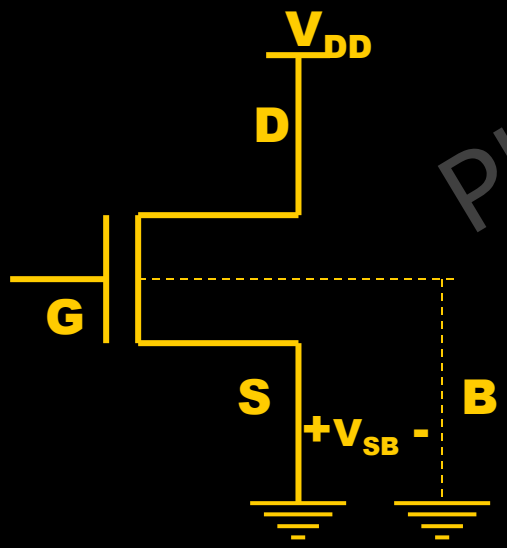
1. Body Effect

$$V_T = V_{T0} + \gamma[(2\Phi_b + |V_{SB}|)^{1/2} - (2\Phi_b)^{1/2}]$$

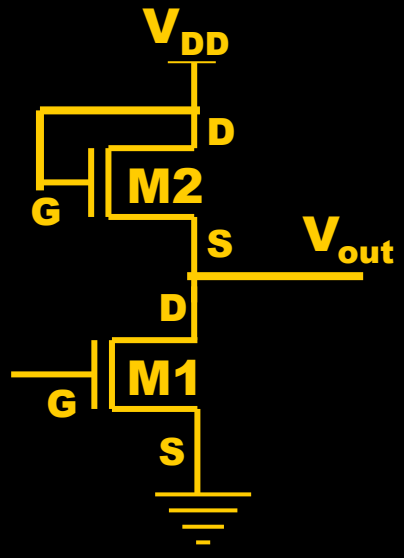
Where, $\gamma = (t_{ox}/\varepsilon_{ox})(2q\,\varepsilon_{Si}N_A)^{1/2}$

$\Phi_b = kT/q\ ln(N_A/N_i)$;

N_i – carrier concentration in intrinsic silicon.



No body effect



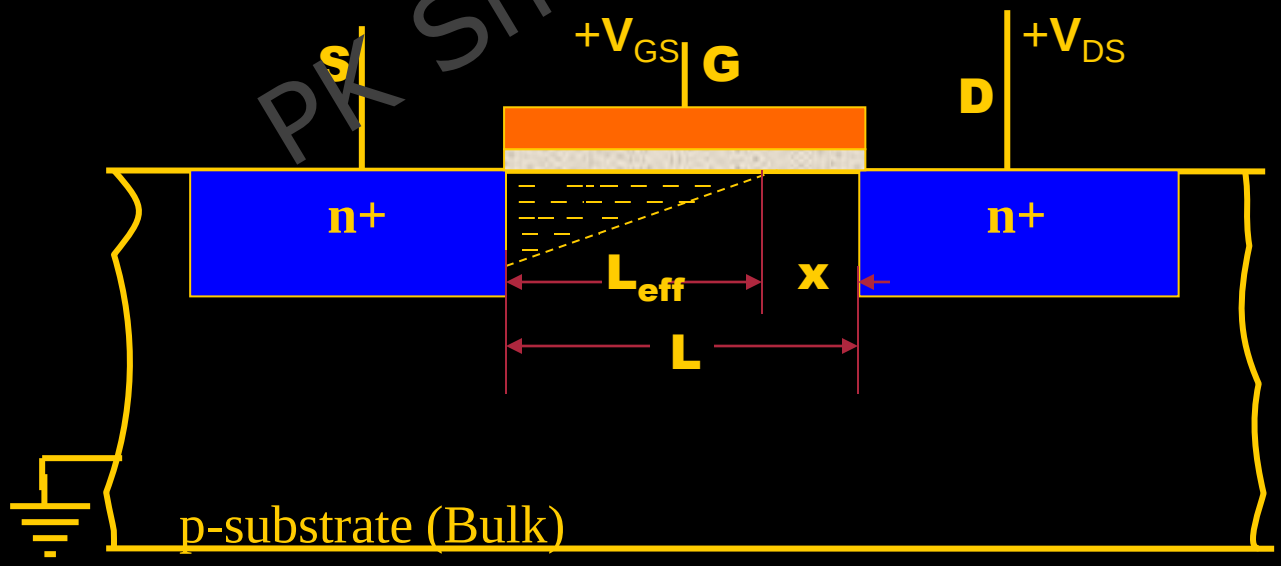
M2 has body effect

2. Channel-length Modulation

Since channel pinch-off takes place in saturation region, $L_{eff} = (L-x)$

$\therefore I_{DS} = \frac{1}{2} \mu_n C_{ox} W/L(V_{GS}-V_T)^2(1+\lambda V_{DS})$,

where λ is the channel-length modulation factor = $1/L_{eff}\ \partial x/\partial V_{DS}$



3. Mobility Variation

$$I_{DS} = \tfrac{1}{2}\,\mu_n C_{ox}\, W/L(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

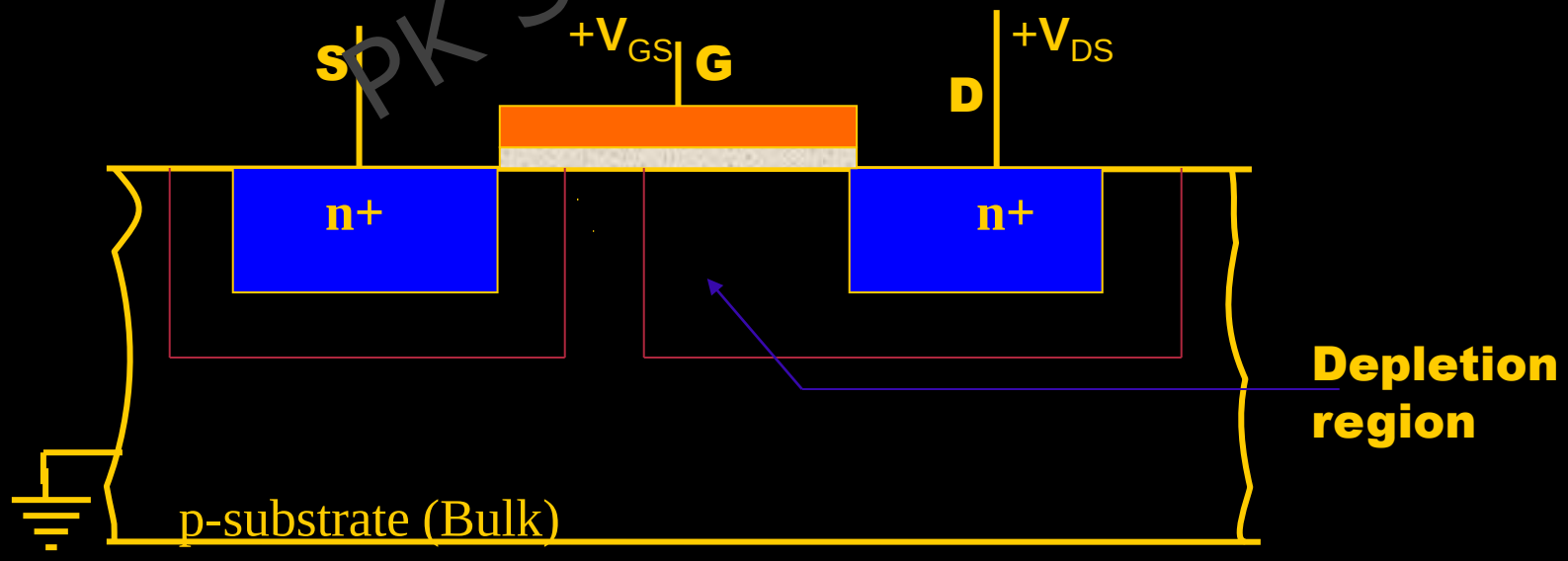
Mobility varies with the type of charge carrier

Mobility decreases with increasing doping conc.

Mobility decreases with increasing temperature

4. Drain Punchthrough

When the drain is at a high enough voltage w.r.t. the source, the depletion region around the drain may extend to the source, thus causing current to flow irrespective of the gate voltage (i.e., even if it is zero). This is known as drain punchthrough.



- Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region.

5. Impact Ionization

"Hot" electrons impacting the drain, dislodging holes that are then swept toward the negatively charged substrate and appear as a substrate current. This is known as **impact ionization**.

These hot electrons can penetrate even the gate oxide, causing a gate current. Eventually this can lead to degradation of MOS device parameters (V_T, subthreshold current, transconductance), which in turn can lead to the failure of circuits.

References:

1. Weste, Eshraghian, ***Principles of CMOS VLSI Design***, Addison-Wesley, 2nd Edition.

2. Pucknell, Eshraghian, ***Basic VLSI Design,*** Prentice Hall of India, Third Edition.