CMOS Switching Characteristics

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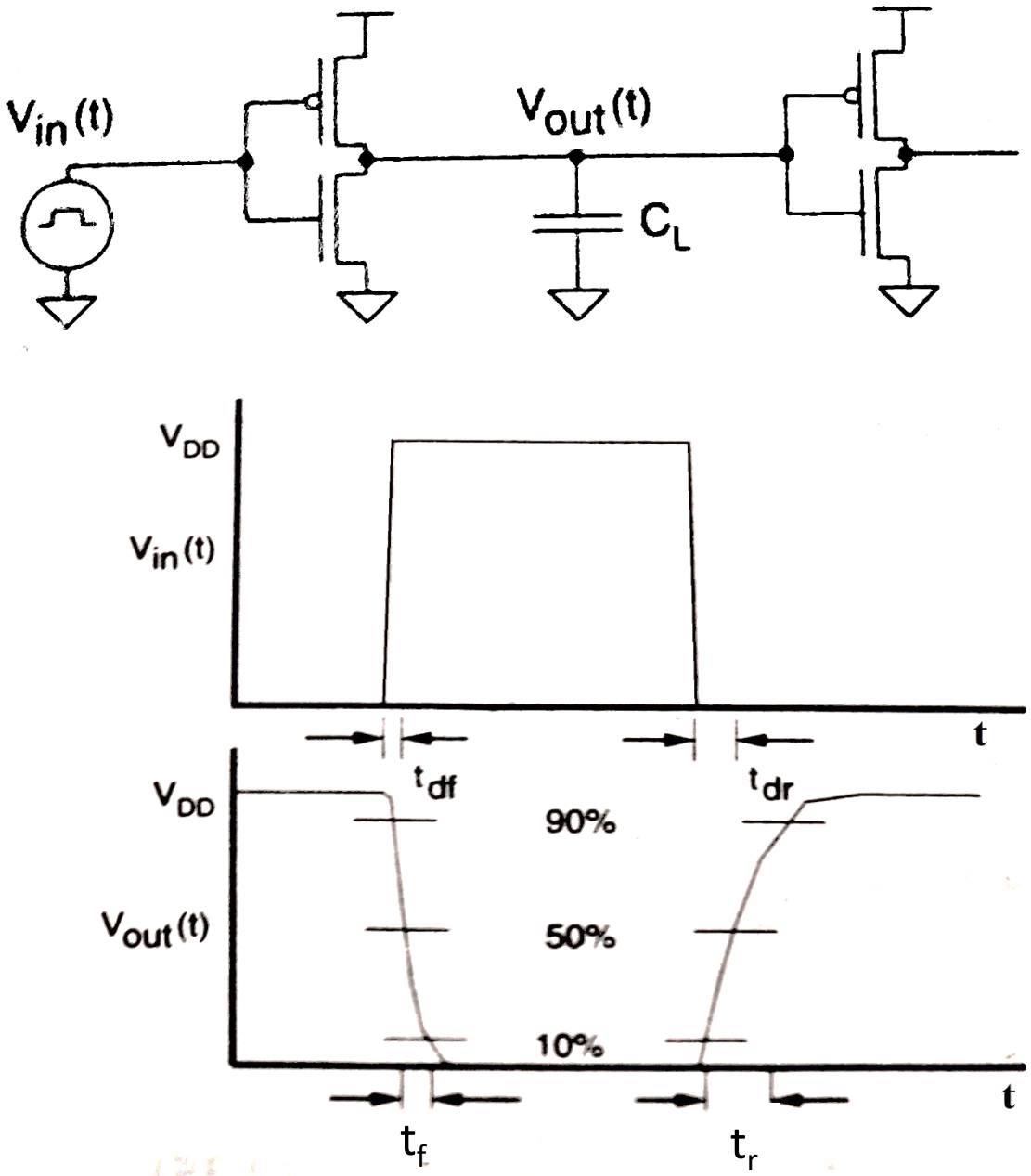
- To describe the switching characteristics of a CMOS inverter we develop 2 models:
    1. Analytic Delay Model
    2. Empirical Delay Model
- These models help to understand the parameters that affect CMOS delay
- The switching speed of a CMOS gate is limited by the time taken to charge and discharge the load capacitance C_L
- An input transition results in an output transition that either charges C_L toward V_{DD} or discharge C_L toward V_{SS}

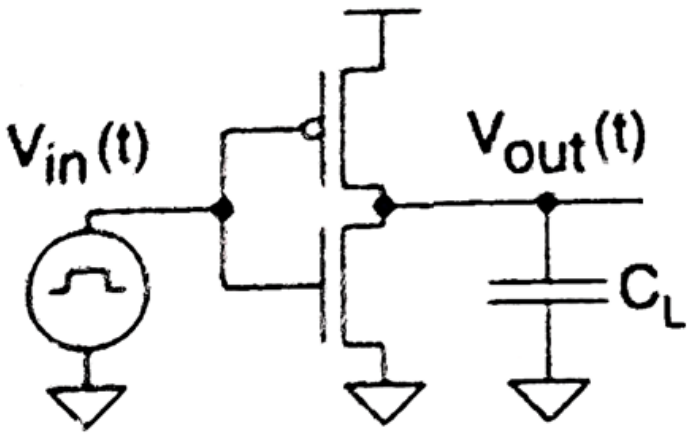
Delay – Definitions

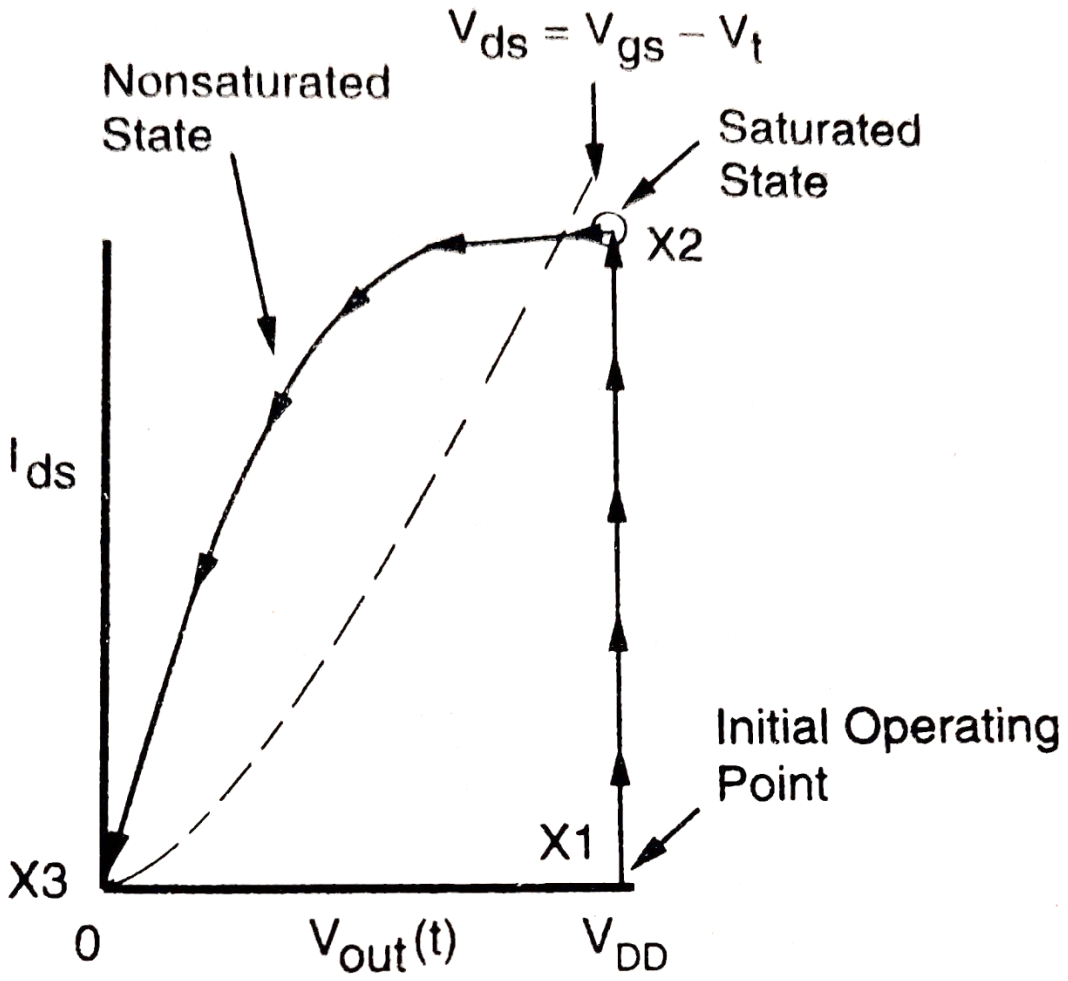
- ***Rise time***, t_r = time for a waveform to rise from 10% to 90% of its steady-state value
- ***Fall time***, t_f = time for a waveform to fall from 90% to 10% of its steady-state value
- ***Delay time***, t_d = time difference between input transition (50%) and the 50% output level. (This is the time taken for a logic transition to pass from input to output)



Switching characteristic for CMOS inverter

Analytic Delay Model





Trajectory of n-transistor operating point during Switching when the input $V_{in}(t)$ is a step wave form

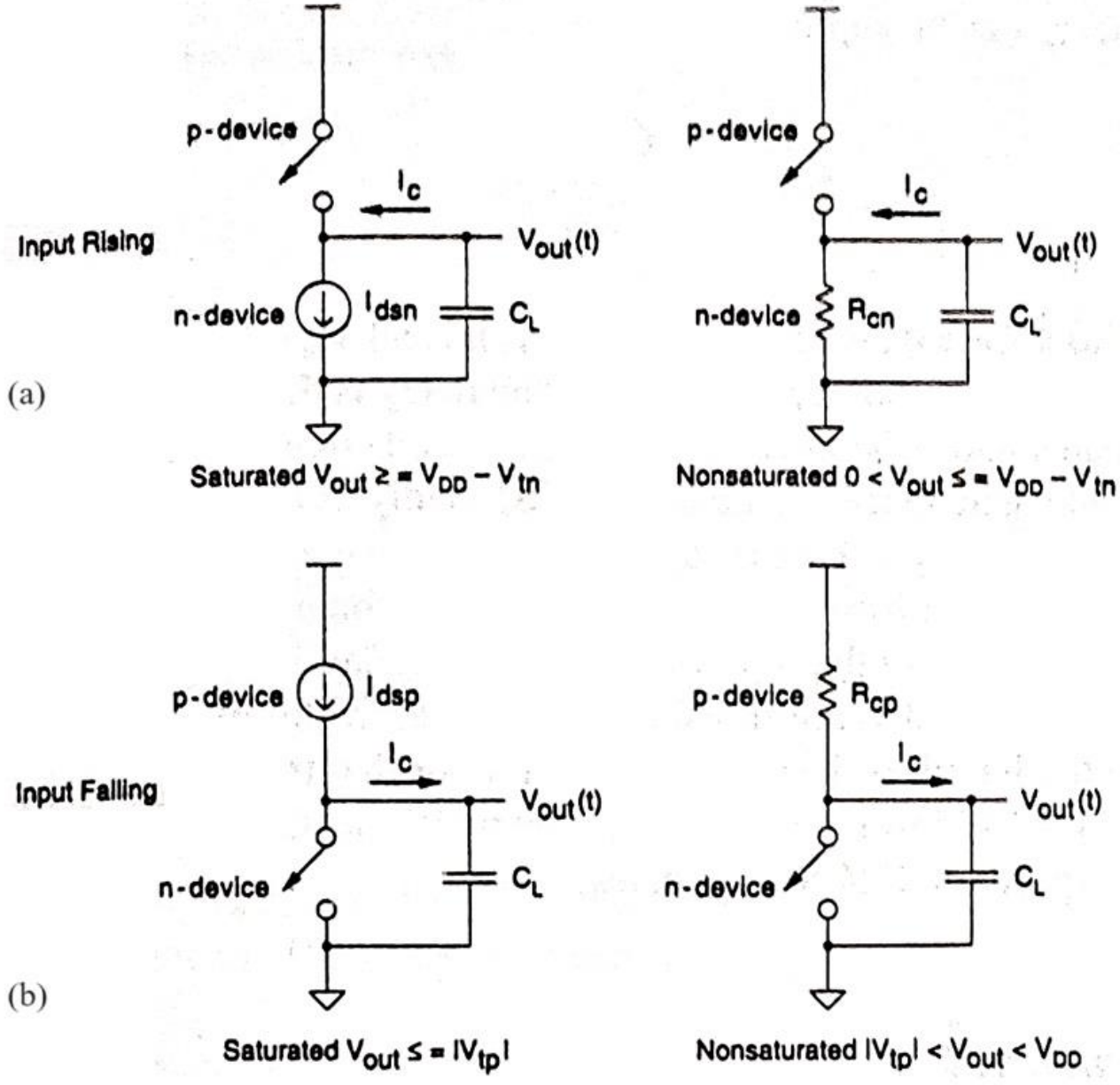
Analytic Delay Model

Fall Time:

The fall time, t_f, consists of 2 intervals:

1. t_{f1} = period during which the capacitor voltage, V_{out}, drops from $0.9V_{DD}$ to $(V_{DD} - V_{tn})$

2. t_{f2} = period during which the capacitor voltage, V_{out}, drops from $(V_{DD} - V_{tn})$ to $0.1V_{DD}$


(a)
Input Rising
p-device
I_c
$V_{out}(t)$
n-device
I_{dsn}
C_L
Saturated $V_{out} \geq = V_{DD} - V_{tn}$
p-device
I_c
$V_{out}(t)$
n-device
R_{cn}
C_L
Nonsaturated $0 < V_{out} \leq = V_{DD} - V_{tn}$
(b)
Input Falling
p-device
I_{dsp}
I_c
$V_{out}(t)$
n-device
C_L
Saturated $V_{out} \leq = |V_{tp}|$
p-device
R_{cp}
I_c
$V_{out}(t)$
n-device
C_L
Nonsaturated $|V_{tp}| < V_{out} < V_{DD}$

When the n-device is operating in the saturation region,

$$C_L \frac{dV_{out}}{dt} + \frac{\beta_n}{2}(V_{DD} - V_{tn})^2 = 0.$$

Integrating from $t = t_1$, corresponding to $V_{out} = 0.9\ V_{DD}$, to $t = t_2$ corresponding to $V_{out} = (V_{DD} - V_{tn})$ results in

$$t_{f1} = 2\frac{C_L}{\beta_n (V_{DD} - V_{tn})^2} \int_{V_{DD} - V_{tn}}^{0.9 V_{DD}} dV_{out}$$

$$= \frac{2C_L (V_{tn} - 0.1 V_{DD})}{\beta_n (V_{DD} - V_{tn})^2}$$

When the n-device begins to operate in the linear region, the discharge current is no longer constant. The t_{f2} taken to discharge the capacitor from (V_{DD}-V_{tn}) to 0.1V_{DD} can be obtained as,

$$t_{f2} = \frac{C_L}{\beta_n (V_{DD} - V_{tn})} \int_{0.1V_{DD}}^{V_{DD}-V_{tn}} \frac{dV_{out}}{\frac{V_{out}^2}{2(V_{DD}-V_{tn})} - V_{out}}$$

$$= \frac{C_L}{\beta_n (V_{DD} - V_{tn})} ln\left(\frac{19V_{DD} - 20V_{tn}}{V_{DD}}\right)$$

$$= \frac{C_L}{\beta_n V_{DD}(1-n)} ln(19 - 20n),$$

with $n = V_{tn}/V_{DD}$.

Thus the complete term for the fall time, t_f, is

$$t_f = 2\frac{C_L}{\beta_n V_{DD}(1-n)}\left[\frac{(n-0.1)}{(1-n)} + \frac{1}{2} ln(19 - 20n)\right]$$

- The fall time, t_f, can be approximated as,

$$t_f = \mathrm{k} \times \frac{C_L}{\beta_n V_{DD}}$$

- This implies the delay is directly proportional to the load capacitance. Hence, to achieve high speed circuits C_L must be minimized
- Secondly, it is inversely proportional to supply voltage. That is, as the supply voltage is raised the delay time is reduced
- Finally, the delay is inversely proportional to the β of the driving transistor and hence the delay decreases with β

Rise Time:

- Due to the symmetry of the CMOS circuit, a similar approach may be used to obtain the rise time, t_r

$$t_r = 2\frac{C_L}{\beta_p V_{DD}(1-p)}\left[\frac{(p-0.1)}{(1-p)} + \frac{1}{2}ln(19-20p)\right]$$

with $p = |V_{tp}|/V_{DD}$.

As before, this may be approximated by

$$t_r \cong 3 \rightarrow 4\frac{C_L}{\beta_p V_{DD}}.$$

For equally sized n- and p-transistors, where $\beta_n = 2\beta_p$,

$$t_f = \frac{t_r}{2}.$$

- Thus the fall time is faster than the rise time.
- Therefore, if we want to have approximately the same rise and fall time for an inverter, we need to make,

$$\beta_n \Big/ \beta_p = 1$$

- This implies that the channel width for the p-device must be increased to approximately 2 to 3 times that of the n-device, so

$$w_p = 2 - 3W_n$$

Delay Time:

- In most CMOS circuits, the delay of a single gate is dominated by the output rise and fall times. The delay is approximately given by

$$\mathbf{t_{dr}} = \frac{t_r}{2} \quad \text{and} \quad \mathbf{t_{df}} = \frac{t_f}{2}$$

An alternative formulation is given by

$$t_{df} = A_N \frac{C_L}{\beta_n},$$

where A_N is a process constant for a specific supply voltage. A_N has been derived as

$$A_N = \frac{1}{V_{DD}(1-n)} \left[\frac{2n}{1-n} + ln\left(\frac{2(1-n) - V_O}{V_O} \right) \right],$$

where

$$n = \frac{V_{tn}}{V_{DD}} \quad \text{and} \quad V_O = \frac{V_{out}}{V_{DD}}$$

For $V_{tn} = 0.7$ volts, $V_{DD} = 5$ volts, $V_{out} = 2.5$ volts, A_N is .283.
Similarly,

$$t_{dr} = A_p \frac{C_L}{\beta_p},$$

where A_P is a process constant for a specific supply voltage.
A_P has been derived as

$$A_p = \frac{1}{V_{DD}(1+p)} \left[\frac{-2p}{1+p} + ln \left(\frac{2(1+p) - V_O}{V_O} \right) \right],$$

where

$$p = \frac{V_{tp}}{V_{DD}}$$

For $V_{tp} = -0.7$, $V_{DD} = 5$, $V_{out} = 2.5$, A_P is .283.
The average gate delay for rising and falling transitions is

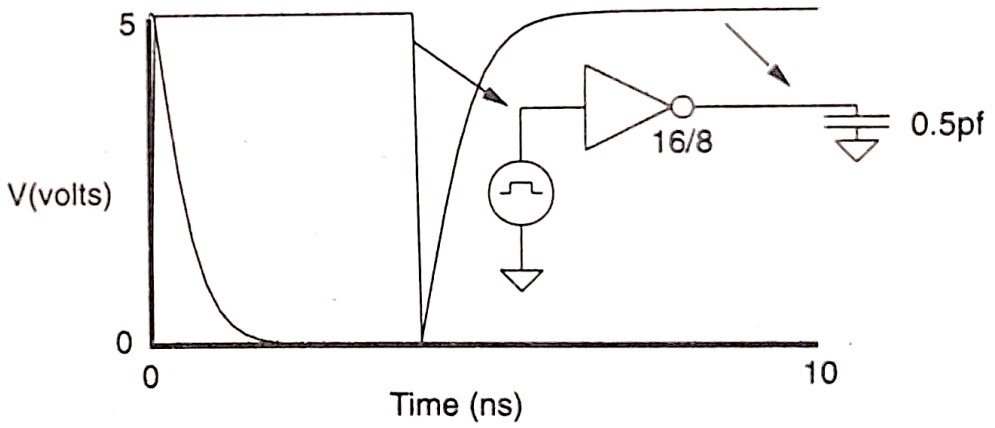
$$t_{av} = \frac{t_{df} + t_{dr}}{2}.$$

- Fig. below illustrates a SPICE simulation of a step input applied to an inverter driving a capacitive load.
- The process parameters for the simulation are:

  V_{tn} = 0.767 volts, V_{tp} = -0.938 volts, $\beta_n = 4.04 \times 10^{-4}$, $\beta_p = 3.48 \times 10^{-4}$, V_{DD} = 5 volts, C_L = 0.5pF

  Substituting these in eqns. for t_r, t_f , t_{dr} & t_{df} we get,

  t_r = 1.04ns, compared with 1.14ns from SPICE (level 1)
  t_f = 0.83ns, compared with 0.89ns from SPICE (level 1)
  t_{df} = 0.5ns, compared with 0.52ns from SPICE (level 1)
  t_{dr} = 0.4ns, compared with 0.45ns from SPICE (level 1)



Empirical Delay Models

- In an empirical delay model, a circuit simulator is used to model the inverter or gate in question and then the measured values are back substituted into appropriate delay equations

Ex.: One can back substitute into below equations to obtain values for A_N and A_P.

$$t_{df} = A_N \frac{C_L}{\beta_n} \quad \text{and} \quad t_{dr} = A_P \frac{C_L}{\beta_p}$$

$$A_P = t_{dr-spice}\frac{\beta_p}{C_L} = .52 \times 10^{-9} \times \frac{3.48 \times 10^{-4}}{0.5 \times 10^{-12}} = .36\ (.31\ \text{calc})$$

$$A_N = t_{df-spice}\frac{\beta_n}{C_L} = .45 \times 10^{-9} \times \frac{4.04 \times 10^{-4}}{0.5 \times 10^{-12}} = .36\ (.29\ \text{calc}).$$

These constants may now be used to predict delay values for a wide range of gates. That is, for gates with $W_p = 2W_n$,

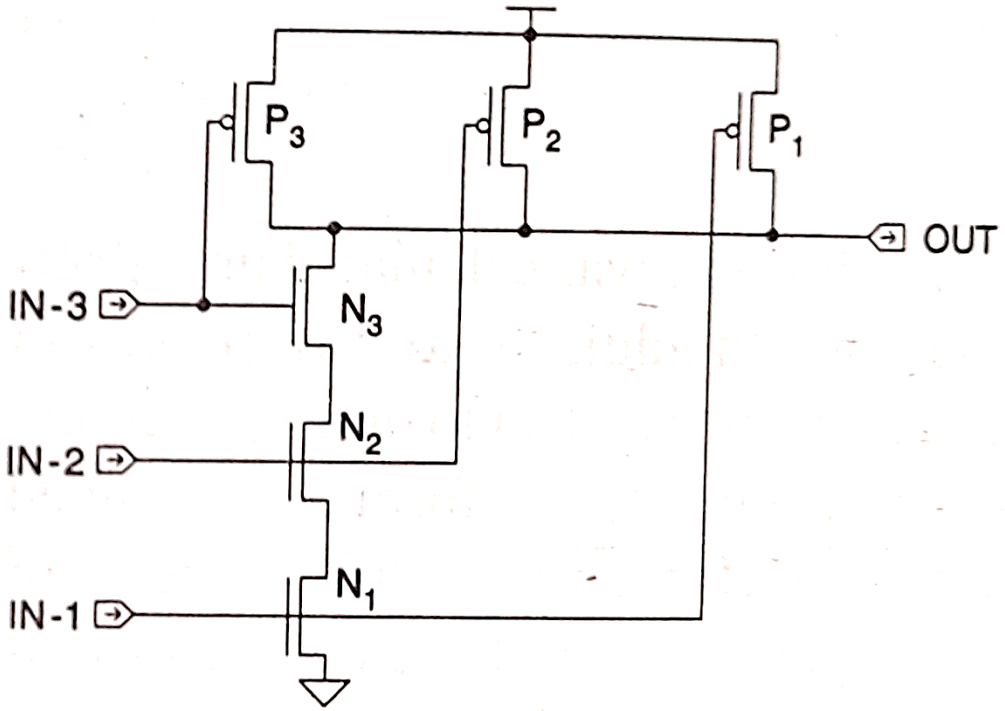
$$t_{dr} = .36\frac{C_L}{\beta_p} \qquad t_{df} = .36\frac{C_L}{\beta_n}.$$

- Notice that these equations now represent the delay in terms of an RC delay where the effective resistance of the transistor is given by 0.36/β

Gate Delays

- The delay of simple gates may be approximated by constructing an “equivalent” inverter.

- **Ex:** 3-input NAND gate



$$\beta_{neff} = \frac{1}{\frac{1}{\beta_{n1}} + \frac{1}{\beta_{n2}} + \frac{1}{\beta_{n3}}} \quad \text{(summation of series conductances)} \qquad \textbf{(4.51)}$$

For $\beta_{n1} = \beta_{n2} = \beta_{n3}$

$$\beta_{neff} = \frac{\beta_n}{3}.$$

For the pull-up case, only one p-transistor has to turn on to raise the output. Thus,

$$\beta_{peff} = \beta_p.$$

For $\beta_p = 0.3\,\beta_n$

$$t_r = k\frac{C_L}{0.3\beta_n V_{DD}},\quad t_f = k\frac{C_L}{\frac{\beta_n}{3}V_{DD}}$$

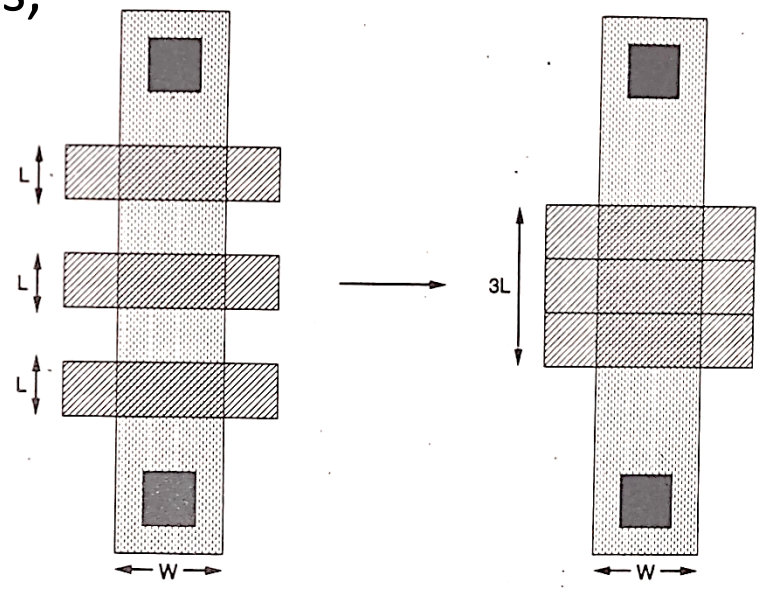
$$\frac{t_r}{t_f} \approx 1.$$

For a more graphical understanding of this,

$\beta_{series} = \beta_n/3$

Hence,

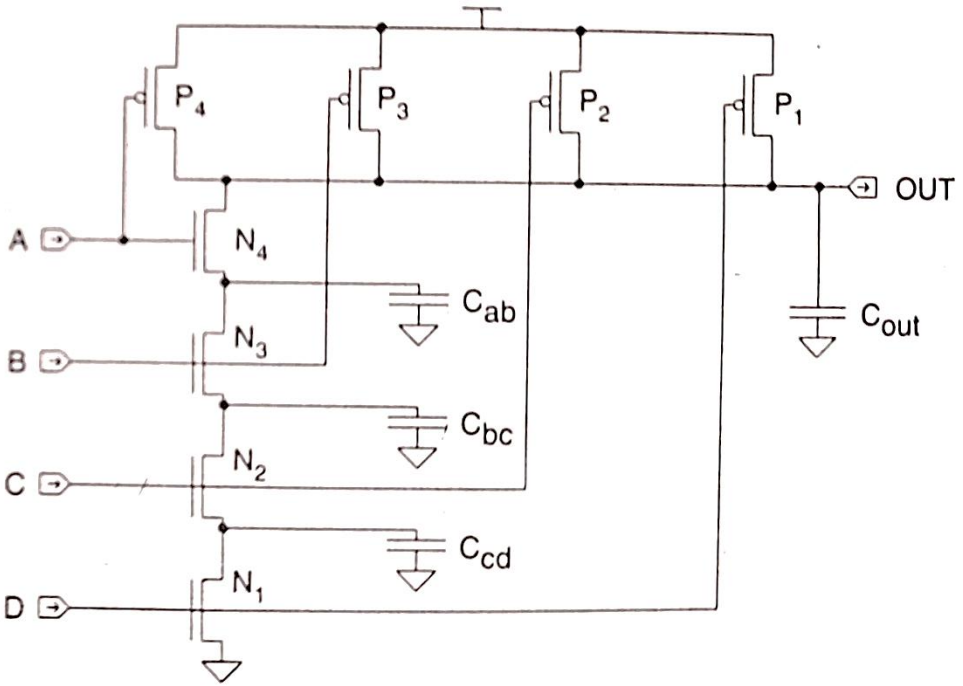
$$\tau_{series} = k\frac{C_L}{\frac{\beta_n}{3}V_{DD}}$$



Switch-Level RC Models

RC modeling techniques represent transistors as a resistance discharging or charging a capacitance.

- Simple RC Delay Model
- Penfield-Rubenstein Delay Model
- Penfield-Rubenstein Slope Delay Model



Simple RC Delay Model

Penfield-Rubenstein Delay Model

Penfield-Rubenstein Slope Model