Q & A

- IF THE WIDTH OF A TRANSISTOR INCREASES, THE CURRENT WILL

  INCREASE DECREASE NOT CHANGE

- IF THE LENGTH OF A TRANSISTOR INCREASES, THE CURRENT WILL

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- IF THE SUPPLY VOLTAGE OF A CHIP INCREASES, THE MAXIMUM TRANSISTOR CURRENT WILL

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- IF THE WIDTH OF A TRANSISTOR INCREASES, ITS GATE CAPACITANCE WILL

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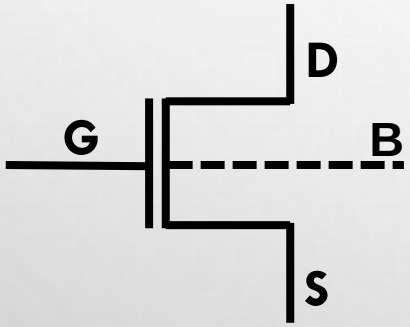
CMOS INVERTER DESIGN

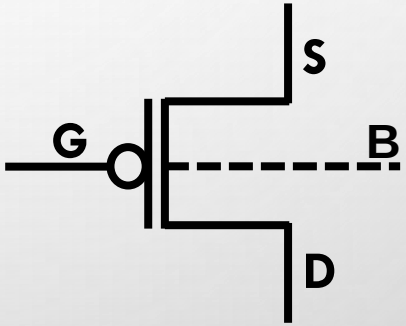
- Prashanth Kumar Shetty
MSIS, Manipal

CMOS INVERTER

CMOS inverter makes use of both NMOS and PMOS transistors



NMOS

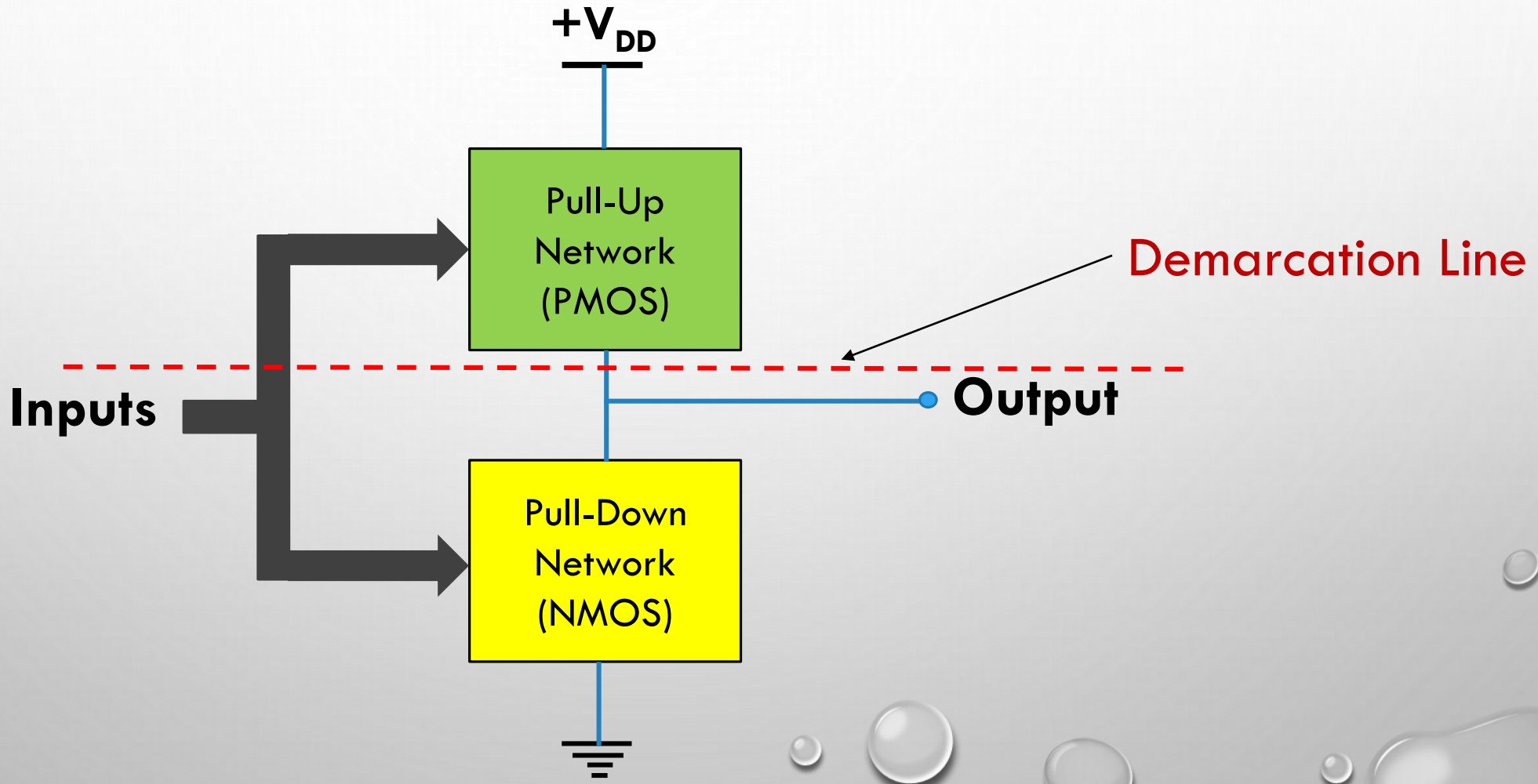


PMOS

OUTLINE

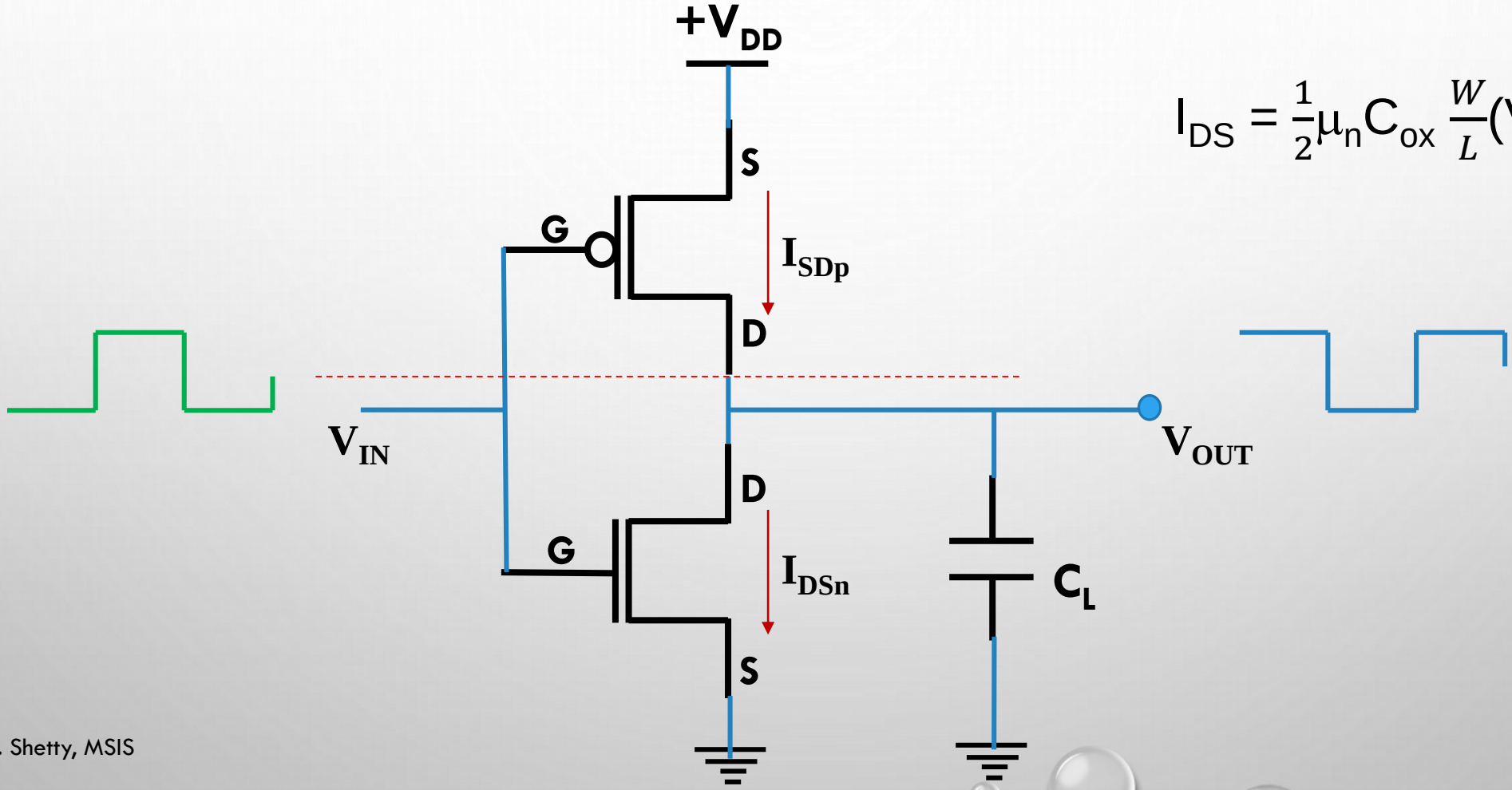
- ROBUSTNESS OF CMOS INVERTER – THE STATIC BEHAVIOR
  - SWITCHING THRESHOLD
  - NOISE MARGINS
- PERFORMANCE OF CMOS INVERTER – DYNAMIC BEHAVIOR
  - PROPAGATION DELAY
- POWER DISSIPATION
  - STATIC DISSIPATION
  - DYNAMIC DISSIPATION

CMOS CIRCUITS



CMOS INVERTER CIRCUIT

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_T)^2$$



Choosing the P and N Transistor Sizes

Two principal objectives: *Drive strength, Speed, Power, Noise margin*

- *To balance rise and fall drive strengths* $\Rightarrow$ Conductances should be made equal

  $\mu_n \approx K \mu_p$ where K = 2.7

  $\therefore W_p = K W_n$

- *To make the gate as fast as possible*

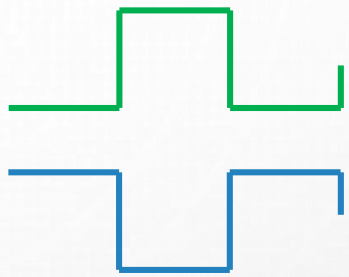
  Theoretically, the P to N transistor ratio which gives the fastest delay is $K^{0.5}$

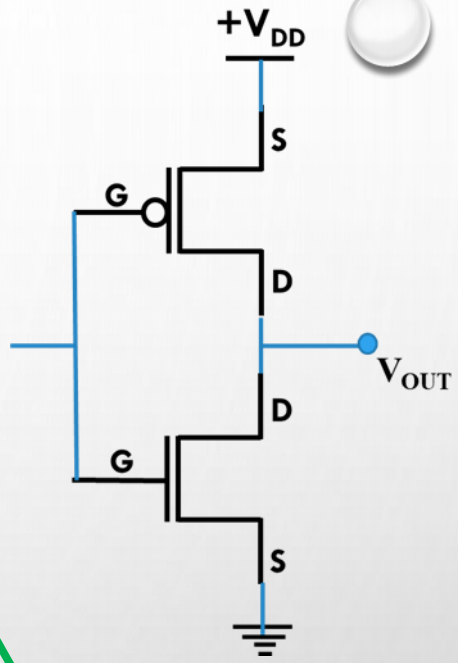
  For an inverter, if K=2.7, this means a P:N transistor ratio of about **1.6**

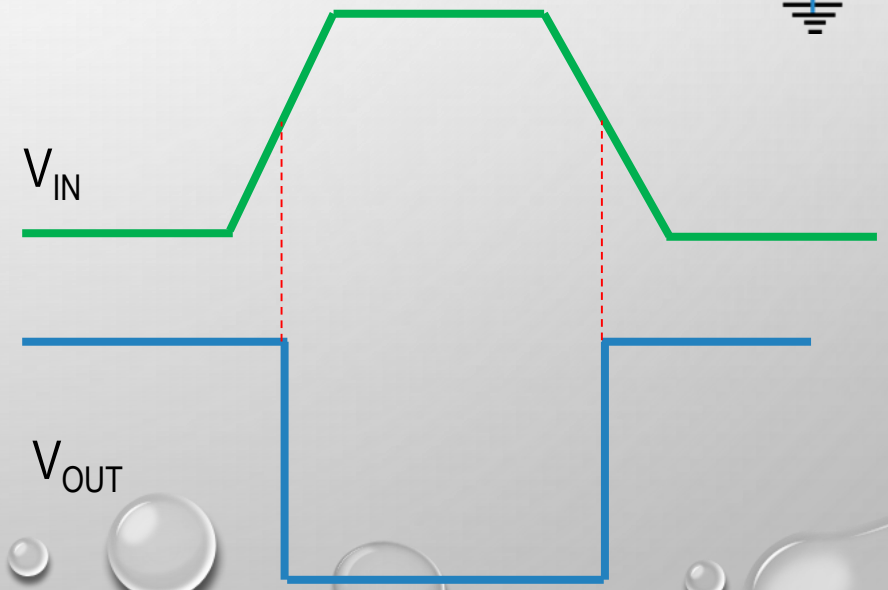
For inverters, a ratio of P=2N is commonly chosen as a compromise between fastest speed and balanced outputs.

CMOS INVERTER: DC ANALYSIS

- DC RESPONSE: V_{OUT} VS. V_{IN} FOR A GATE
- INVERTER
  - WHEN $V_{IN} = 0 \rightarrow V_{OUT} = V_{DD}$
  - WHEN $V_{IN} = V_{DD} \rightarrow V_{OUT} = 0$
  - IN BETWEEN, V_{OUT} DEPENDS ON TRANSISTOR CURRENT
  - BY KCL, MUST SETTLE SUCH THAT: $I_{DSN} = |I_{DSP}|$
  - WE CAN SOLVE EQUATIONS
  - GRAPHICAL SOLUTION GIVES VERY GOOD INSIGHT







TRANSISTORS OPERATION REGIONS

- CURRENT DEPENDS ON TRANSISTOR'S OPERATION REGION
- FOR WHAT V_{IN} AND V_{OUT} ARE NMOS AND PMOS IN
  - CUTOFF ?
  - LINEAR ?
  - SATURATION ?

NMOS AND PMOS OPERATION

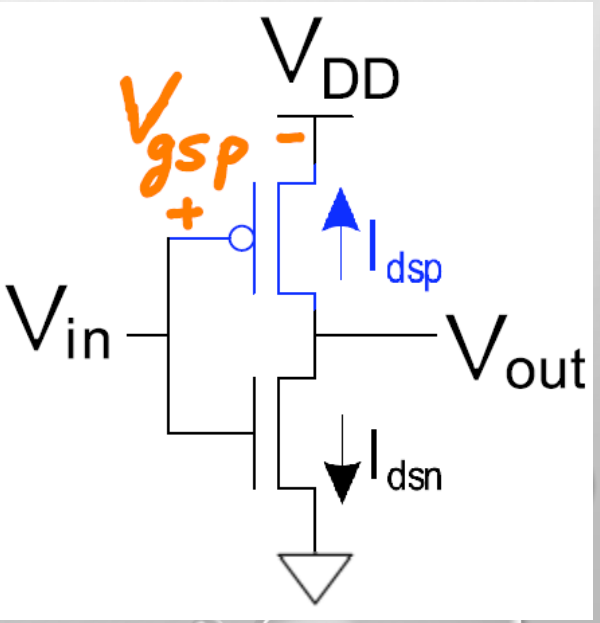
$V_{GSN} = V_{IN}$

$V_{DSN} = V_{OUT}$

$V_{GSP} = V_{IN} - V_{DD}$

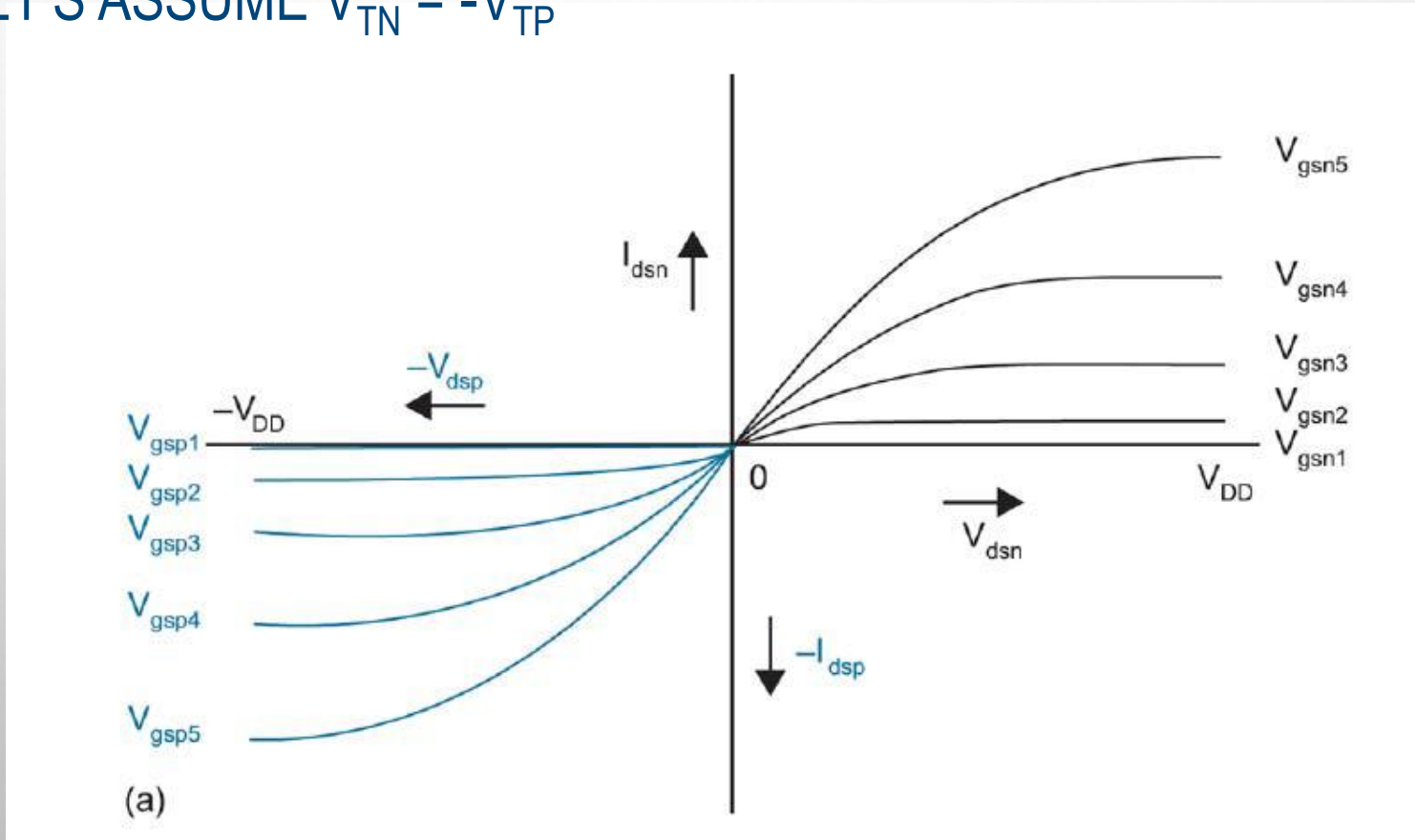
$V_{DSP} = V_{OUT} - V_{DD}$

	Relationships between voltages for the three regions of operation of a CMOS inverter		
	Cutoff	**Linear**	**Saturated**
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$



GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: **I-V** CHARACTERISTICS

- MAKE PMOS WIDER THAN NMOS SUCH THAT $B_N = B_P$
- FOR SIMPLICITY LET'S ASSUME $V_{TN} = -V_{TP}$

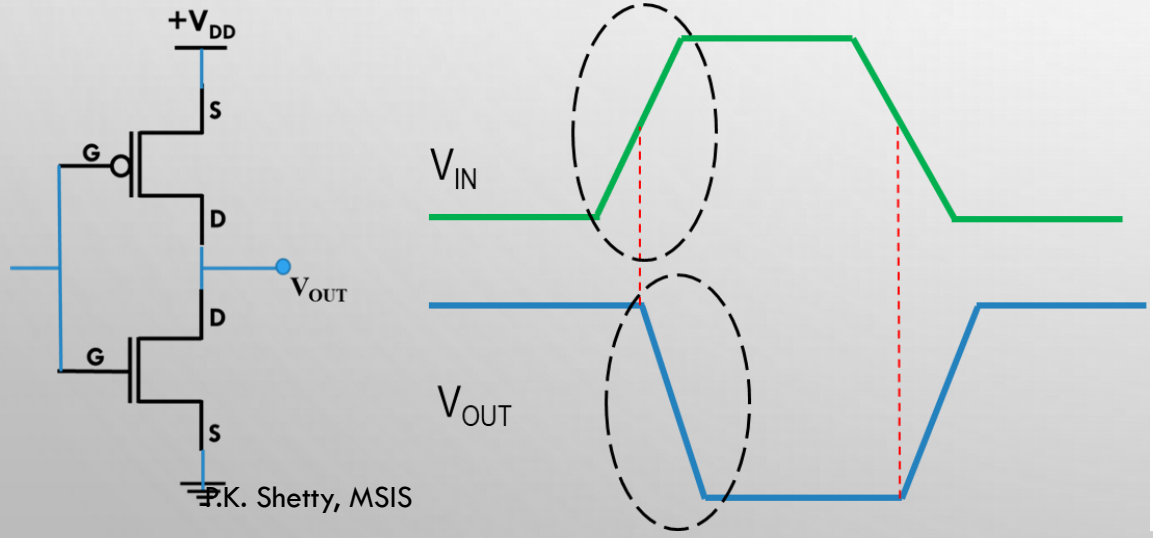


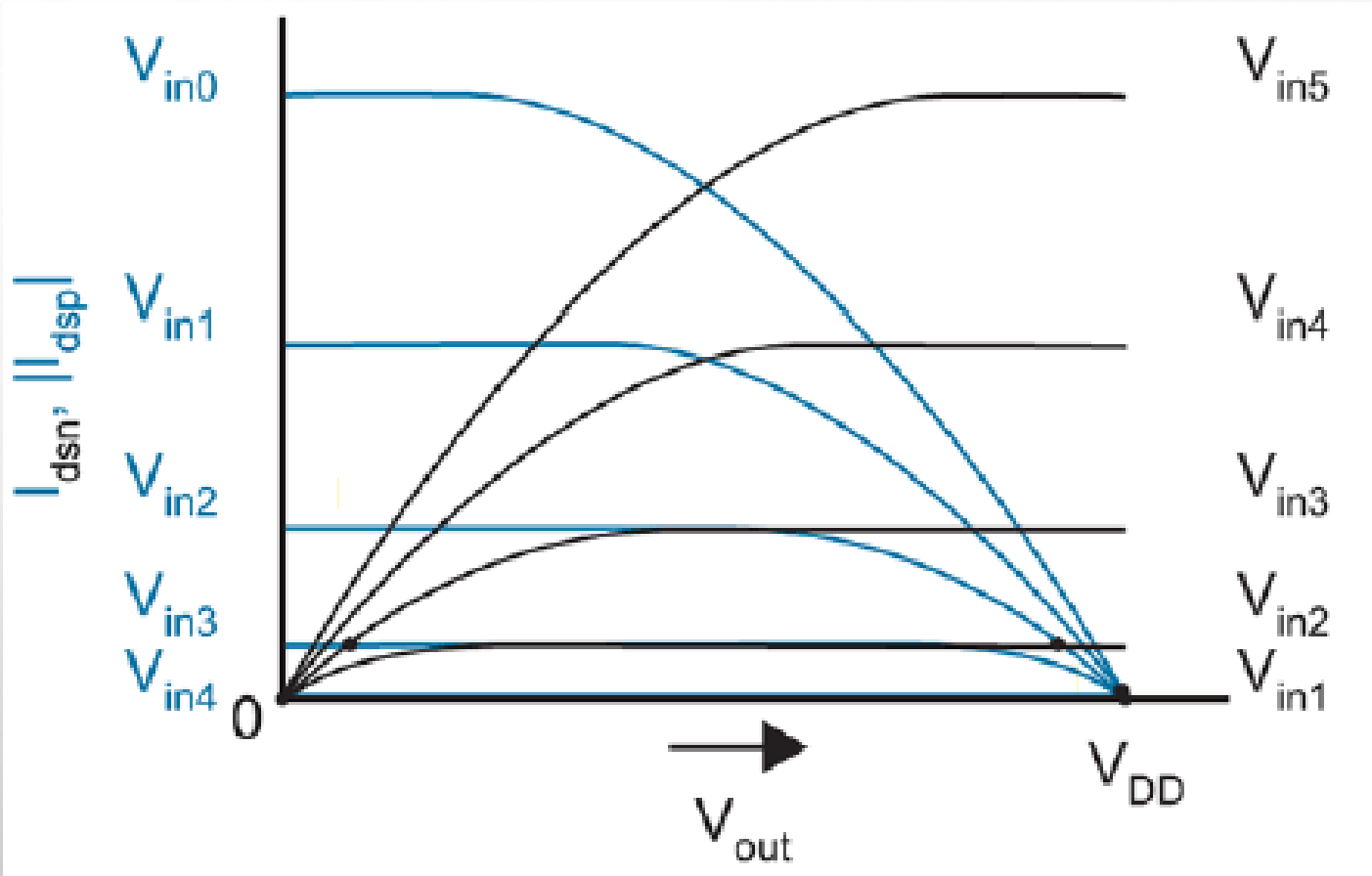
GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: I_{DS} vs. V_{out}, V_{in}

- LOAD LINE ANALYSIS:

  FOR A GIVEN VIN:

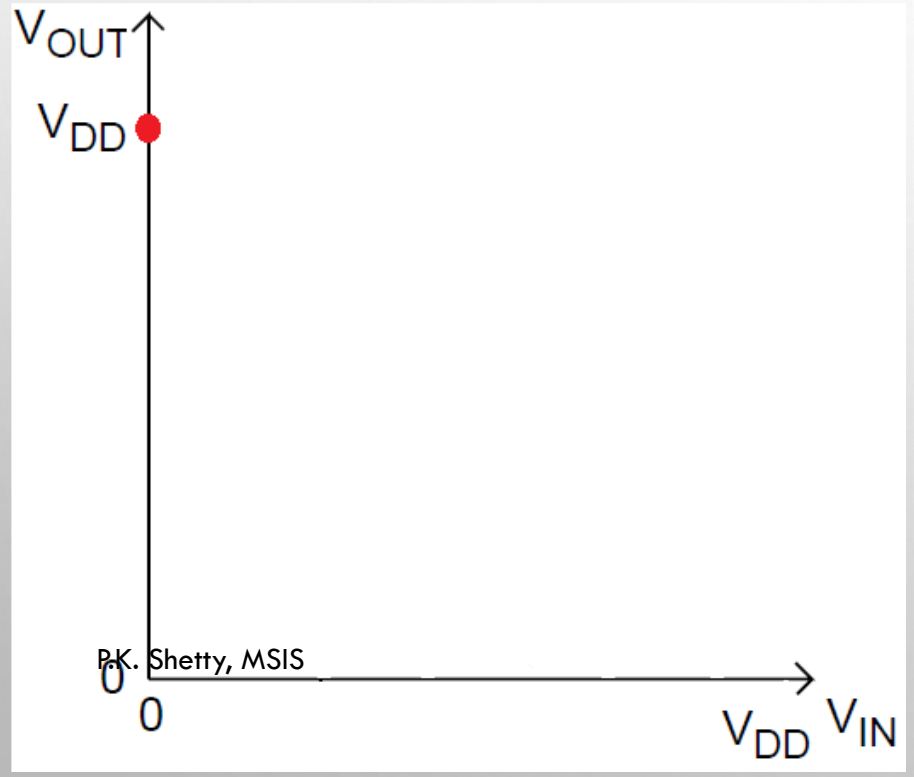
  - PLOT IDSN, IDSP VS. VOUT
  - VOUT MUST BE WHERE |CURRENTS| ARE EQUAL

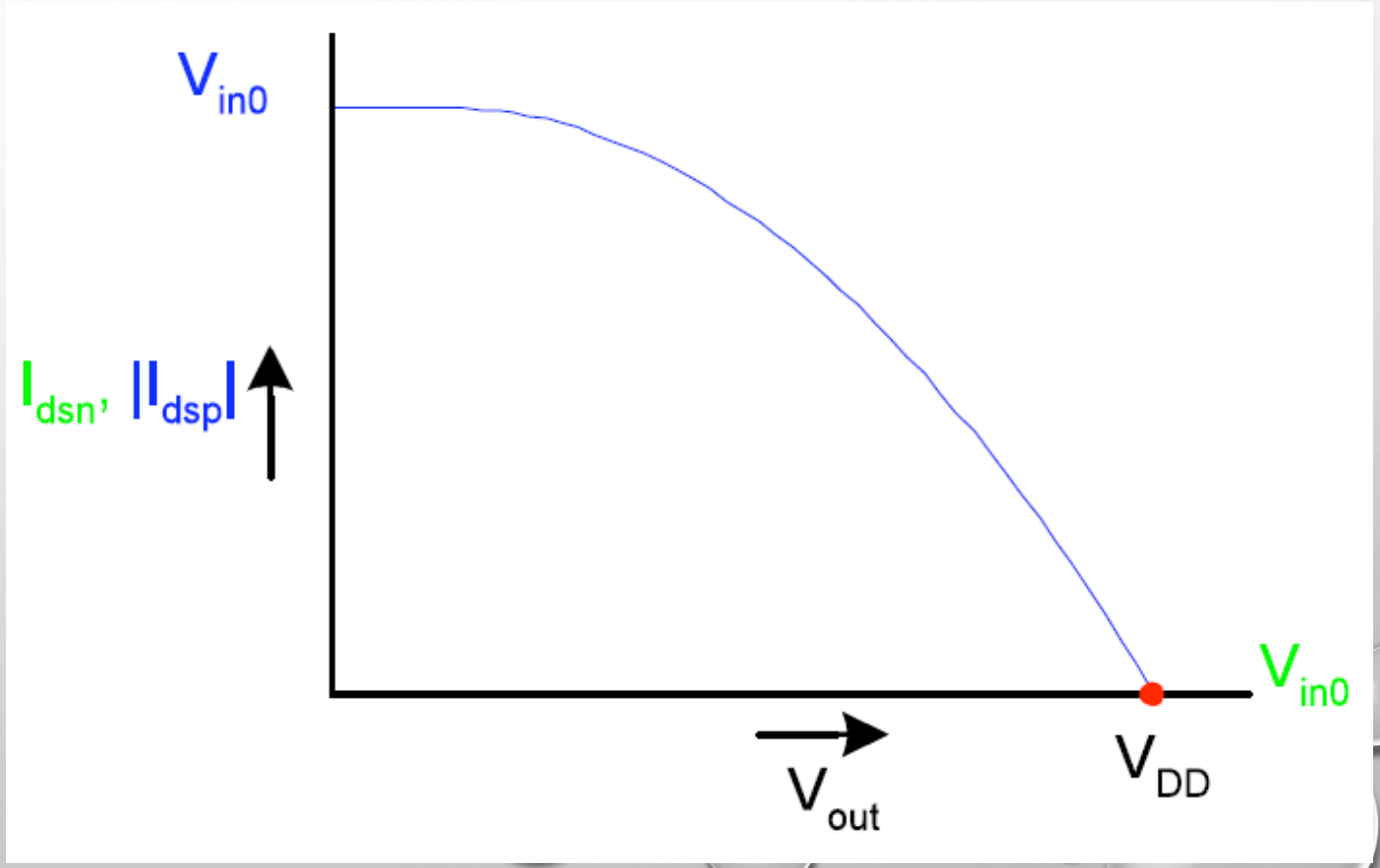




GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: LOAD LINE ANALYSIS

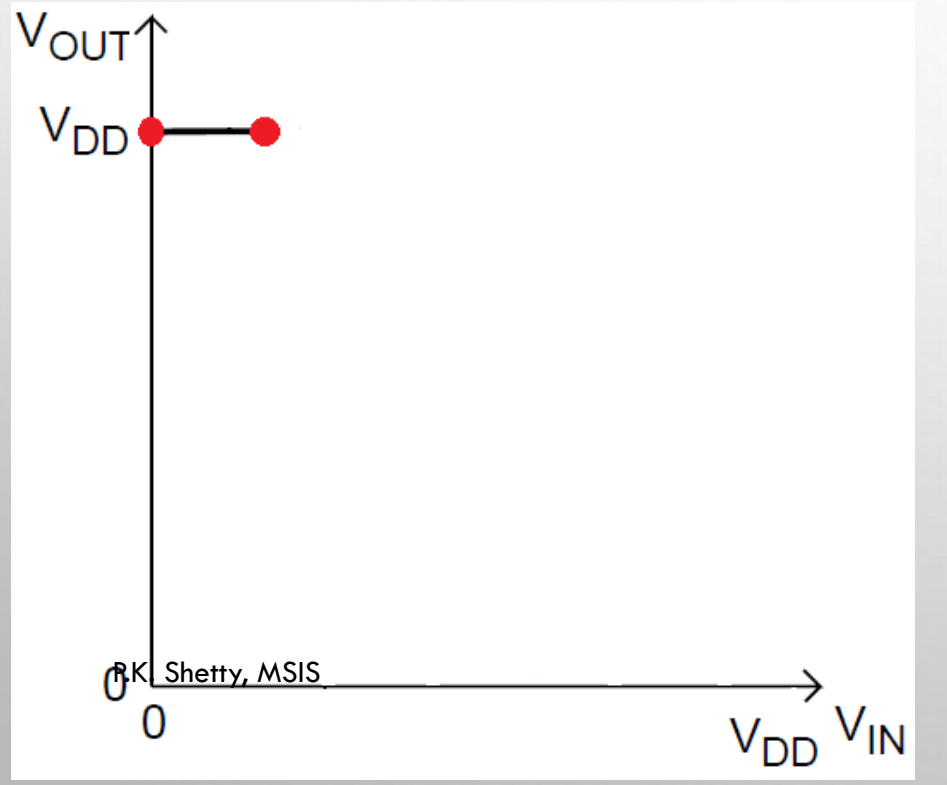
- $V_{IN} = 0$

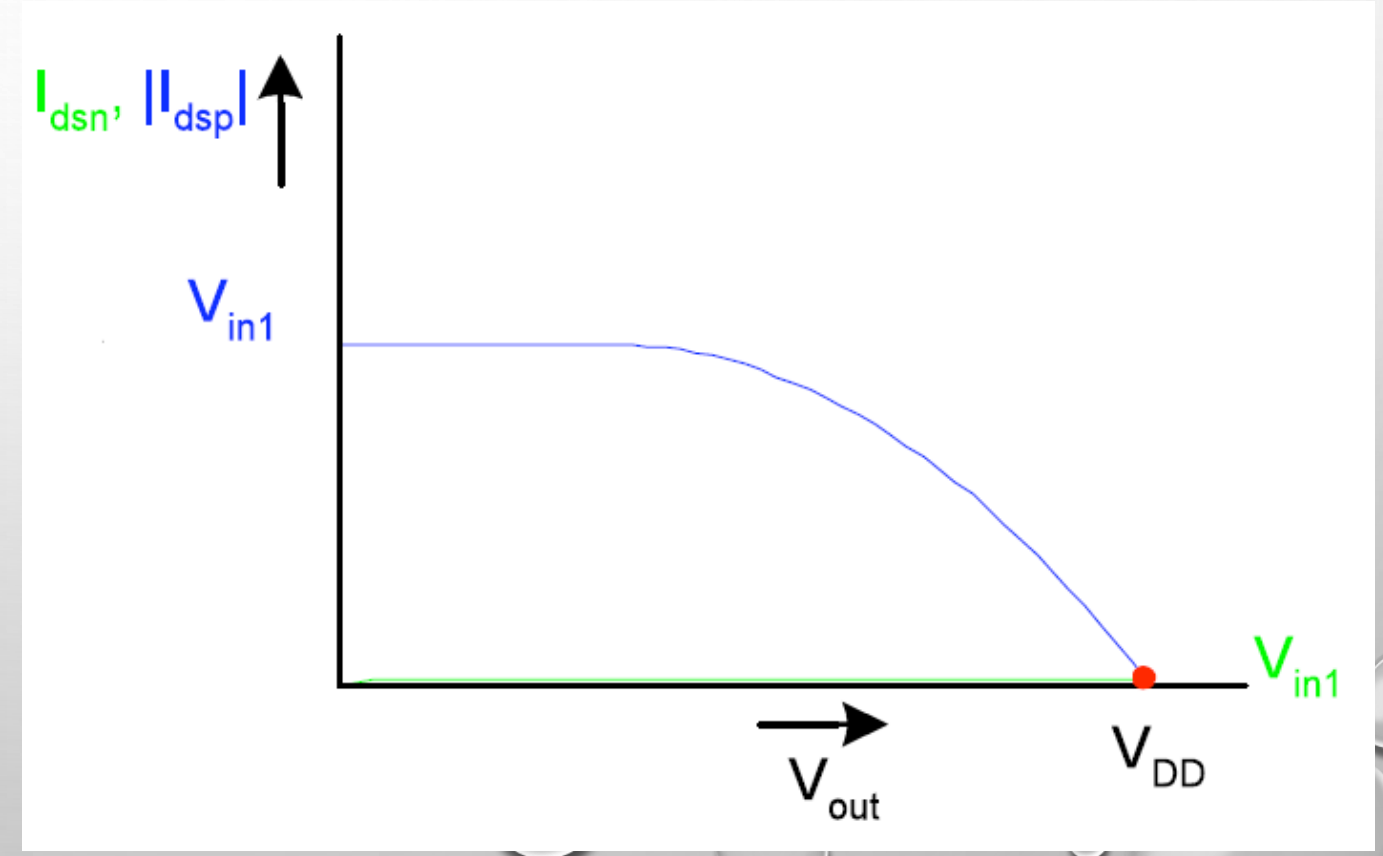




GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: LOAD LINE ANALYSIS

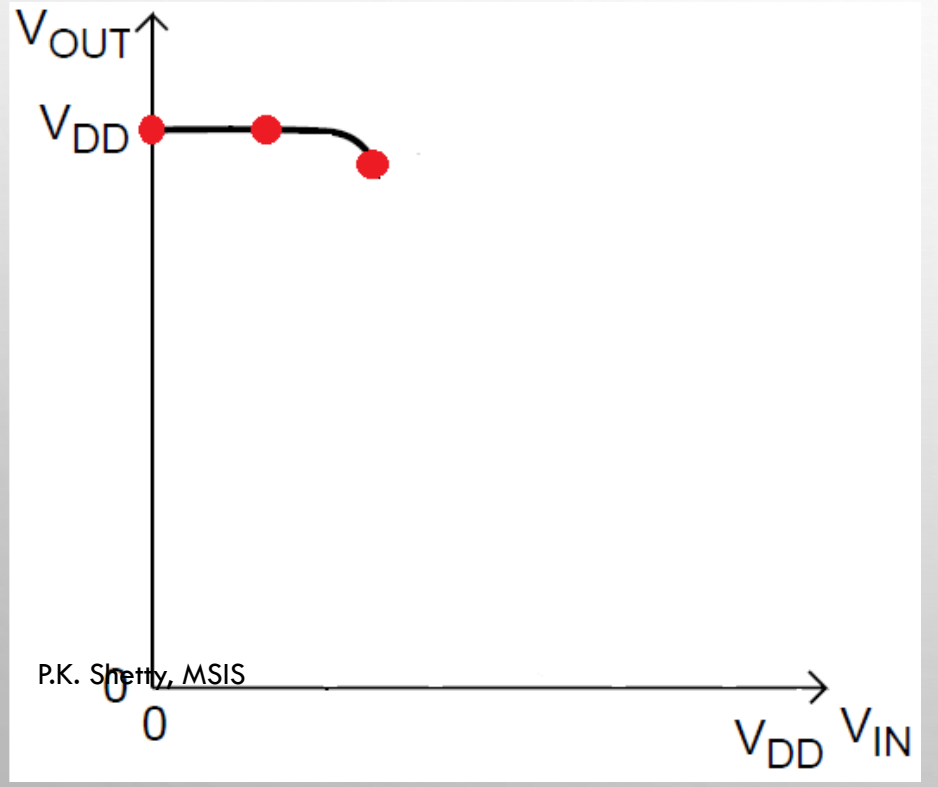
- $V_{IN} = 0.2V_{DD}$

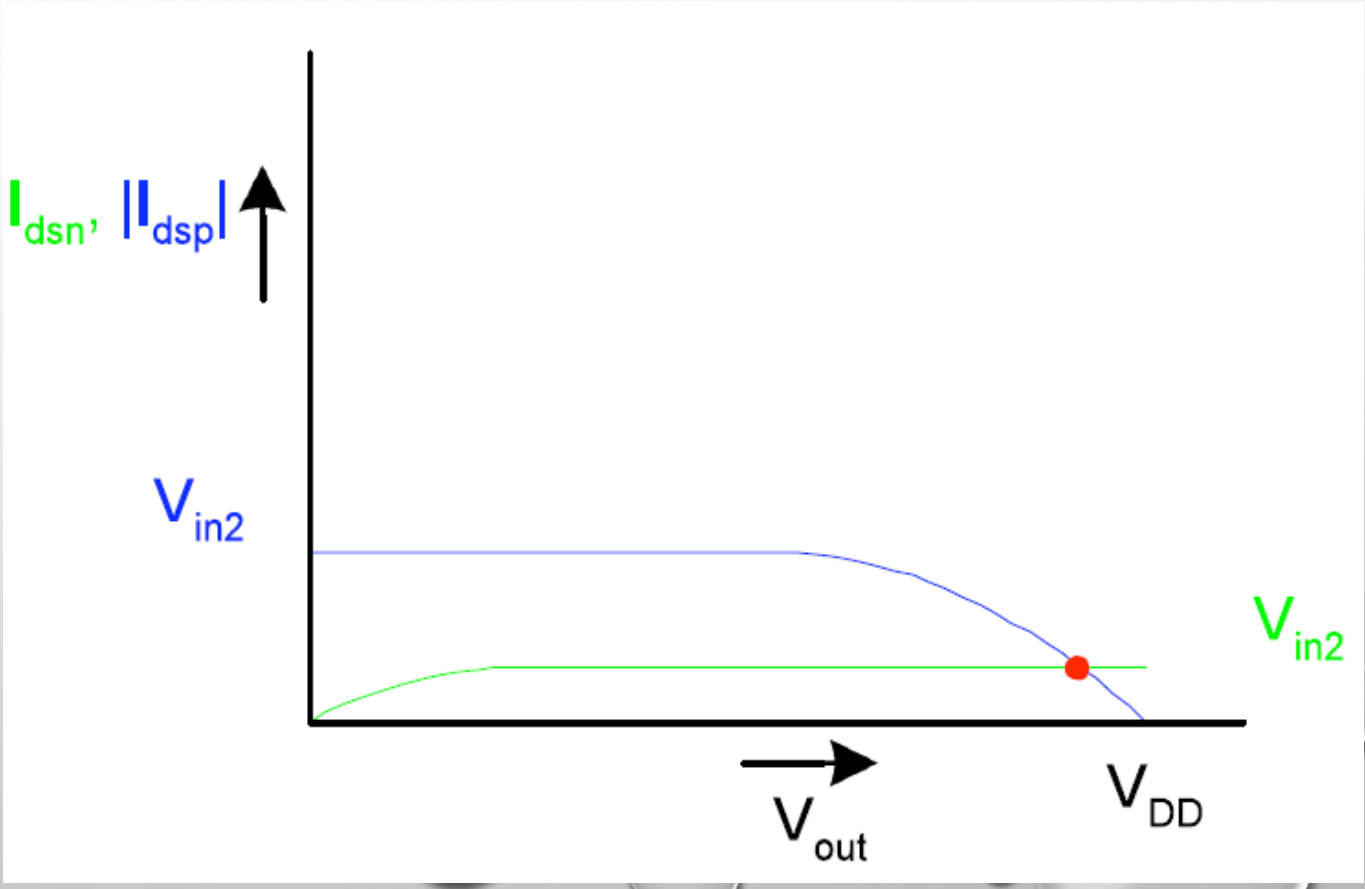




GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: LOAD LINE ANALYSIS

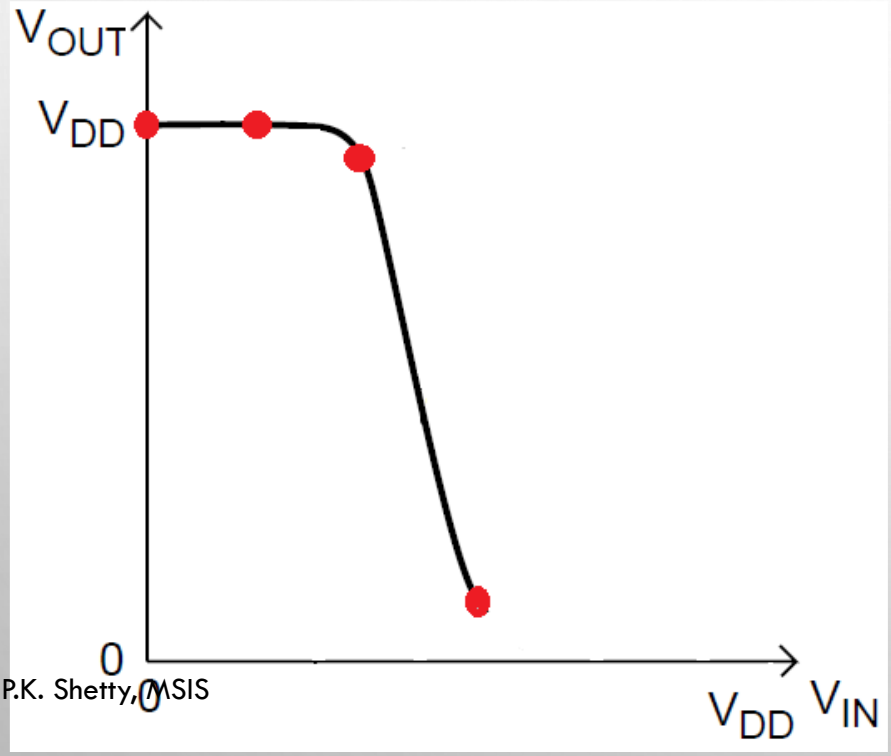
- $V_{IN} = 0.4V_{DD}$

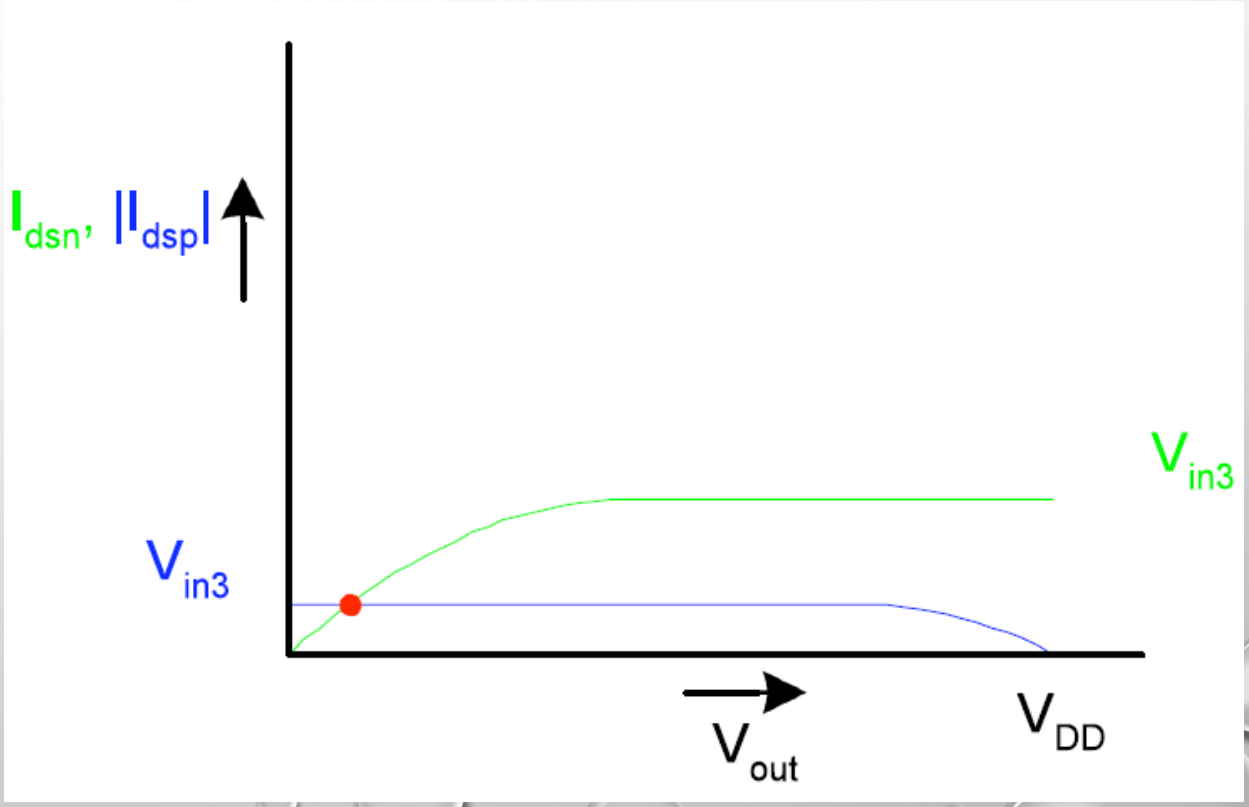




GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: LOAD LINE ANALYSIS

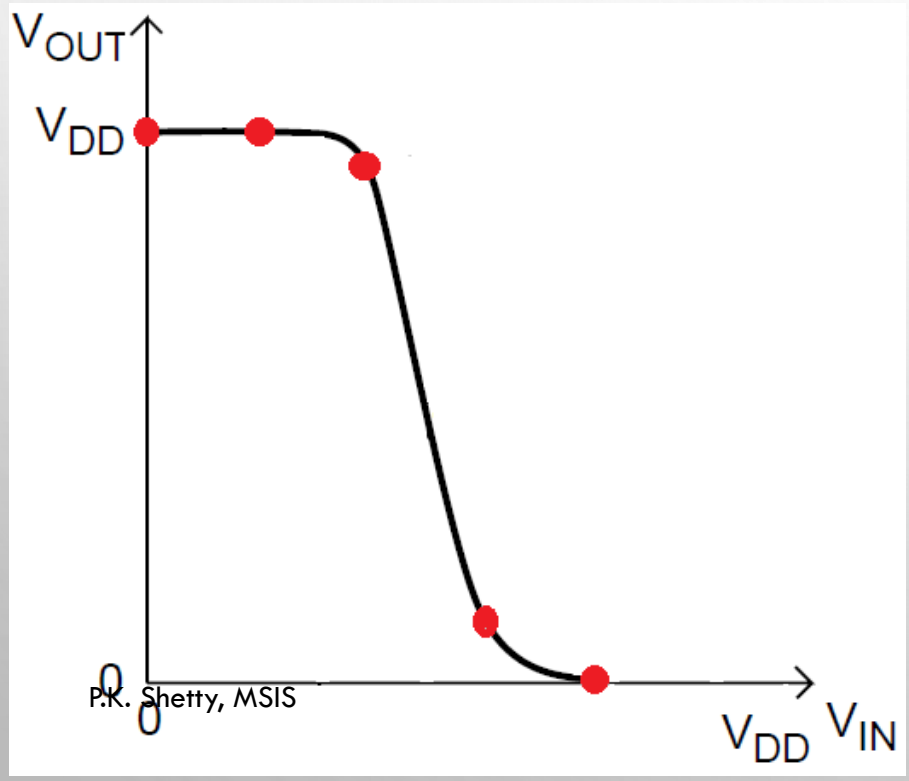
- $V_{IN} = 0.6V_{DD}$

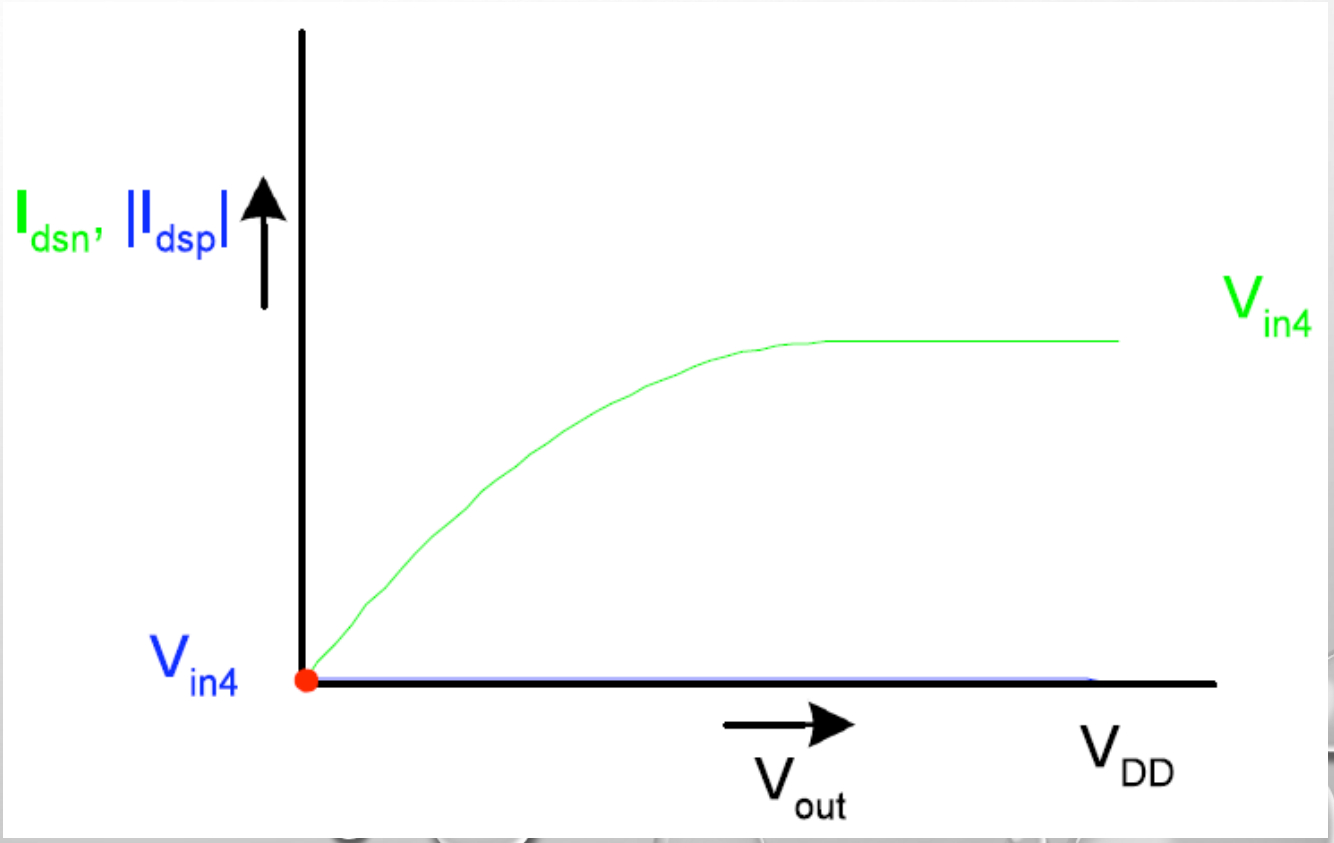




GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: LOAD LINE ANALYSIS

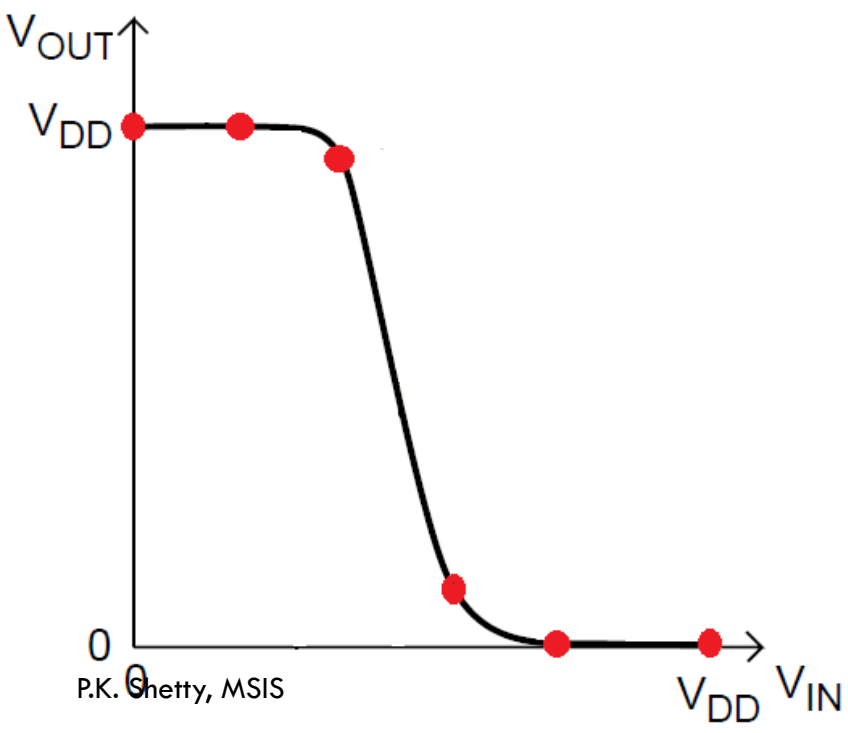
- $V_{IN} = 0.8V_{DD}$

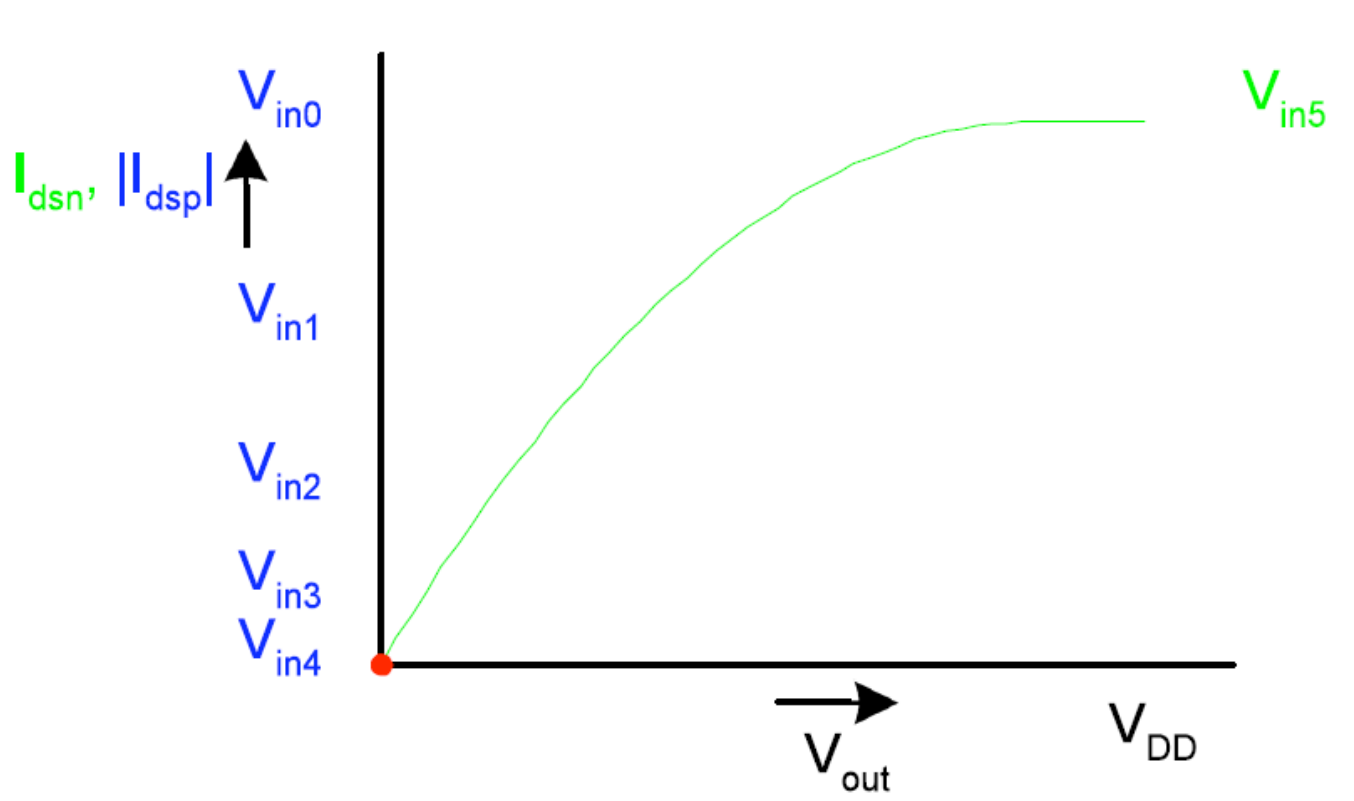




GRAPHICAL DERIVATION OF THE INVERTER DC RESPONSE: LOAD LINE ANALYSIS

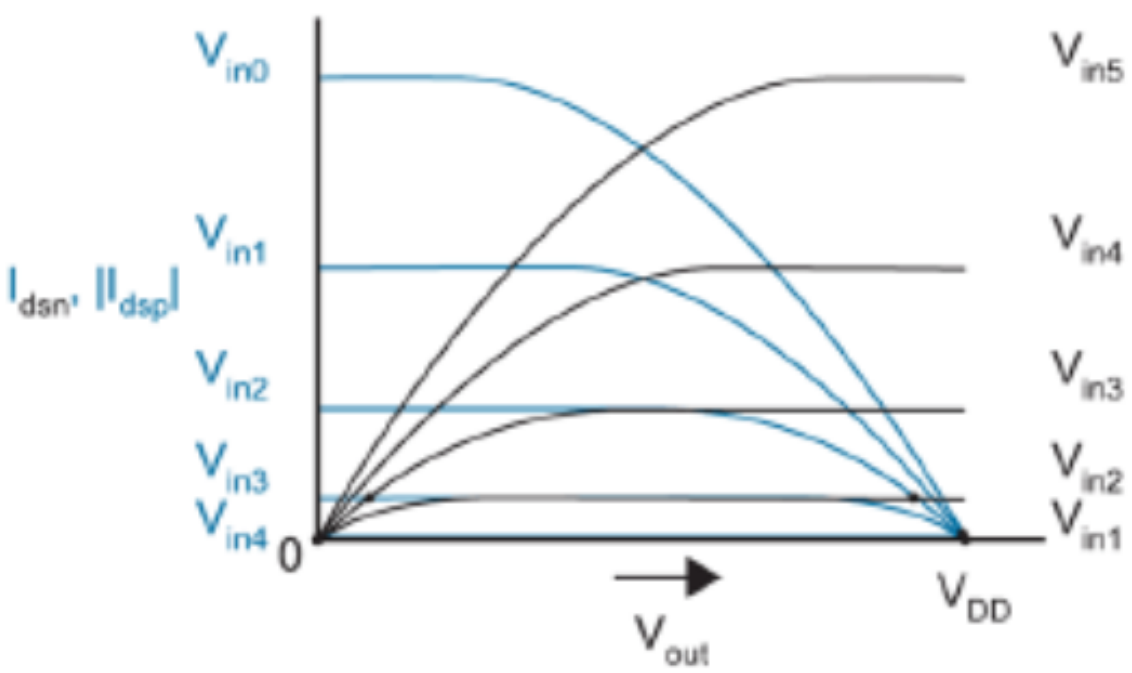
- $V_{IN} = V_{DD}$

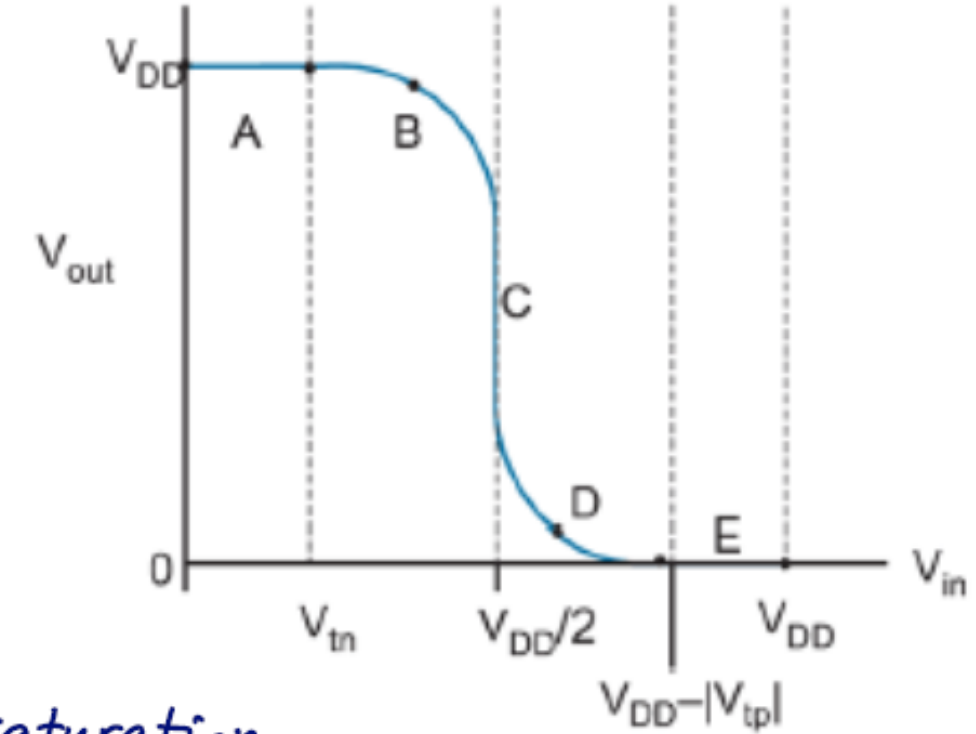




DC TRANSFER CURVE

- TRANSCRIBE POINTS ONTO V_{IN} VS. V_{OUT} PLOT

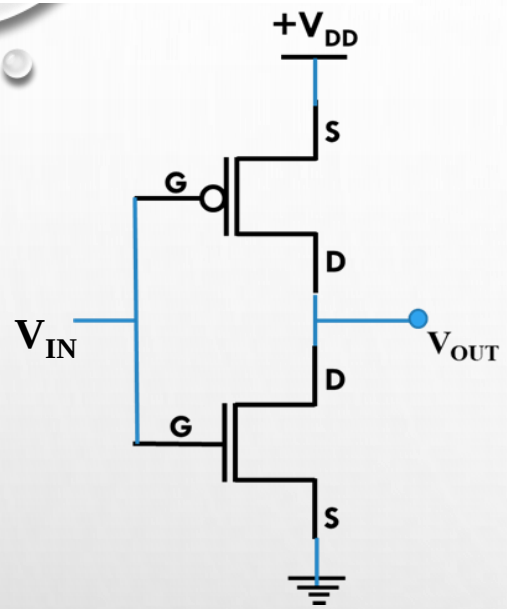




In region C both transistors are in saturation.

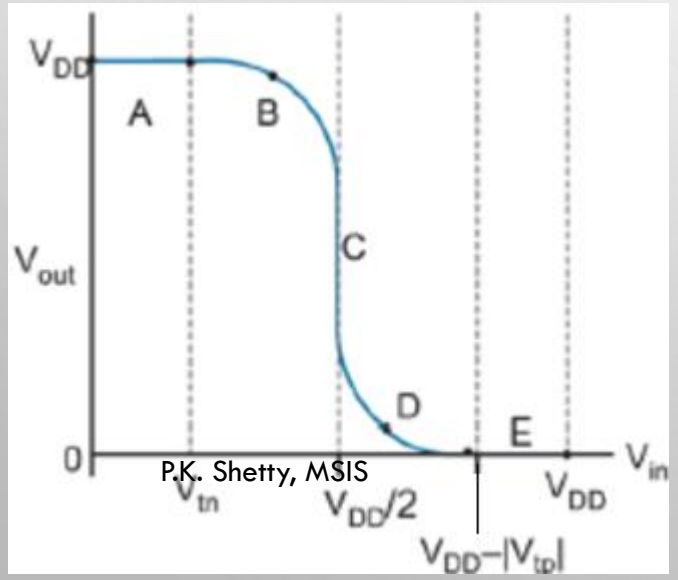
Ideal transistors are only in region C for $V_{in} = \frac{V_{DD}}{2}$ and the DC curve slope in C is $-\infty$.

The crossover point where $V_{in} = V_{out}$ is called input threshold.



Relationships between voltages for the three regions of operation of a CMOS inverter

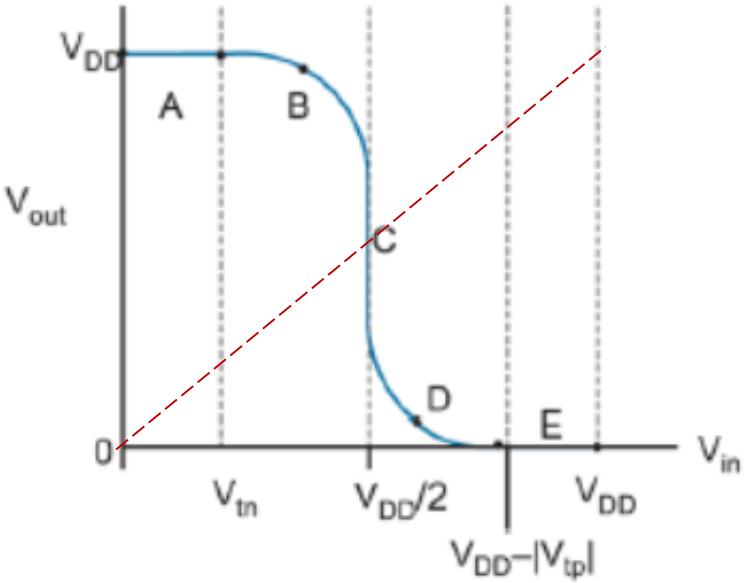
	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

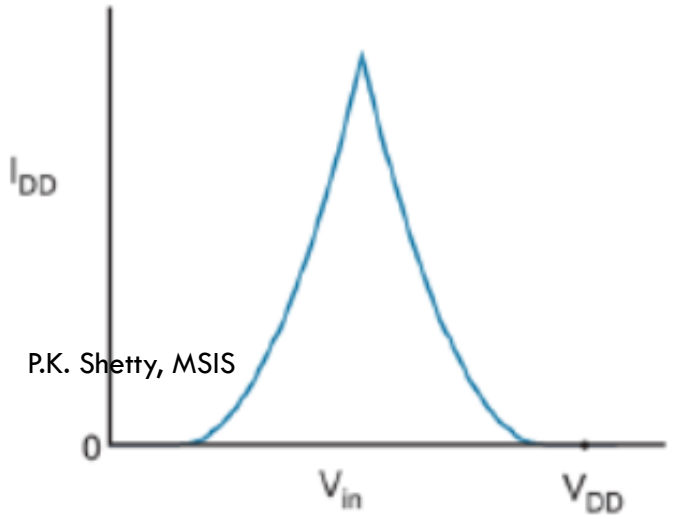


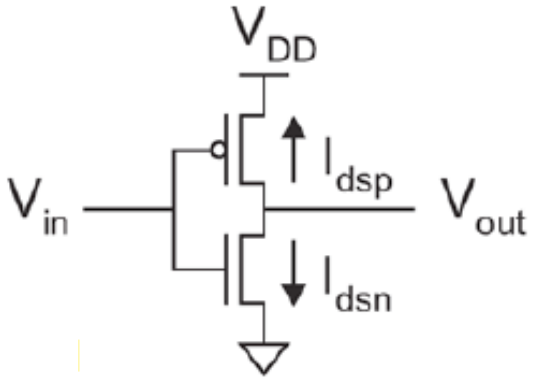
Summary of CMOS inverter operation

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$

DC TRANSFER CURVE: OPERATING REGIONS





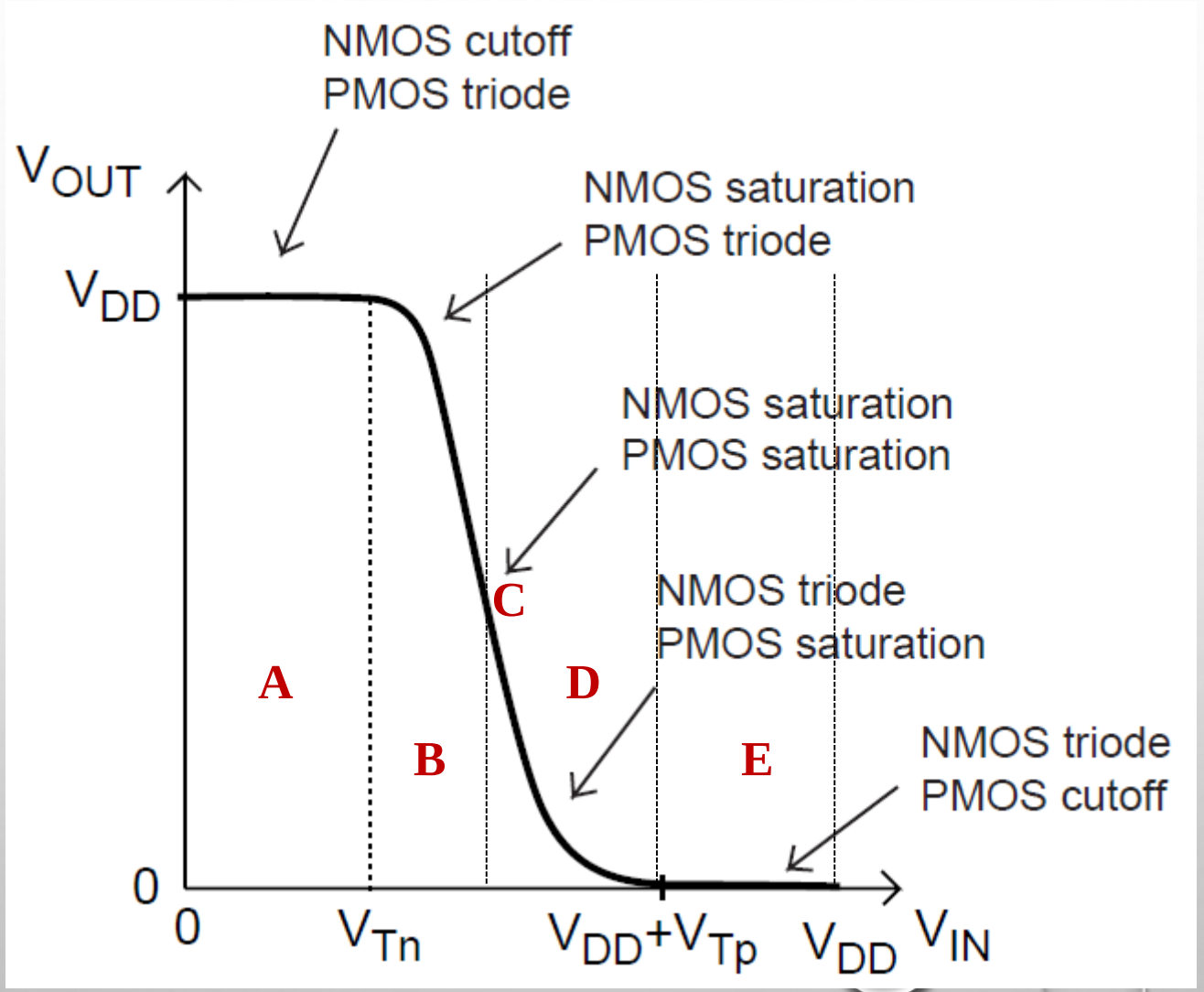


A CMOS inverter

Summary of CMOS inverter operation

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \|V_{tp}\|$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \|V_{tp}\|$	cutoff	linear	$V_{out} = 0$

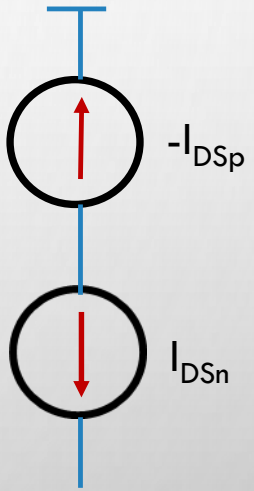
Inverter Voltage Transfer Curve



Inverter Threshold, V_{INV}

In Region C, both the transistors are in saturation region. That is equivalent to two current sources are in series which is an unstable condition.

$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

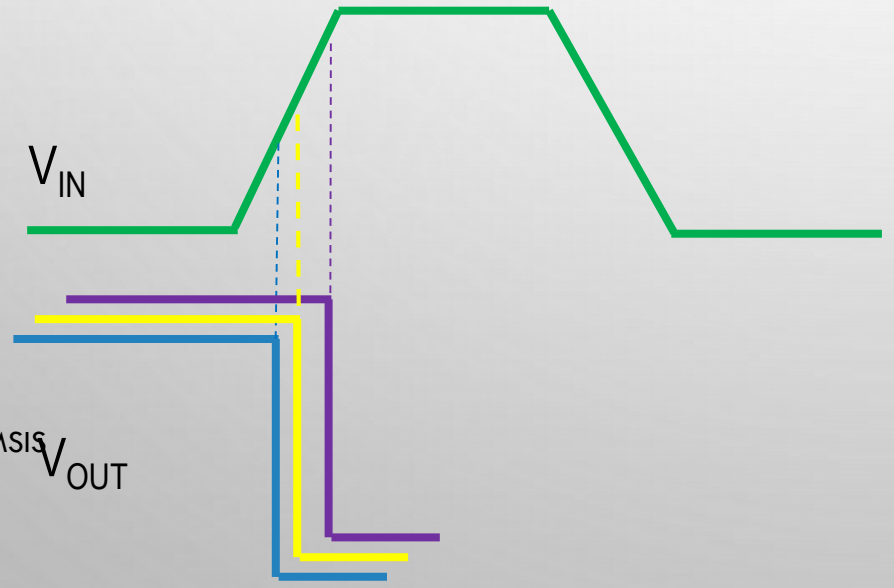


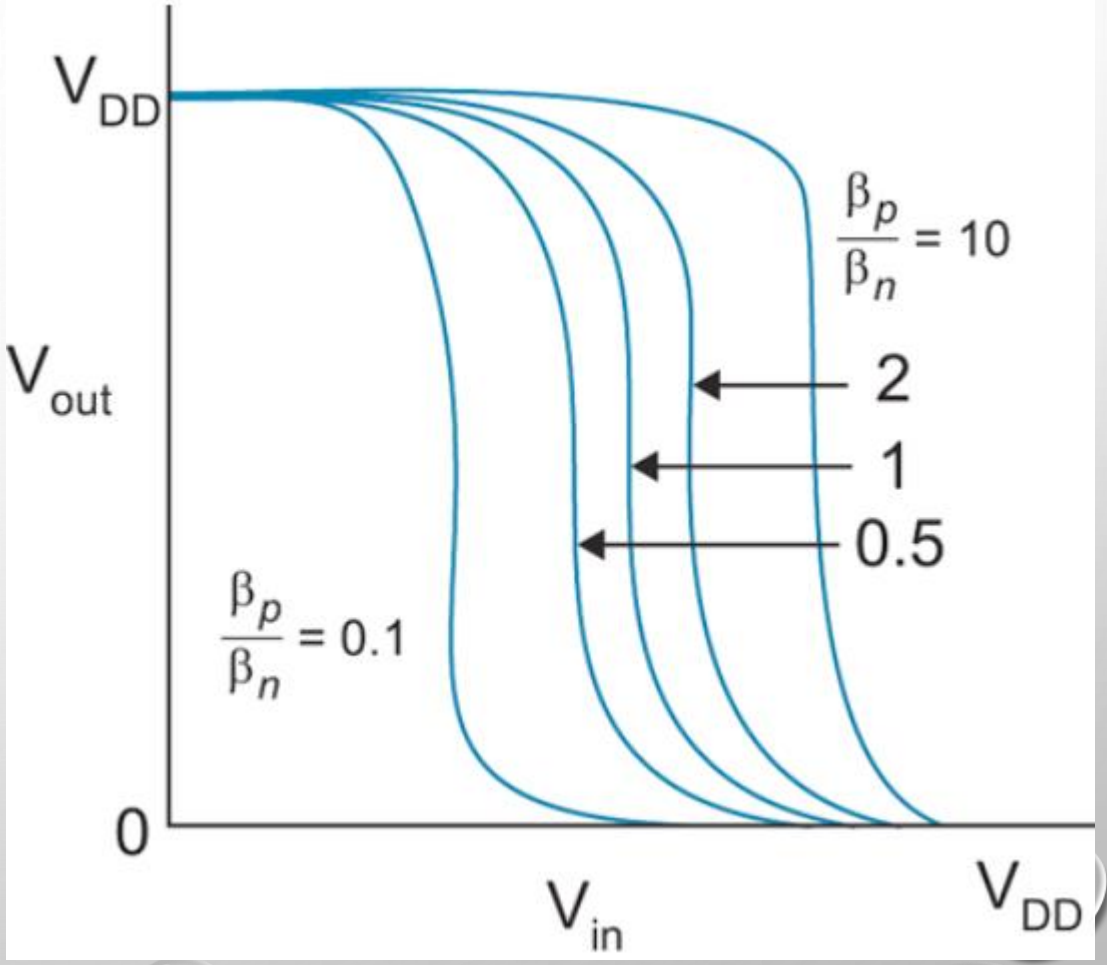
In this point, $V_{in} = V_{out}$ and actual state transition takes place at this point. Hence this is also called as Inverter Threshold, $\mathbf{V_{inv}}$.

If $V_{tn} = -V_{tp}$ and $\beta_n = \beta_p$, then, $\mathbf{V_{in} = V_{DD}/2}$ $\Rightarrow$ Good noise margin

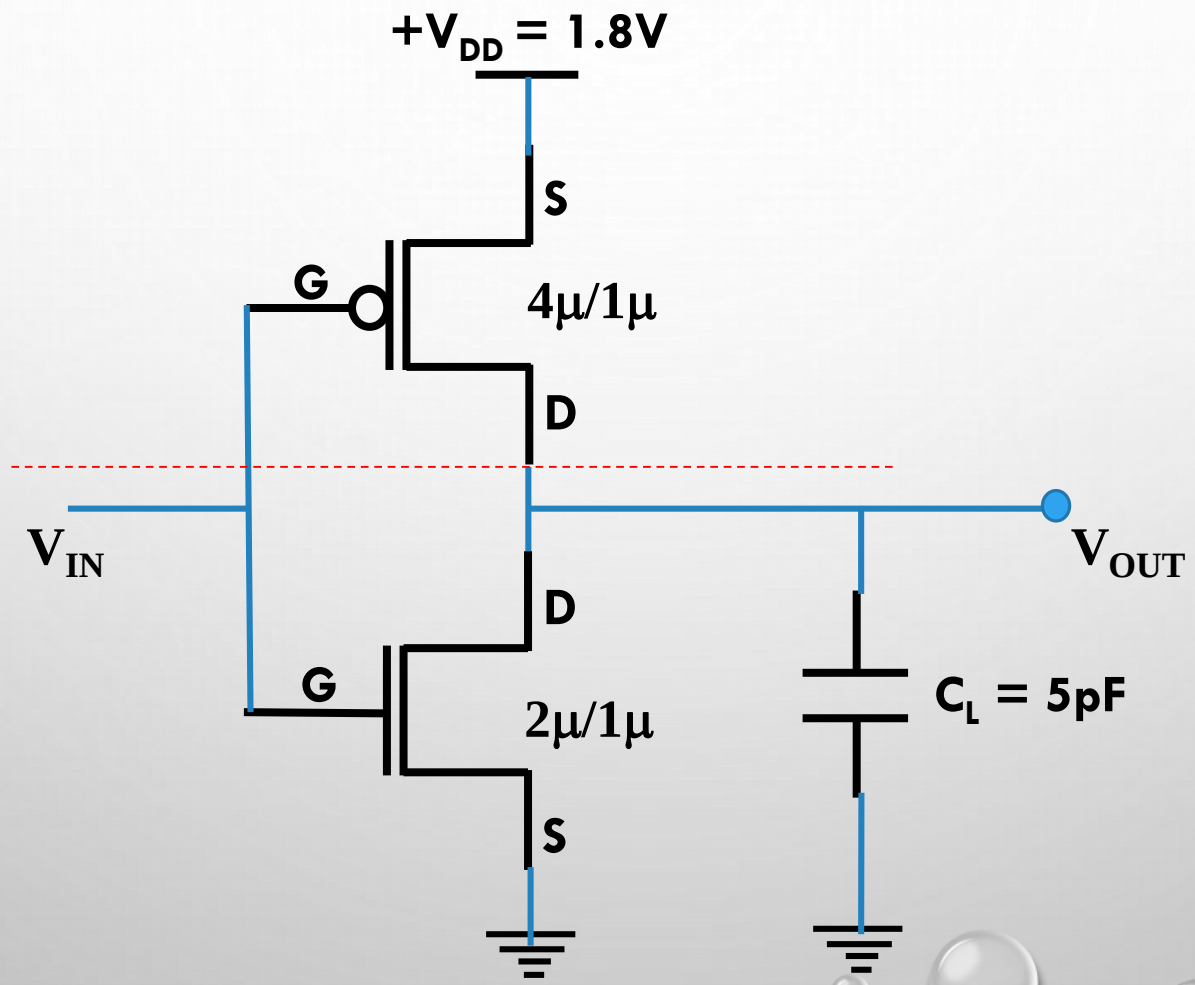
V_{inv} vs. β_n/β_p

- If $\beta_p/\beta_n \neq 1$, switching point will move from $V_{DD}/2 \Rightarrow$ skewed gate
- If $B_p > \beta_n \Rightarrow$ High skewed inverter
- If $\beta_p < \beta_n \Rightarrow$ Low skewed inverter





Simulation using Cadence Virtuoso

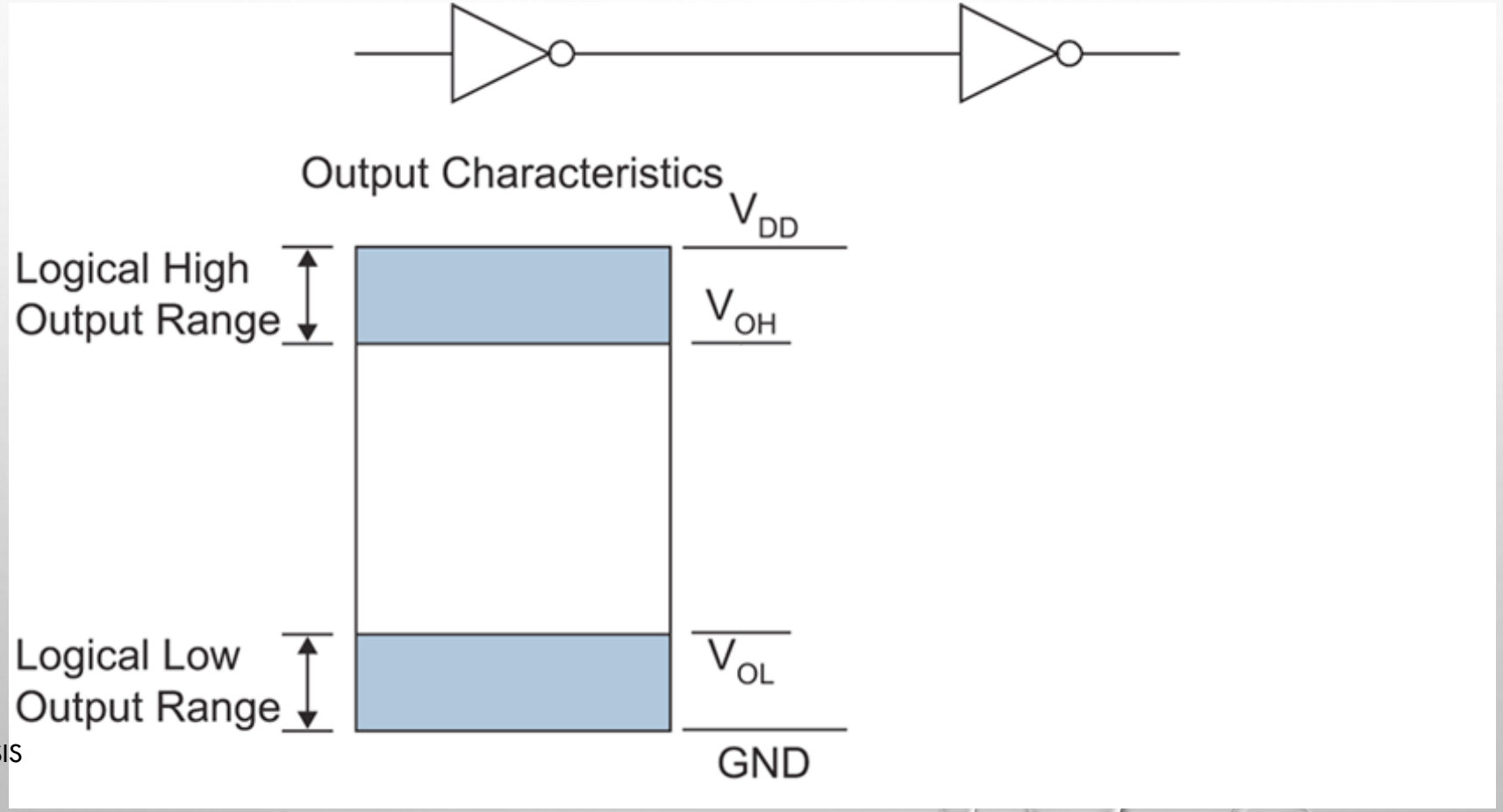


NOISE MARGIN

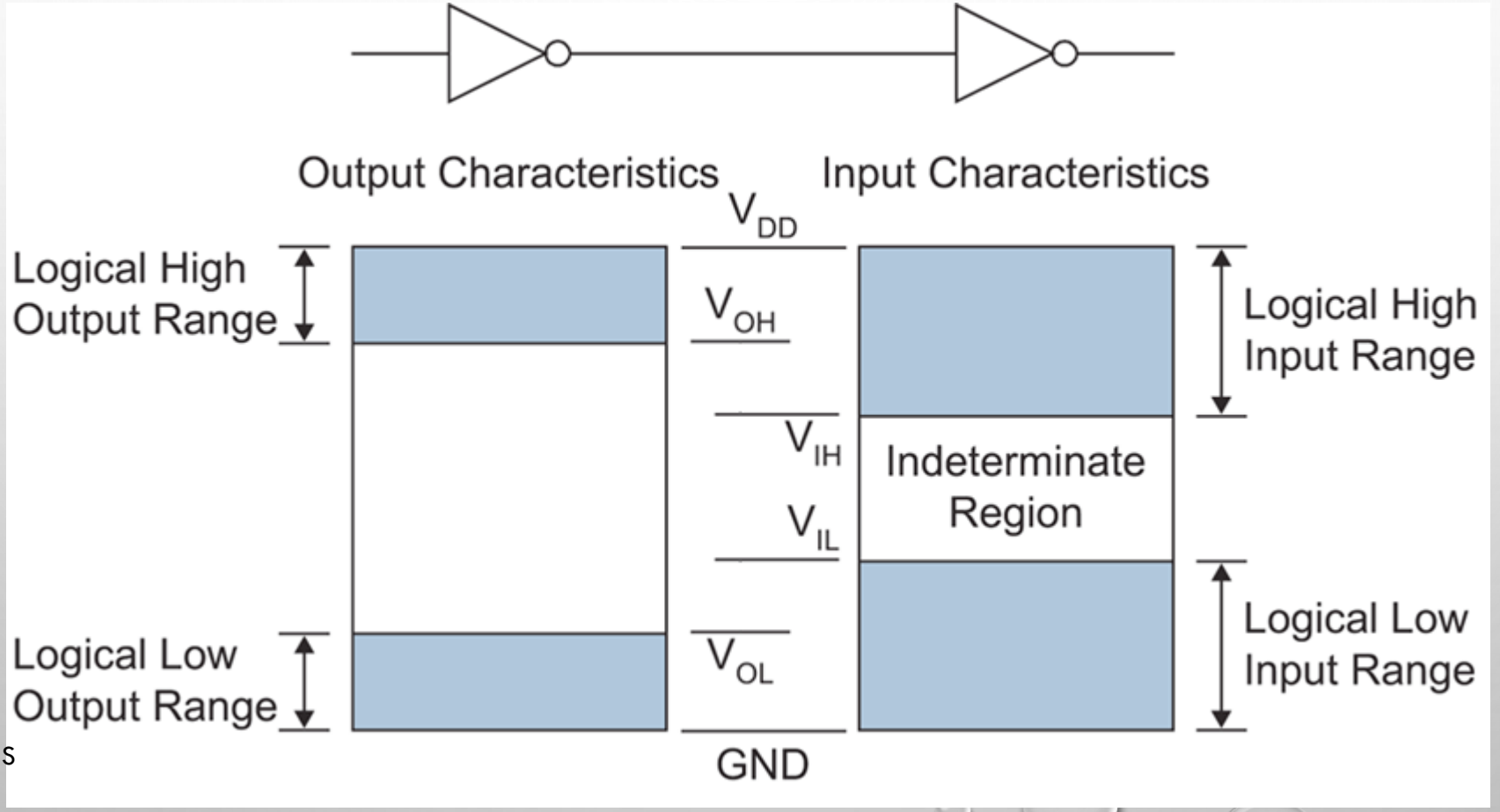
Noise margin

- is the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit
- does make sure that any signal which is logic '**1**'with finite noise added to it, is still recognized as logic '**1**' & not logic '**0**'
- is a parameter closely related to the input-output voltage characteristics
- allows us to determine the allowable noise voltage on the input of a gate so that the output will not be affected

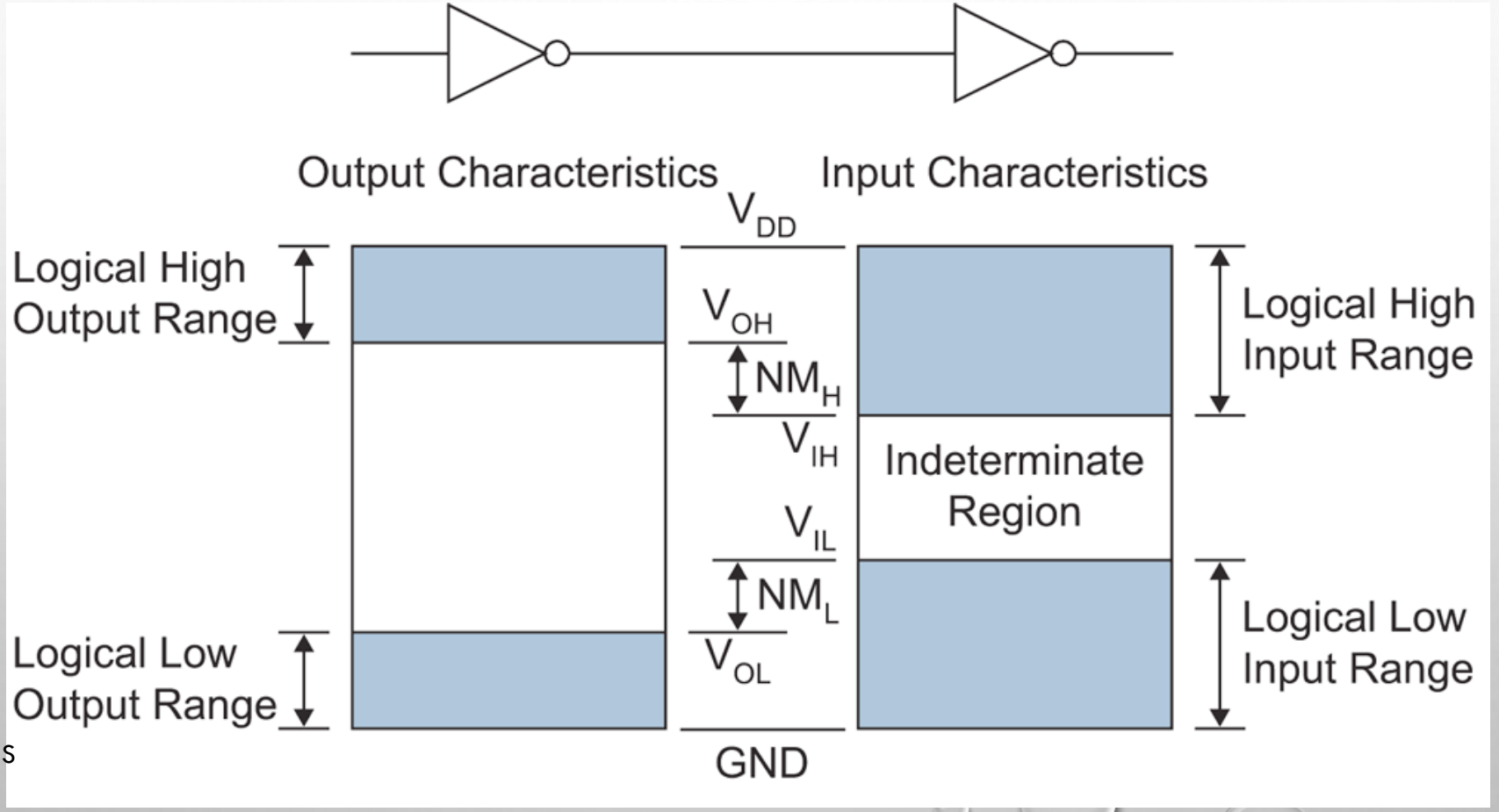
NOISE MARGIN



NOISE MARGIN



NOISE MARGIN



NOISE MARGIN

- Noise margin is specified in terms of 2 parameters:
  - LOW Noise Margin, $\mathbf{NM_L}$
  - HIGH Noise Margin, $\mathbf{NM_H}$

$$NM_L = |V_{ILmax} - V_{OLmax}|$$
$$NM_H = |V_{OHmin} - V_{IHmin}|$$

To optimize both noise margins NM_L and NM_H generally it is desirable to have $V_{IH} = V_{IL}$ & this to be a value that is midway in the logic swing, that is $V_{DD}/2$.

Or, $\mathbf{V_{inv,th} = V_{DD}/2}$

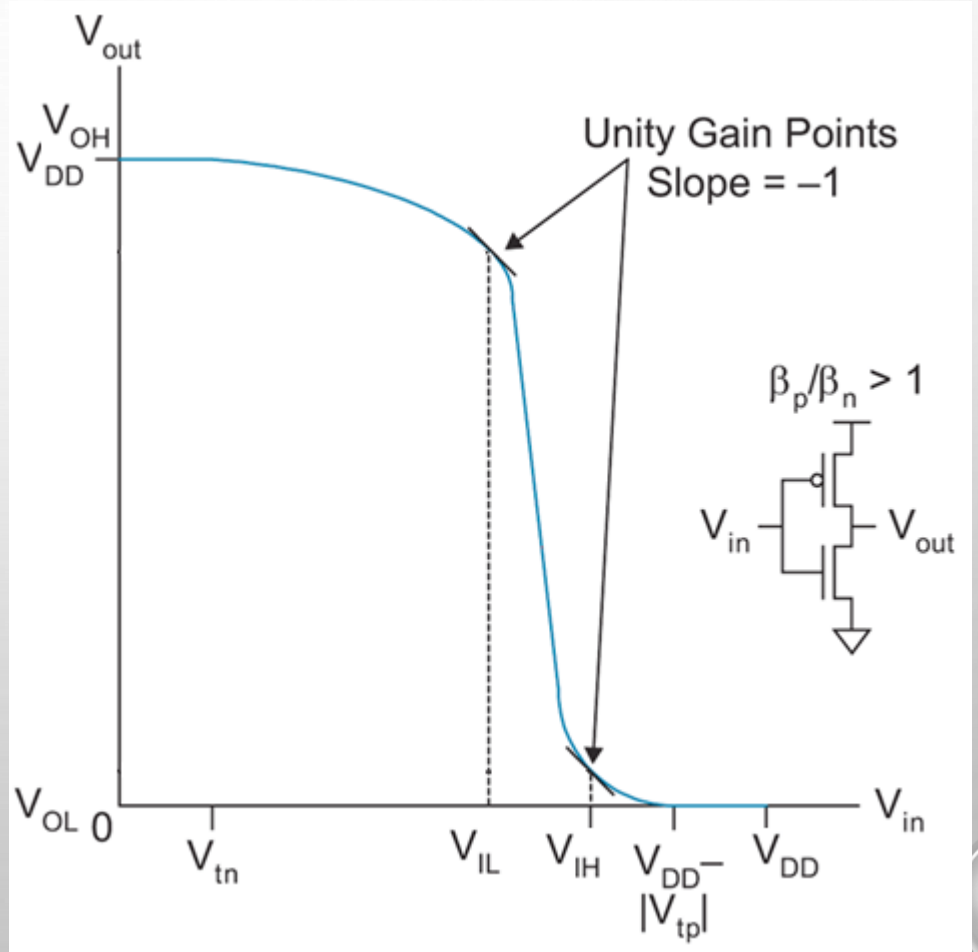
NOISE MARGIN

- To maximize noise margins, select logic levels at unity gain point of DC transfer char.

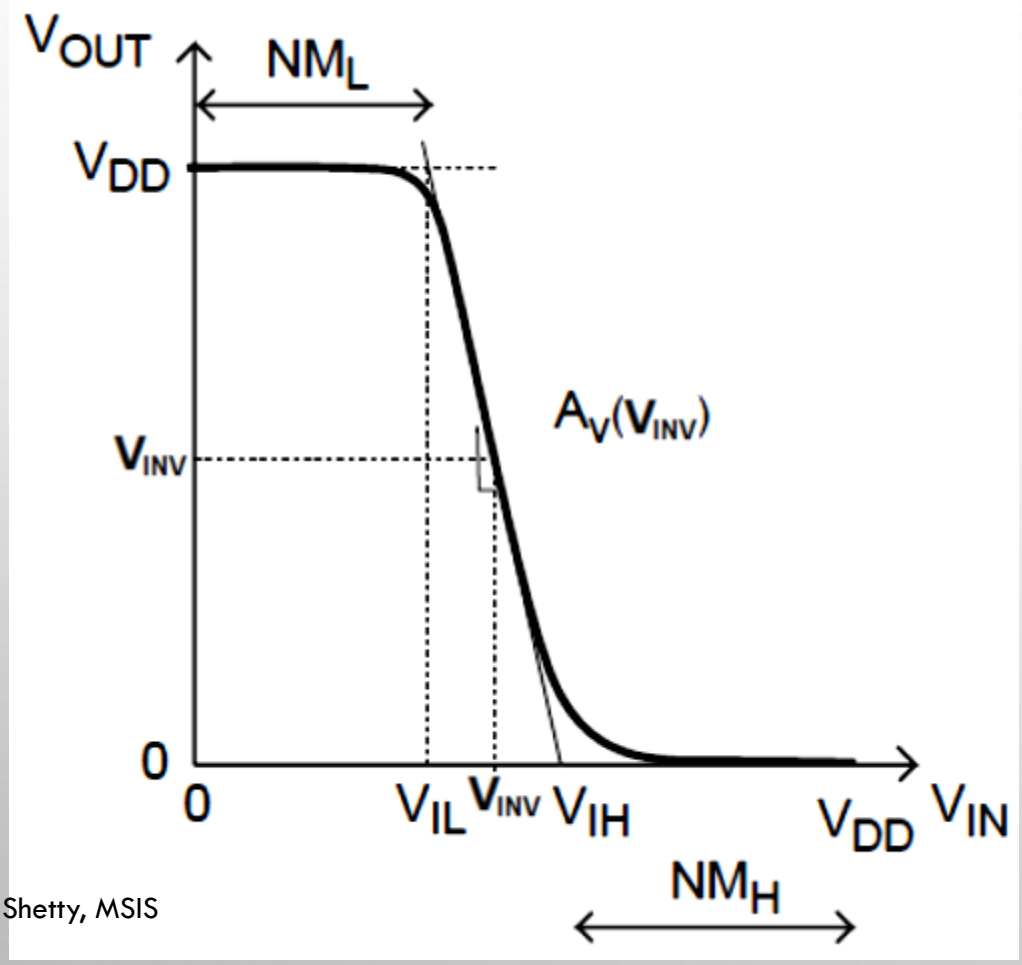
For our Inverter,

$$NM_L = |V_{ILmax} - 0V|$$

$$NM_H = |V_{DD} - V_{IHmin}|$$



Noise Margin Calculation



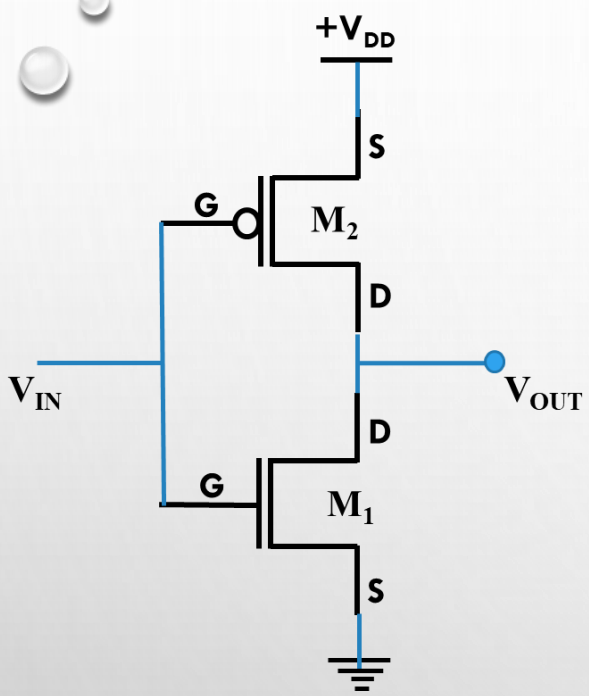
- Calculate V_{INV}
- Calculate A_V (V_{INV})
- Calculate NM_L and NM_H

Calculate V_{INV}

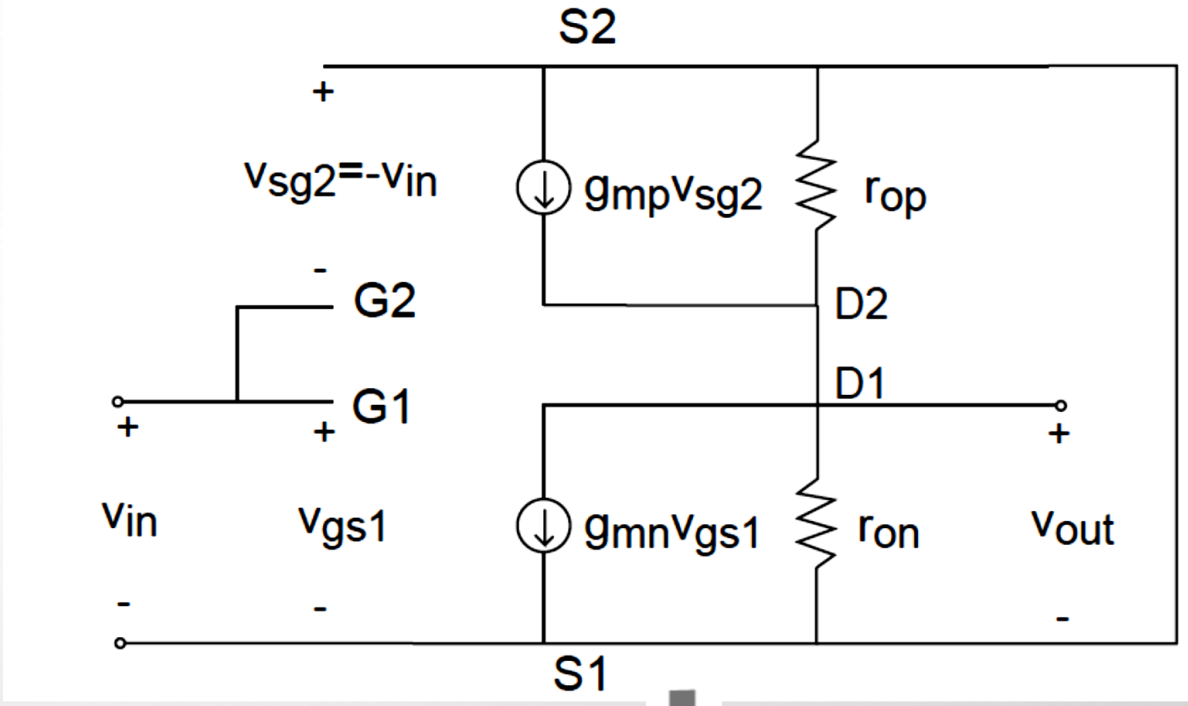
$$V_{INV} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

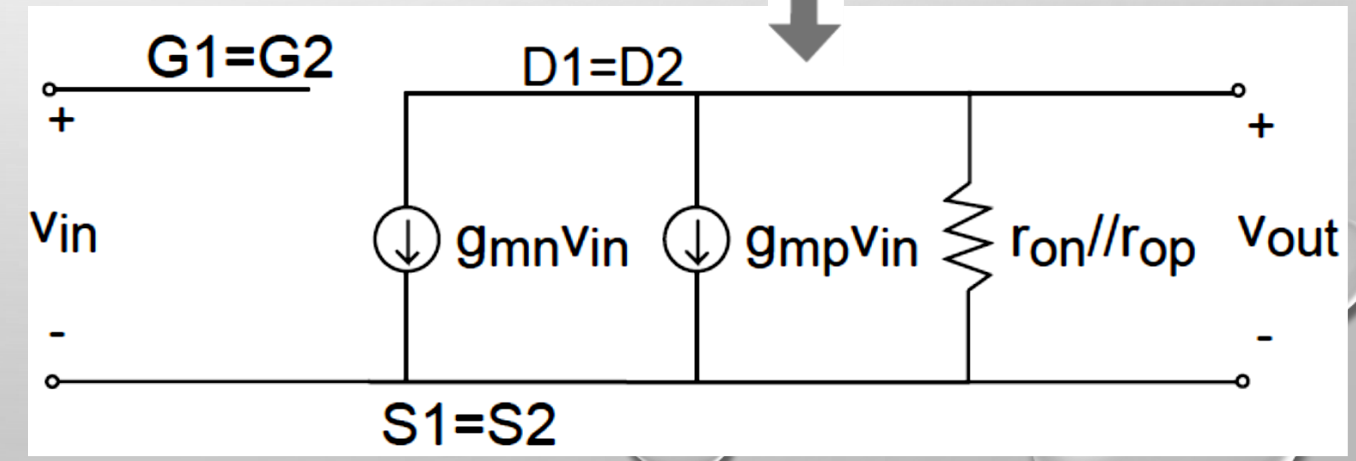
If $V_{tn} = -V_{tp}$ and $\beta_n = \beta_p$, then, $\mathbf{V_{INV} = V_{DD}/2}$

Calculate A_V (V_{INV})



Small Signal Model





$$A_v = -(g_{mn} + g_{mp})(r_{on} // r_{op})$$

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Noise Margin Calculation

- Noise-margin low, NM_L:

$$V_{IL} = V_{INV} - \frac{V_{DD} - V_{INV}}{|A_v|}$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} = V_{INV} - \frac{V_{DD} - V_{INV}}{|A_v|}$$

- Noise-margin high, NM_H:

$$V_{IH} = V_{INV}\left(1 + \frac{1}{|A_v|}\right)$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{INV}\left(1 + \frac{1}{|A_v|}\right)$$

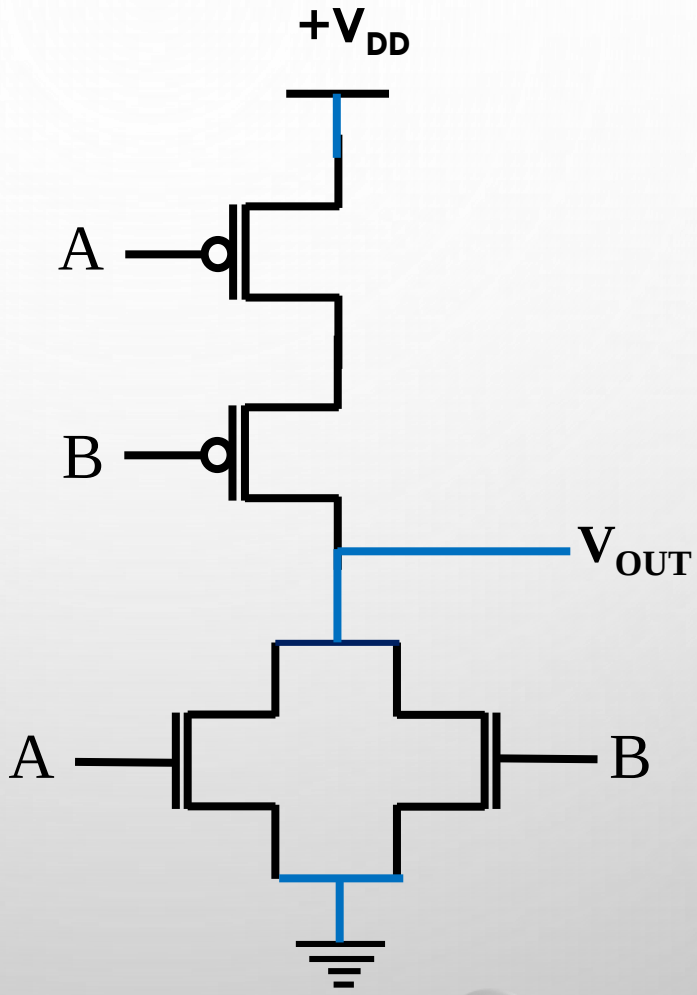
STANDARD SIMPLE GATES

CMOS schematics of:

- NOR Gate
- NAND Gate

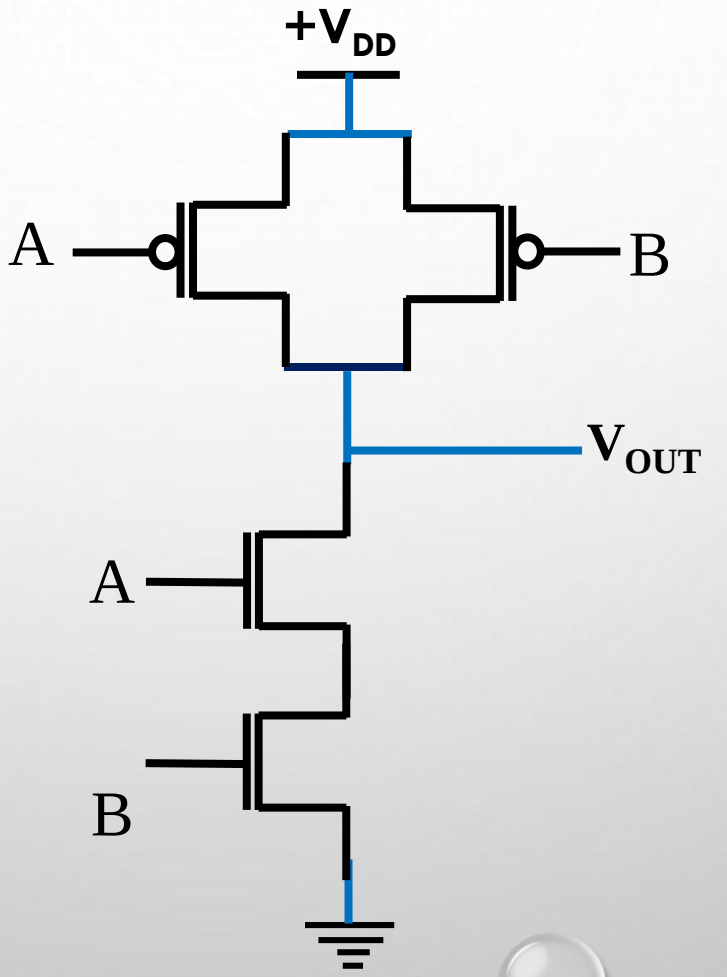
2- INPUT NOR GATE

$$F = \overline{A + B}$$



2- INPUT NAND GATE

$$F = \overline{A \cdot B}$$

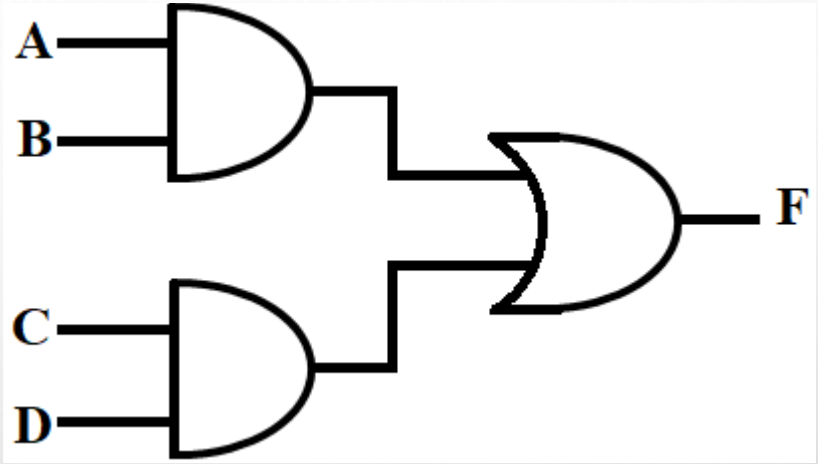


COMPOUND CMOS GATES

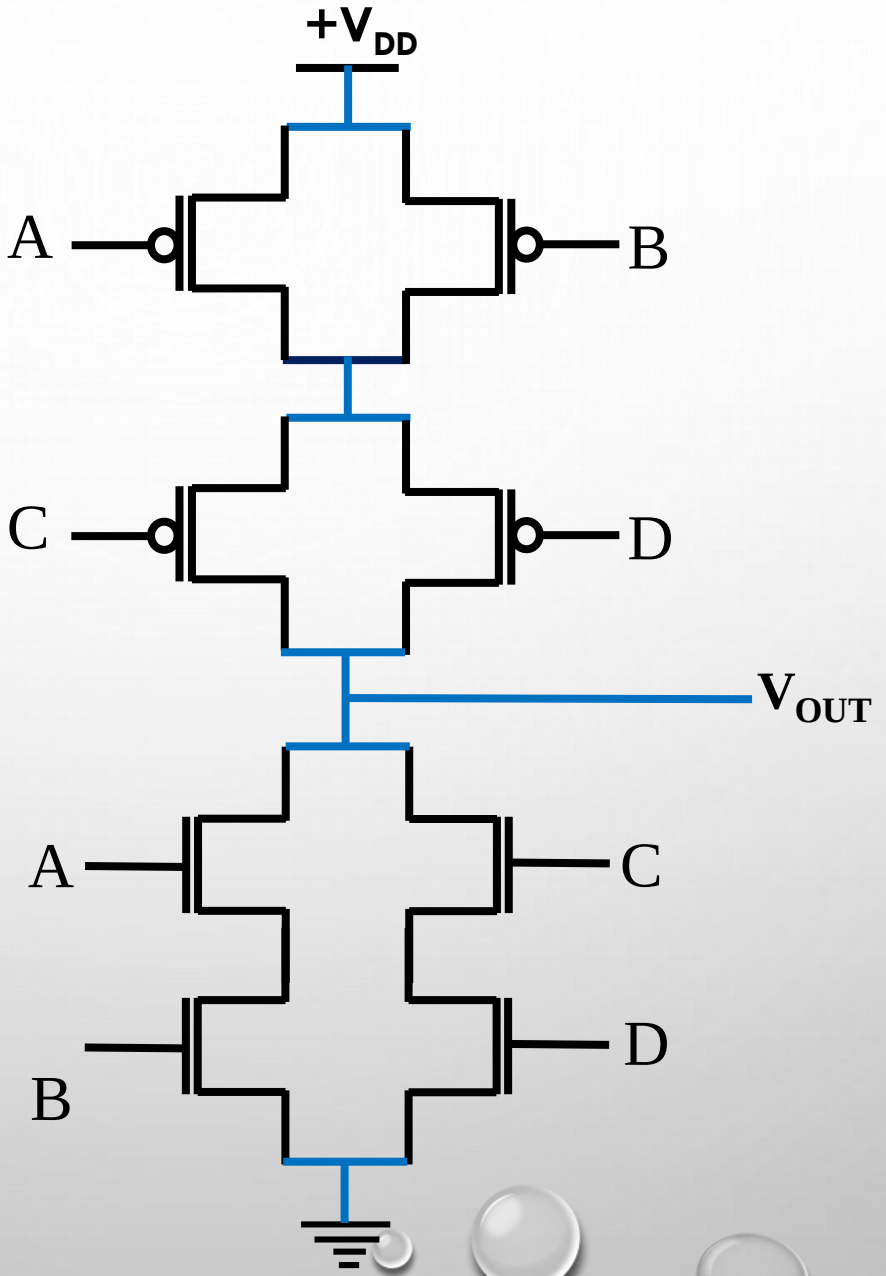
Design CMOS logic gates for the following functions:

1. F = (A.B + C.D)'
2. F = ((A+B+C).D)'
3. Z = (((A.B) + C).D)'
4. Z = ((A.B) + C.(A+B))'

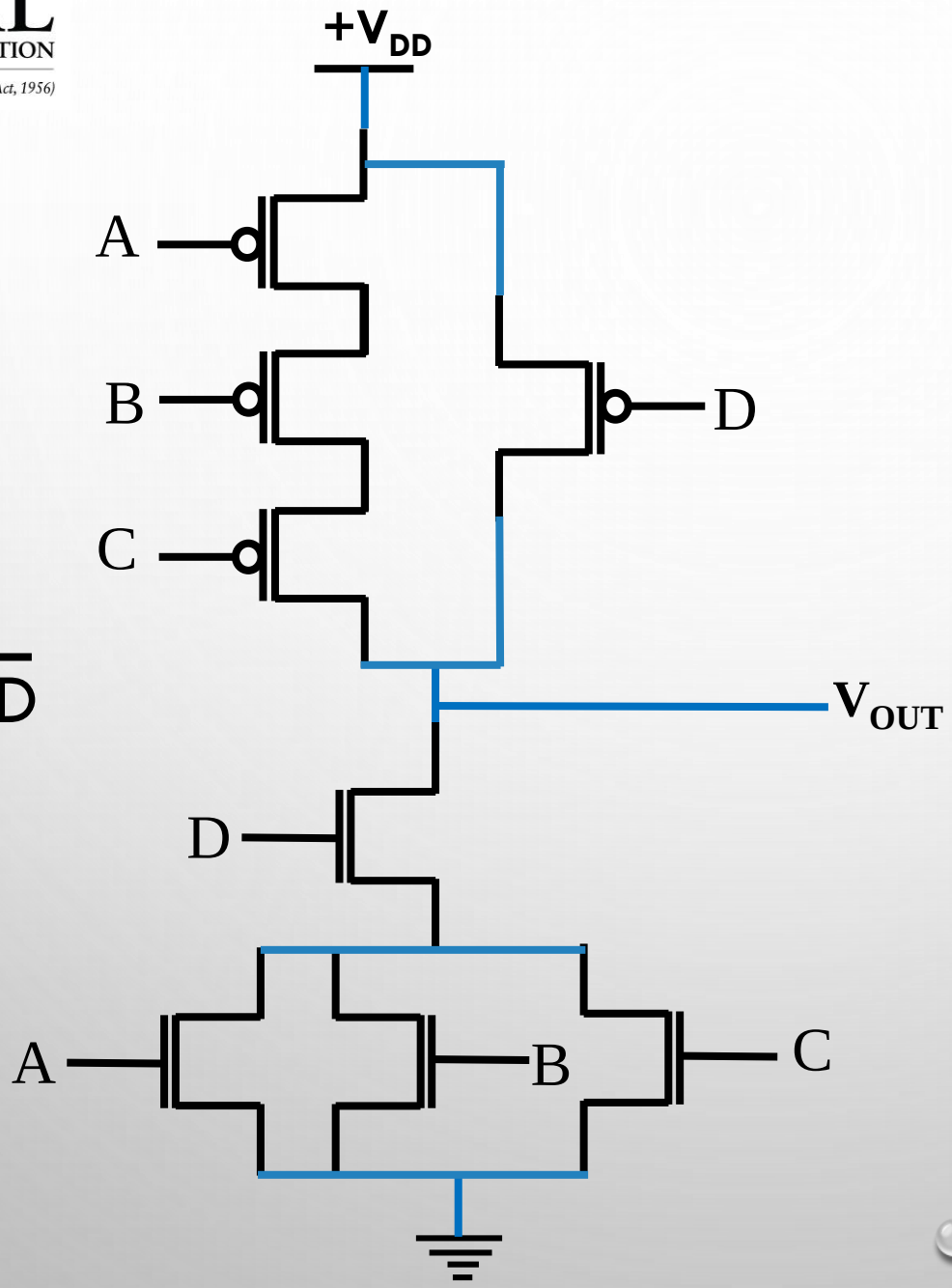
$$F = \overline{(A.B + C.D)}$$

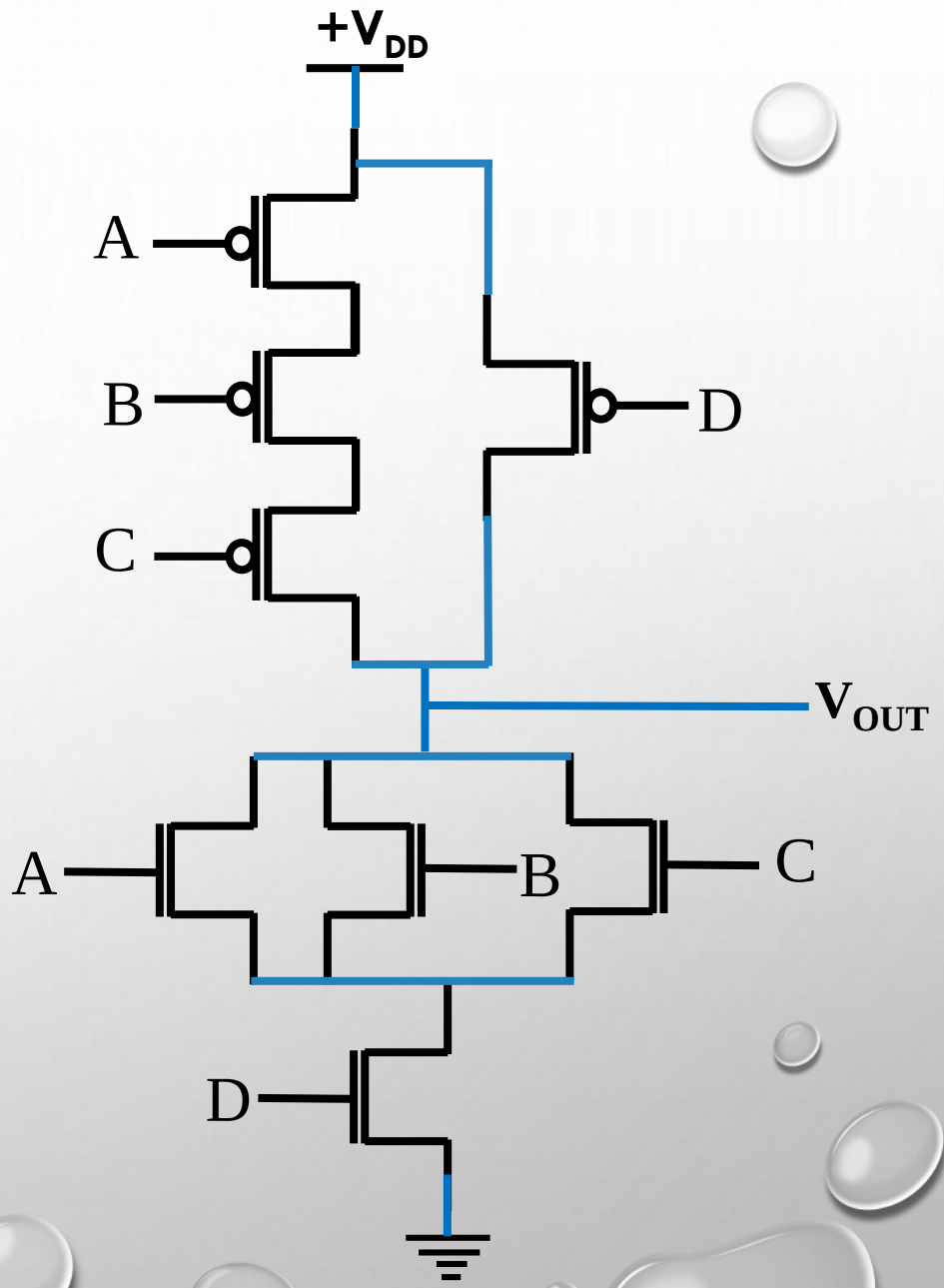


$$F = \overline{(A.B + C.D)}$$



$$F = \overline{(A+B+C).D}$$





COMPOUND CMOS GATES

- Can a compound gate be arbitrarily complex?
  - NO, propagation delay is a strong function of fan-in:

$$t_p = a_0 \cdot FO + a_1 \cdot FI + a_2 \cdot (FI)^2$$

- FO $\Rightarrow$ Fan-out, number of loads connected to the gate:
  - 2 gate capacitances per FO + interconnect
- FI $\Rightarrow$ Fan-in, Number of inputs in the gate:
  - Quadratic dependency on FI due to:
    - Resistance increase
    - Capacitance increase
- Avoid large FI gates (Typically FI ≤ 4)