2. CRYSTAL GROWTH AND WAFER PREPARATION

Semiconductor Material Preparation

High-quality and high-performance semiconductor requires extremely pure processing materials.

The raw material, **Silicon** ore, **S_iO_2** (next to oxygen, it is the most abundant element in nature, 27.8%, and is found in a natural state in rocks and sand) must be mined and ***completely purified***.

Silicon Refinement: **The required silicon purity can be obtained in the following steps:**

1. Metallurgical Grade Silicon (MGS – 98% pure) is obtained by heating sand with coal

$$\underset{(s)}{S_iO_2} + \underset{(s)}{2C} \longrightarrow \underset{(l)}{S_i} + \underset{(g)}{2CO}$$

2. Formation of Trichlorosilane: Reaction at high temperature with hydrogen chloride (HCl) to form a complex chemical mixture containing trichlorosilane.

$$\underset{(s)}{S_i} + \underset{(g)}{3HCl} \longrightarrow \underset{(g)}{S_iHCl_3} + \underset{(g)}{H_2}$$

Silicon Refinement:

3. Separation and purification of trichlorosilane:

This step gives 99.999999% pure trichlorosilane.

4. Hidrogen reduction of ultrapure trichlorosilane:

This gives Electronic Grade polycrystalline silicon (EGS) by reaction with hydrogen at 1,100 – 1,200ºC.

$$\underset{\text{(gas)}}{2S_iHCl_3} + \underset{\text{(gas)}}{2H_2} \longrightarrow \underset{\text{(crystal)}}{2S_i} + \underset{\text{(gas)}}{6HCl}$$

Crystal v/s Amorphous

- In some materials, the atoms occupy very definite positions relative to each other. These positions are repeated throughout the material. Such materials are called **Crystals**.

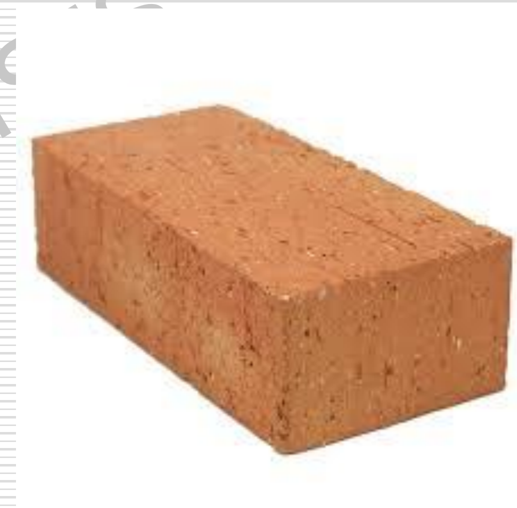
  Eg:- Silicon, Germanium.

- Materials without a definite arrangement of their atoms are called **Amorphous**.

  Eg:- Plastic

Analogy

Amorphous

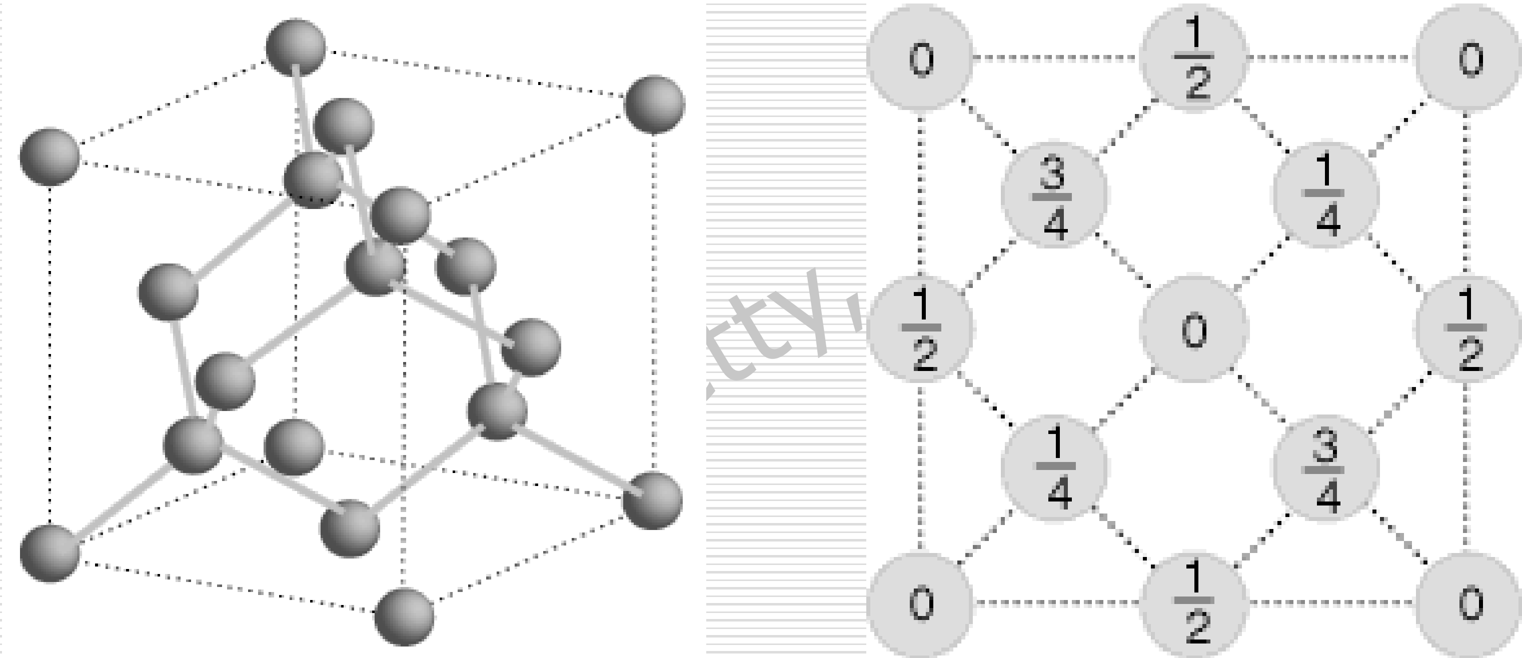


Crystal

Unit Cells

- There are 2 levels of atomic organization possible for crystalline materials.
- **First level** – Organization of individual atoms.
- The basic repeating unit of the arrangement of atoms or molecules is a **unit cell**.
- Silicon unit cell has 18 atoms arranged into a diamond structure.

Silicon Crystal Structure



Arrangement of Silicon atoms in a Unit Cell, with the numbers indicating the height of the atom above the base of the cube as a fraction of the cell dimension.

Polycrystals v/s Single Crystals

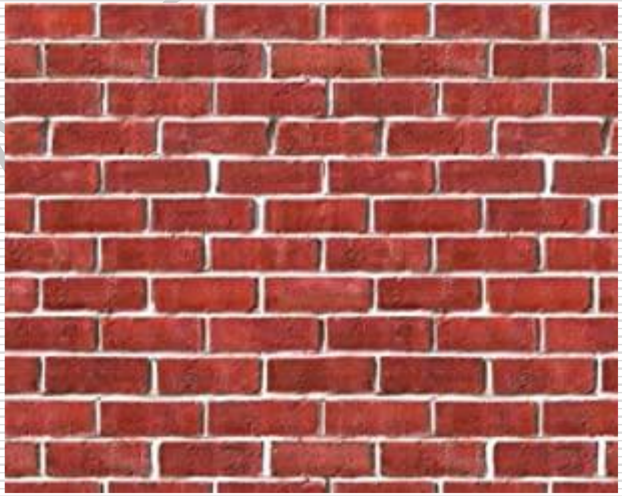
Second level - Organization of unit cells.

Single crystals – Unit cells are all neatly and regularly arranged relative to each other.

Polycrystals – Unit cells are not in a regular arrangement to each other.
Eg.:- Intrinsic semiconductor.

Polycrystals v/s Single Crystals

Polycrystals



Single crystal

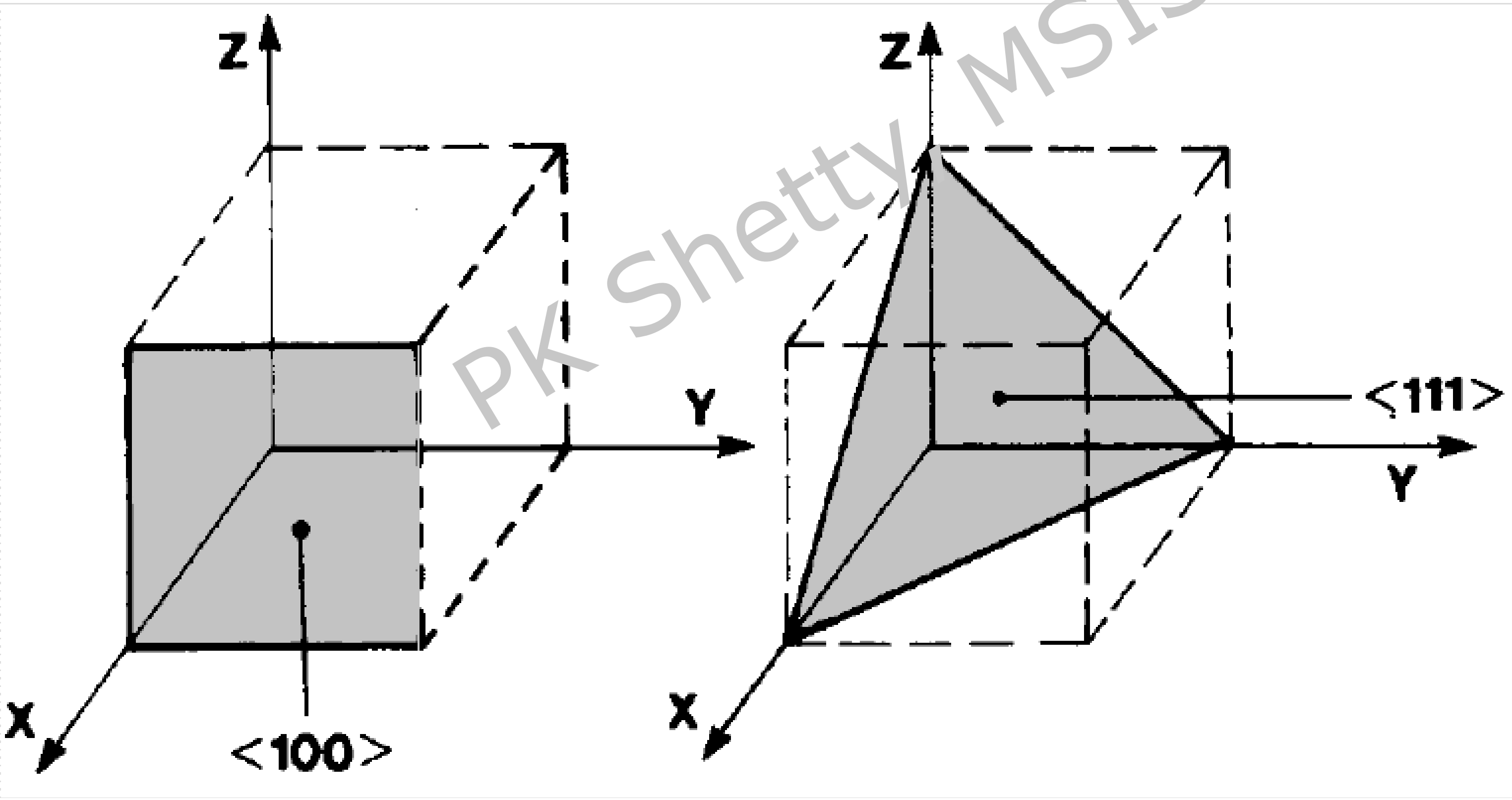
Element

- Amorphous
- Crystal
  - Single Crystal
  - Polycrystals

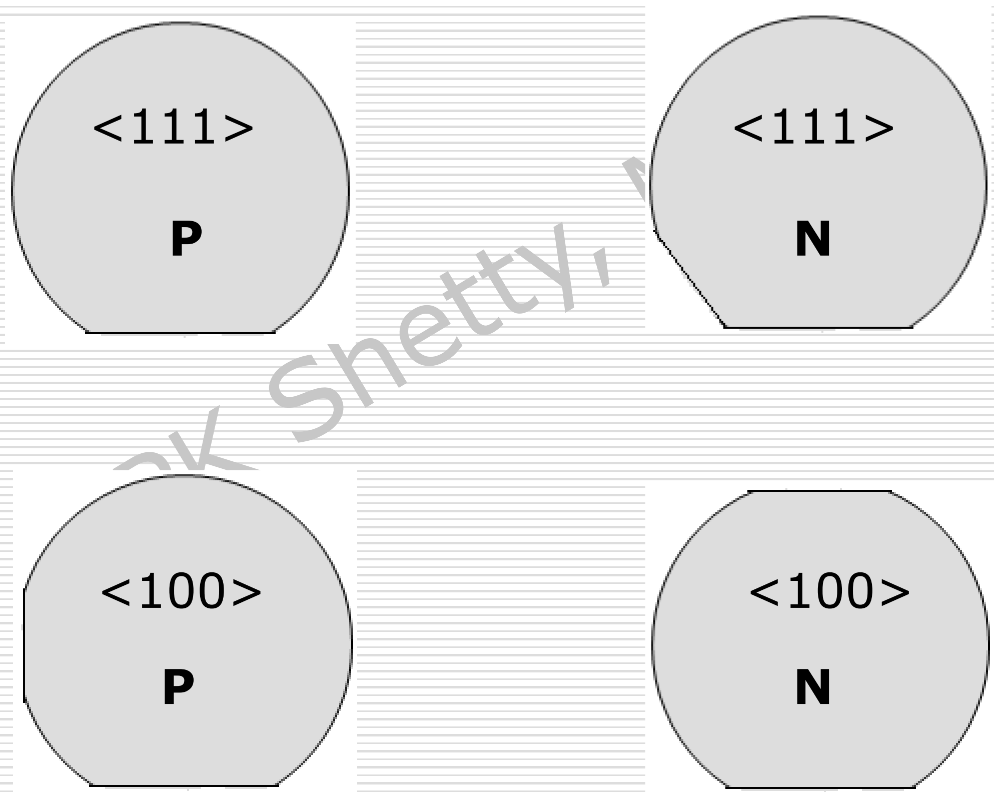
Crystal Orientation

- Different crystal planes are identified by a 3-digit number: Miller Indices.
- Most popular crystal planes/orientations:
  - <**100**> (Square in shape) : MOSFET , GaAs
  - <**111**> (Triangular in shape) : BJT
- Every plane differ from others in its chemical, electrical and physical properties.

Crystal planes



Crystal Orientation



Crystal Growing

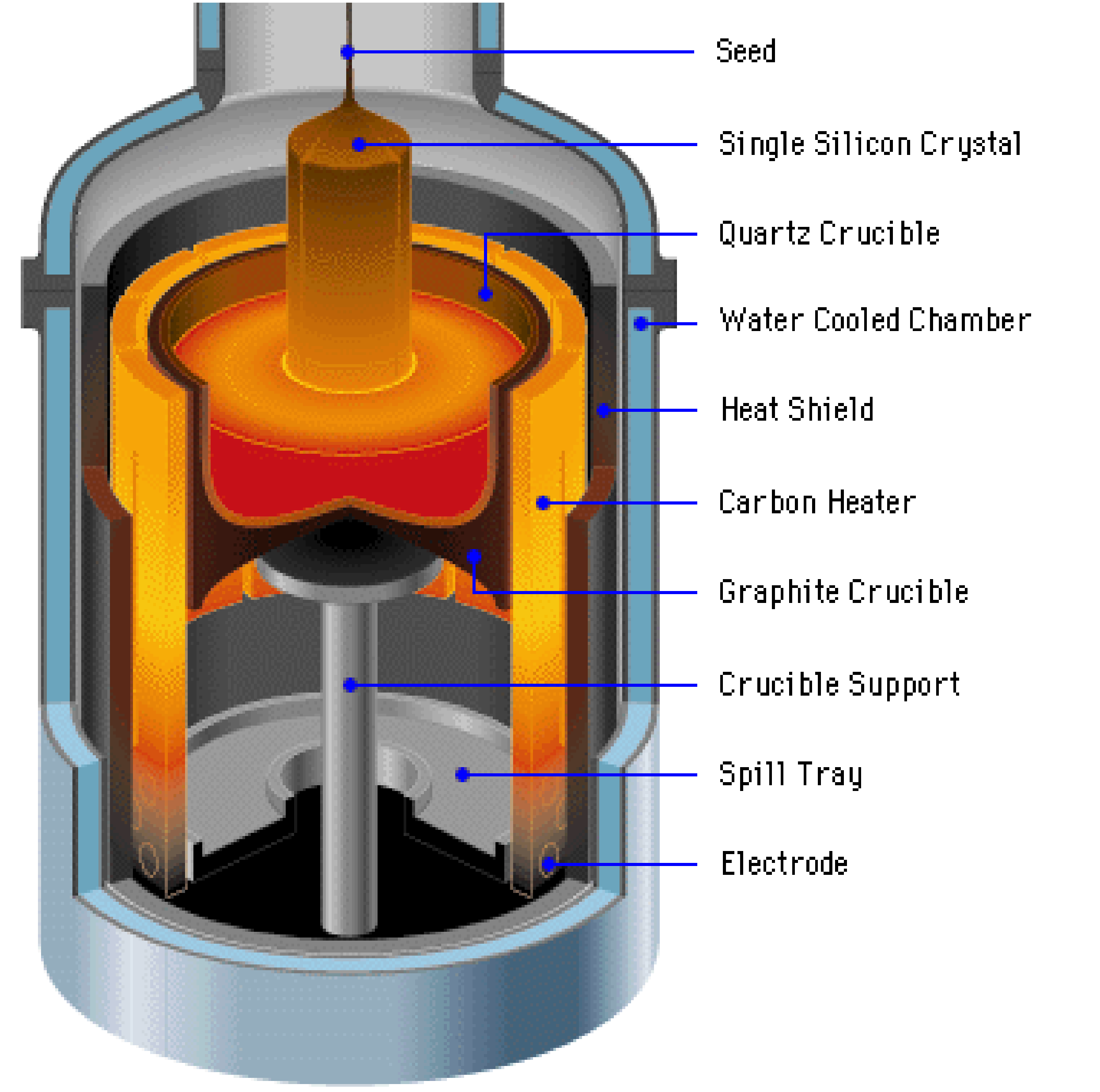
The process of converting the polycrystal chunks to a large crystal of single crystal structure, of the correct orientation and containing the proper amount of dopant is called **crystal growing**.

Crystal Growing Methods

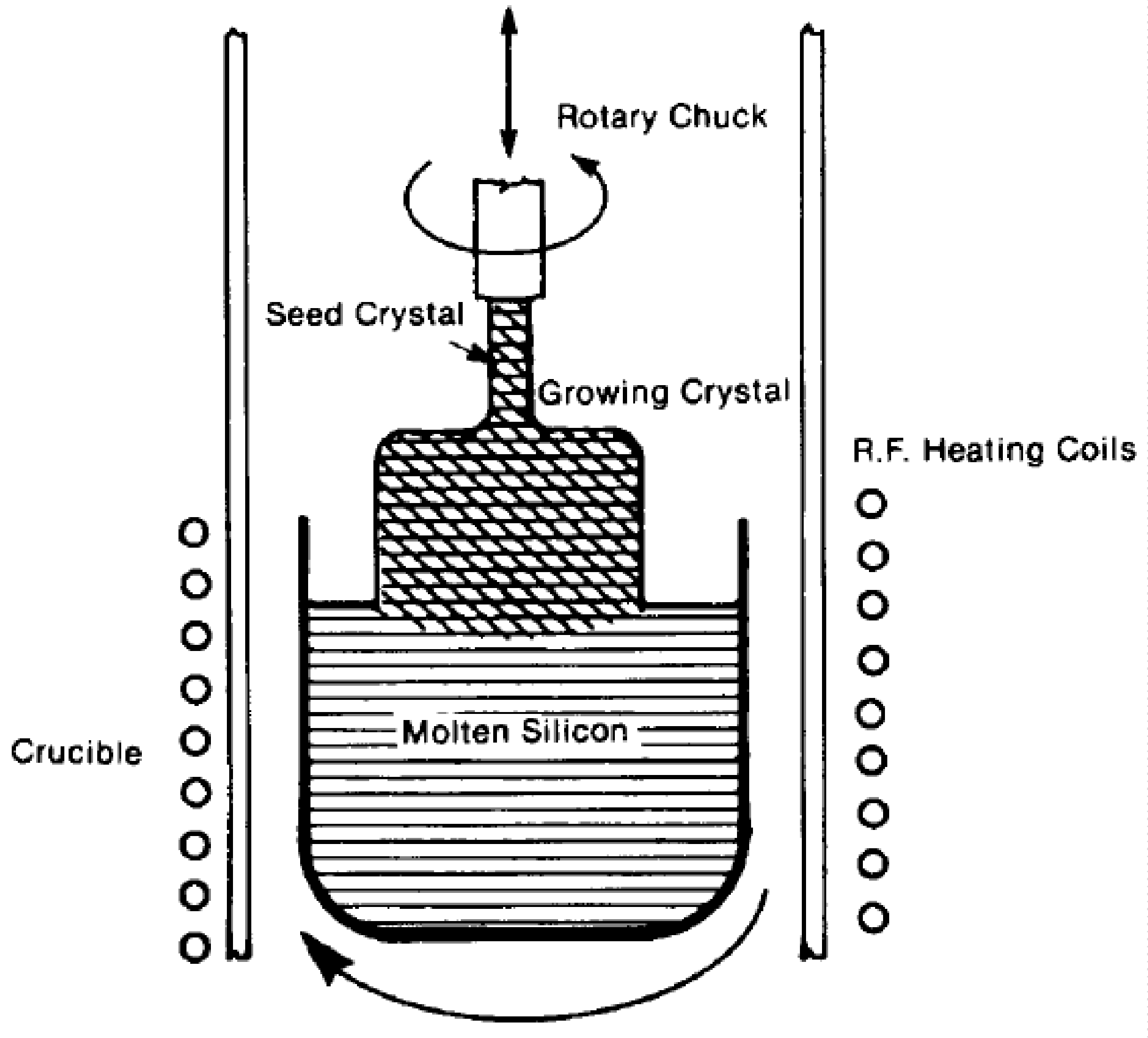
There are 3 methods to grow crystals:

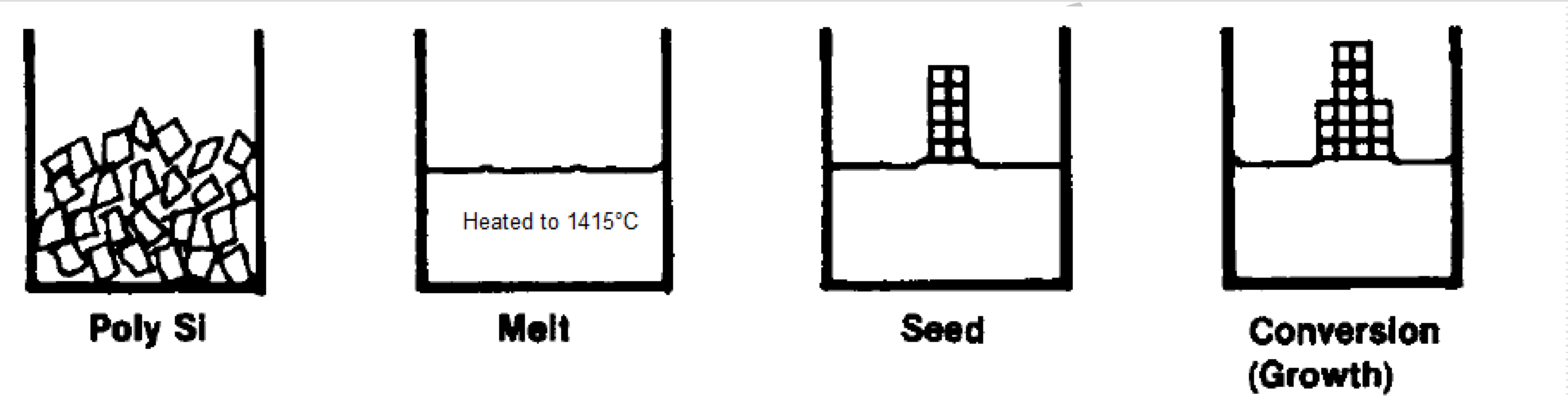
1. **Czochralski (CZ) method.**
2. **Liquid Encapsulated Czochralski (LEC) method.**
   (used for the growing gallium arsenide crystals)
3. **Float-Zone method.**

1. Czochralski (CZ) method



1. Czochralski (CZ) method





To achieve doping uniformity, crystal perfection, and diameter control, the seed and crucible (along with the pull rate) are rotated in opposite directions during the entire crystal-growing process.

Crystal and Wafer Quality

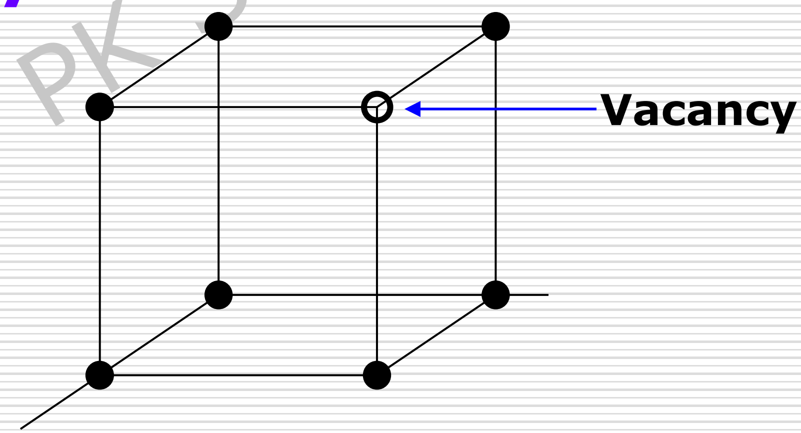
- Semiconductor devices require a high degree of crystal perfection. But even with the most sophisticated techniques, a perfect crystal is unobtainable
- The imperfections, called **crystal defects**, result in process problems by causing uneven silicon dioxide film growth, poor epitaxial film deposition, uneven doping layers in the wafer, and other problems
- In finished devices, the crystal defects cause unwanted current leakage and may prevent the devices from operating at required voltages.

Crystal Defects

1. Point defects
2. Dislocations
3. Growth Defects
   a. Crystal Slip
   b. Crystal twinning

Crystal Defects

1. Point defects
   - When contaminants in the crystal becomes jammed in the crystal structure causing **strain**
   - Atom missing from a location in the structure – **vacancy**



Crystal Defects

2. Dislocations – misplacement of the unit cells in a single crystal.

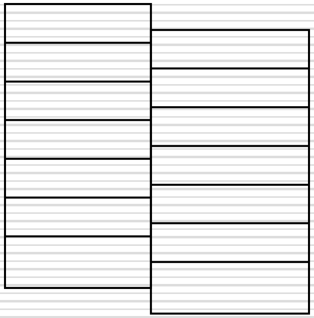
Wafer dislocations are revealed by a special etch of the surface.

A typical wafer has a density of 200 to 1000 dislocations per square centimeter.

Etched dislocations appear on the surface of the wafer in shapes indicative of their crystal orientation. ⟨111⟩ wafers etch into triangular dislocations, and ⟨100⟩ wafers show "squarish" etch pits

Crystal Defects

3. Growth defects – structural defect - rejection
    - Crystal ***slip***: *slippage of the crystal along crystal planes*
    - Crystal ***twinning***: *crystal grows in two different directions from the same interface*



Crystal slip

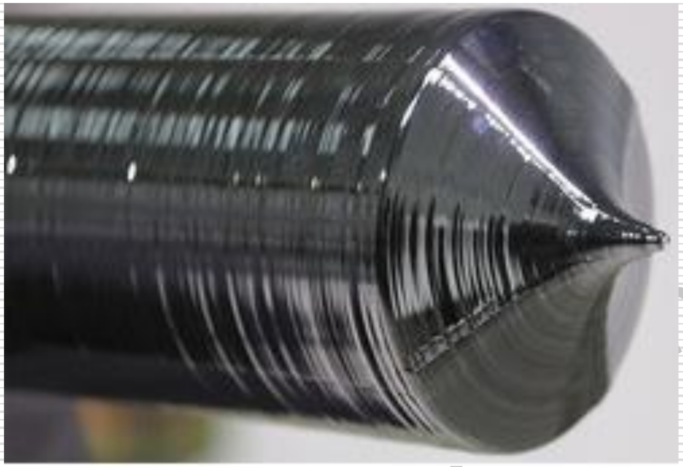
Wafer Preparation

1. End cropping – chop-off tapered ends
2. Diameter grinding
3. Crystal orientation, conductivity, and resistivity check
4. Flat grinding
5. Wafer slicing
6. Rough polish
7. Chemical-mechanical polishing (CMP)
8. Backside processing
9. Edge grinding

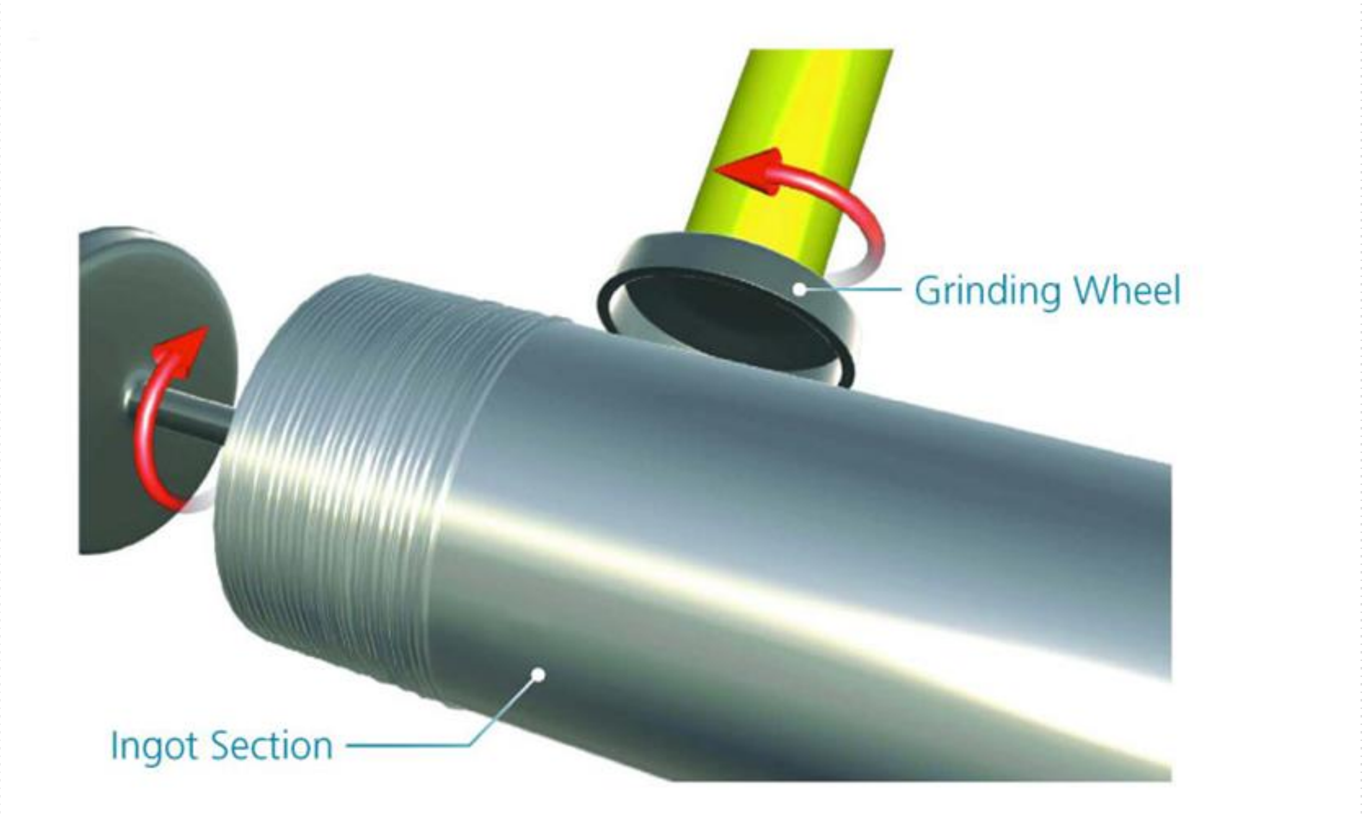
Wafer Preparation – Contd.

10. Wafer evaluation
11. Oxidation
12. Packaging

1. End Cropping



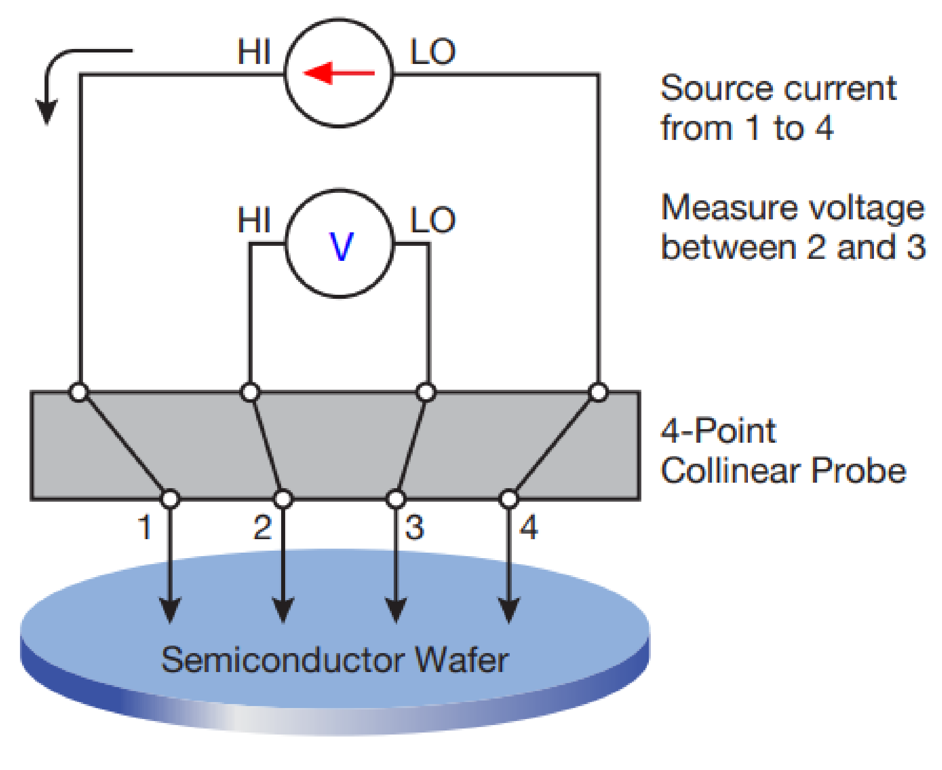
2. Diameter Grinding



3. Crystal orientation, conductivity, and resistivity check

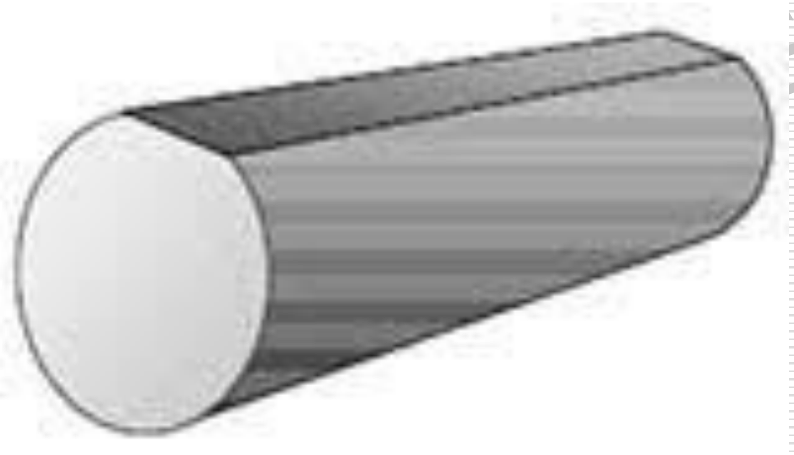
- Crystal Orientation: 100 / 111
- Conductivity: N / P
- Resistivity

Resistivity Check

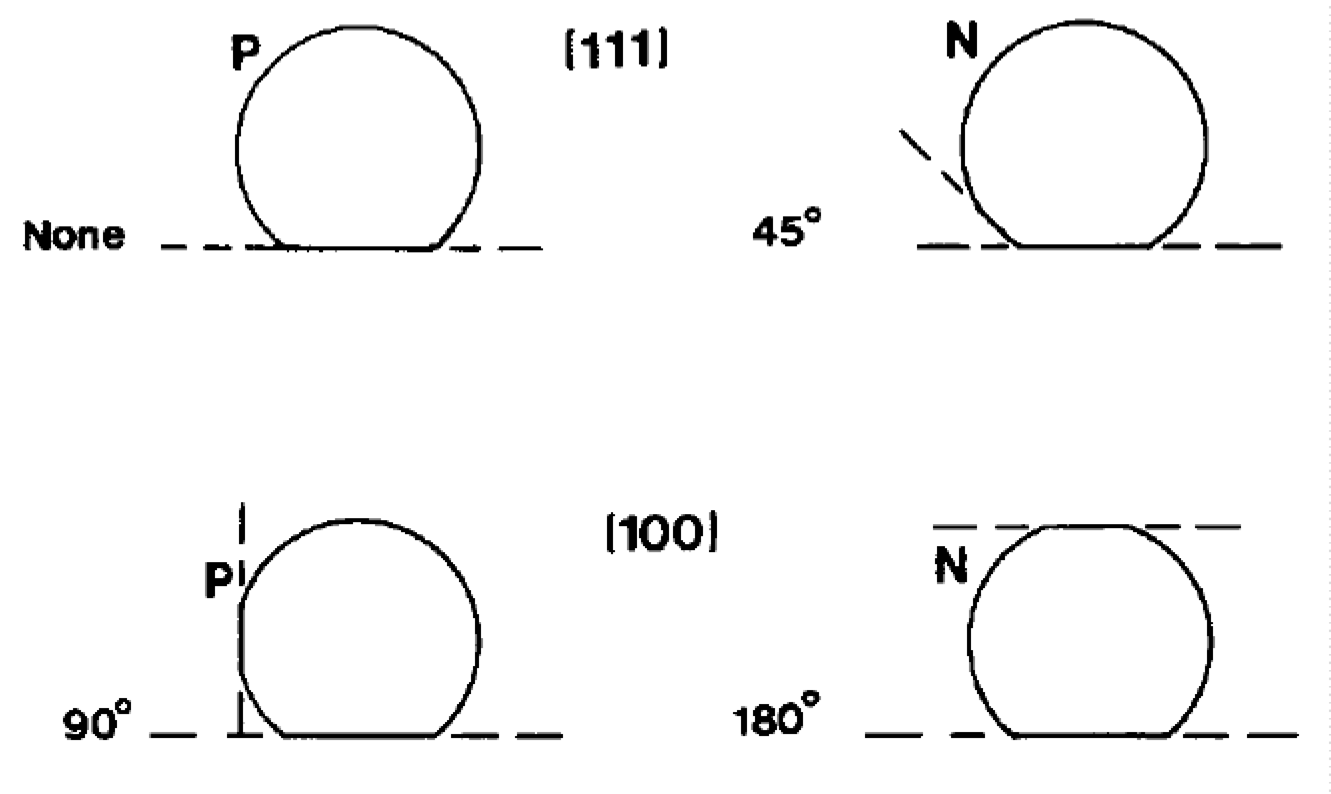


Four-point probe resistivity check

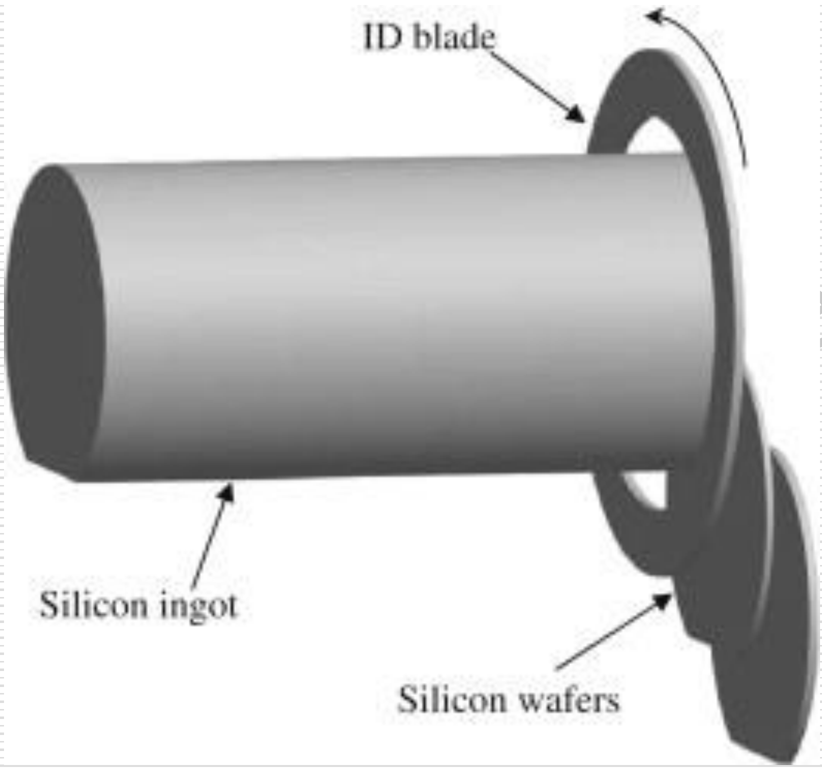
4. Flat Grinding

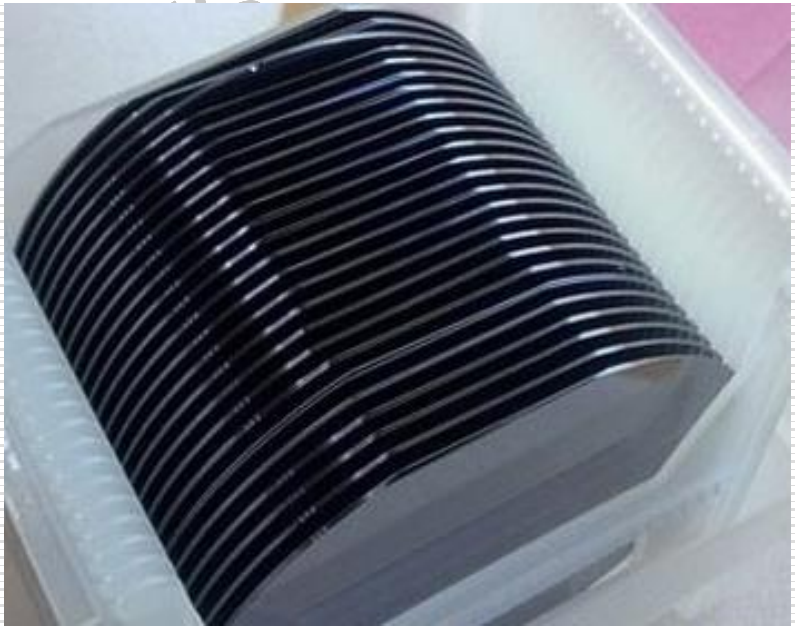


Flat Grinding



5. Wafer Slicing

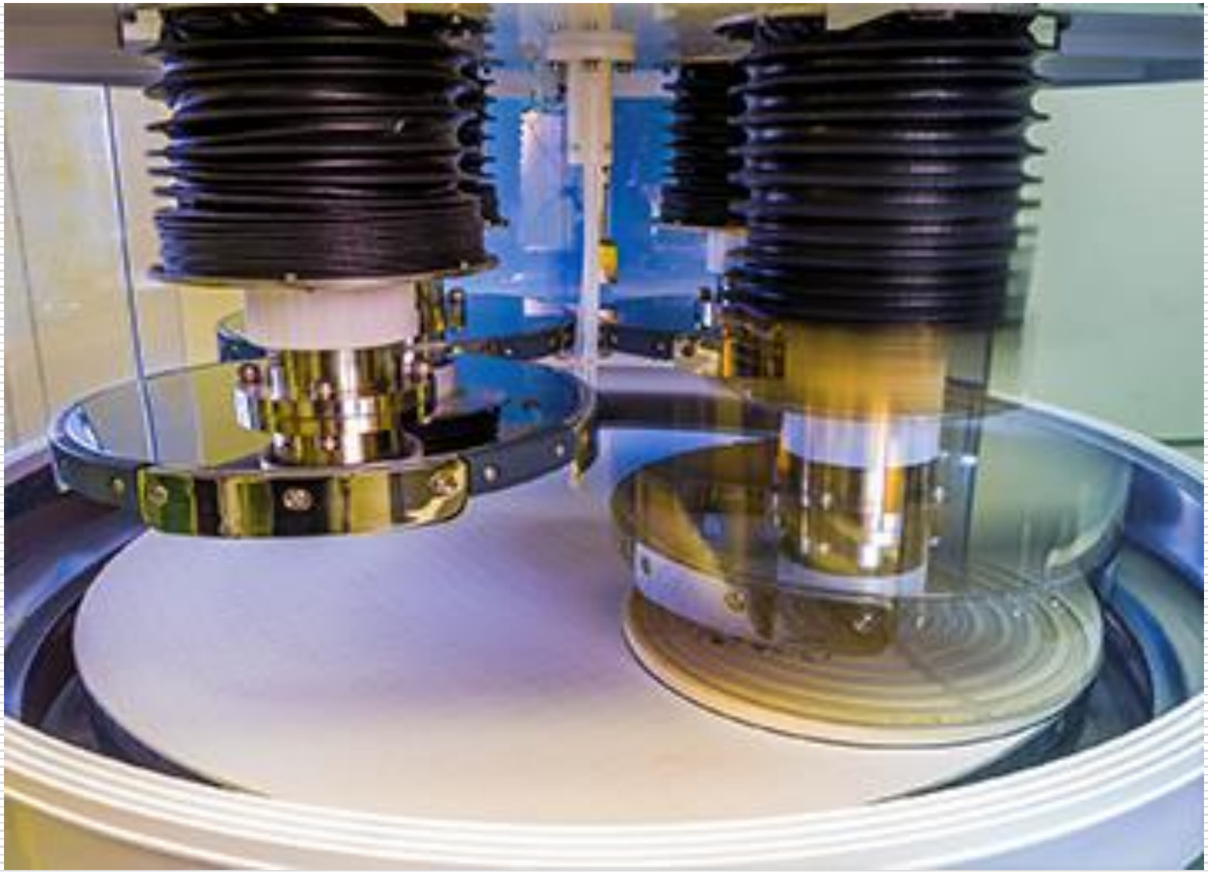




Wafer Polishing

6.Rough polish,

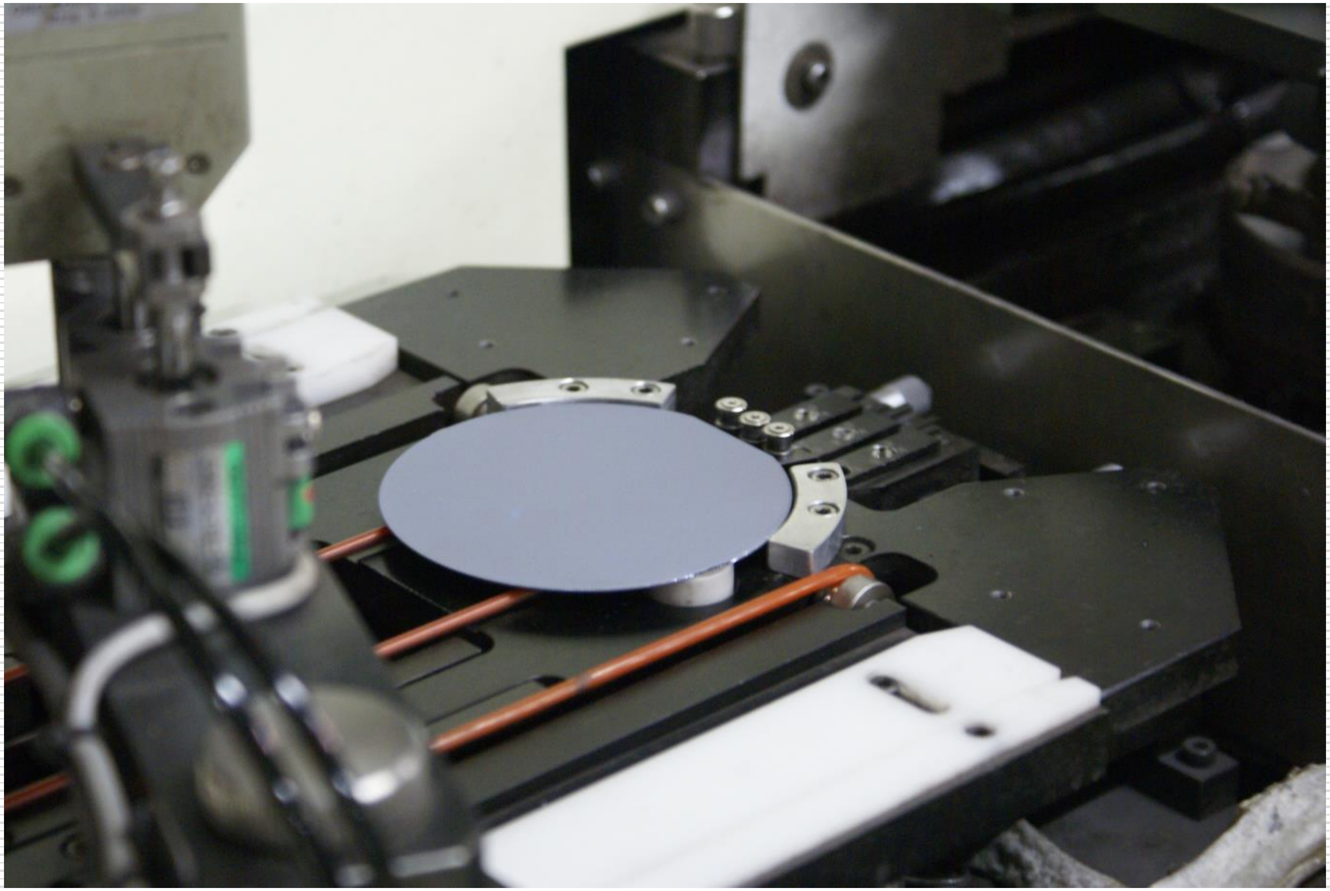
7. Chemical-mechanical polishing (CMP)

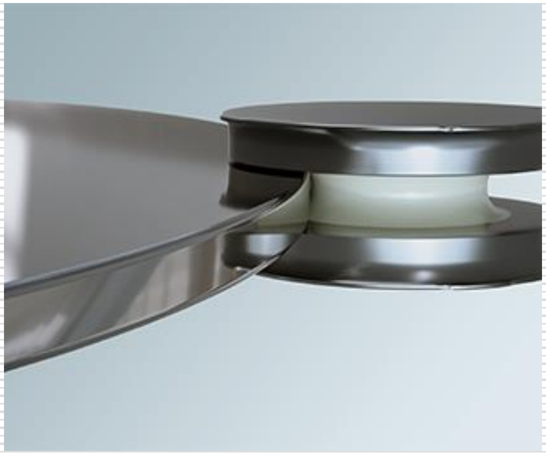


Polished Wafer

8. Backside processing

9. Edge grinding





10. Wafer evaluation

11. Oxidation

12. Packaging