CMOS Process Technology

Modern CMOS processes

- about 25 masks
- about n = 200 process steps
- Number of masks heavily impacts unit price of the chip. Each mask costs n*$1k (total mask cost typ. $200k). Lithography is slow.
- The cost of a complete mask set + fabrication for a 130nm or 90 nm ASIC design can be well over 1 million dollars. In combination with the even higher cost of designing the chip.
- up to 7 (and sometimes more - IBM's POWER9 processors has 17) metal layers
- Poly layers: 1 or 2 (standard) or more (non-standard, e.g. EEPROM)

CMOS Processing Technologies

The 4 main CMOS processing technologies are:

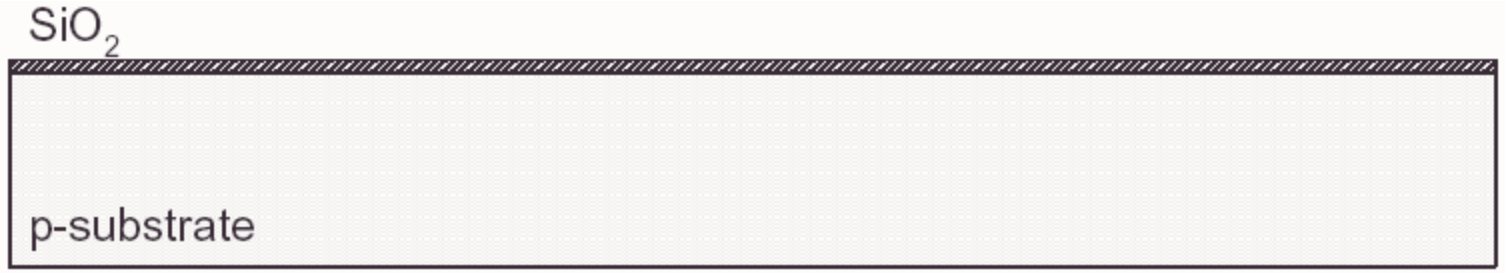
- n-well process
- p-well process
- Twin-tub process
- Silicon on Insulator (SOI)

Today's standard: **n-well CMOS process** with self-aligned polysilicon gates

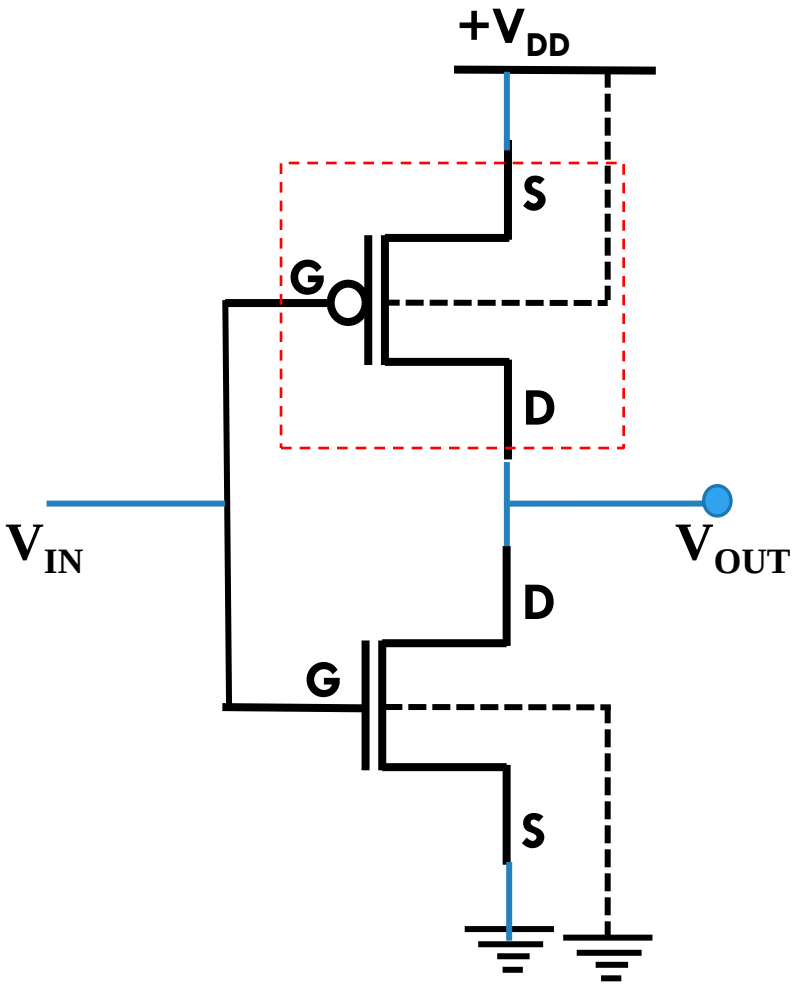
N-well CMOS Process steps

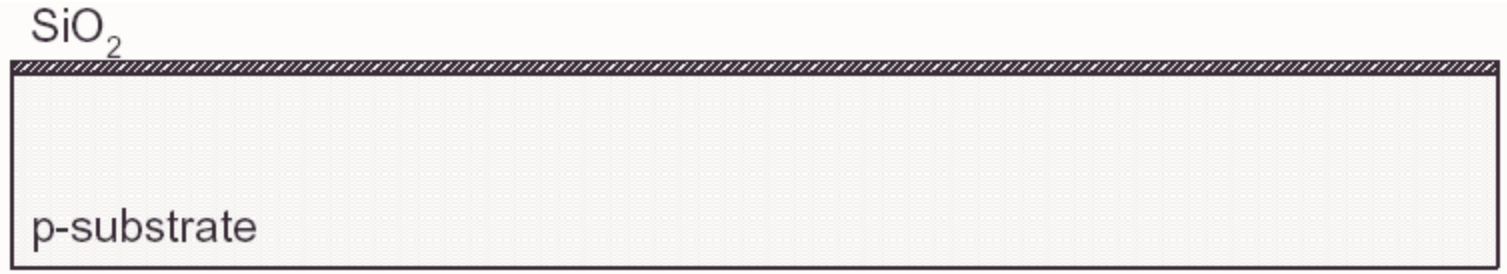
- Process step: Wafer fabrication
  - Czochralksi (CZ) method:
    - Seed of single crystalline Si is immersed in molten Si (1425°C).
    - Molten Si contains desired level of p-type doping.
    - Seed is gradually pulled out while rotating (30-180mm/h)
    - Result: Large single-crystal cylindrical ingot
  - Ingot is sliced into thin wafers
    - Wafer sheet resistance: 50 – 200 Ω.
    - Initial wafer thickness: 500 - 1000 μm
    - Wafer diameter: 75-300mm (12 inch)
  - Wafers are polished and etched to remove surface damages

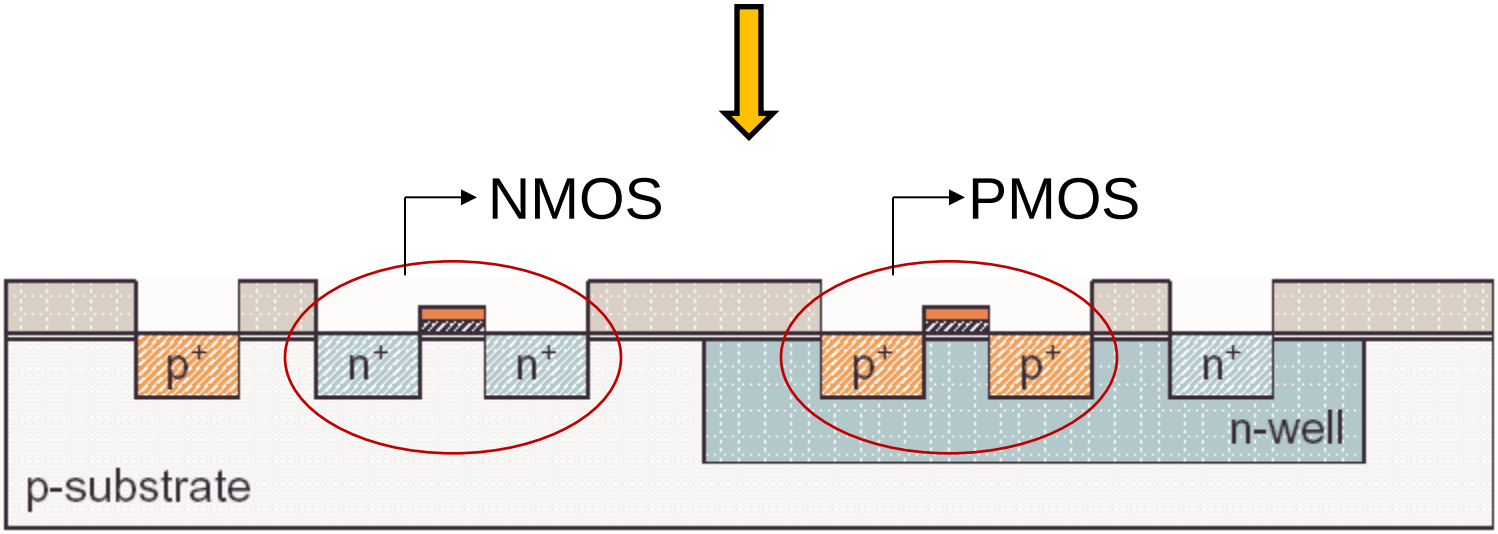
- Process step: Grow thin layer of S_iO_2 on p-type wafer
  - Place wafer in an oxidizing atmosphere at around 1000°C
  - Unique property of S_i : a very uniform oxide layer can be produced on the surface with little strain in the lattice
  - Oxide layers can be very thin (e.g. 50Å=5nm), only a couple of atomic layers
  - Oxide can be used as gate dielectric (Thinox, TOX). Oxide can also be grown thick (field oxide, FOX) as a foundation for interconnect lines
  - Oxide also serves as a protective coating during many process steps (like in this process step)

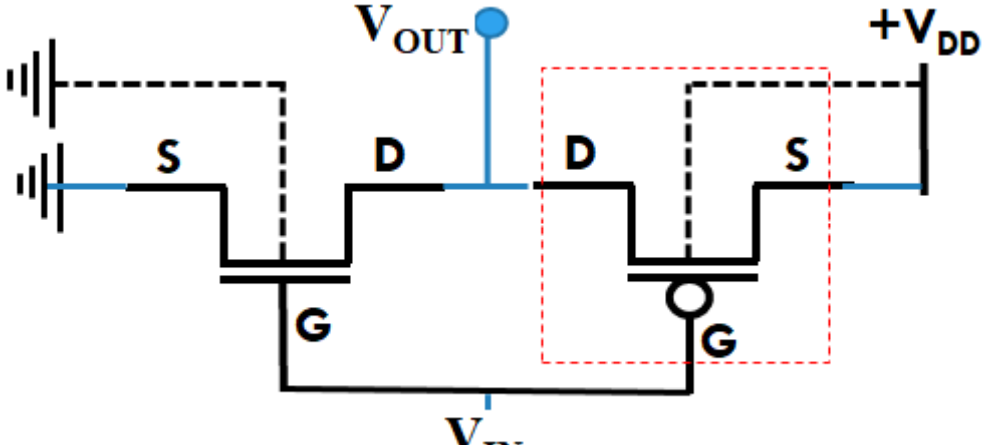


CMOS Inverter

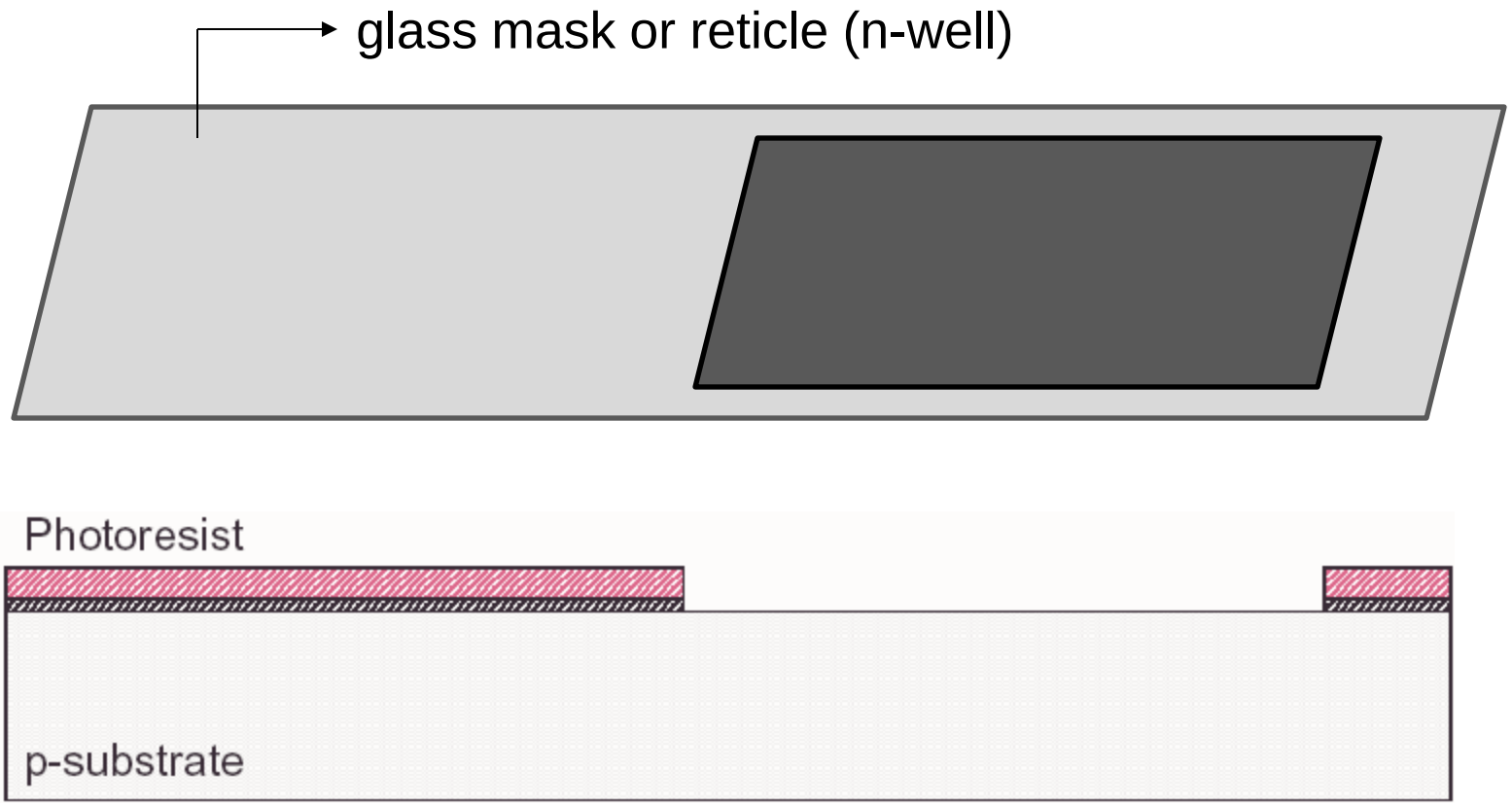



SiO2
p-substrate


NMOS
PMOS
p+
n+
n+
p+
p+
n+
n-well
p-substrate


VOUT
+VDD
S
D
D
S
G
G

- Process step: Lithography sequence for n-well
  - Photolithography: Transfer circuit layout information to the wafer Layout consists of polygons. Layout is first “written” to a transparent glass “mask” by a precisely controlled electron beam.



- Process step: Lithography sequence for n-well

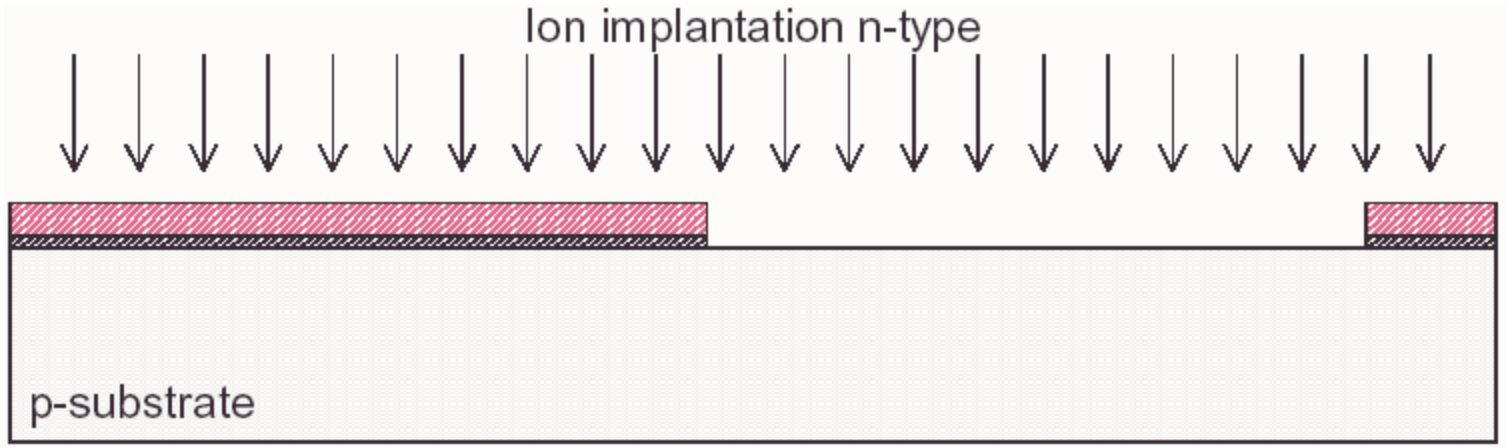
  – Negative Photoresist (PR) deposition

    PR: A material whose etching properties change upon exposure to light. Negative PR “hardens” in regions exposed to UV light. Positive PR “hardens” in regions not exposed to UV light.

  – Exposure to ultraviolet (UV) light using the n-well mask

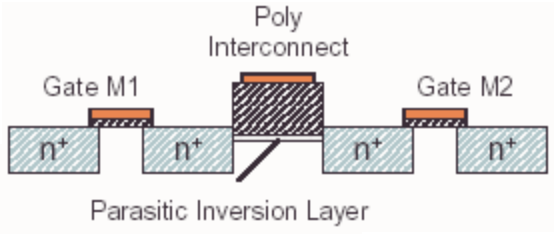
  – Selective etching. Etchant dissolves “soft” PR.

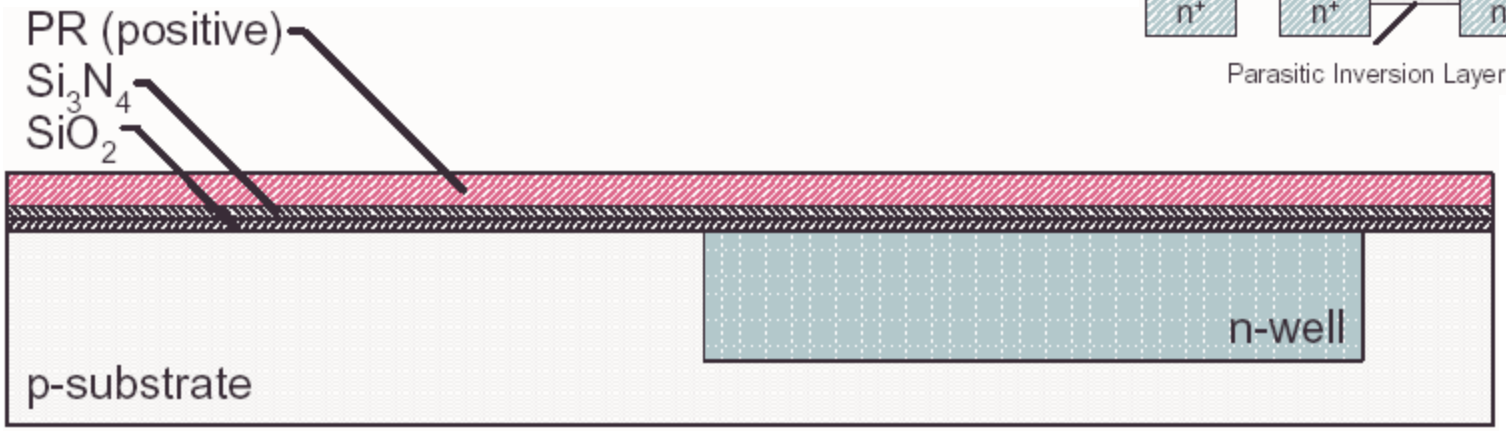
- Process step: Create n-wells through ion implantation
  - n-wells required for p-channel devices
    - n-channel devices will be fabricated directly in the native p-substrate
  - Ion implantation: Selectively introduce dopants (N or P or As) into the wafer
    - Doping atoms are accelerated as a high-energy focused beam, hitting the surface and penetrating the exposed areas. Doping level determined by intensity and duration of implantation.
    - Retrograde profile: Peak of the doping concentration occurs well below the surface.



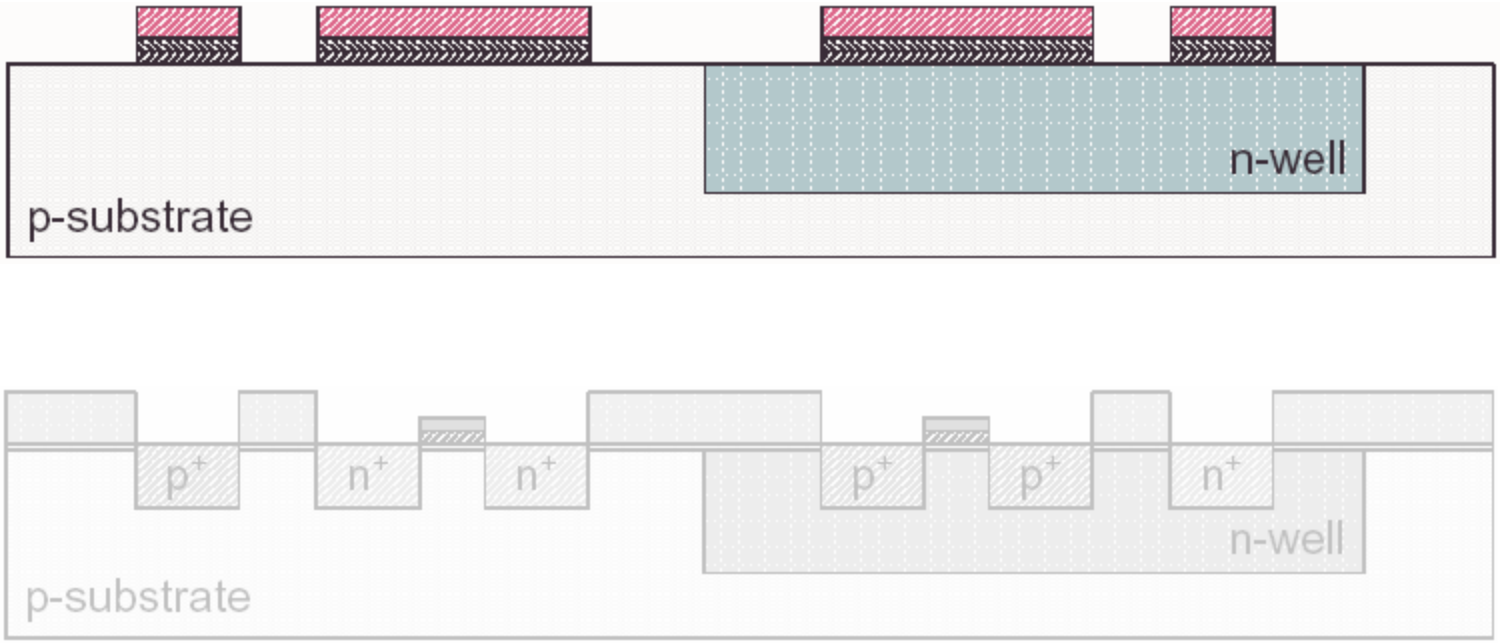
- Process step: Remove PR and oxide layer
  - n-well completed
  - Note: Ion implantation damages the Si lattice
    - Si lattice can be repaired through an annealing process. Annealing: Wafer is heated to 1000°C for 15-30min allowing the lattice bonds to form again. Annealing causes dopant diffusion in all directions (e.g. side diffusion of S/D regions). Therefore, wafer is annealed only once after all implantations have been completed.

- Process step: Channel-stop implant (1)
  - Channel-stop implant to prevent parasitic MOSFETs
    - Prevents conduction between unrelated transistor sources and drains (and wells). Two n+ regions and the FOX form a transistor. FOX is thick, therefore transistor has a large V_{th}. Nonetheless, a sufficiently positive potential on the interconnect line will turn on the transistor slightly (causing a leakage path). Channel-stop implant raises V_{th} of parasitic transistor to a very large value.
  - Create a stack of silicon dioxide, silicon nitride, & positive PR

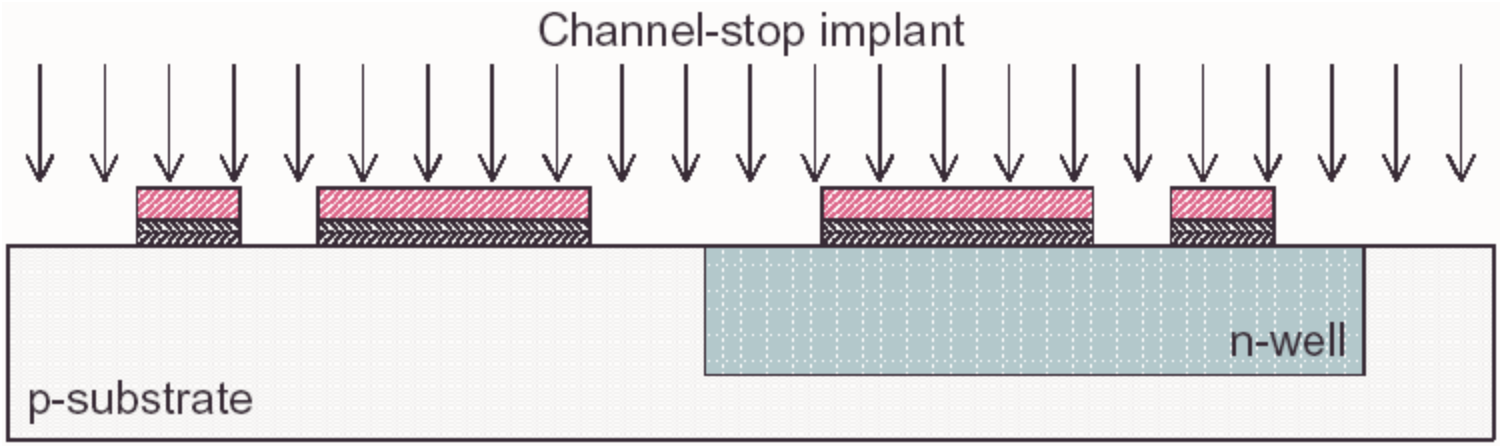




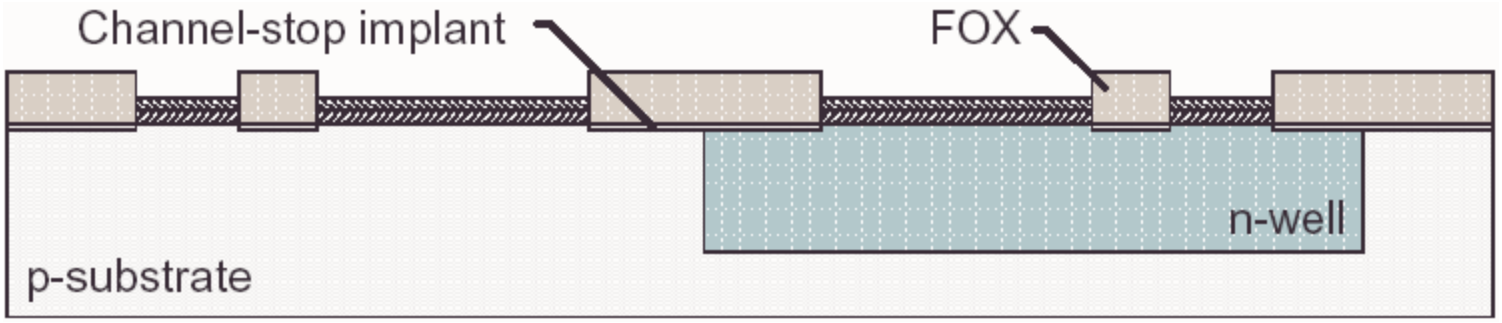
- Process step: Channel-stop implant (2)
  - Lithography sequence for channel-stop implant (based on positive PR)
  - “Active” mask is used
    - Active or diffusion areas include the source/drain regions and the p+ and n+ openings for the substrate and well ties.



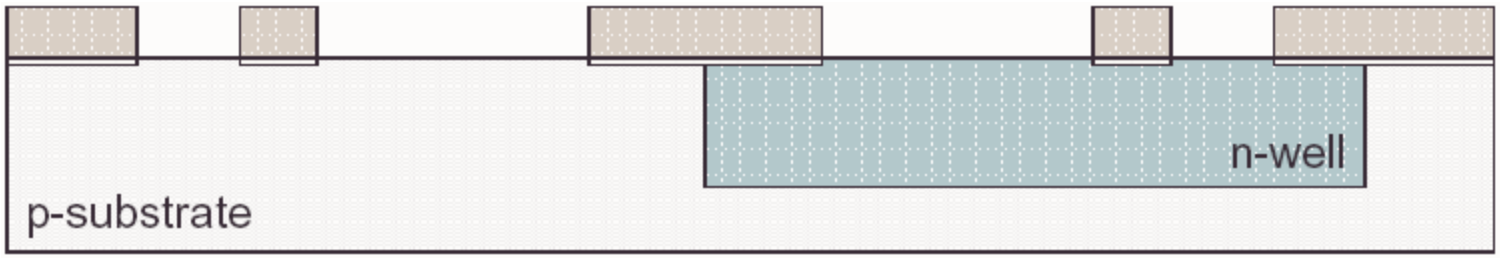
- Process step: Channel-stop implant (3)
  - Perform channel-stop ion implantation



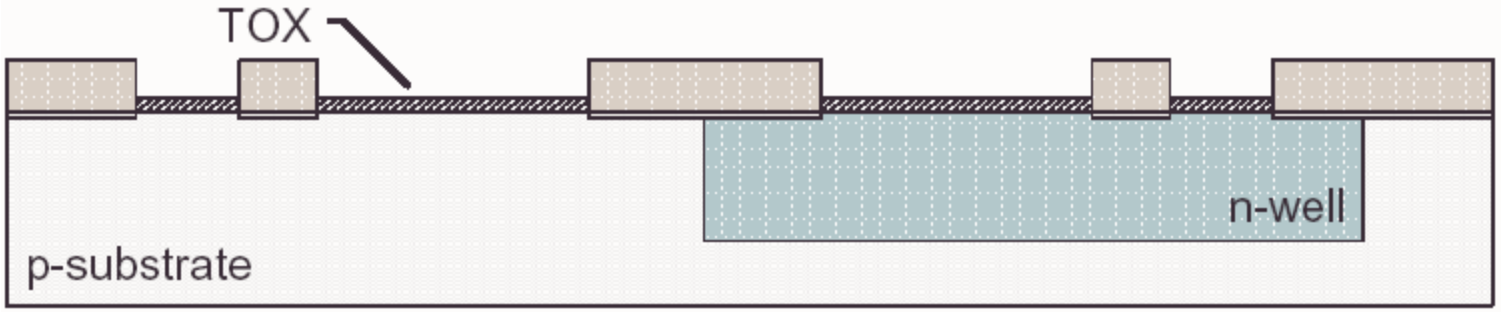
- Process step: Channel-stop implant (4)
  - Remove PR
  - Thick oxide layer is grown in the exposed silicon areas producing the field oxide (FOX)
    - FOX grows in areas where the silicon nitride layer is absent



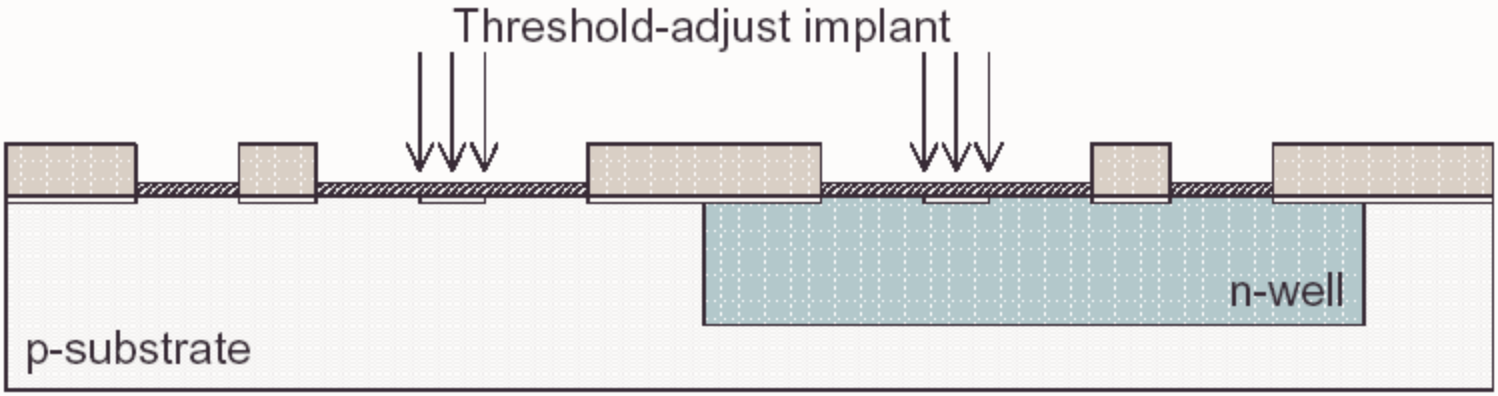
- Process step: Channel-stop implant (5)
  - Remove protective silicon nitride layer
  - Remove protective thin oxide layer
  - Result: Active areas are exposed



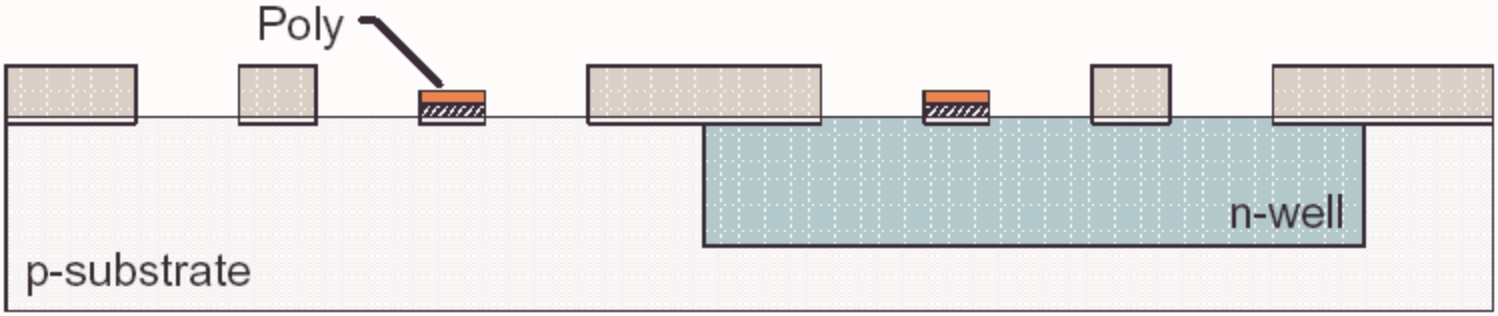
- Process step: Growth of gate oxide
  - Growth of gate oxide serving as gate dielectric (TOX)
    - The growth of the gate oxide is a very critical step in the process. It's thickness $\mathbf{t_{ox}}$ determines a multitude of parameters of MOSFETs (current handling, transconductance, reliability). In order to achieve good matching of transistors extremely uniform thickness across the wafer is required. The oxide is therefore grown in a slow low-pressure CVD (chemical vapor deposition) process. Also, the cleanness of the silicon surface underneath the oxide affects the electrical behavior of the MOSFET.



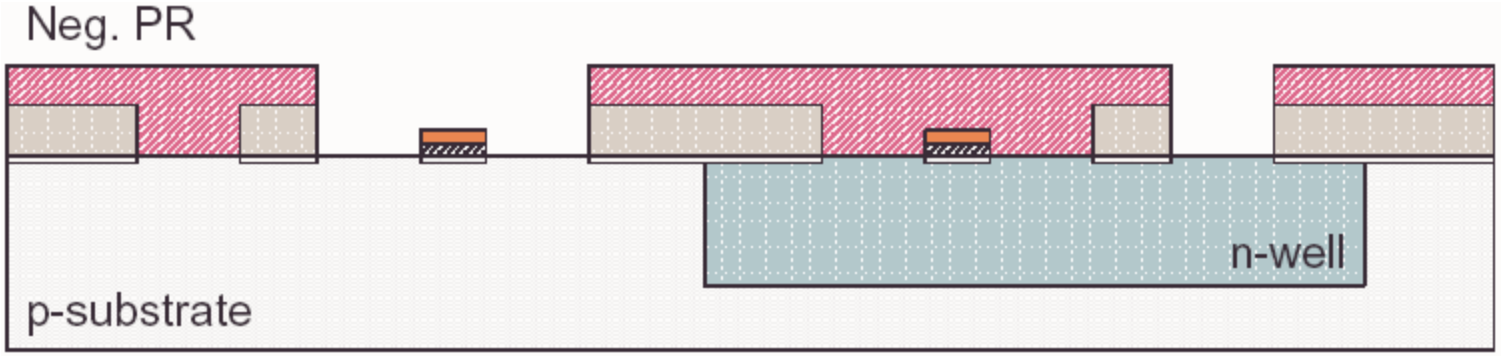
- Process step: Threshold-adjust implant
  - Threshold-adjust implant after photolithographic process
    - The “native” threshold voltage of transistors is typically far from the desired value ($V_{THN} \approx 0V$ and $V_{THP} \approx -1V$). A thin layer of dopants near the surface is implanted to adjust the native threshold voltage. Thresholds of both NMOS and PMOS transistors will become more positive.



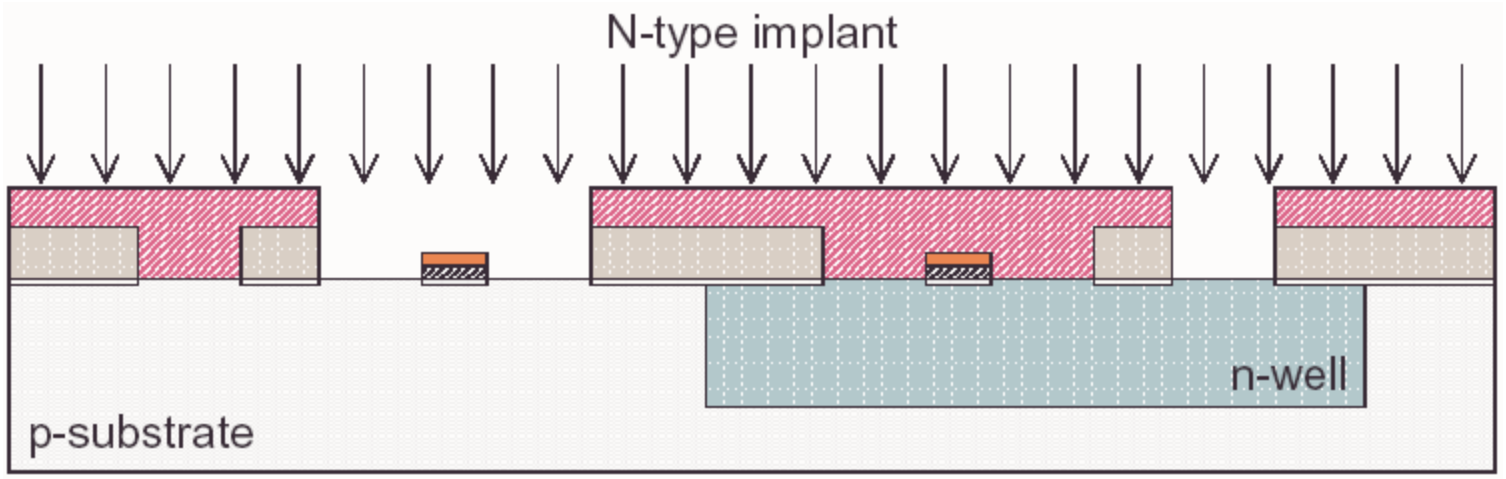
- Process step: Create polysilicon (poly) layer
  - Deposit a layer of polysilicon on top of the gate oxide
    - Polysilicon is noncrystalline (or “amorphous”) silicon because this layer grows on top of silicon dioxide, i.e. cannot form a crystal. Since polysilicon only serves as a conductor its amorphous nature is unimportant.
  - Carry out “poly mask” lithography



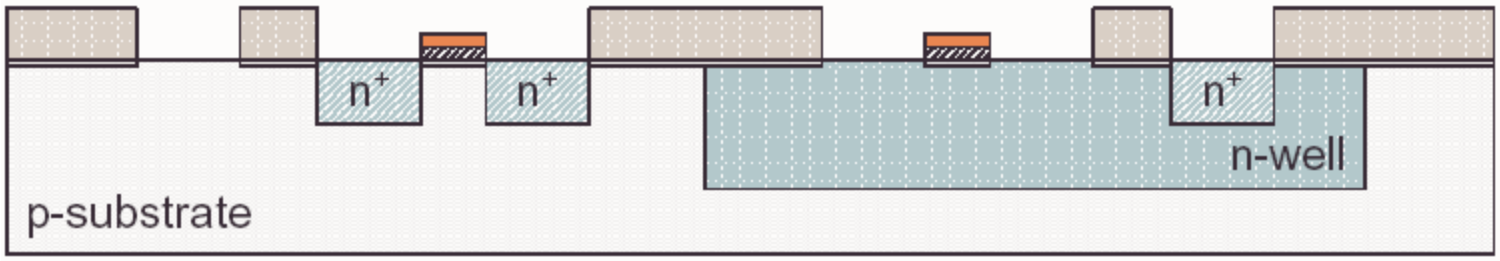
- Process step: n-type implant (1)
  - Deposit negative photoresist
  - Photolithography using “N source/drain mask”
    - After the photolithography all areas to receive an n+ implant are exposed. These areas consist of source and drain junctions of NMOS transistors, and the n-well ties.



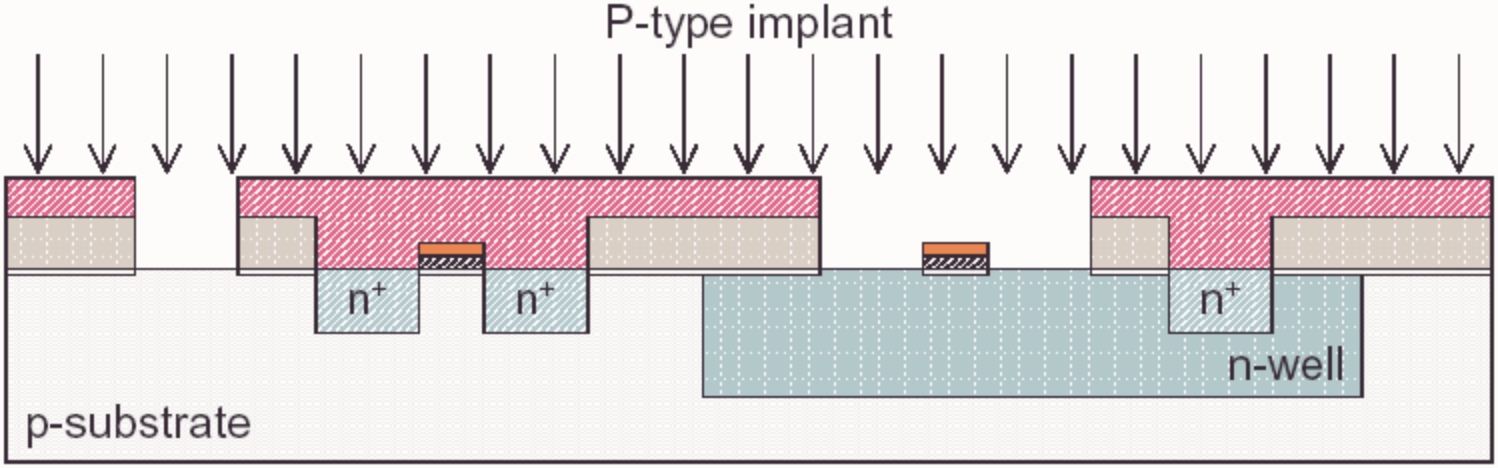
- Process step: n-type implant (2)
  - Ion implantation
    - Ion implantation forms the S/D regions of NMOS transistors and n-well ties. Note that the implant also dopes the polysilicon layer of the NMOS transistors, reducing its sheet resistance.



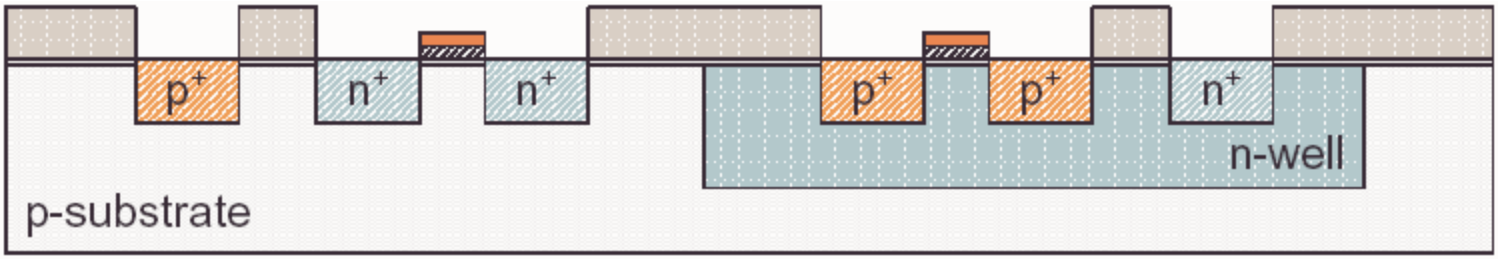
- Process step: n-type implant (3)
  - Remove PR
  - Self-aligned structure
    - The sequence of creating the gates first prior to n-type implantation yields a **self-aligned gate** structure. The S/D regions are implanted at precisely the edges of the gate area. A small misalignment in lithography has no major effect (it simply makes one junction slightly narrower than the other).



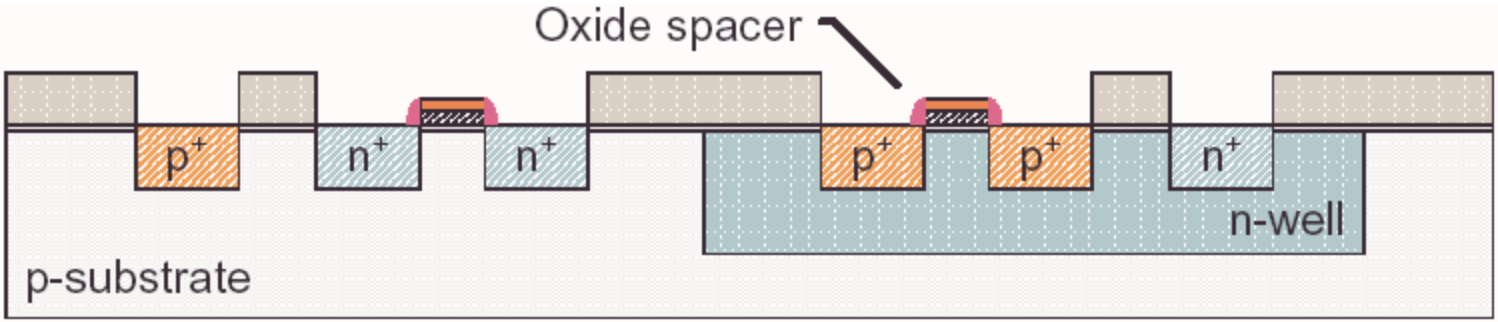
- Process step: p-type implant (1)
  - Photolithography sequence using “P source/drain mask”
    - After the photolithography all areas to receive an p+ implant are exposed. These areas consist of source and drain junctions of PMOS transistors, and the substrate ties.
  - Ion implantation
    - The implant also dopes the polysilicon layer of the PMOS transistors, reducing its sheet resistance.



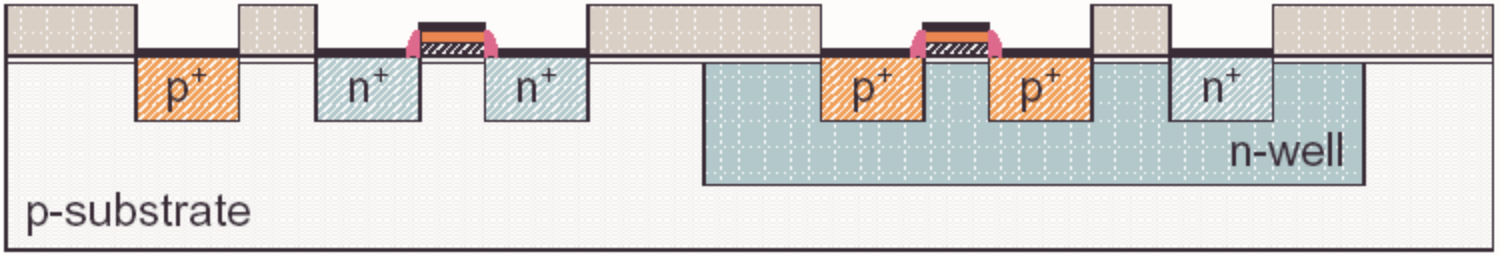
- Process step: p-type implant (2)
  - Remove PR
  - Basic transistor fabrication complete
  - Remaining processing steps: “Back-end processing”



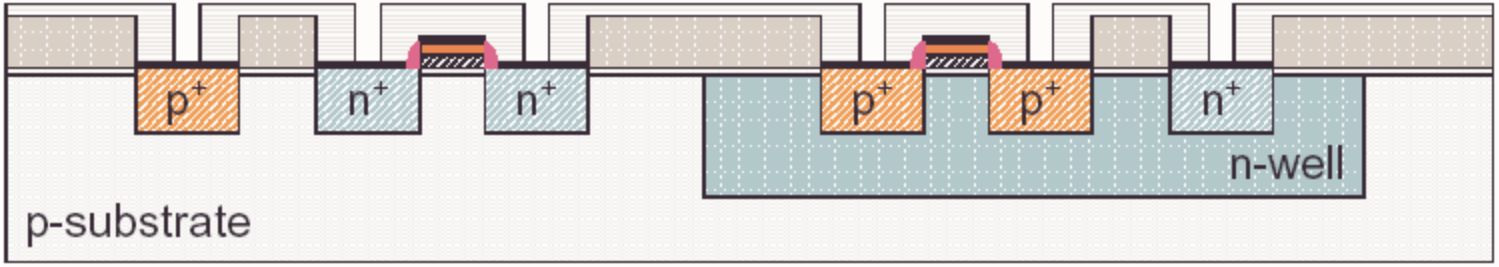
- Process step: Silicidation (1)
  - Creation of oxide spacer
    - Purpose of Silicidation: Reduction of sheet resistance of doped polysilicon and S/D regions by about an order of magnitude. During silicidation active areas (S/D regions, substrate and well ties) are covered with a thin layer of highly conductive material (titanium silicide or tungsten). The silicidation process begins with creating an oxide spacer at the edges of the polysilicon gate such that the deposition of the silicide will not short the gate to the S/D regions.



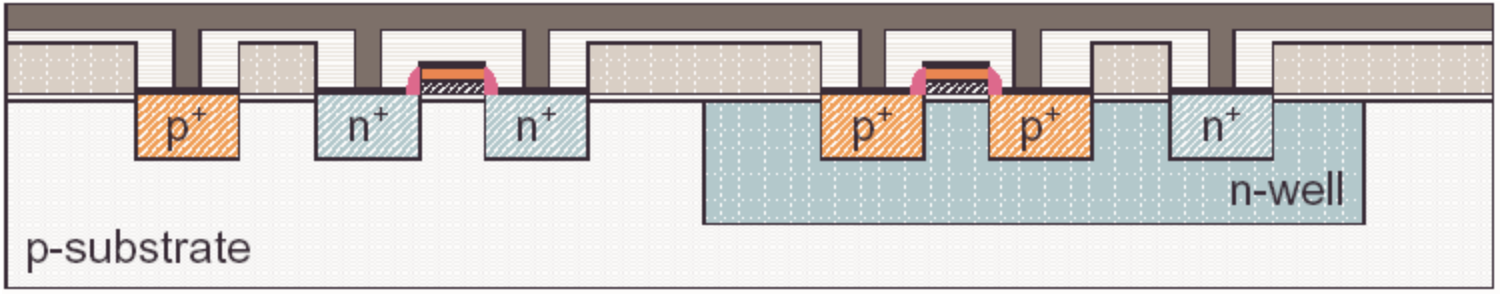
- Process step: Silicidation (2)
  - Silicidation
    - Deposition of conductive material through CVD process



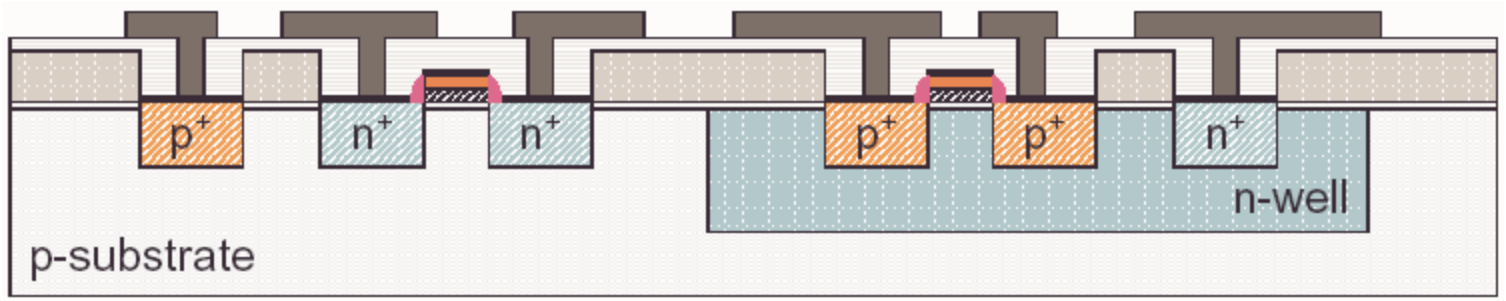
- Process step: Contact windows
  - Cover wafer with a thick layer of oxide
    - Thickness: 300 - 500nm
  - Lithography using the “contact mask”
  - Plasma etching
    - For increased reliability, contacts to the gate polysilicon are not placed on top of the gate area



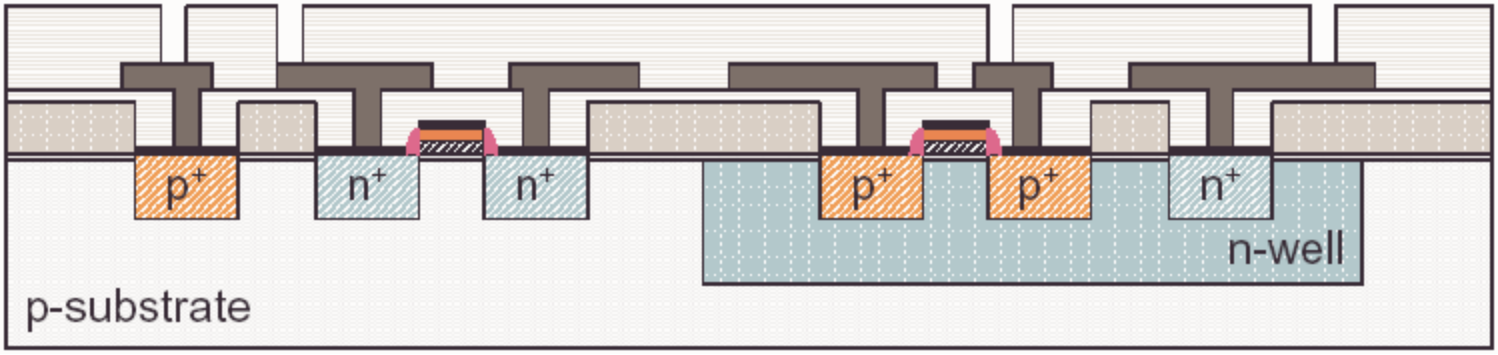
- Process step: Metal interconnect 1 (1)
  - Deposit layer of metal over the entire wafer
    - Common metals: Aluminium or copper



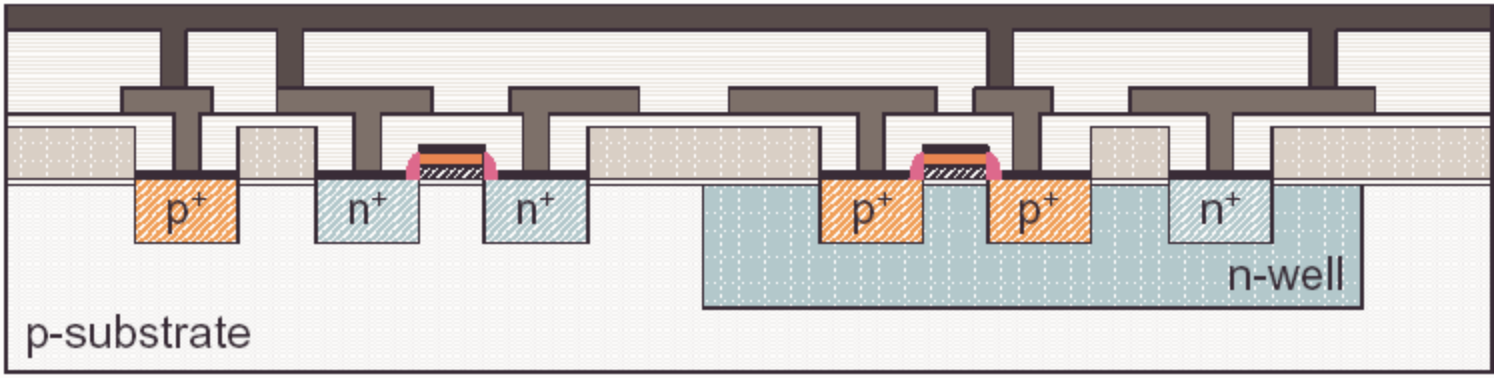
- Process step: Metal interconnect 1 (2)
  - Photolithography sequence using “Metal-1 mask”
  - Metal selectively etched



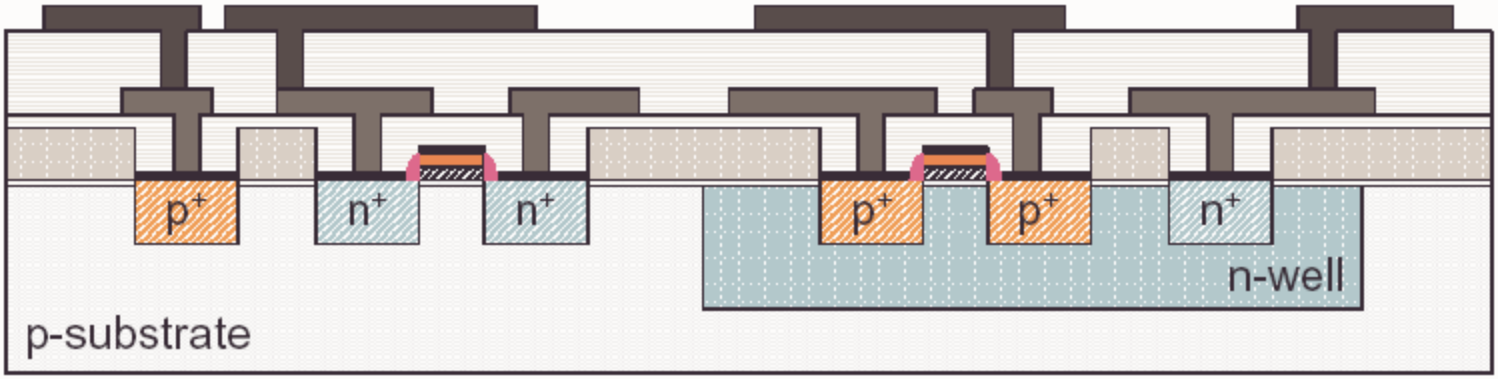
- Process step: Via windows
  - Cover wafer with a layer of SiN_3
  - Lithography using the “via mask”
  - Plasma etching



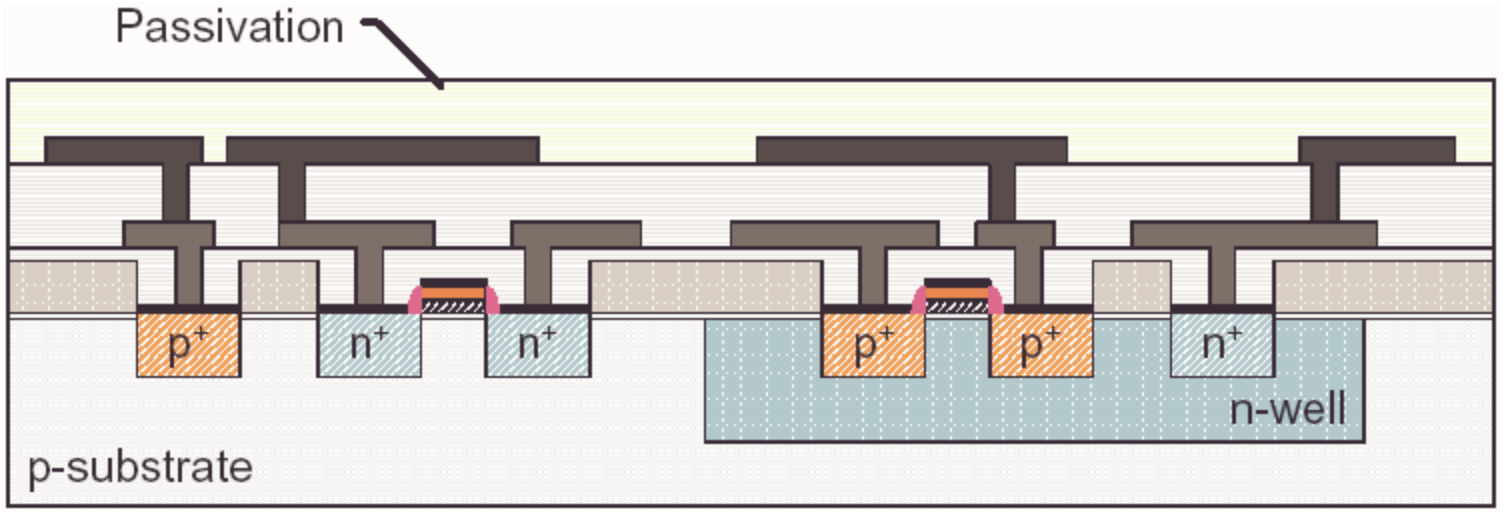
- Process step: Metal interconnect-2 (1)
  - Deposit layer of metal over the entire wafer



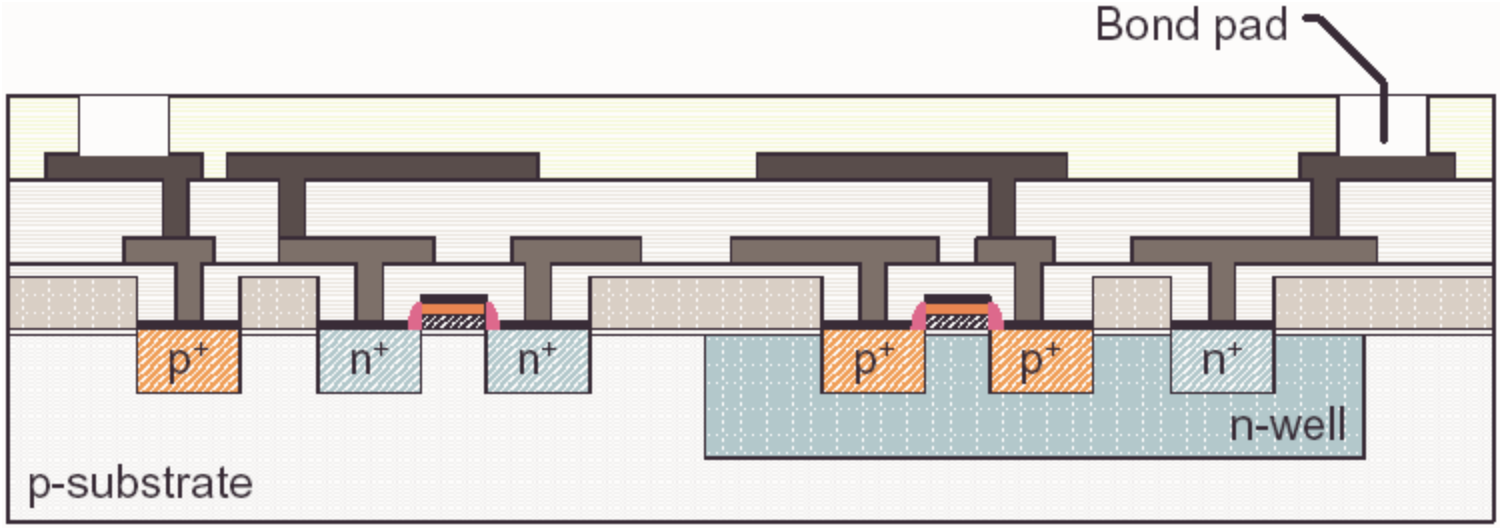
- Process step: Metal interconnect-2 (2)
  - Photolithography sequence using “Metal-2 mask”
  - Metal selectively etched
  - Metal interconnect layers:
    - Two masks required for each additional metal layer: “via-*n* mask” and “metal-*n* mask”
    - Reliability: Dimensions of contacts/vias cannot be changed by layout designer (to avoid “contact spiking”). If a large contact area is required, many small contacts/vias are used in parallel.



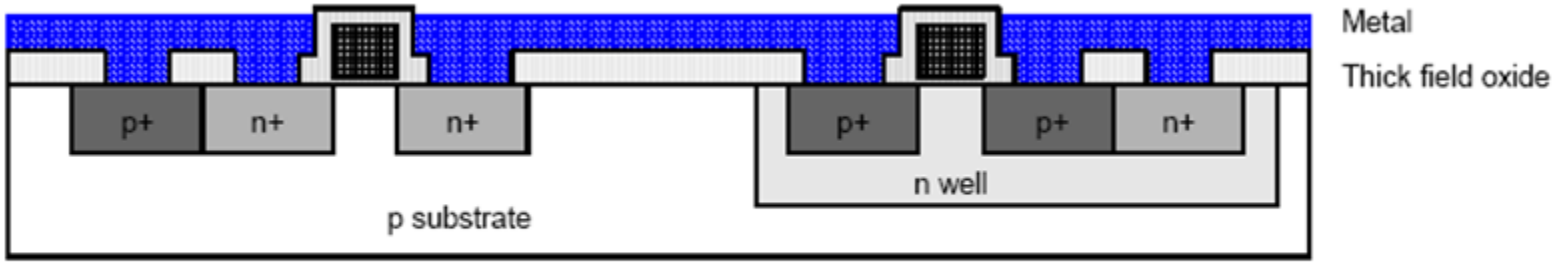
- Process step: Passivation
  - Passivation
    - Wafer is covered with a layer of “glass” or “passivation”, protecting the surface against damages caused by subsequent mechanical handling and dicing.



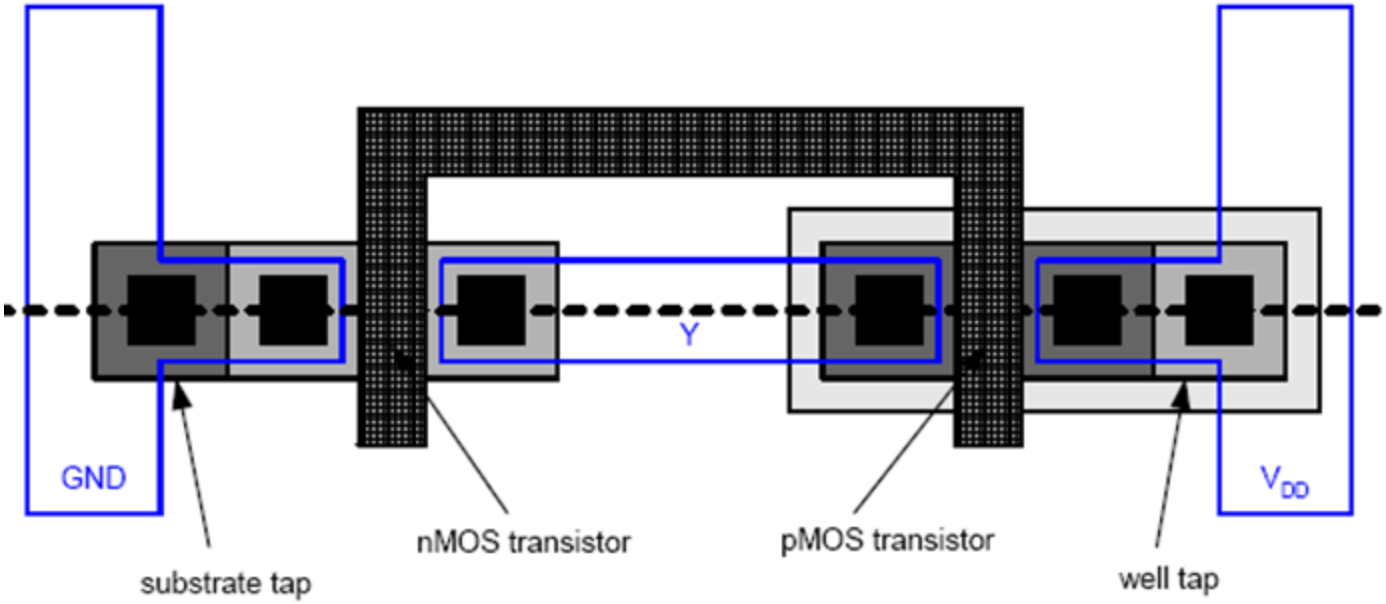
- Process step: Contact windows for bond pads
  - Photolithography sequence
- Final processing steps:
  - Testing, dicing, packaging, bonding, testing.



Layout (mask) view of the Inverter



Layout (mask) view of the inverter.



Masks: