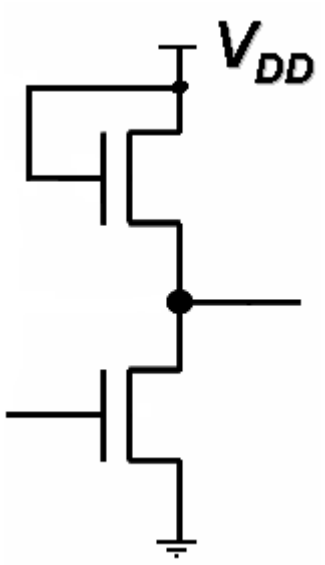
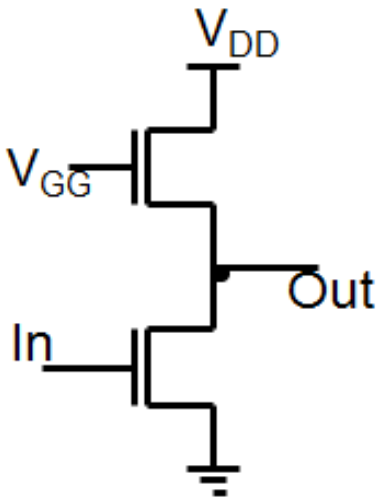
Power Dissipation in CMOS

Single Channel Inverters



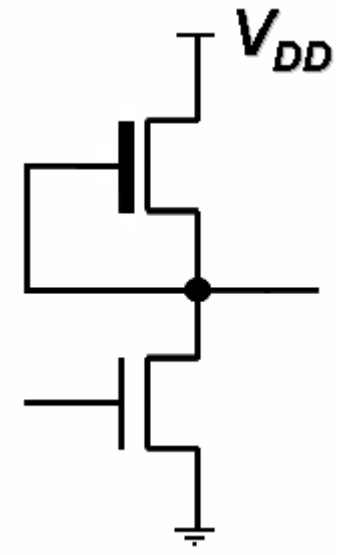
NELS

$P \alpha V^3_{DD}$



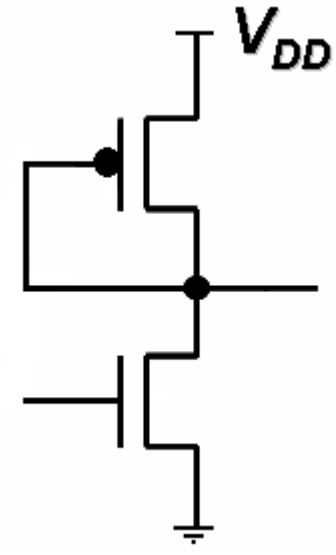
NELT

$P \alpha V^3_{DD}$



HMOS

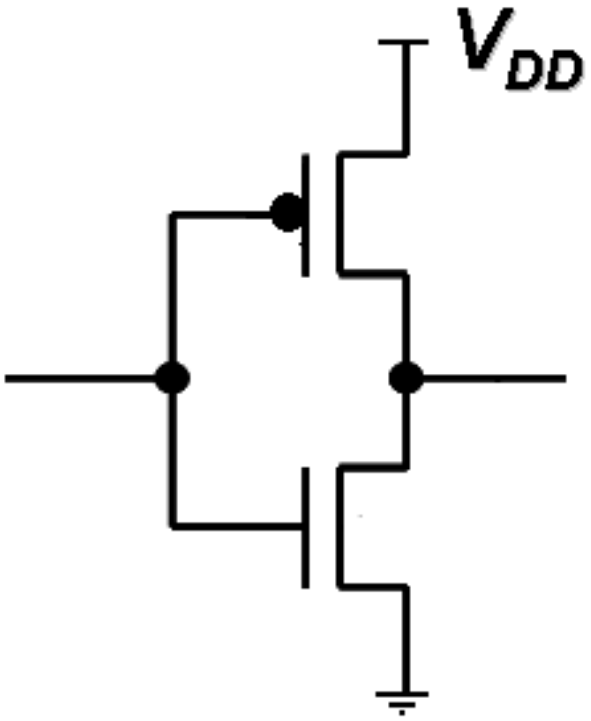
$P \alpha V_{DD}$



Pseudo-nMOS

$P \alpha V^3_{DD}$

CMOS Logic (Inverter)



No static leakage path exists for either 1 *or* 0 *input.*

Components of Power Dissipation

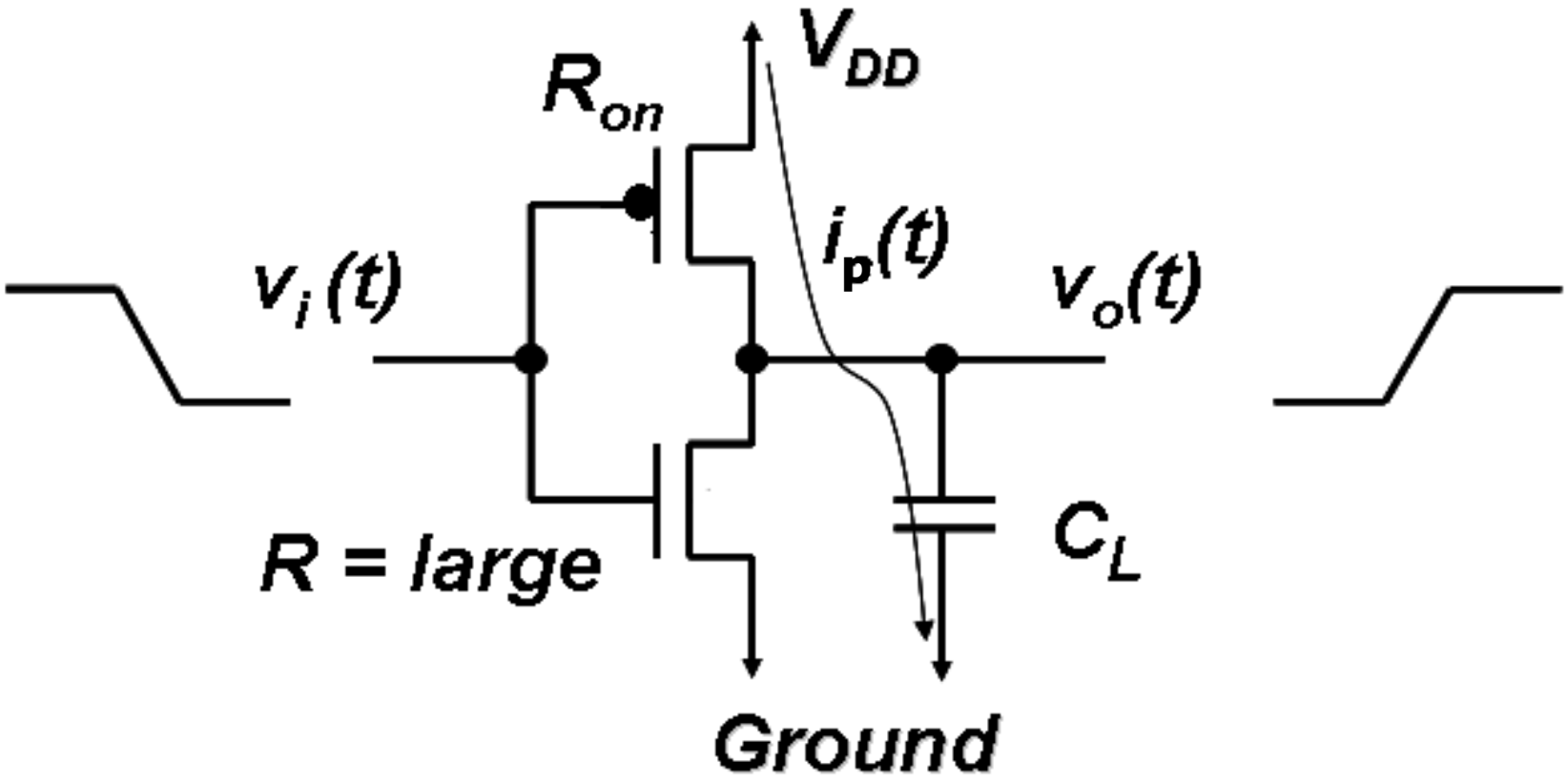
- Dynamic Component ($\mathbf{P_{dyn}}$)
  - Switching p.d. ($\mathbf{P_{sw}}$)
    - Logic activity
    - Glitches
  - Short-circuit p.d. ($\mathbf{P_{sc}}$)
- Static Component ($\mathbf{P_{stat}}$)
  - Leakage p.d.

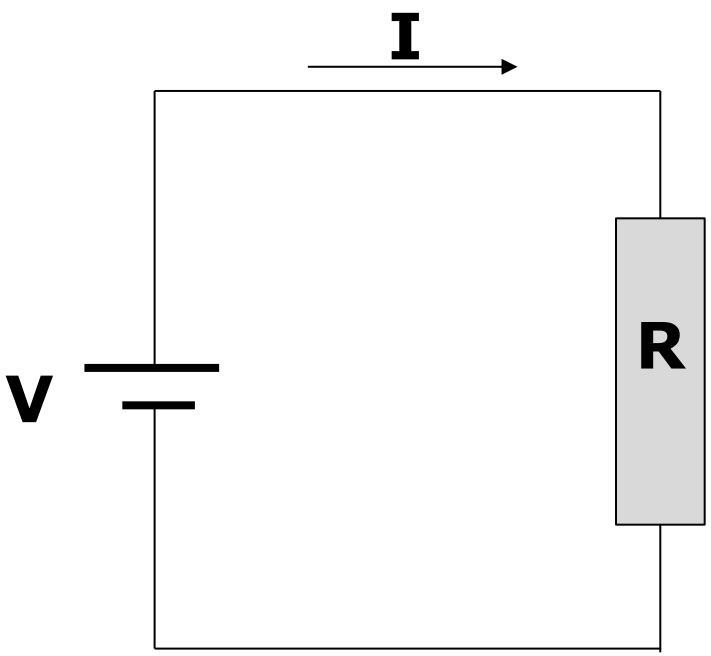
$$P_{total} = P_{dyn} + P_{stat}$$
$$= (P_{sw} + P_{sc}) + P_{stat}$$

$$I_D = I_S\left(e^{\frac{V_{Dq}}{kT}} - 1\right)$$

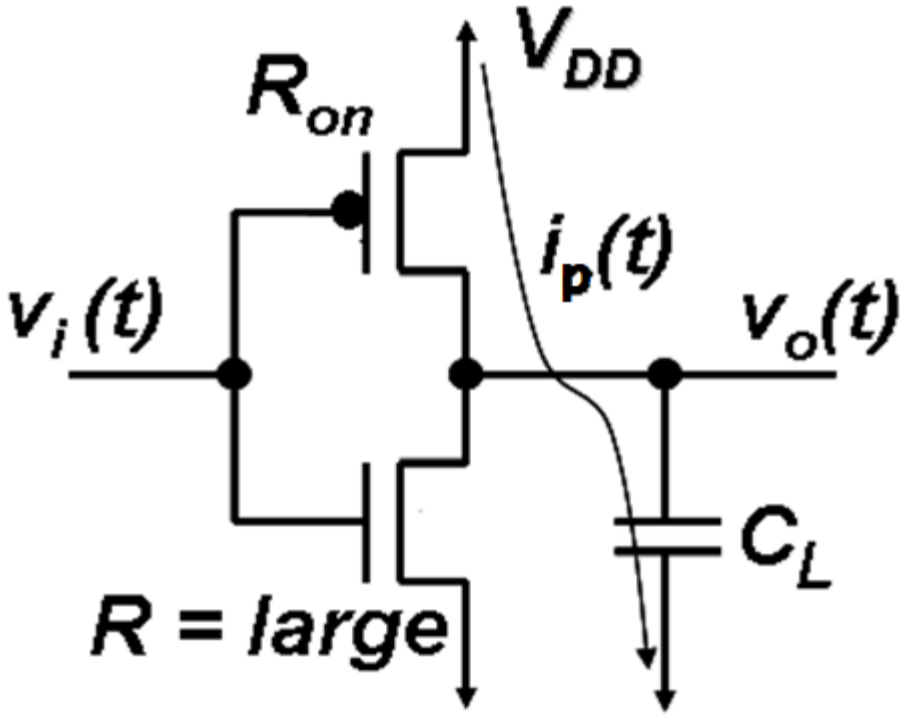
For a small-geometry IC diode, $I_S = 1E^{-16}$.

Switching Power : P_{sw}





$$P = V \times I$$



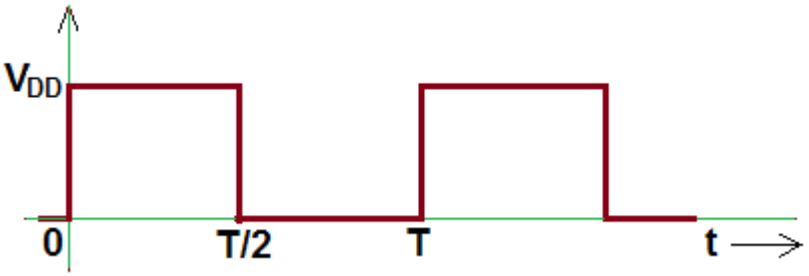
Switching Power : P_{sw}

$$P_{sw} = \frac{1}{T}\int_0^{T/2} i_N(t)\, V_{\text{Out}}\, dt + \frac{1}{T}\int_{T/2}^{T} i_P(t)(V_{DD} - V_{\text{Out}})dt$$

Since $i_N(t) = C_L dV_{\text{Out}}/dt$ and analogously for $i_P(t)$,

$$P_{sw} = \frac{C_L}{T}\int_0^{V_{DD}} V_{\text{Out}}\; dV_{\text{Out}} + \frac{C_L}{T}\int_{V_{DD}}^{0} (V_{DD} - V_{\text{Out}})d(V_{DD} - V_{\text{Out}})$$

$$\boxed{P_{sw} = \frac{C_L {V_{DD}}^2}{T}}$$



Switching Power : P_{sw}

- Gate output rising transition
  - Energy stored in capacitor = $C_L V_{DD}^2/2$
  - Energy dissipated in pMOS transistor = $C_L V^2_{DD}/2$
- Gate output falling transition
  - Energy dissipated in nMOS transistor = $C_L V^2_{DD}/2$
- Energy dissipated per transition = $C_L V^2_{DD}$

$\therefore$ Total Power dissipation:

$$\mathbf{P_{sw} = C_L V^2_{DD} / T}$$

Lowering Switching Power:

Capacitance:
Function of Fan-out, Wire length and transistor sizes.

Clock Frequency:
Increasing

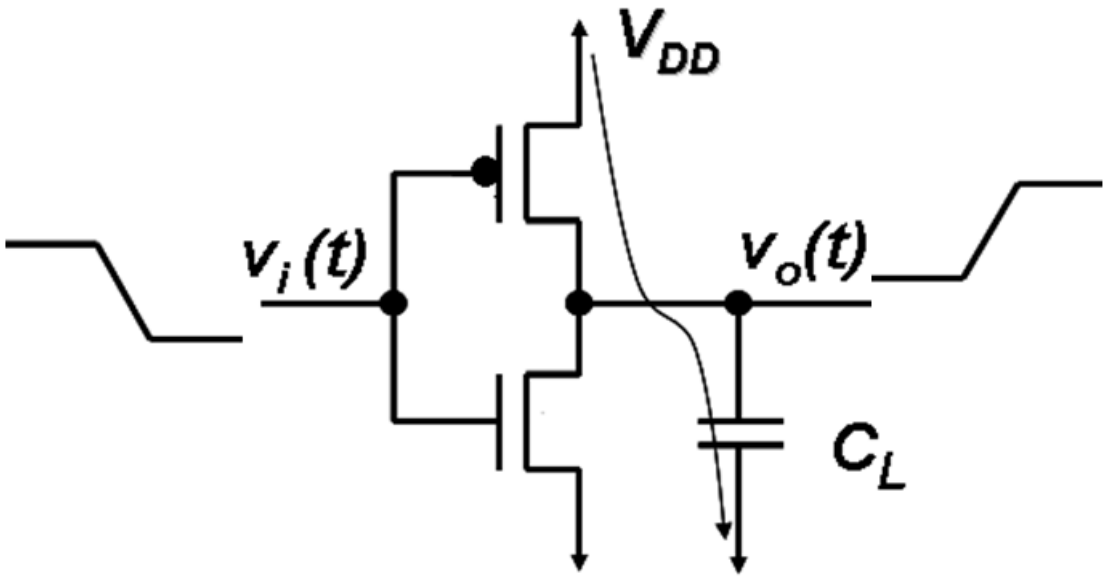
$$P_{sw} = C_L V_{DD}^2 f_{CLK} \alpha$$

Supply voltage:
Dropping with
Successive generations

Activity factor:
How often, on average, do a node switch?

Activity factor

$$P_{sw} = C_L V^2_{DD} f_{CLK} \alpha$$

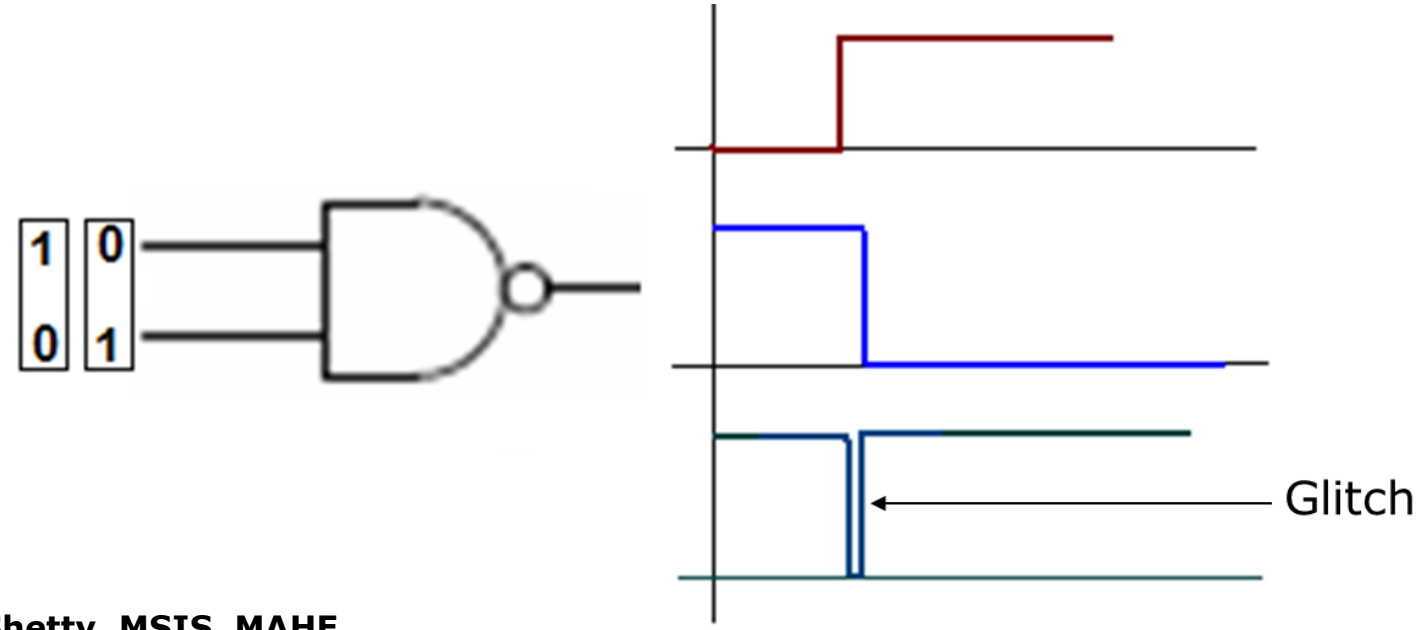


$$P_{sw} = C_L V^2_{DD} f_{CLK} \alpha$$

- Even though power dissipation takes place in a channel resistance, in the equation above the resistance parameter is missing and the power is independent of resistance. Why?

Glitches

- Glitches are temporary changes in the value of the output – unnecessary transitions.
- Are caused due to the skew in the input signals to a gate.



Type of Logic Function: NOR vs. XOR

Example: Static 2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities

$p_{A=1} = 1/2$

$p_{B=1} = 1/2$

Then transition probability

$p_{0\to1} = p_{Out=0} \times p_{Out=1}$

$= 3/4 \times 1/4 = 3/16$

If inputs switch every cycle

$\alpha_{0\to1} = 3/16$

Type of Logic Function: NOR vs. XOR

Example: Static 2-input XOR Gate

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

Assume signal probabilities

$p_{A=1} = 1/2$

$p_{B=1} = 1/2$

Then transition probability

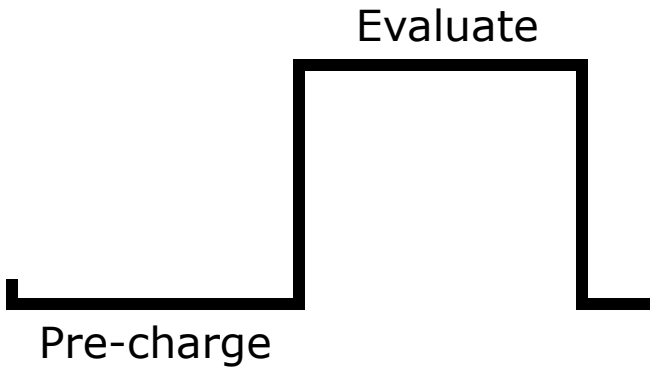
$p_{0\to1} = p_{Out=0} \times p_{Out=1}$

$= 1/2 \times 1/2 = 1/4$

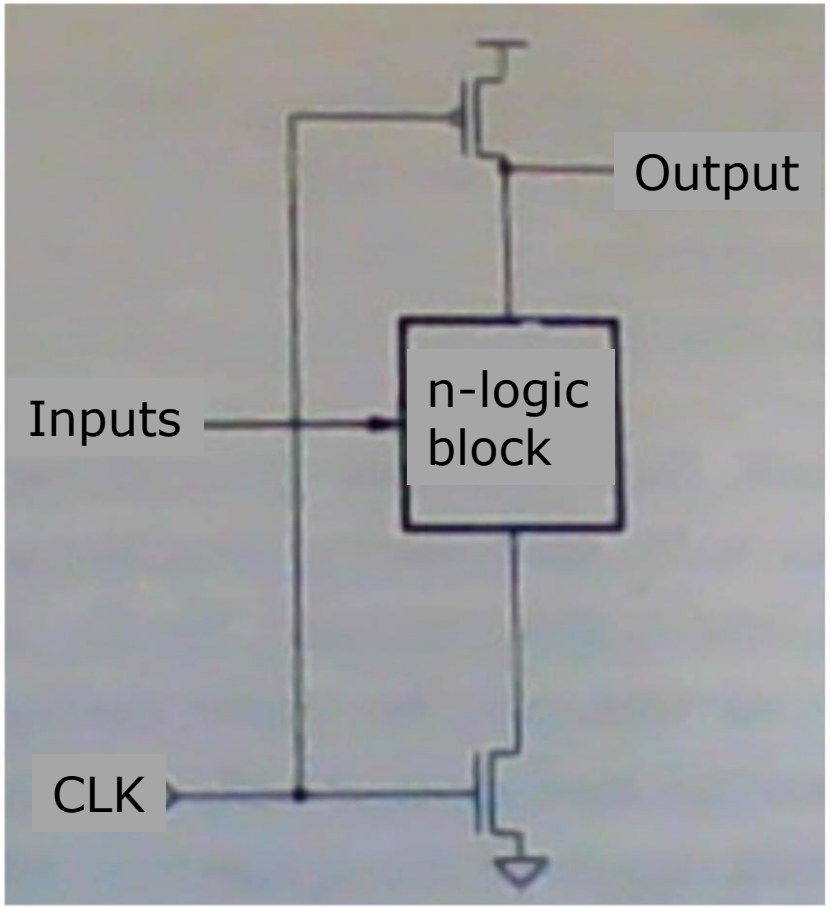
If inputs switch in every cycle

$\alpha_{0\to1} = 1/4$

Dynamic Gate



CLK Waveform



Dynamic Power Consumption is Data Dependent

Dynamic 2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities

$P_{A=1} = 1/2$

$P_{B=1} = 1/2$

Then transition probability

$P_{0\rightarrow1} = P_{out=0} \times P_{out=1}$

$= 3/4 \times 1 = 3/4$

Switching activity always higher in dynamic gates!

$P_{0\rightarrow1} = P_{out=0}$

Glitch Power Dissipation

- Depending on the skew, the gate output voltage may perform a full swing or not.
- An approximation of the energy drawn during the glitch is:

$$P_{glitch} = \frac{1}{T} \cdot C_{load} \cdot V_{dd} \cdot \sum_{i=1}^{n} \Delta V_n$$

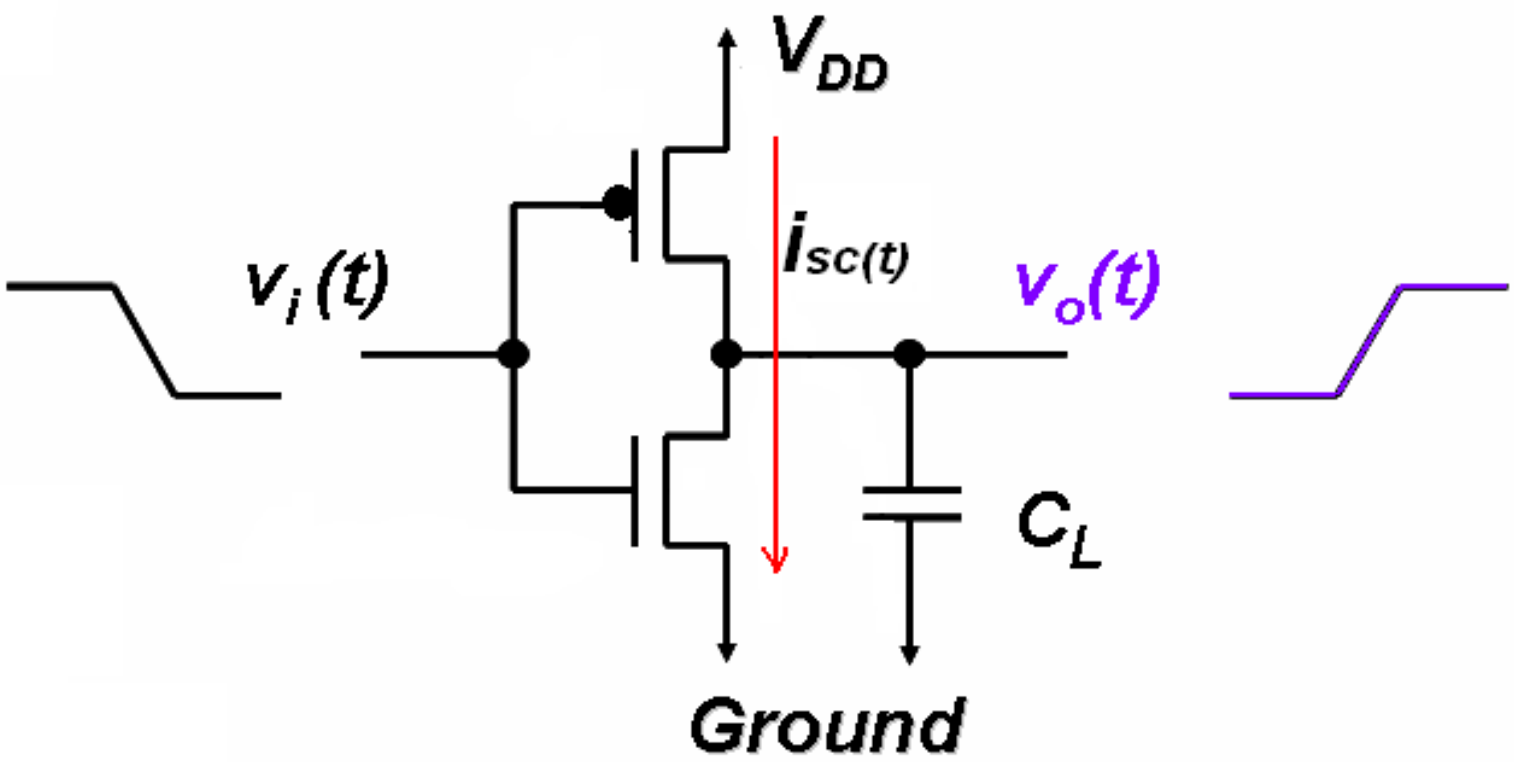
Where ΔV_n is the voltage swing of a sequence of n incomplete transitions within a period of T .

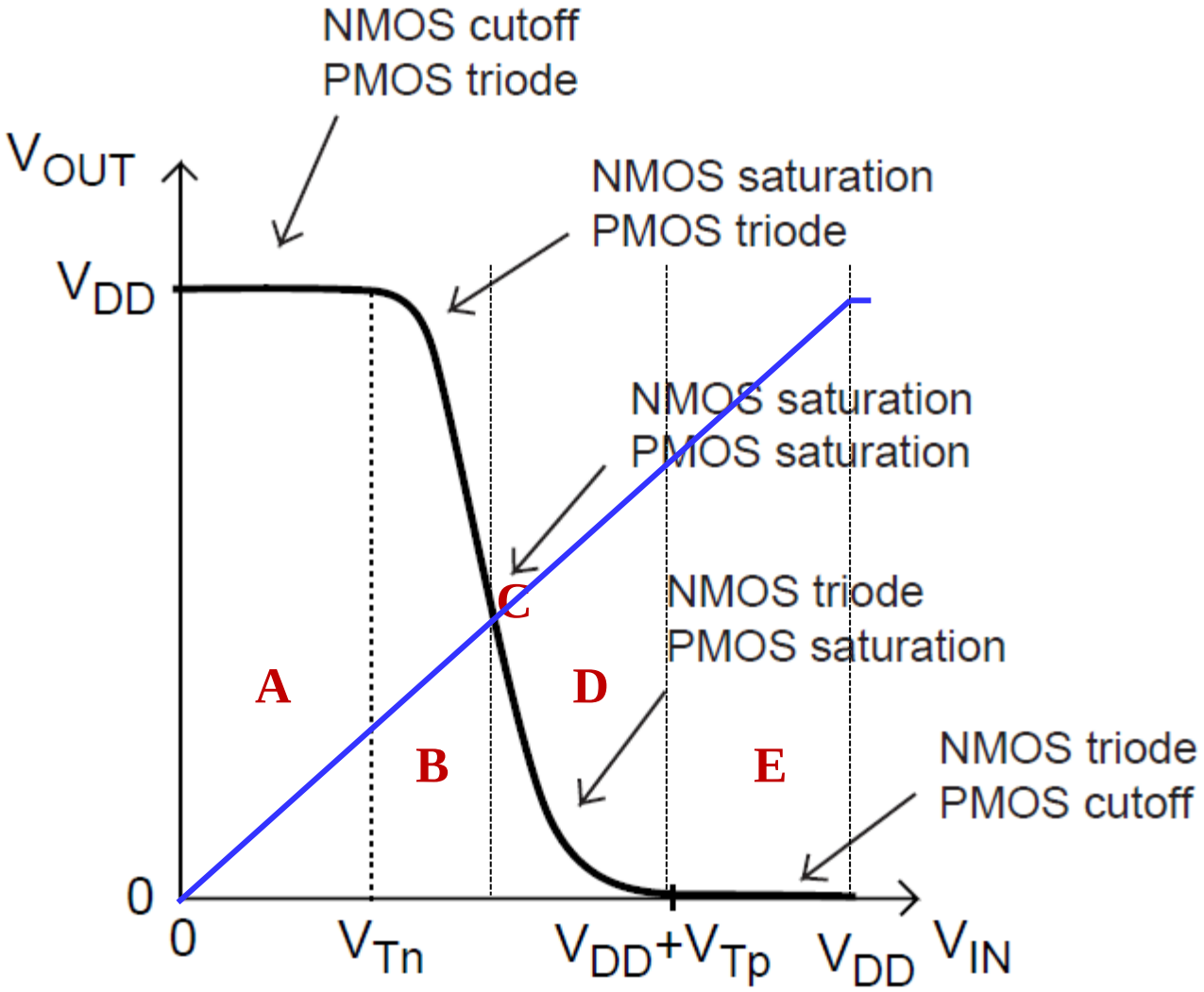
Components of Power Dissipation

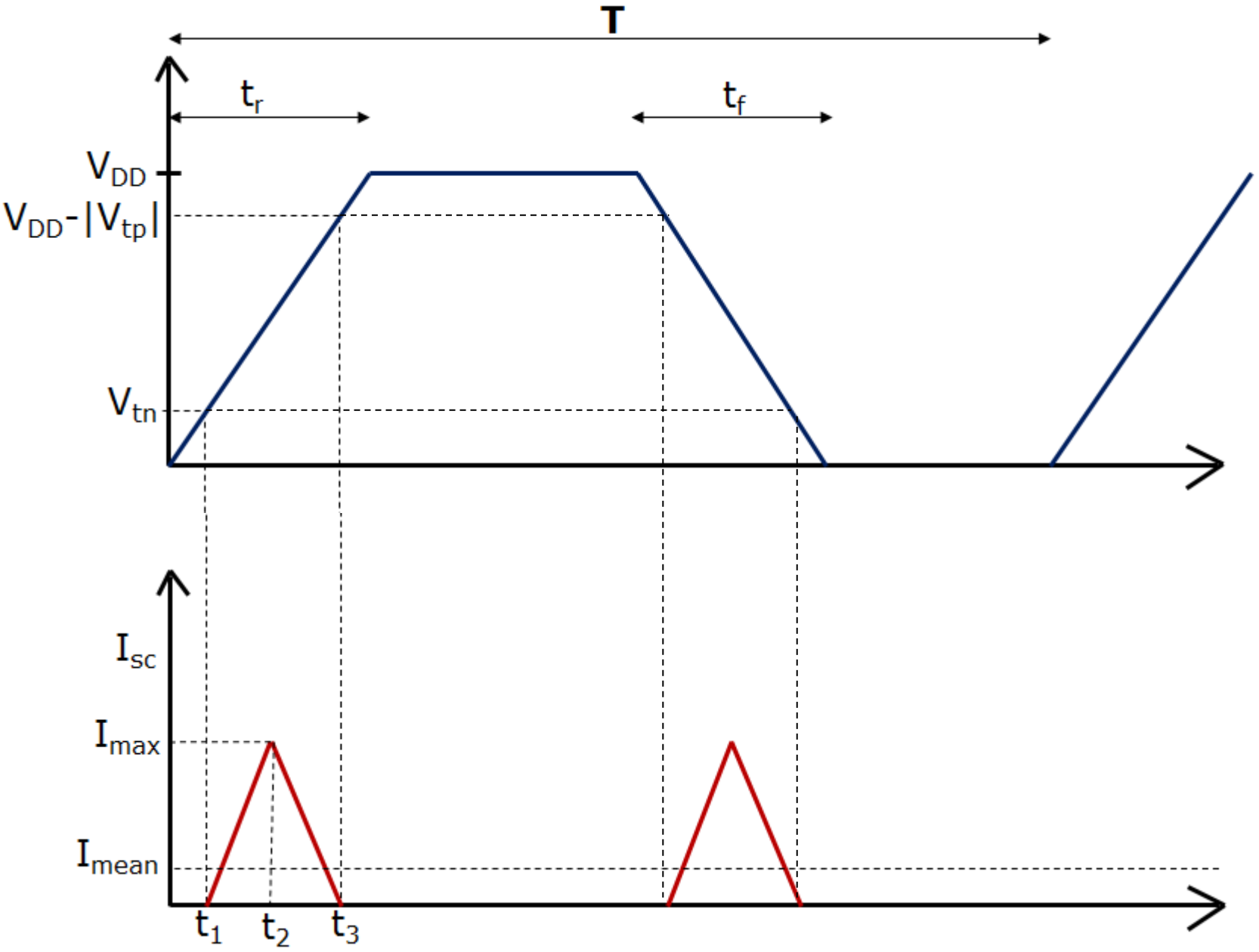
- Dynamic Component ($\mathbf{P_{dyn}}$)
  - Switching p.d. ($\mathbf{P_{sw}}$)
    - Logic activity
    - Glitches
  - **Short-circuit p.d. ($\mathbf{P_{sc}}$)**
- Static Component ($\mathbf{P_{stat}}$)
  - Leakage p.d.

$$P_{total} = P_{dyn} + P_{stat}$$
$$= (P_{sw} + P_{sc}) + P_{stat}$$

Short Circuit Power of a Transition: P_{sc}




NMOS cutoff
PMOS triode
V_{OUT}
NMOS saturation
PMOS triode
V_{DD}
NMOS saturation
PMOS saturation
C
NMOS triode
PMOS saturation
A
D
B
E
NMOS triode
PMOS cutoff
0
0
V_{Tn}
$V_{DD}+V_{Tp}$
V_{DD}
V_{IN}


T
t_r
t_f
V_{DD}
V_{DD}-$|V_{tp}|$
V_{tn}
I_{sc}
I_{max}
I_{mean}
t_1
t_2
t_3

The short-circuit power dissipation is given by

$$P_{sc} = I_{mean} \cdot V_{DD}$$

For the input waveform shown, which depicts the short circuit in an unloaded inverter,

$$I_{mean} = 2 \times \left[\frac{1}{T} \int_{t_1}^{t_2} I(t)\, dt + \frac{1}{T} \int_{t_2}^{t_3} I(t)\, dt \right]$$

assuming that $V_{tn} = -V_{tp}$ and $\beta_n = \beta_p$ $(=\beta)$ and that the behavior is symmetrical around t_2.

$$= 2 \times \frac{2}{T} \int_{t_1}^{t_2} \frac{\beta}{2} \left(V_{in}(t) - V_t \right)^2 dt$$

with

$$V_{in}(t) = \frac{V_{DD}}{t_r} t \; ; \qquad t_1 = \frac{V_{t_n}}{V_{DD}} t_r \; ; \qquad t_2 = \frac{t_r}{2}$$

Peak Short Circuit Current

For an unloaded inverter, assuming that $t_r = t_f = \tau$

$$P_{SC} = \frac{\beta}{12}(V_{DD} - V_{TH})^3 \frac{\tau}{T}$$

- Increases with the size (or gain, β) of transistors
- Increases with rise and fall times of input
- Decreases and eventually becomes zero when V_{DD} is scaled down but the threshold voltages are not scaled down.
- Decreases with load capacitance, C_L
- Largest when $C_L = 0$

Summary: Short-Circuit Power

- Short-circuit power is consumed by each transition (increases with input transition time).
- Reduction requires that gate output transition should not be faster than the input transition (faster gates can consume more short-circuit power).
- Scaling down of supply voltage with respect to threshold voltages reduces short-circuit power; completely eliminated when $V_{DD} \leq |V_{tp}| + V_{tn}$.

Solution:

- Theorem – A CMOS gate consumes no short-circuit power when $V_{DD} \leq V_{tn} + |V_{tp}|$, i.e., supply voltage is lower than the sum of the threshold voltage magnitudes for the n and p channel MOSFETs.

- Proof: The short-circuit conduction requires that a pull-up path through pMOS devices and a pull-down path through nMOS devices should be simultaneously on. If the common gate voltage for both devices is V_{in}, where $0 \leq V_{in} \leq V_{DD}$, then a necessary condition for short-circuit conduction is:

$$V_{tn} \leq V_{in} \leq V_{DD} - |V_{tp}|$$

In order to make this condition impossible, we must ensure that the upper bound on V_{in} does not exceed the lower bound. Thus,

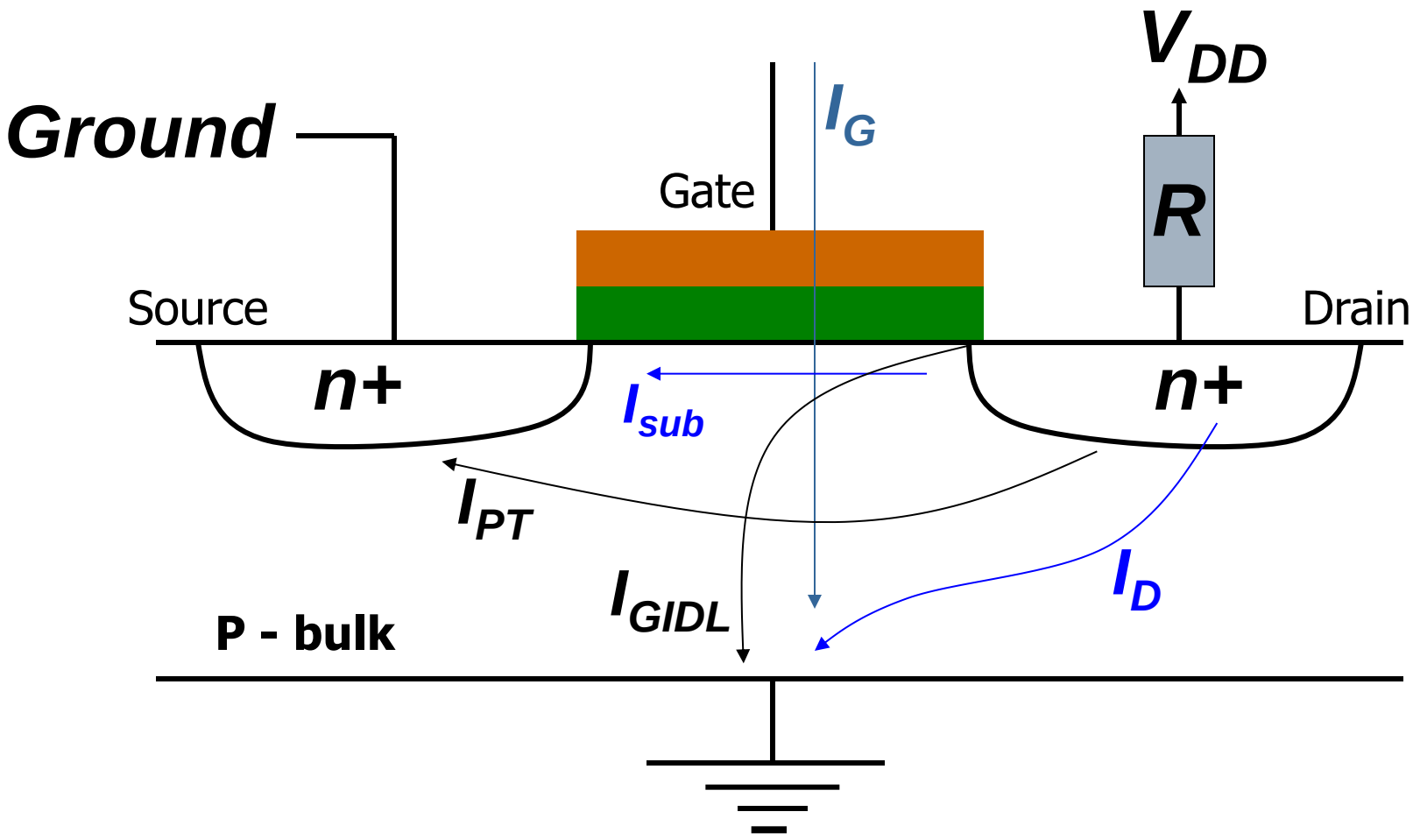
$$V_{DD} - |V_{tp}| \leq V_{tn}$$

Therefore, $V_{DD} \leq V_{tn} + |V_{tp}|$

Components of Power

- Dynamic
  - Signal transitions
    - Logic activity
    - Glitches
  - Short-circuit
- Static
  - Leakage

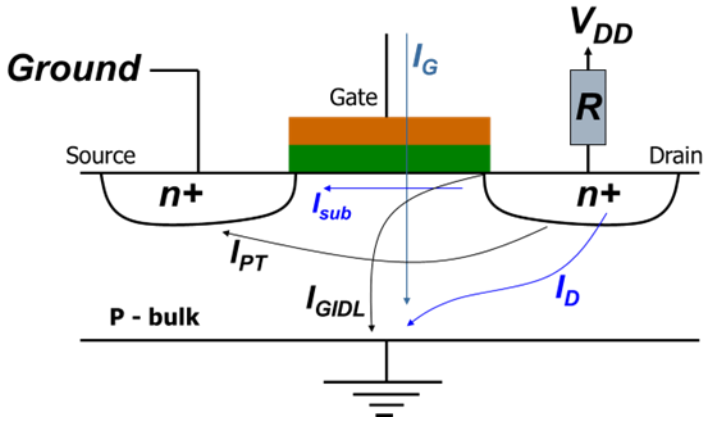
Leakage Power:



nMOS Transistor

Leakage Current Components

1. Subthreshold leakage, I_{sub}
2. Reverse bias pn junction leakage, I_D
3. Gate induced drain leakage, I_{GIDL} due to tunneling at the gate-drain overlap
4. Drain source punch-through, I_{PT} due to short channel and high drain-source voltage
5. Gate tunneling, I_G through thin oxide; *may become significant with scaling.*



1. Subthreshold Leakage, I_{sub}

- Occurs when $V_{GS} < V_{TH}$ (weak inversion), where minority carrier concentration is small, but not zero.
- Subthreshold conduction is dominated by the diffusion current
- This leakage component is the dominant modern device OFF-state leakage due to the low V_{TH} that is used.

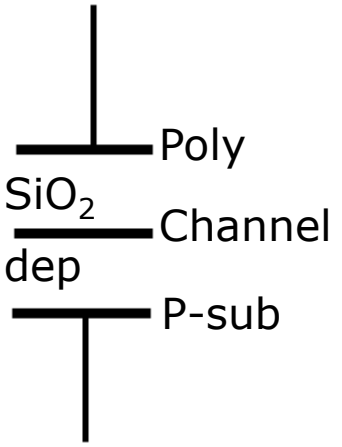
Subthreshold Leakage, I_{sub}

a) For Long Channel Devices:

$$I_{sub} = \mu_0 C_{ox} (W/L) v_T^2 \exp\{(V_{GS} - V_{TH}) / \eta v_T\}$$

μ_0: *zero bias carrier surface mobility*
C_{ox}: *gate oxide capacitance per unit area*
L: *channel length*
W: *gate width*
$v_T = kT/q$: *thermal voltage*
η: *a technology parameter*

Where, $\eta = 1 + \frac{C_b}{C_g}$.



$$C_b = \frac{\epsilon_{si}}{w_d} \quad , \quad C_g = \frac{\epsilon_{ox}}{t_{ox}}.$$

where ϵ_{ox} and ϵ_{si} denote the dielectric constants of the oxide and silicon, resp, w_d is the depletion width under the *channel and* t_{ox} is the gate oxide thickness.

b) For Short Channel Devices:

$$I_{sub} = \mu_0 C_{ox}(W/L)v_T^2 \exp\{(V_{GS} - V_{TH} + nV_{DS})/\eta v_T\}$$

V_{DS} = *drain to source voltage*
n: a DIBL constant

W. Nebel and J. Mermet (Editors), *Low Power Design in Deep Submicron Electronics*, Springer, 1997, Section 4.1 by J. Figueras, pp. 81-104