MANIPAL
ACADEMY of HIGHER EDUCATION
(Institution of Eminence Deemed to be University)

MANIPAL SCHOOL OF INFORMATION SCIENCES
(A Constituent unit of MAHE, Manipal)

ASSIGNMENT – 1
DIGITAL SYSTEMS AND VLSI DESIGN LAB

Reg. Number	Name	Branch
241038005	Chaitanya S Rao	VLSI

Submitted to

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Manipal School of Information Sciences,
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11/11/2024

Questions:

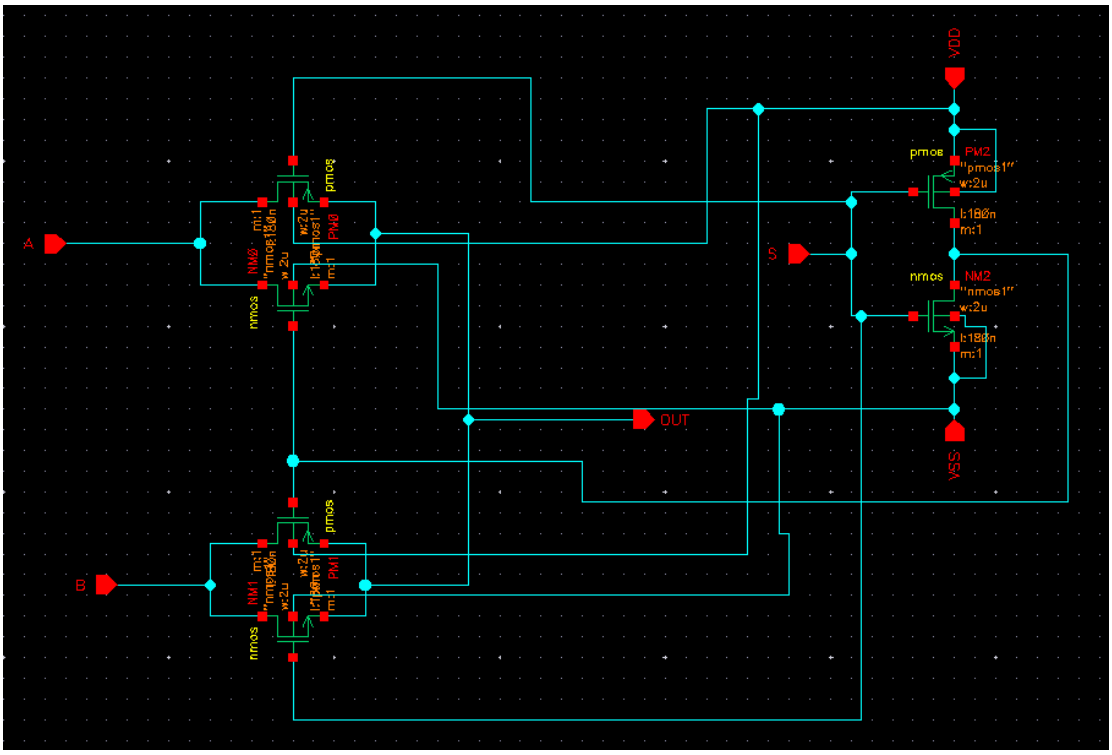
1 Design a 2:1 MUX using transmission gates.
2 Design a 4:1 MUX making use of the symbols of 2:1 MUX designed above.
3 Simulate the behaviour of this design.

Draw the layout for the above design and verify its correctness by spice extraction, LVS, RC extraction and simulation.

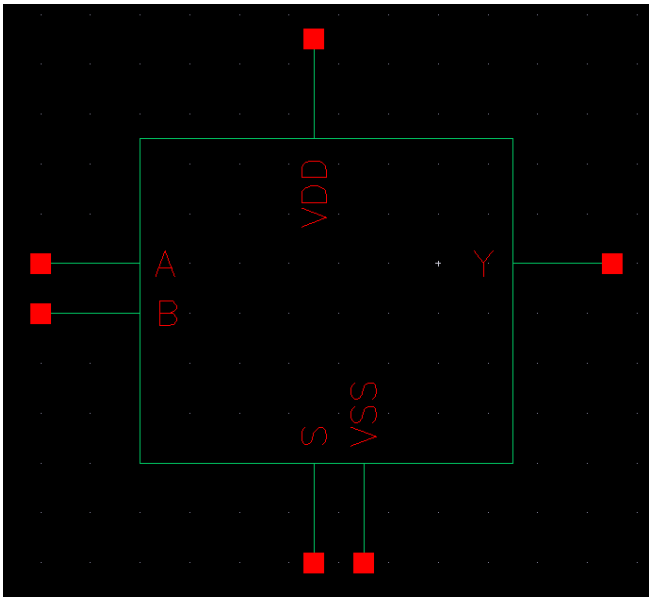
SOLUTION:

1. 2:1 MUX

SCHEMATIC:



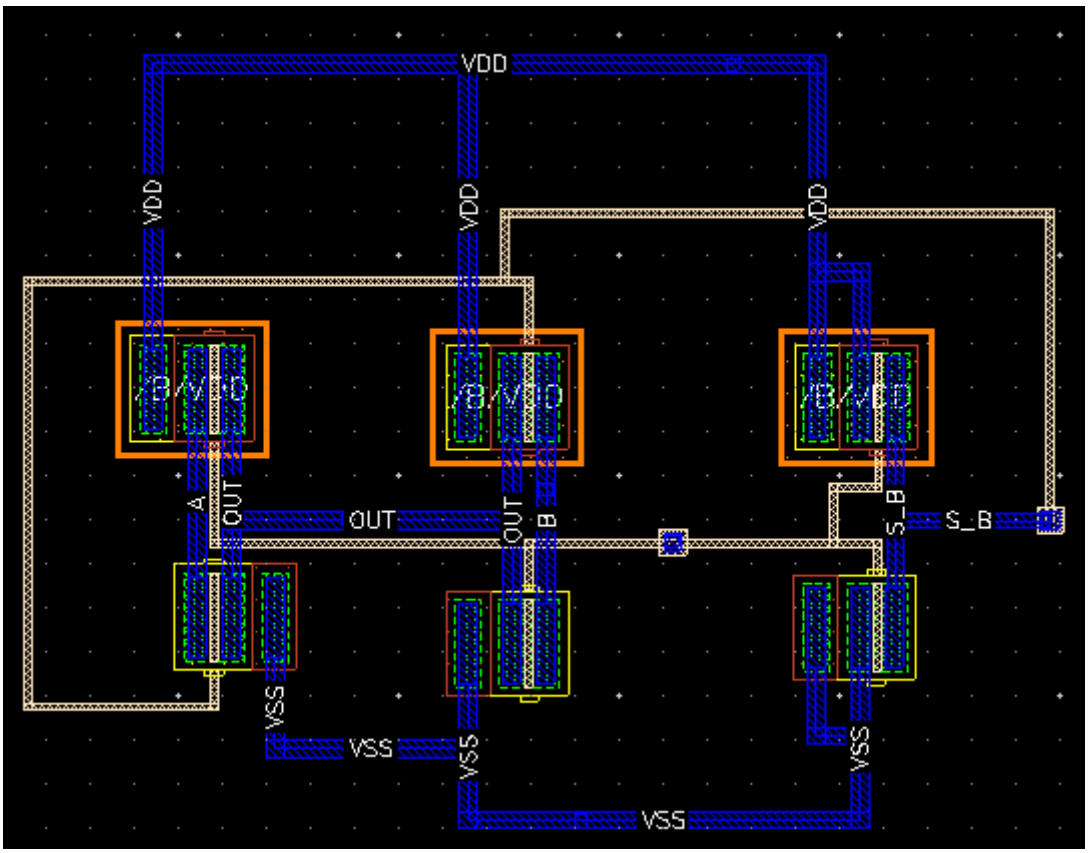
SYMBOL:

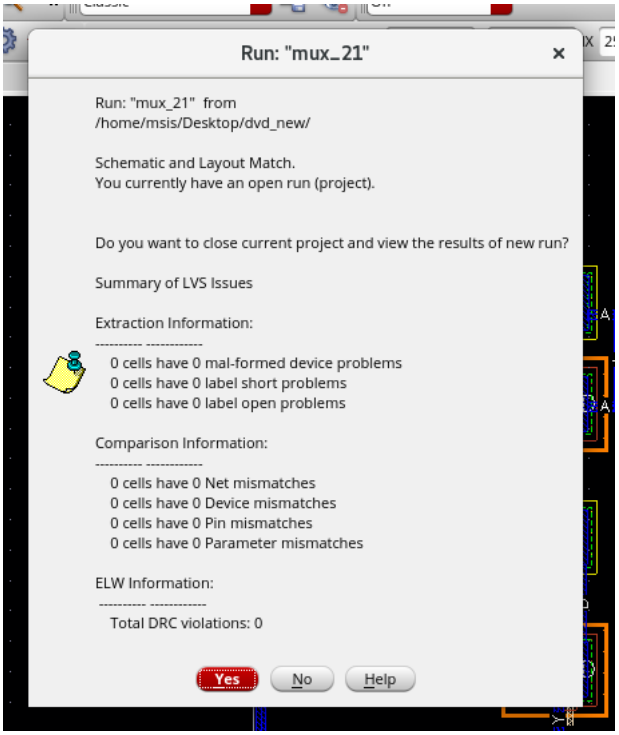


WAVEFORM:

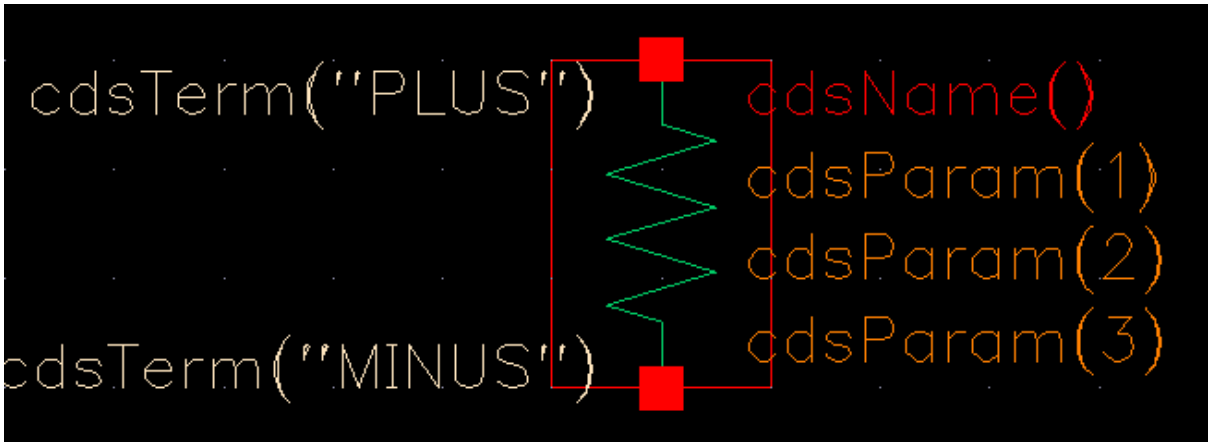

Virtuoso (R) Visualization & Analysis XL
Transient Response
/A
/B
/S
/out
time (ns)

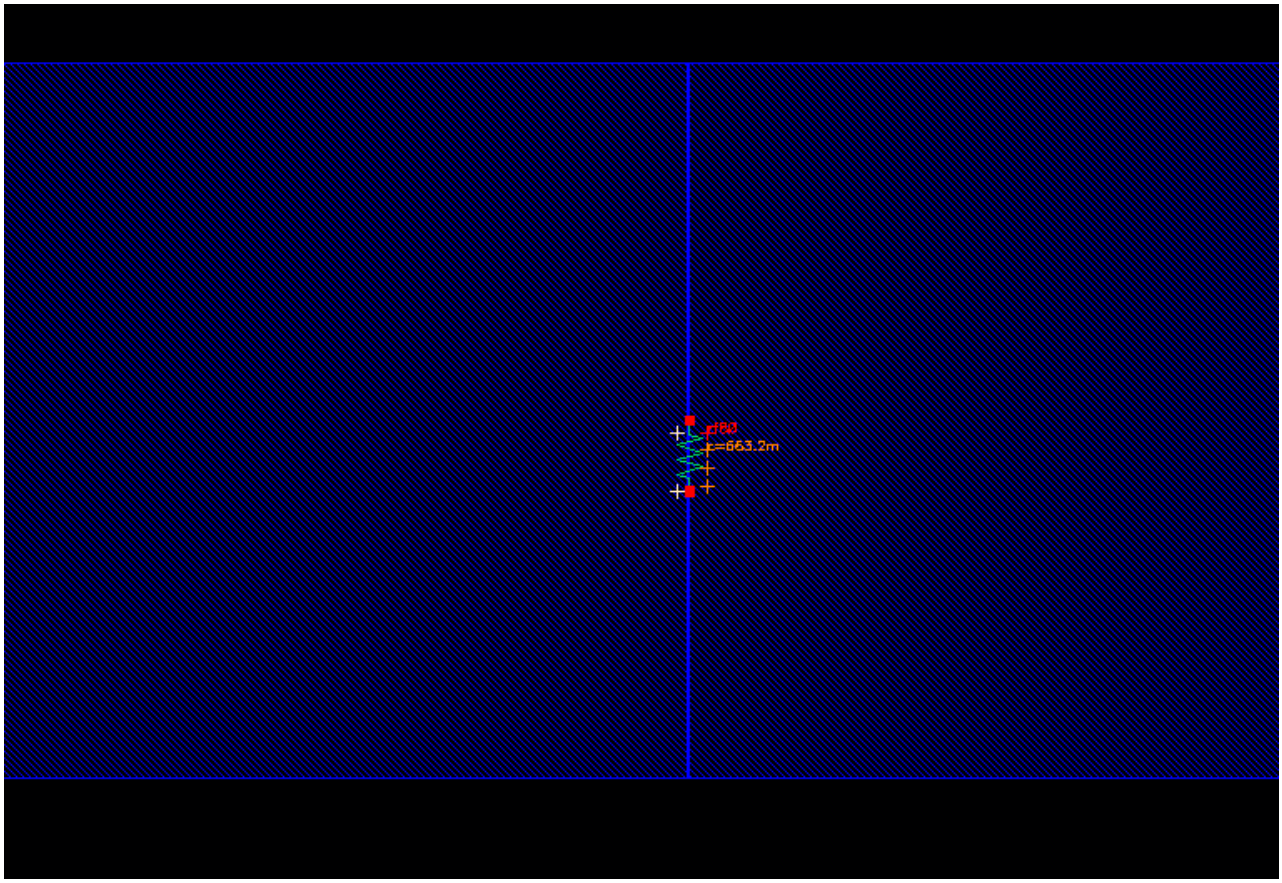
LAYOUT:


VDD
VSS
OUT
A
B
S_B



RC extraction:

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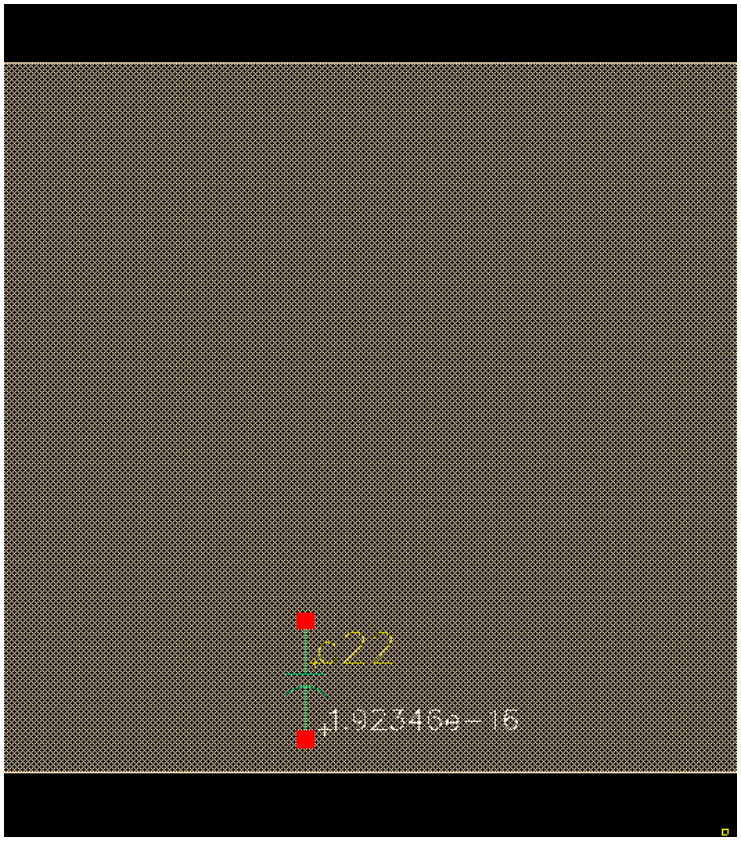
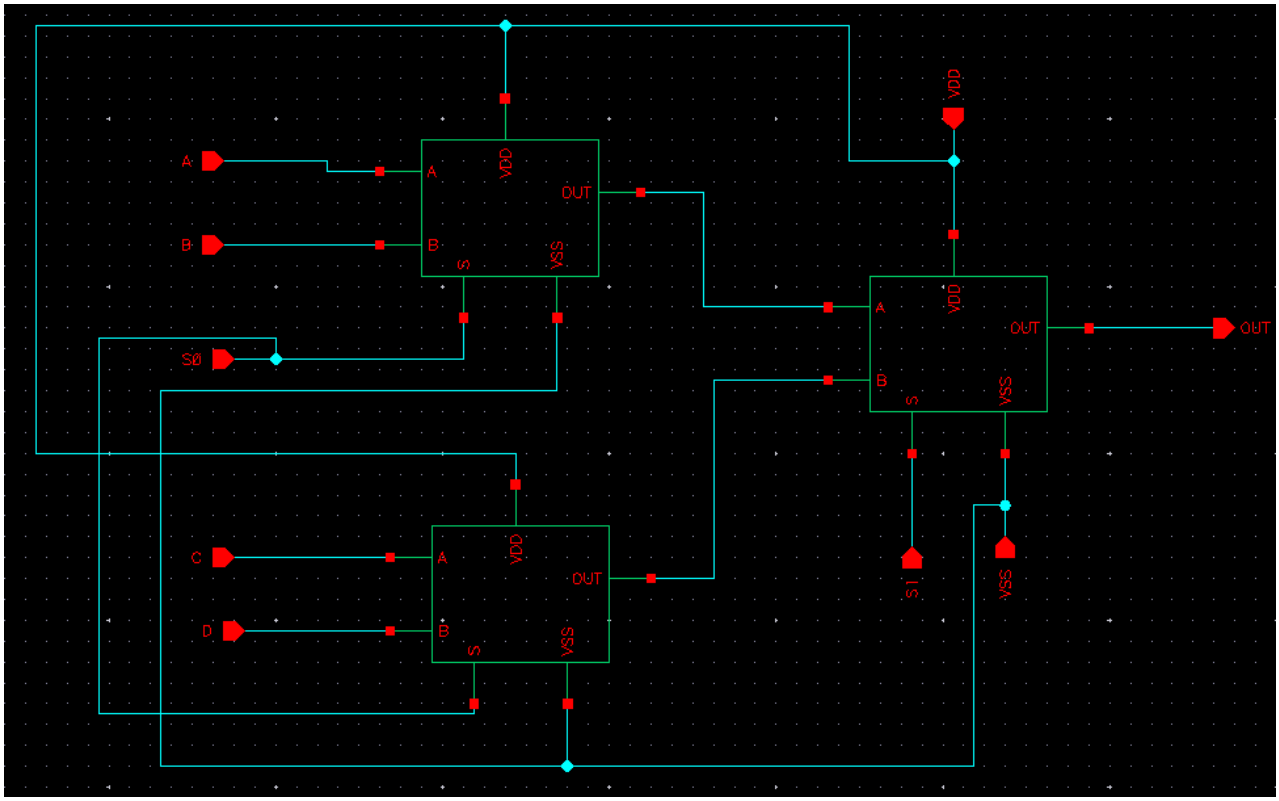
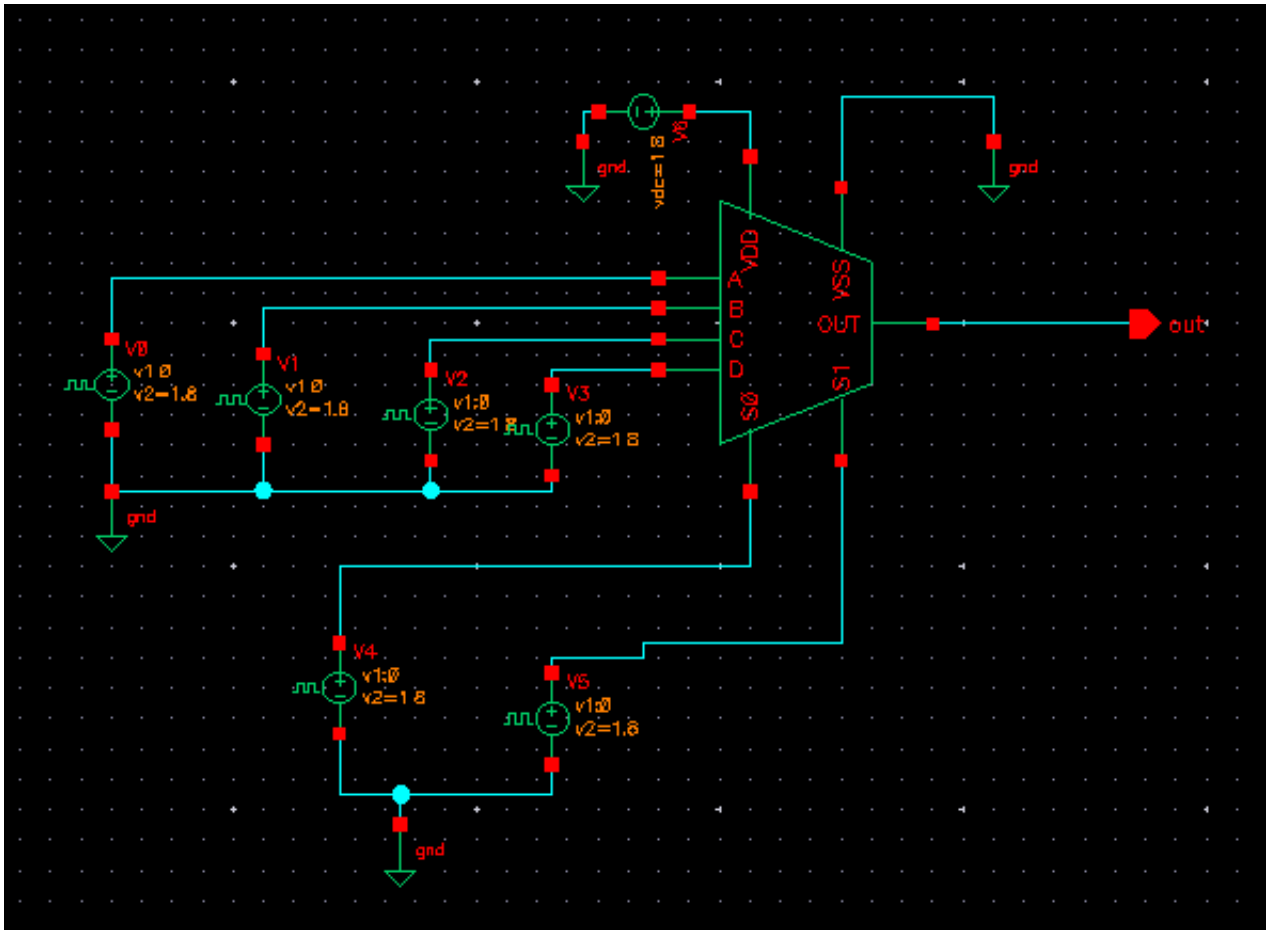

c22
1.923469e-16

2. 4:1 MUX

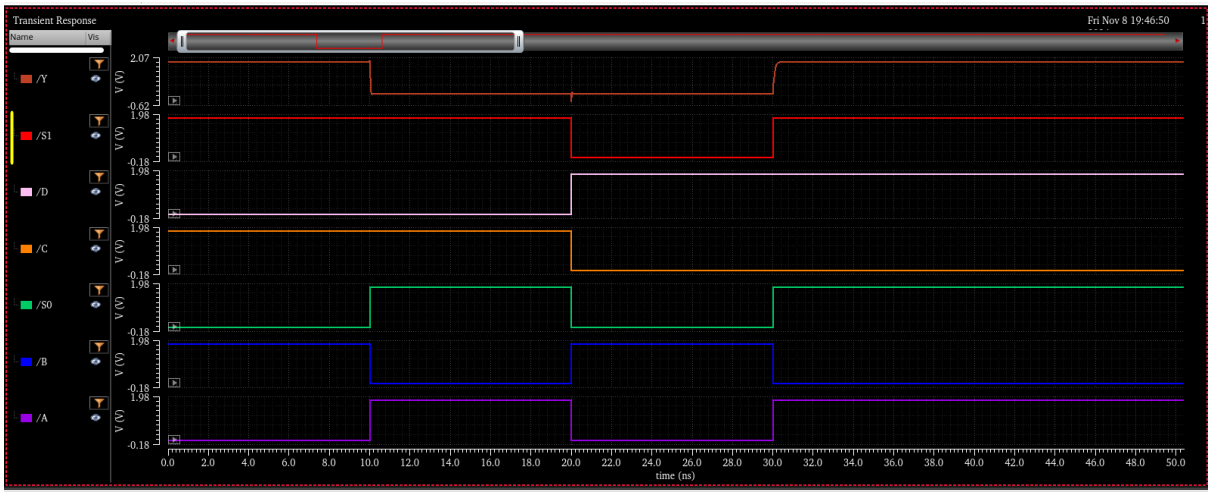
SCHEMATIC:



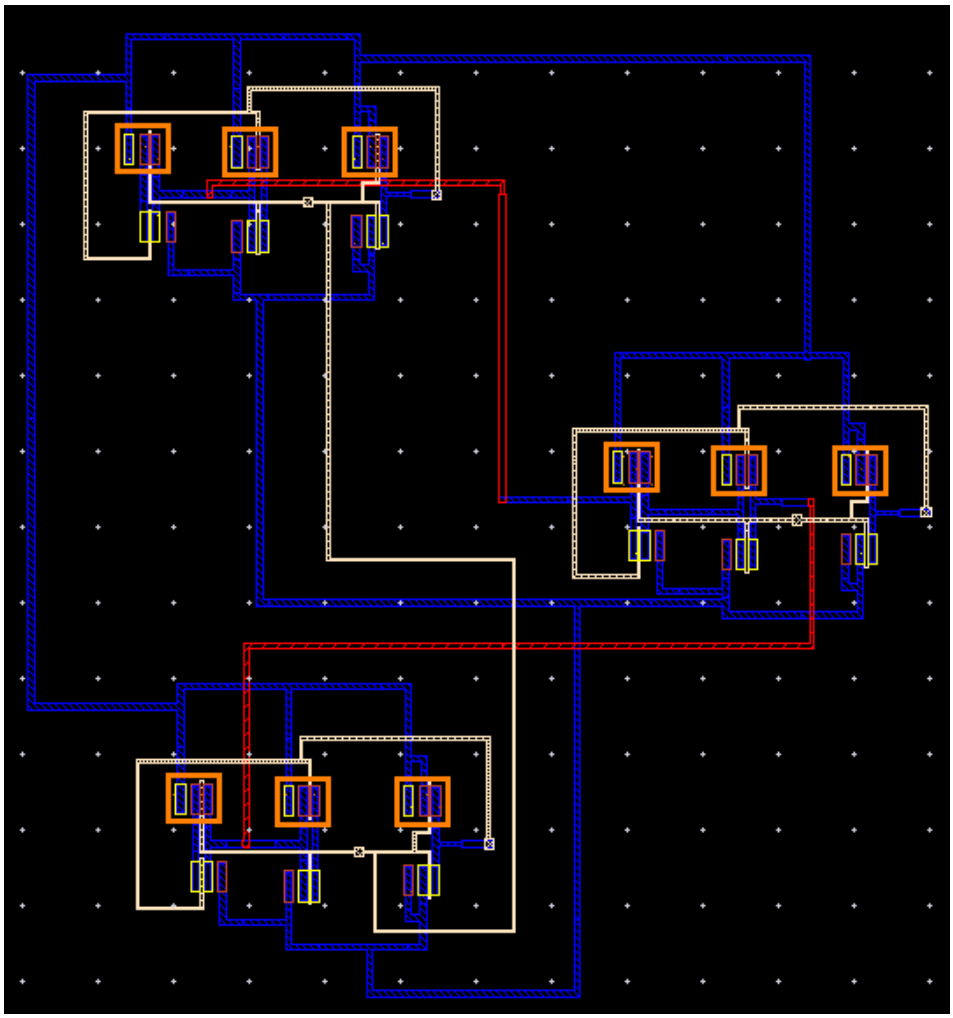
Test circuit:

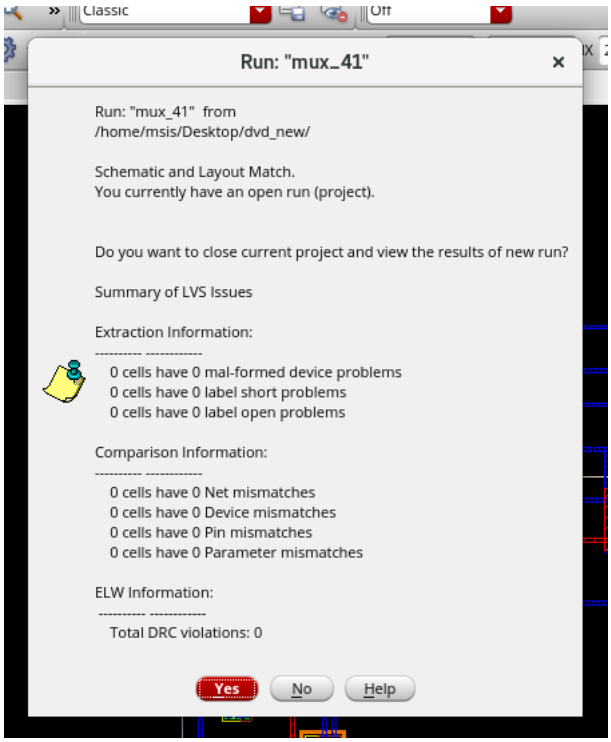


WAVEFORM:

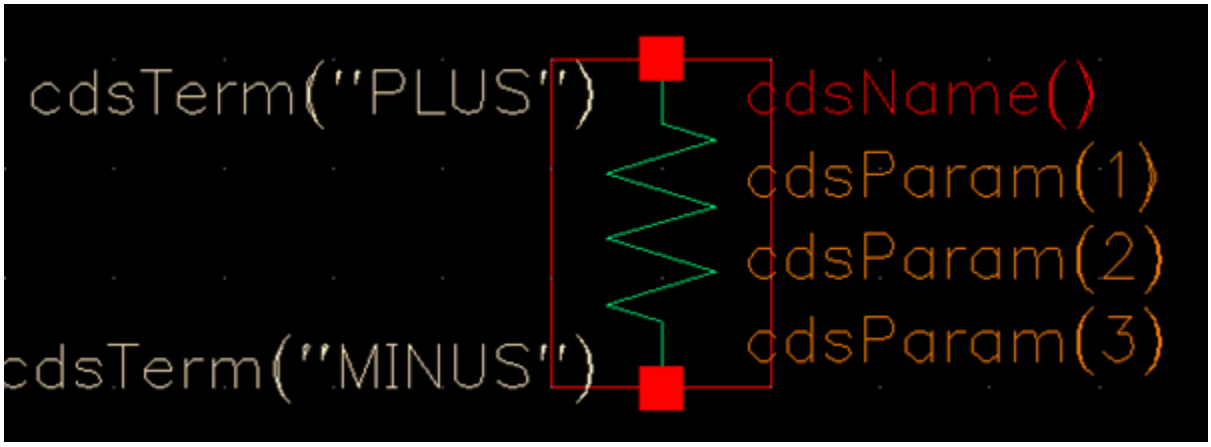


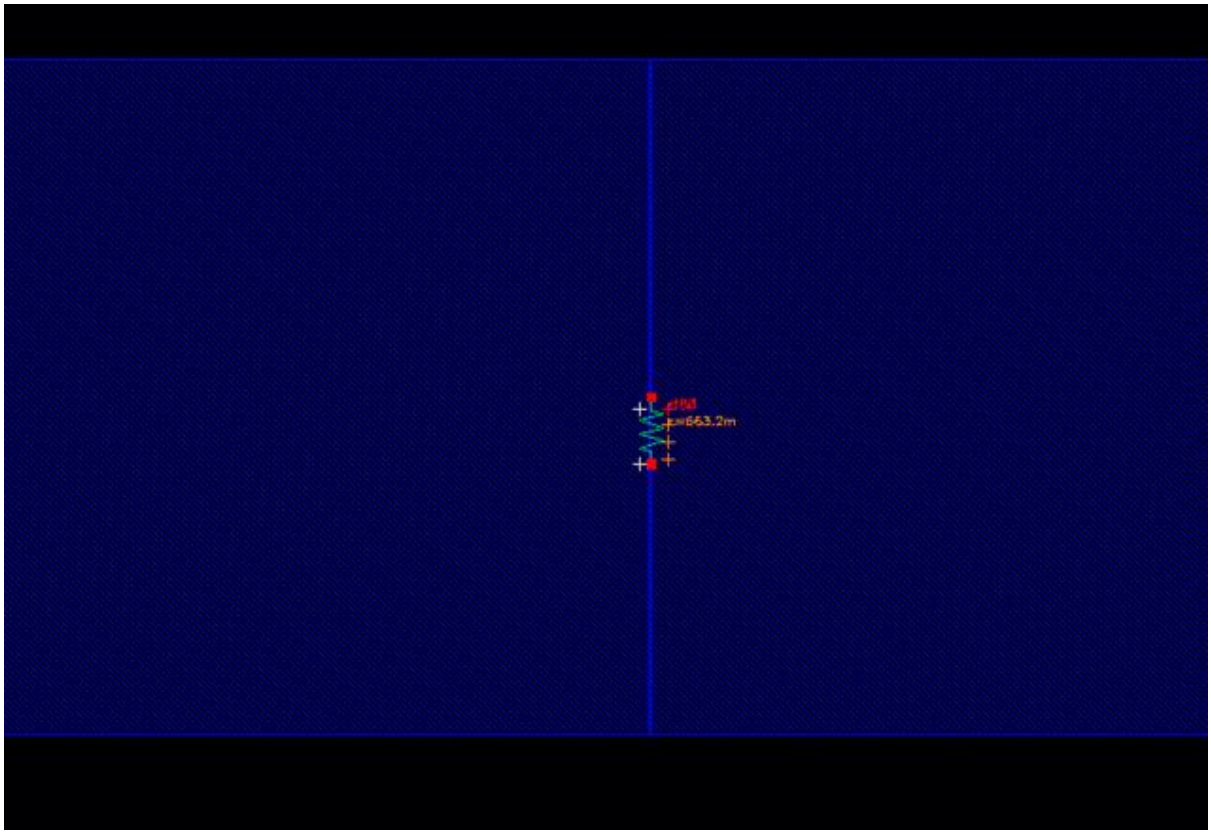
LAYOUT:

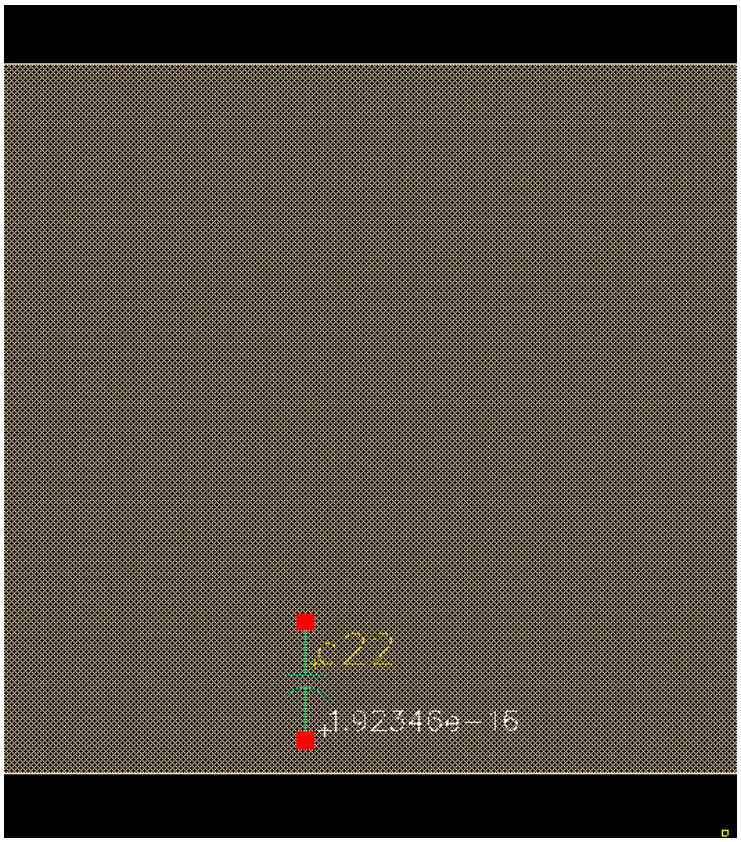




RC extraction:






c22
1.923469−16