LATCHUP IN CMOS

OUTLINE

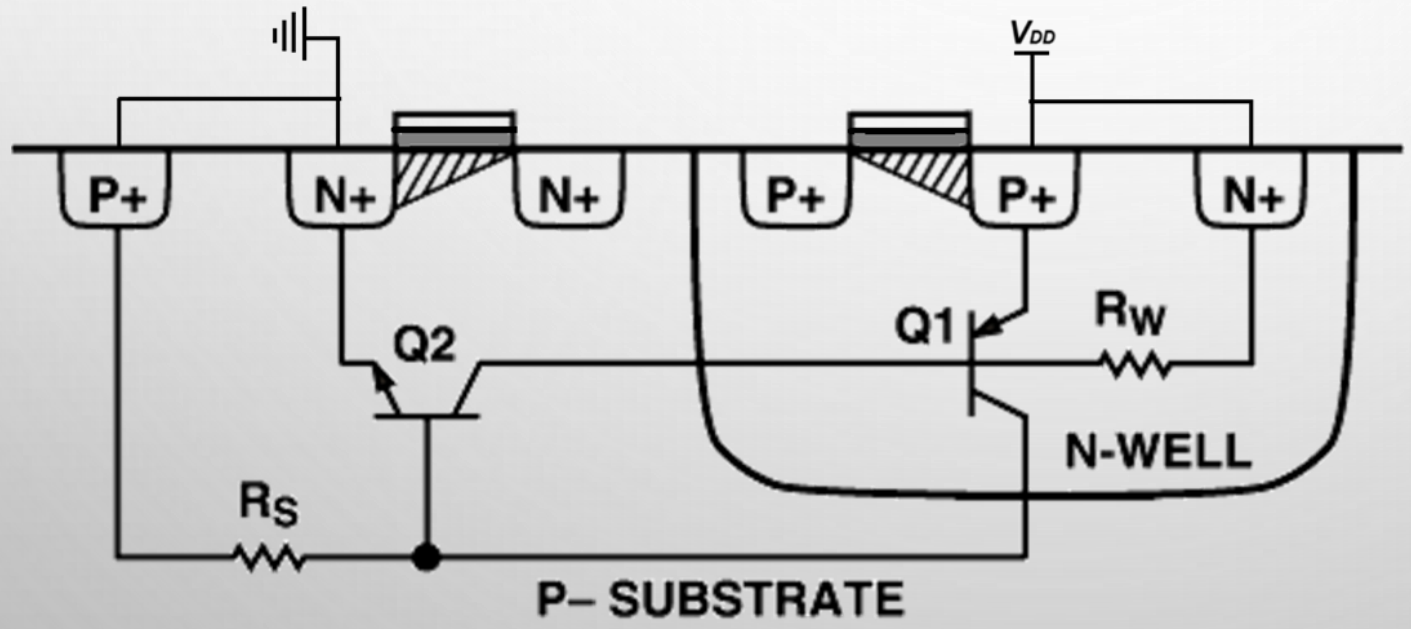
- Latch-up
  - Physical Origin of Latch-up
  - Latch-up Triggering
- Latch-up Prevention

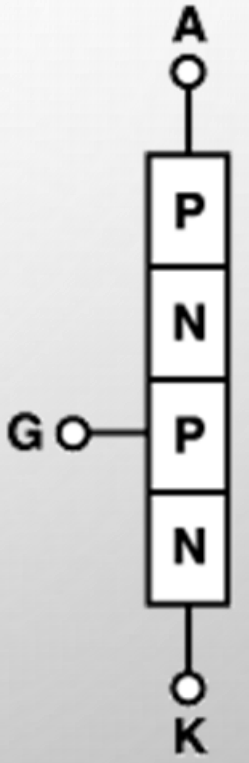
Latch-up

- Latchup refers to short circuit / low impedance path formed between power and ground rails in an IC leading to high current and damage to the IC.
- It occurs due to interaction between parasitic pnp and npn transistors.

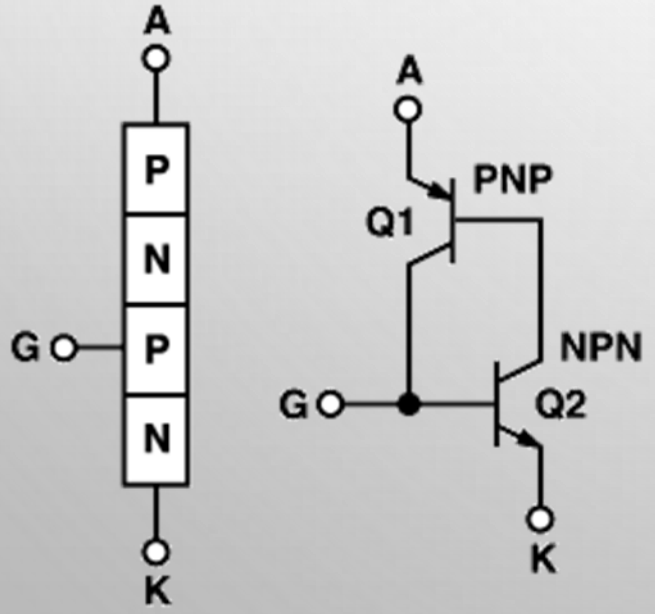
Latch-up

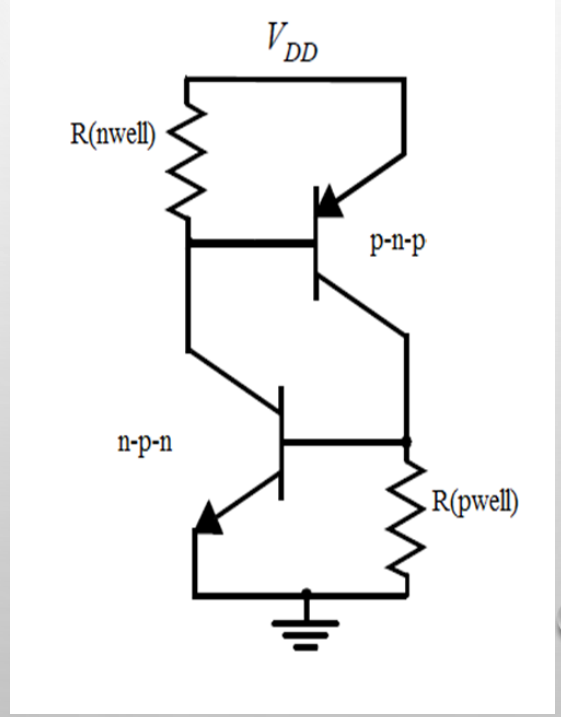
- The n-p-n-p structure is formed by the source of the NMOS, the p-substrate, the n-well and the source of the PMOS, which resembles a Silicon Controlled Rectifier (SCR) as shown.

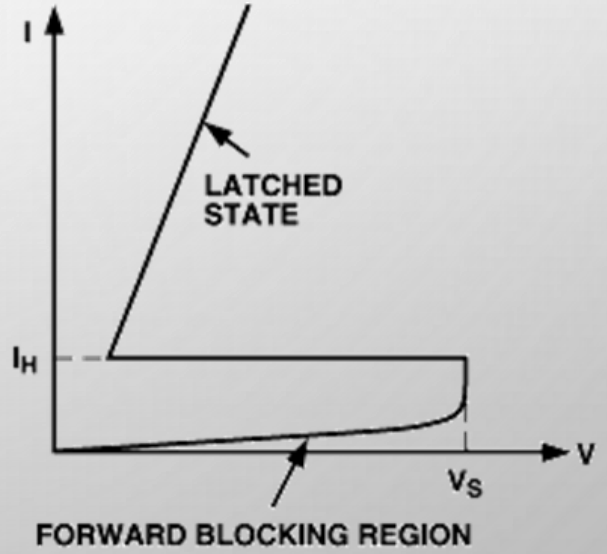




- When one of the two bipolar transistors gets forward biased (due to current flowing through the well, or substrate), it feeds the base of the other transistor. This +ve f/b increases the current until the circuit fails or burns out.
- Due to short circuiting of the power rail and ground rail, eventually causes excessive current, and can even permanently damage the device.







Latch-up Triggering

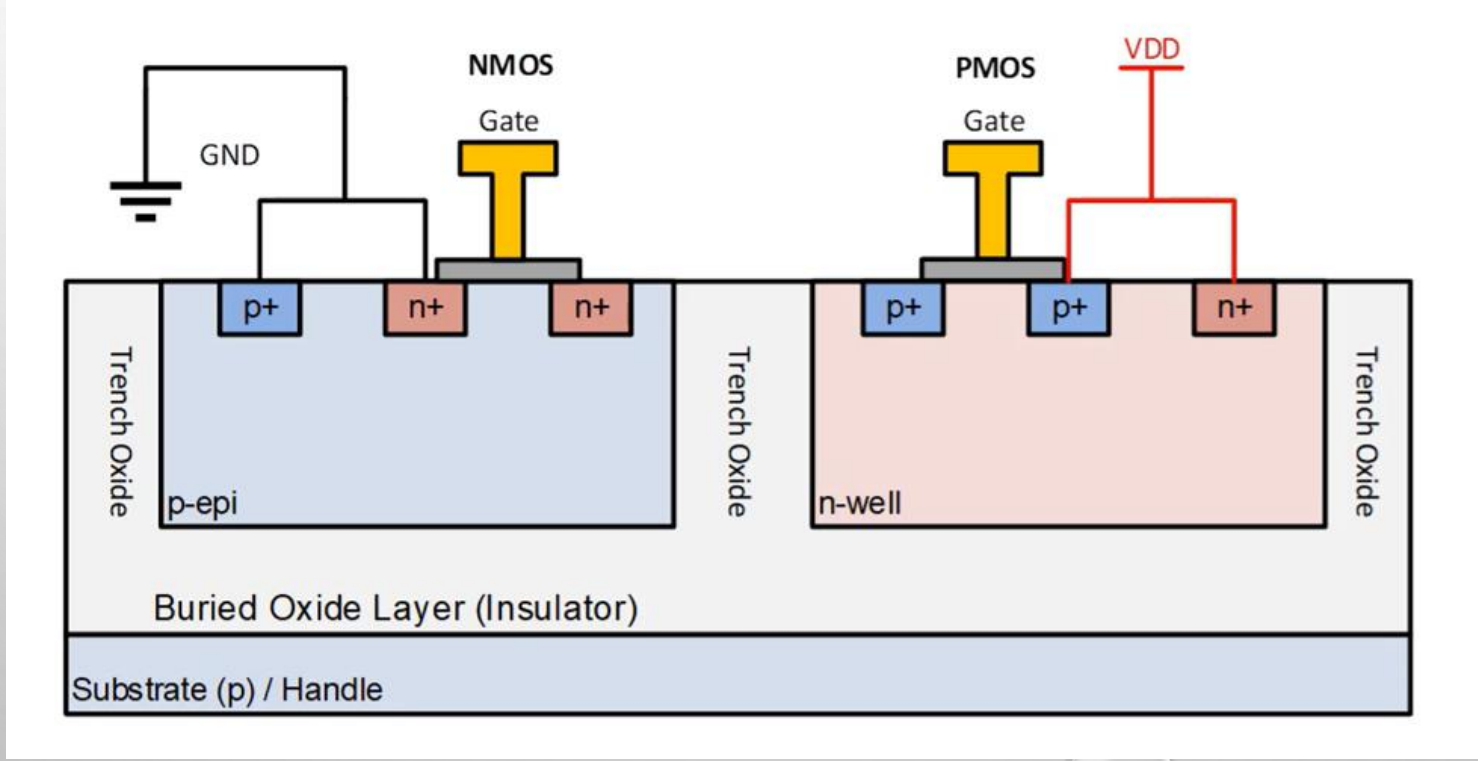
- A common cause of latch-up is a positive or negative voltage spike on an input or output pin of a digital chip that exceeds the rail voltage by more than a diode drop.
- The supply voltage exceeding the absolute maximum rating, often from a transient spike in the power supply
- Ionizing radiation (e.g. in space or nuclear environments) applications. It can be eliminated by radiation hardening.
- High-power microwave interference can also trigger latch-ups
- More susceptible to latch-up at higher temperatures.

Latch-up Prevention Techniques

In view of its negative effects on device performance, latch-up prevention is a key concern for CMOS IC designers. There are a variety of methods commonly employed to prevent latch-up.

1. Putting a high resistance in the path so as to limit the current through supply and make $\beta 1 * \beta 2 < 1$.
2. Surrounding PMOS and NMOS transistors with an insulating oxide layer (trench) to isolate NMOS and PMOS devices. This breaks parasitic SCR structure. This means additional processing steps and a rather complex device structure.
3. Another commonly used method involves increasing the distance between NMOS and PMOS devices and placing guard rings between devices.
4. Latchup Protection Technology circuitry which shuts off the device when latch-up is detected.

Surrounding PMOS and NMOS with an insulating oxide layer (trench)



Placing guard rings between devices